Combining Input Amplifiers and Converters for Frequency Domain Applications

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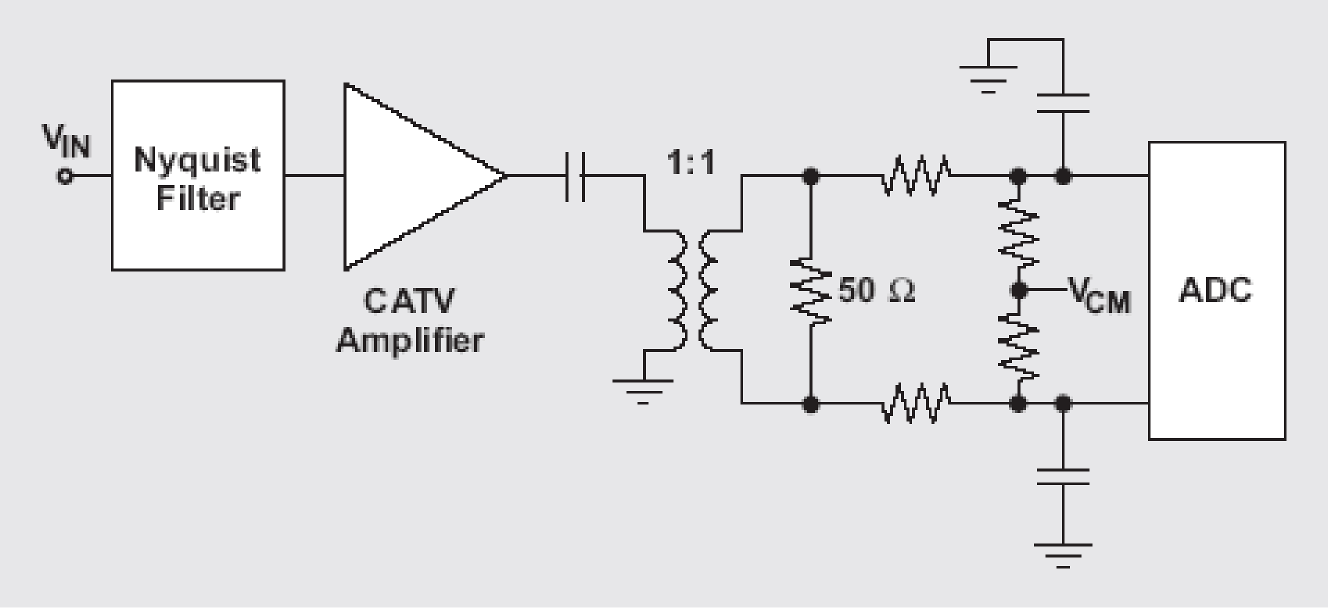
All High Speed, High Performance ADCs have Differential Inputs

- Drive amplifier circuit needs to provide differential inputs
- If input signal is single ended, must convert to differential
  - Can be done with single ended Amps and transformers
  - Can be done with FDA (Fully Differential Amplifiers)
- Better performance if input signal is differential

Single Ended amp with transformer interface



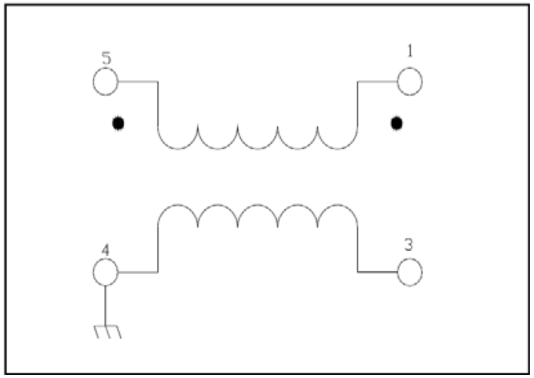
Two factors limit this approach

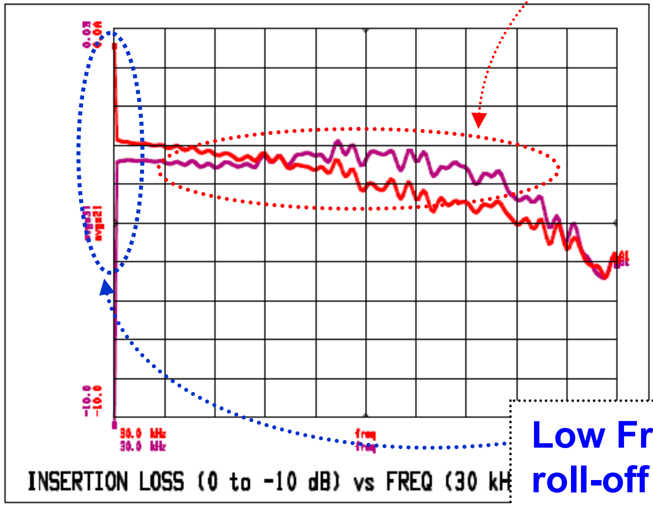
- Amplifier (often not present)
  - Single-ended architecture must consume a great deal of power to keep HD2 components low.
- Transformer
  - If no amplifier, then limited choices in voltage gain (via turns ratio)
  - Limits low frequencies
  - Pass-band flatness can be an issue because of ripple.

Transformers -

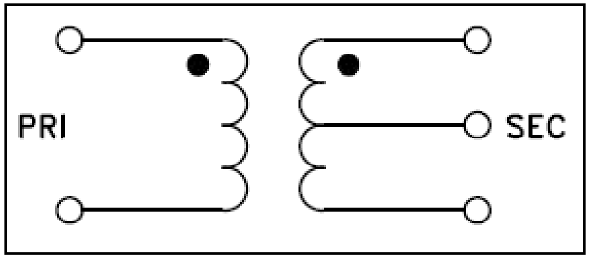
Will not pass DC signals and losses vary over the pass-band

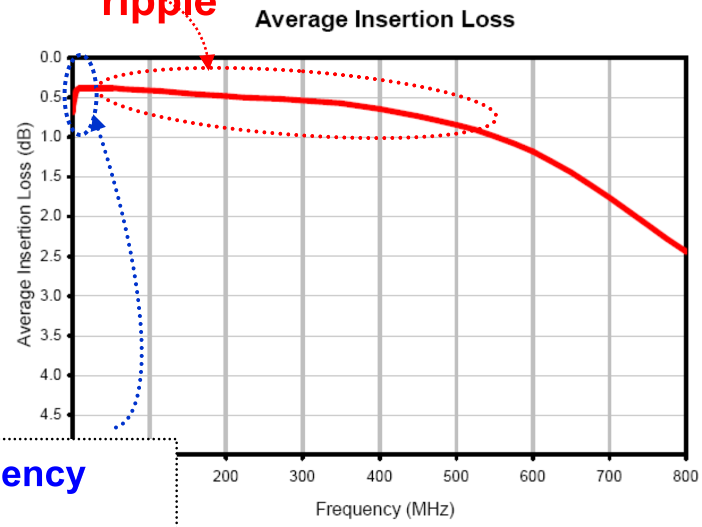
Example 1: High BW balun
Macom ETC1-13





Example 2: Isolation Transformer
Minicircuits ADT1-1WT



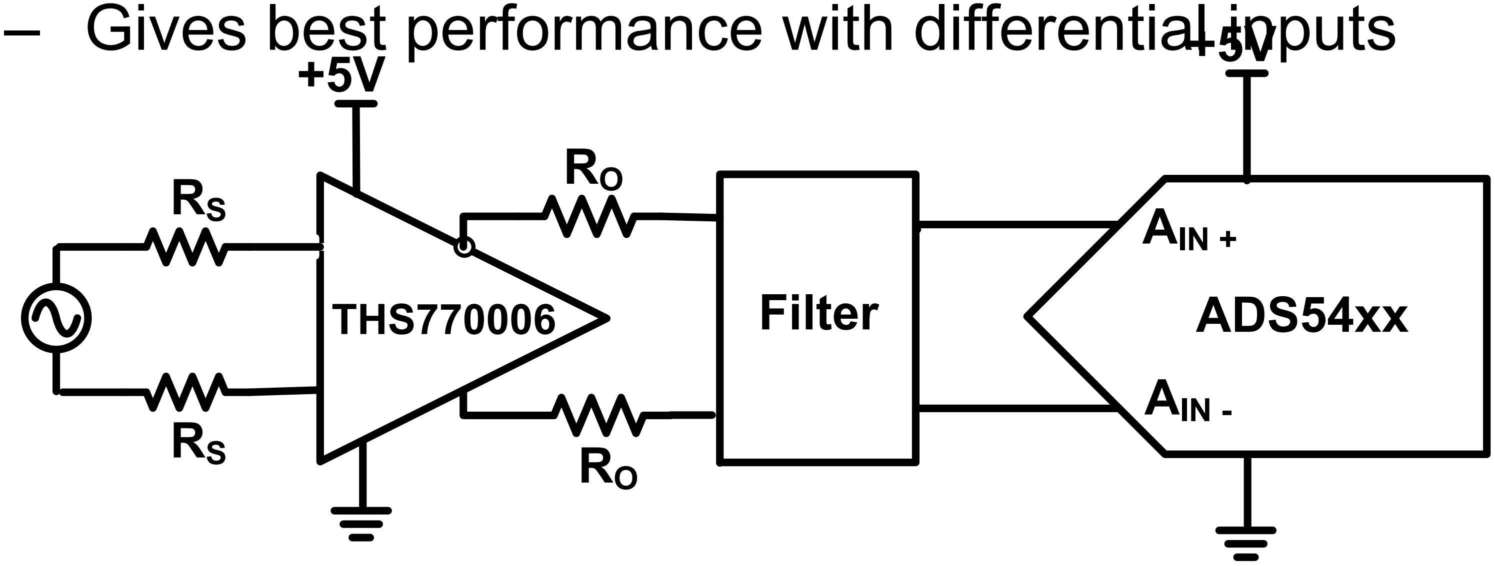


Passband ripple

Low Frequency roll-off
Will not pass DC

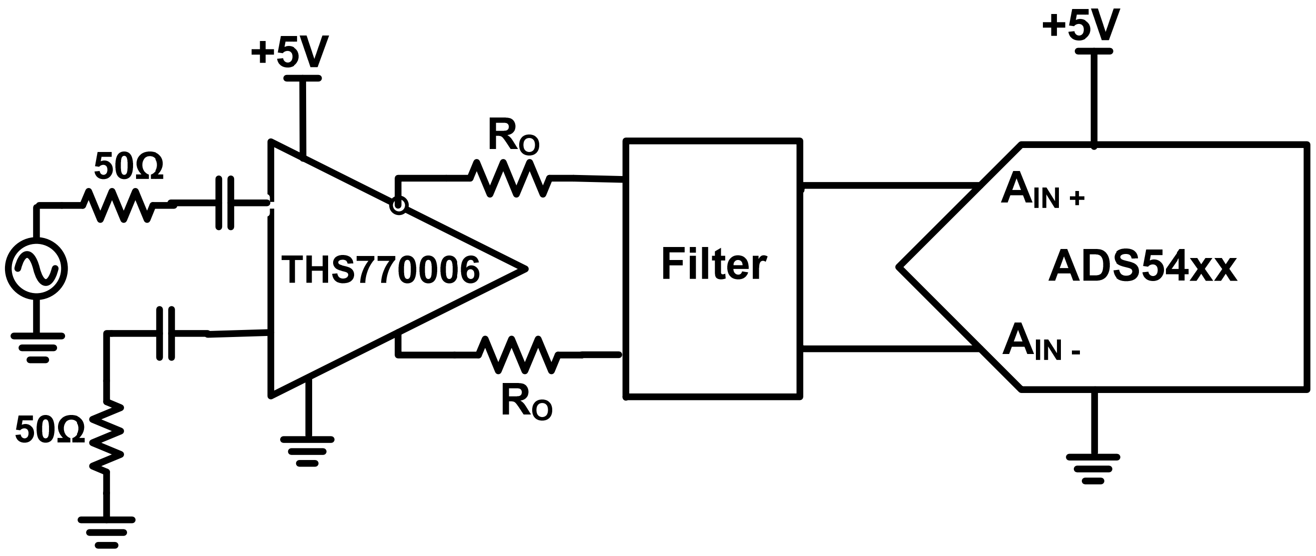
High-Speed FDAs offer reduced power and cost as active A/D drivers

- Broadband Fully Differential Amplifiers (FDAs)
  - Easy & efficient way to provide DC-coupled interface with gain.
    - Less power consumption than an RF amp.
    - Flexible gain options
  - Gives best performance with differential inputs



Single Ended to Differential with FDAs

- Can efficiently provide
  - Gain
  - Perform Single Ended to Differential conversion
  - Level shift to input common mode of ADC

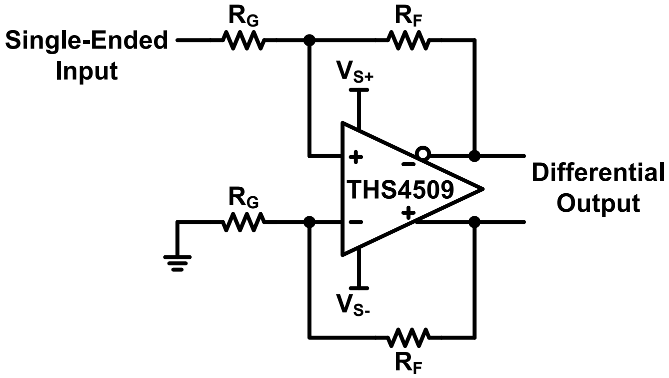


Other single-ended-to-differential Amplifier Configurations

◆ Op amps can provide single-ended-to-differential conversion with lower power & cost

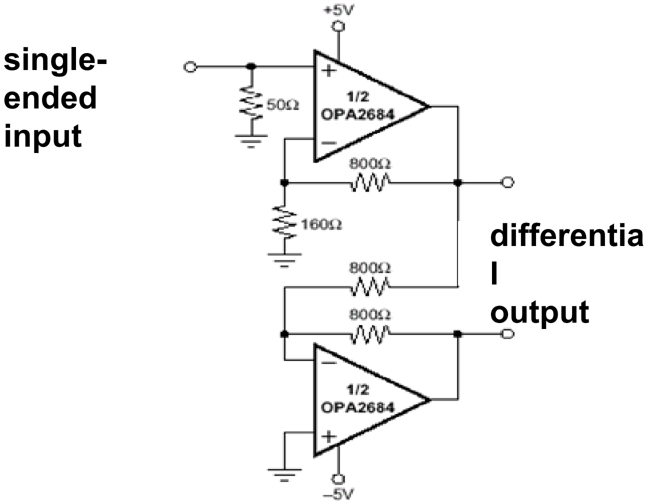
1. Fully Differential Op Amps (FDAs)

- Feature differential inputs and outputs, and output common mode control.
- Provide an easy means for DC-coupled SE-DIFF conversion.
  - Independent output common mode control.
  - Much better SFDR performance for fully differential inputs/outputs.



2. Dual Op Amps for SE-DIFF conversion.

- Some of these work pretty well, but can give modest
  SFDR performance
- Best performance limited to lower frequencies

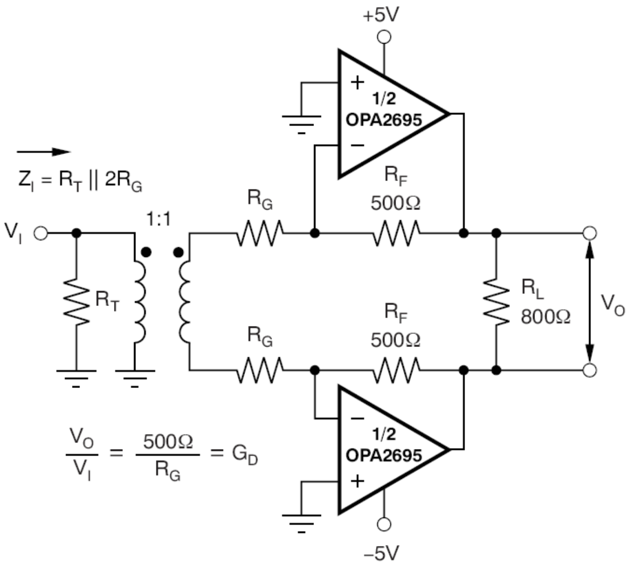


Other single-ended-to-differential Amplifier Configurations (cont'd)

3. Transformers with Dual Op Amps

- ◆ Transformers provide the best distortion & noise option for SE/DIFF conversion for AC-coupled applications.
  - Be aware of frequency limitations. The signal spectrum must not be near edges of transformer pass-band.

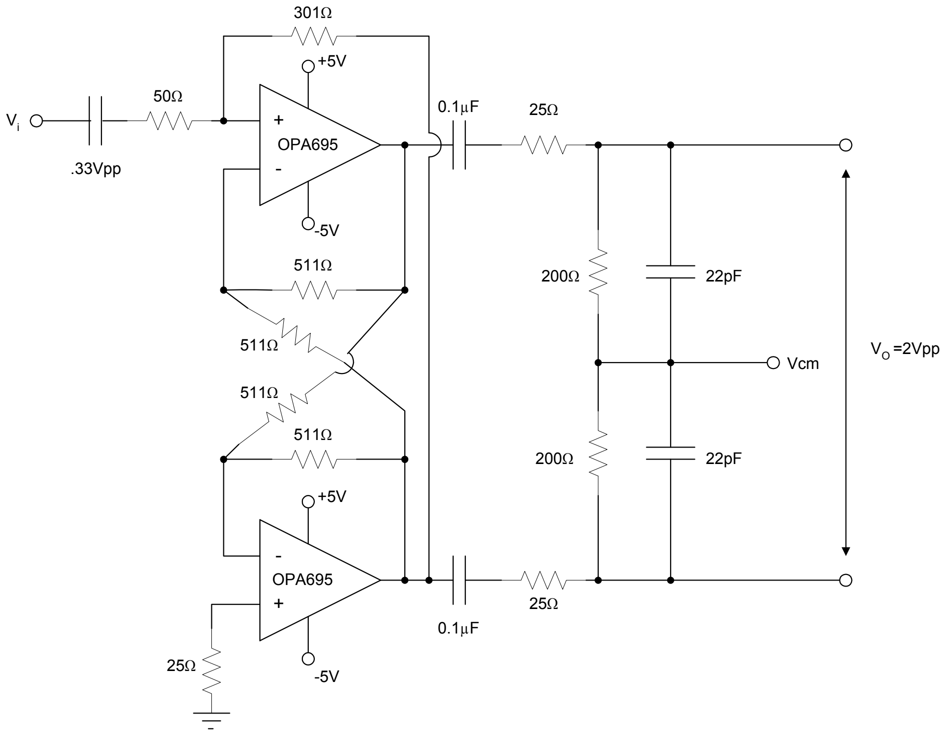
single-ended input

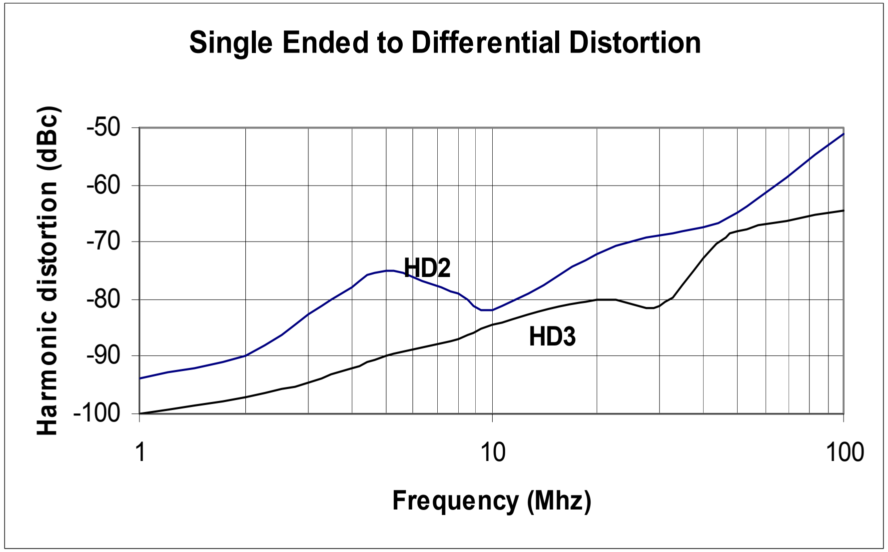


differential output

Op Amp Circuits for Single-Ended to Differential Conversion: cont'd

Example using 2 op amps for single ended to differential output





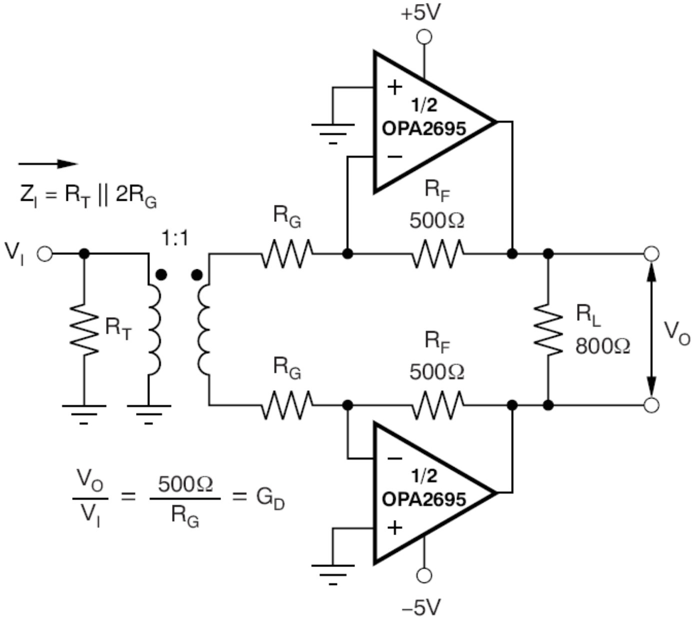
Tested performance using a very good layout board.

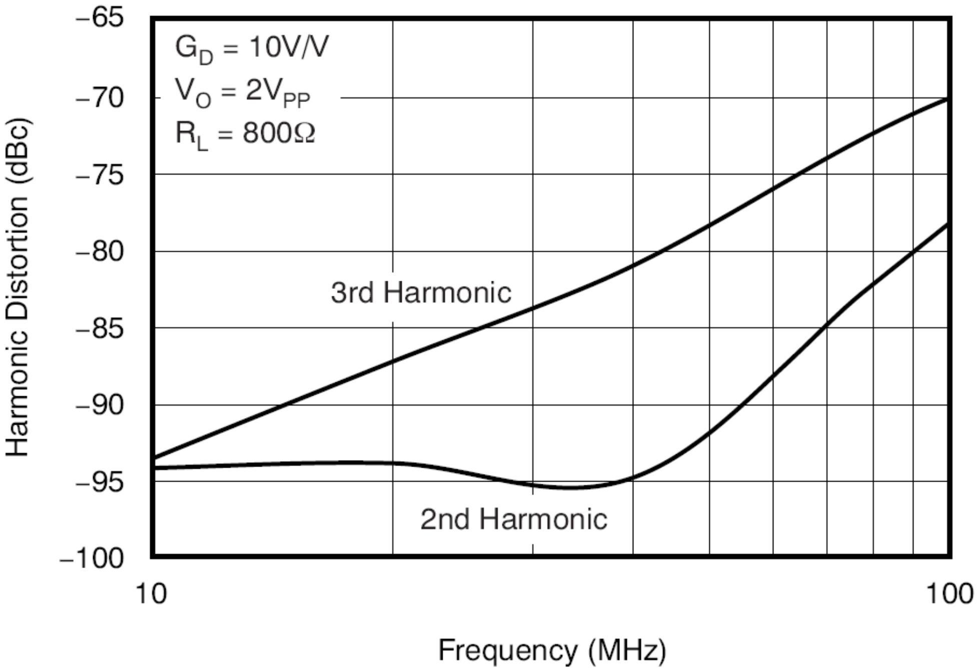
Op Amp Circuits for Single-Ended to Differential Conversion (cont'd)

Example using 2 op amps for single ended to differential output using a transformer on the input

a. Better noise figure

b. Can establish output common-mode voltage by driving that voltage into positive (+) inputs





Differential I/O Solutions

Running two amplifier stages or an FDA at the output of transformer provides significant opportunity for HD2 and HD3 reduction vs. a single-ended stage driving a final transformer stage.

This leads into much more power efficient designs for a given targeted SFDR level. Along with this lower power, comes a little higher amplifier noise than classic IF or CATV amplifiers. Thus, the noise calculation, and noise power bandwidth control, become critical to get the full benefit of this approach without giving up system level SNR performance.

Using Op Amps or FDAs as Differential I/O Interfaces

- Op amps can provide a simple diff-in to diff-out operation if:
    - No requirement for a DC-coupled channel.
    - No requirement for an output common mode level shift.
- Non-inverting and inverting configurations shown are from the OPA2684 data sheet
    - Data sheet contains a short discussion of the pros and cons for the two approaches.
- An FDA can be used similar to inverting circuit shown.

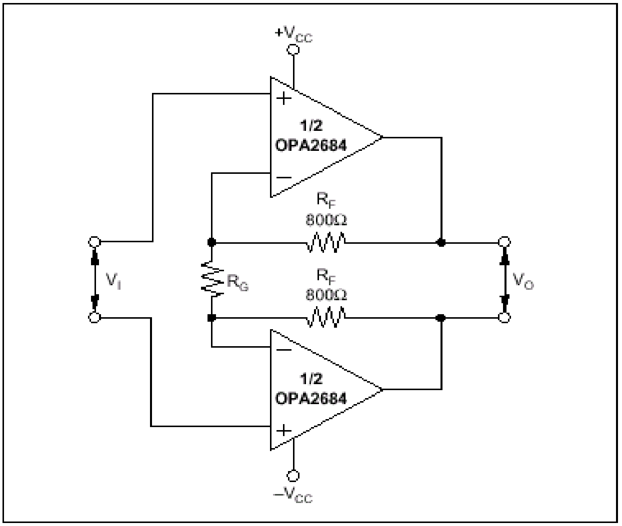
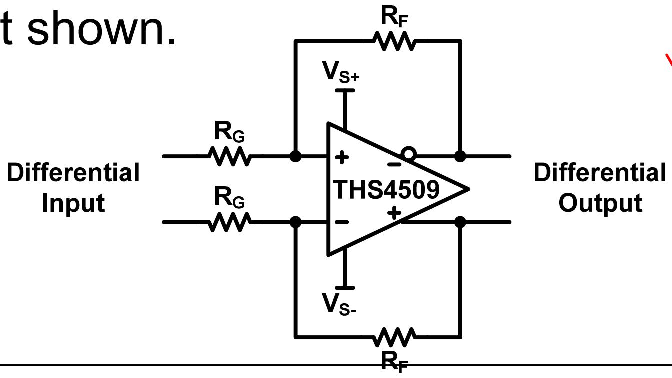


FIGURE 5. Noninverting Differential I/O Amplifier.



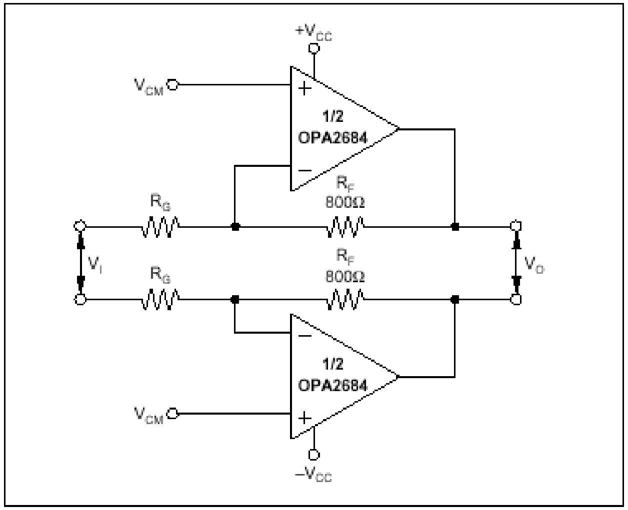
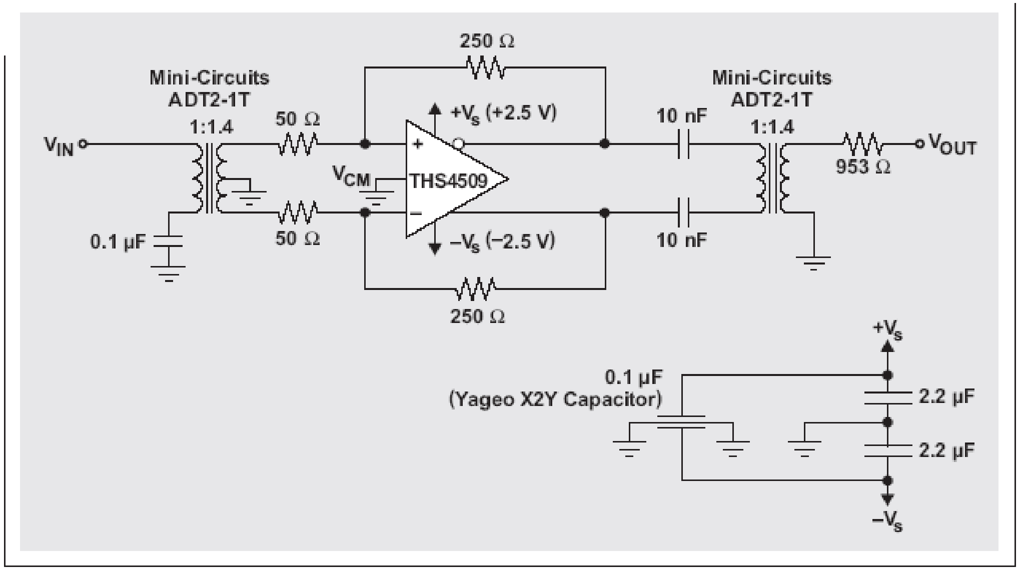


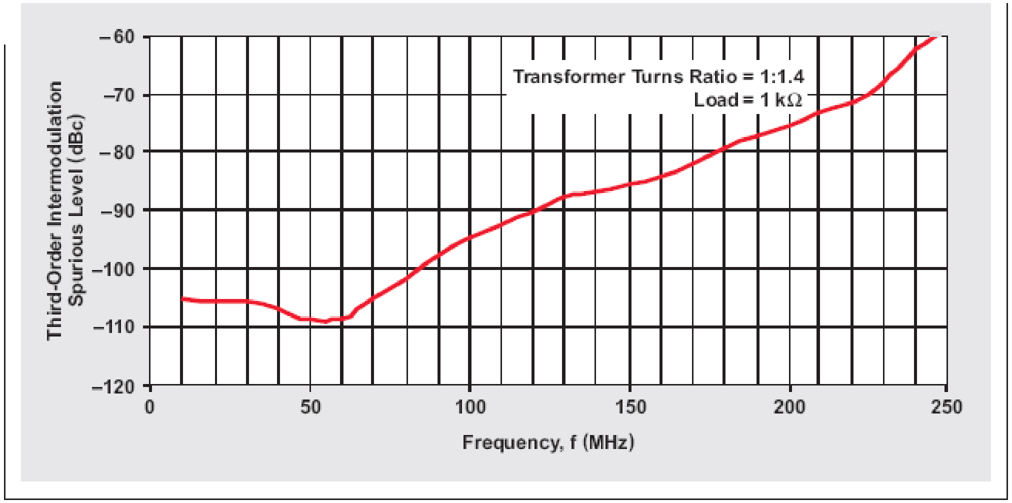
FIGURE 6. Inverting Differential I/O Amplifier.

FDA example using the THS4509



Approximate power consumption is 150mW

Approximate input NF = 8.2dB (from 50Ω source)



Summary of Amplifier + Filter SNR and SFDR Targets

For a given ADC, how do we choose amplifier + filter interface solutions? Key points to consider:

1. **Noise:** Noise adds as an RMS sum; so you need amp to be 10dB better than ADC for minimal degradation.
2. **SFDR**: Spurs add as a linear sum; so you need amp to be 20dB better than ADC for minimal degradation. Note this is theoretical worst case and better performance is often noted.
3. **Data sheet characterization**: Measurements for devices highlight best performance with optimized test solutions and actual performance will vary.
4. **End applications**: Usually require an active interface with amplifier & filter
5. **How much degradation is allowed?** SNR and SFDR will be less for the Amplifier + ADC combination compared to the data sheet. Trade-offs in degradation vs. cost and power will need to me made.

Design Example: Lower Speed, High SFDR SAR and Δ Σ ADC

- Published specs for high resolution SAR and ΔΣ ADC report SFDR > 110dB.
- In theory, an amplifier-based driver circuit for these converters must have HD2/HD3 < -130dBc distortion to keep overall SFDR > 109dB.

- This immediately presents a significant measurement challenge.

  - How to reliably measure very low-distortion amplifiers?

- Two key op amp issues with sub-1MHz high dynamic range designs:

  1. Need to consider the 1/f noise corner frequency in the noise analysis.
  2. Distortion will improve with decreasing frequency.

Op Amp Noise Calculation for a SAR or Δ Σ ADC

Most SAR converters suggest an RC filter from the amplifier to the converter input.

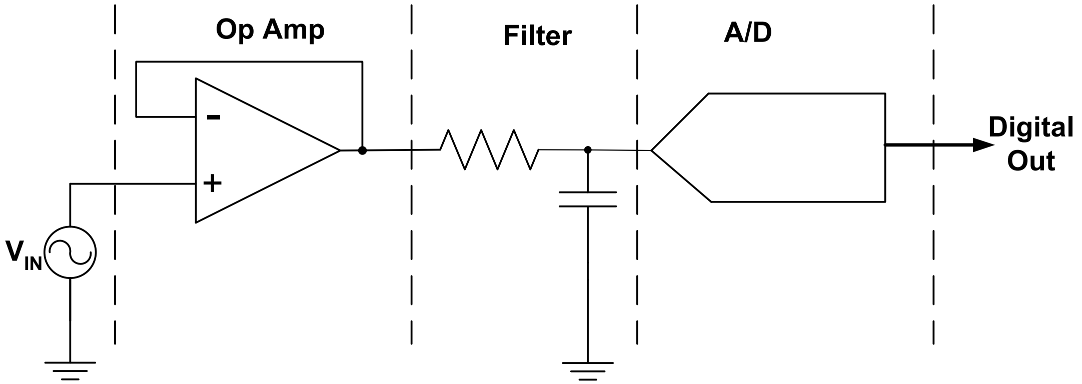
a. The C is often set from a charge transfer perspective

- Relatively short sampling window vs. total conversion time.

b. The R is then set for the amplifier to replace the sampling charge

- Allow the ADC input to settle to the “final” value in the sampling window.

Example circuit:



Whatever the approach, the RC will determine our noise power bandwidth – this will be approximately 1.57 * (1/2πRC) = Noise Power Bandwidth

Noise Calculation for SAR and ΔΣ ADC (cont'd)

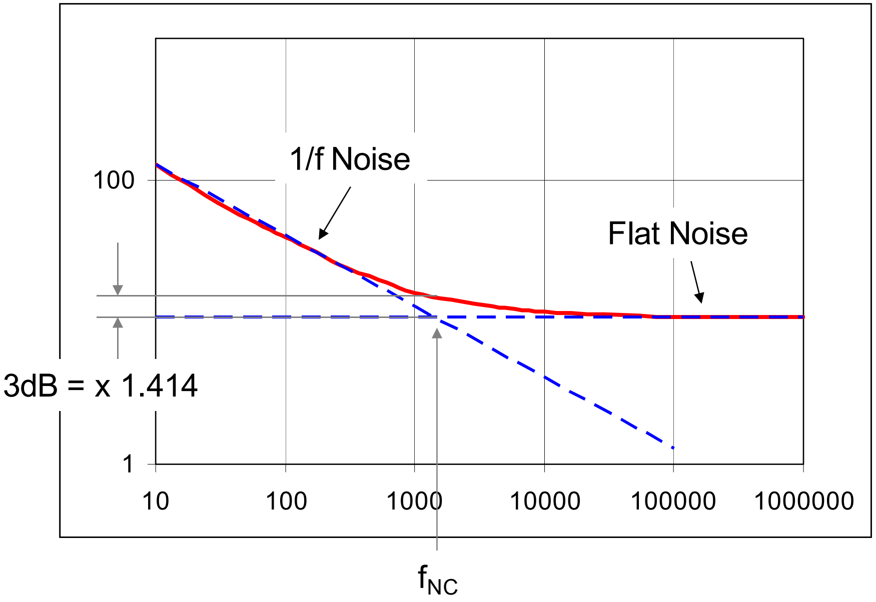
How to estimate the impact of 1/f noise.

Spot noise model: combine the effects of white noise & 1/f noise

Key parameter: F_{3dB} point, where the total noise power has increased 3dB from the flatband value.

$$e_{Total} = e_o \sqrt{1 + \frac{f_{NC}}{f_H - f_L} \ln \frac{f_H}{f_L}}$$

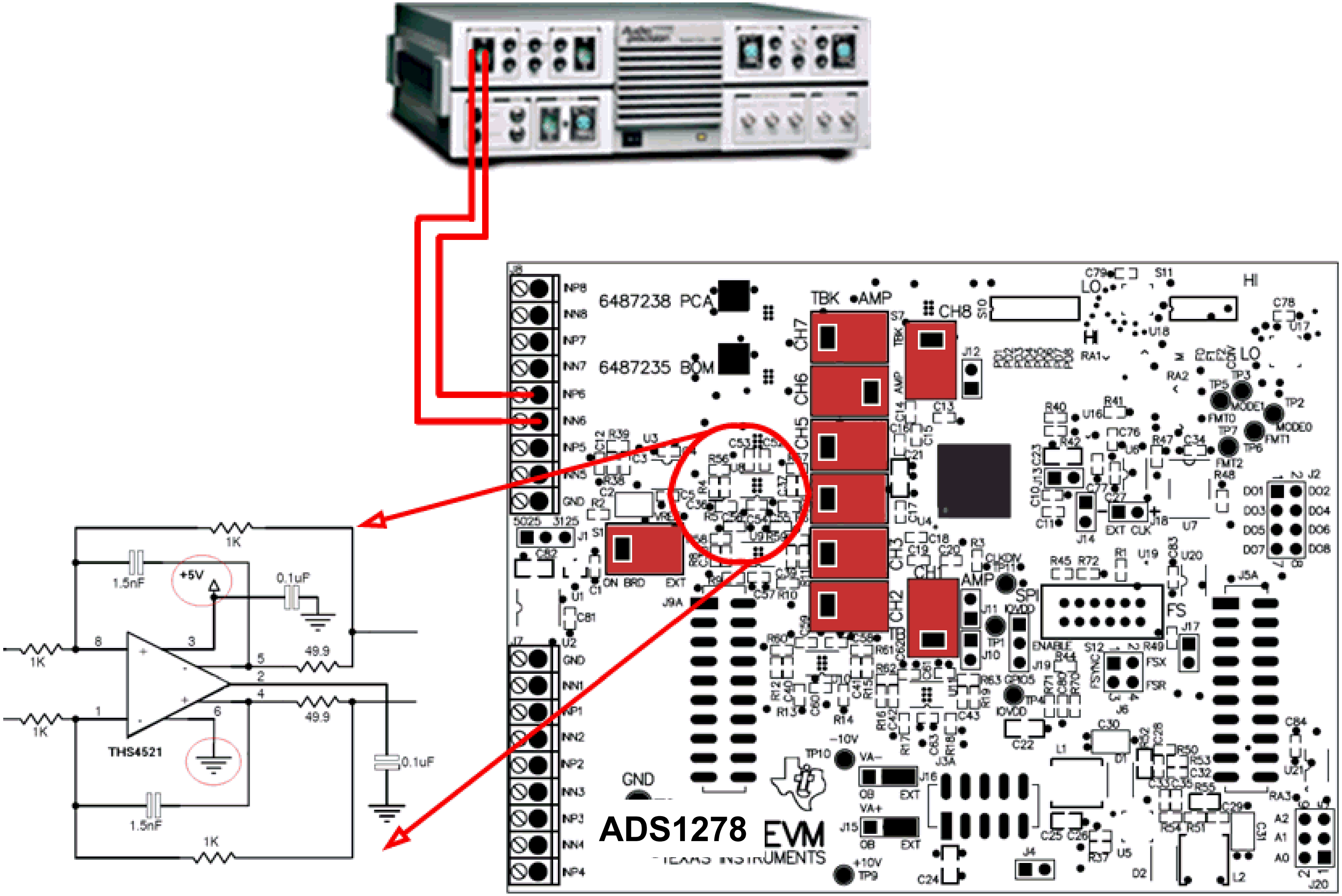
Where:
e_O = Flatband spot noise voltage.
f_{NC} = "Knee" frequency of the published noise curve. Frequency where 1/f noise power equals flat band noise power.
f_L = Lowest frequency
f_H = Noise power bandwidth



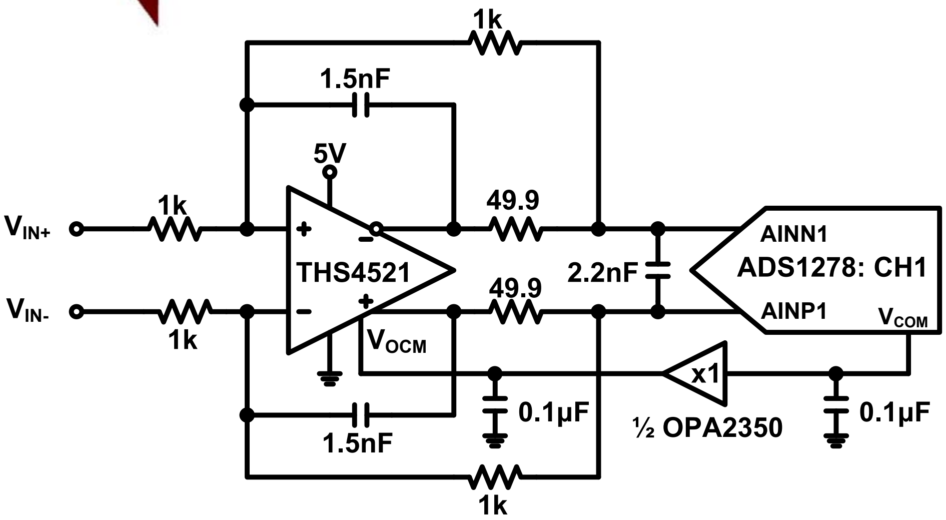
Given; f_L = 10Hz we get multiplication factor from everything in the radical as shown versus f_H

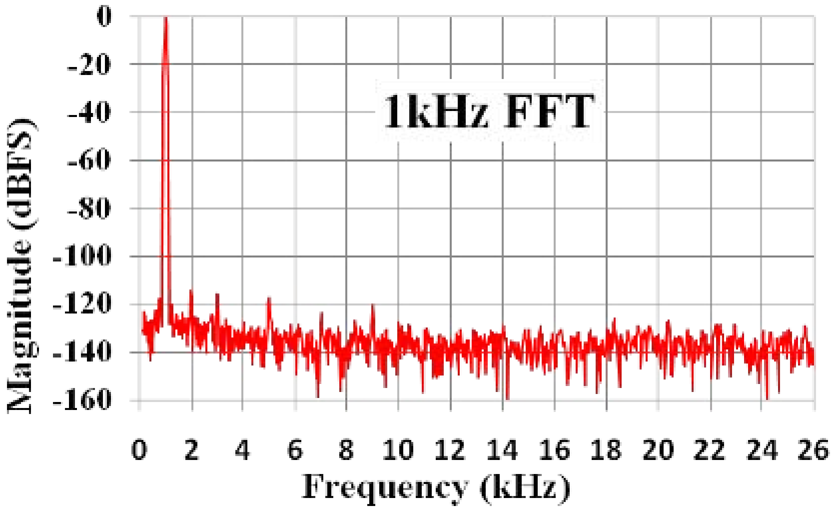
f_H	multiplication factor
1kHz	6.89
10kHz	2.81
100kHz	1.39
1MHz	1.06
10MHz	1.01

THS4521 FDA + ADS1278 Δ ∑ ADC Test



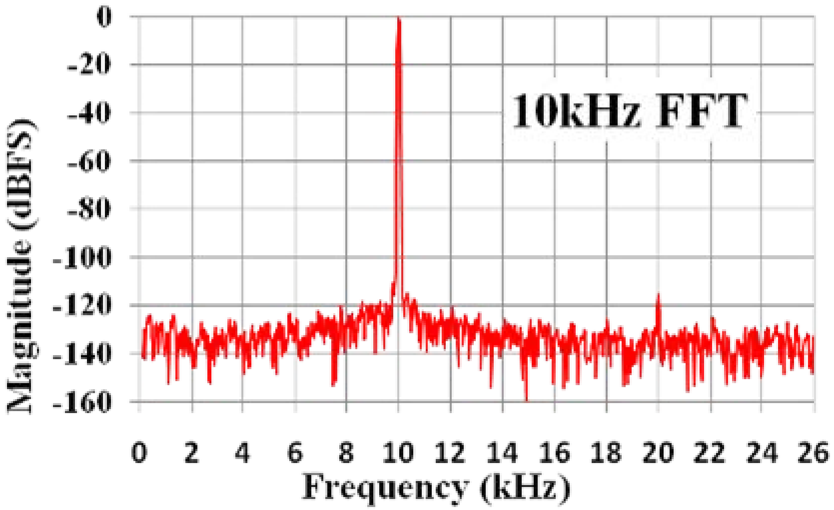
THS4521 + ADS1278 Performance





AC Analysis at f_{SAMPLE} = 52kSPS, input signal -0.5dBFS

Configuration	Freq (kHz)	SNR (dBc)	THD (dBc)	SINAD (dBc)	SFDR (dBc)
THS4521 + ADS1278	1	109	-108	105	114
THS4521 + ADS1278	10	102	-110	101	110
ADS1278 data sheet spec	1	110	-108	NA	109

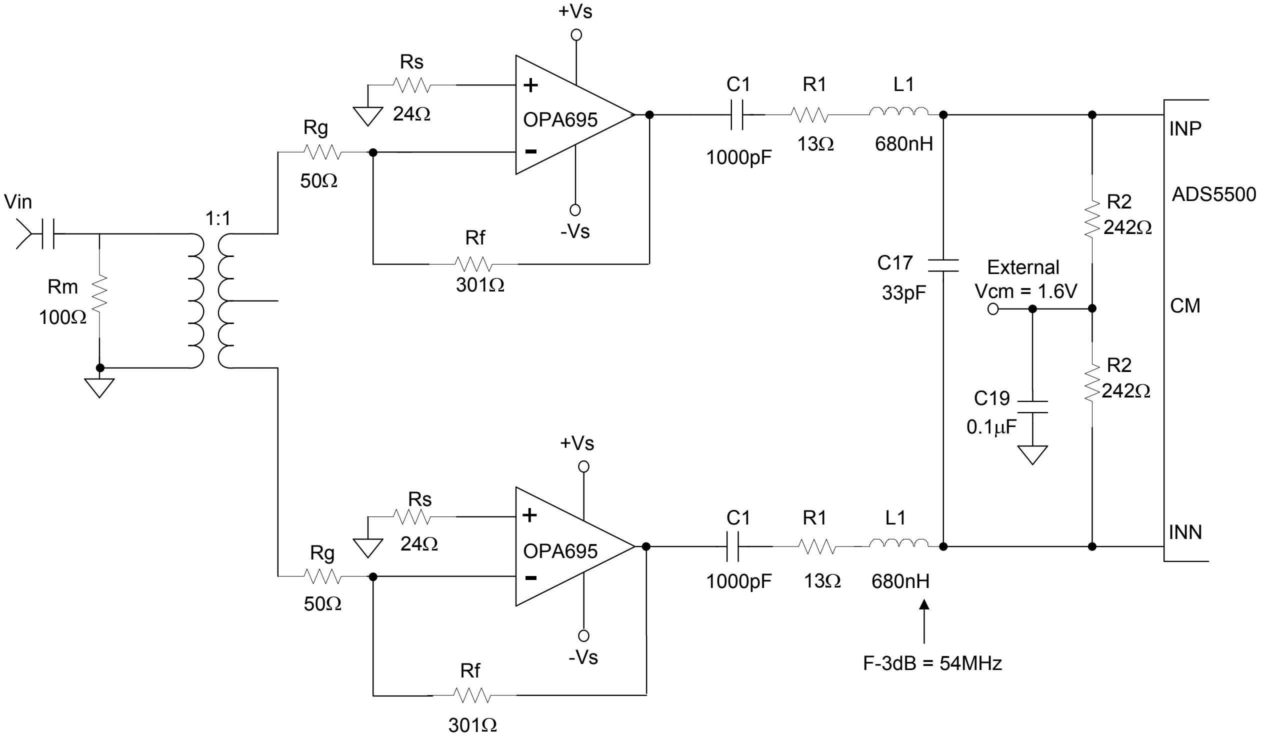


Design Example: 1st Nyquist Sampling (Base-Band)

In some ways, this application is one of the most difficult –

- Signal bandwidth is usually as significant portion of the Nyquist frequency.
  => relatively high noise bandwidth for the last stage.
- A broadband application demands that the filter pass even order terms.
  - Even order suppression is very important for both single & multi-tone products.
  - Places more demands on the driver amp.
- Contrast with narrowband IF applications:
  - A bandpass filter attenuates even order distortion products.
  - HD2 could be relaxed for a driver circuit.
- Currently, the most promising circuit has been an inverting differential topology.
  - Source is coupled in through a step up transformer.
- This circuit has been tested using both op amps and FDA's.
- Most applications are not DC coupled, so a high pass filter is expected – this will come both from the transformer input and the post-filter implementation.

Design Example: 1st Nyquist Sampling (Base-Band) (cont'd)



Apply this approach for a baseband (1st Nyquist Zone) ADS5500 interface.

- A very broadband current feedback op amp is used in the test circuit shown above.
- +/-5V supplies gives 12mA/Channel, 240mW quiescent power for the two amplifiers.
- Design target was a 2MHz to 40Mhz pass-band.
- Low-end cutoff is set by the transformer.
- Signal gain is 15.1dB.

Design Example: 1st Nyquist Sampling (Base-Band) (cont'd)

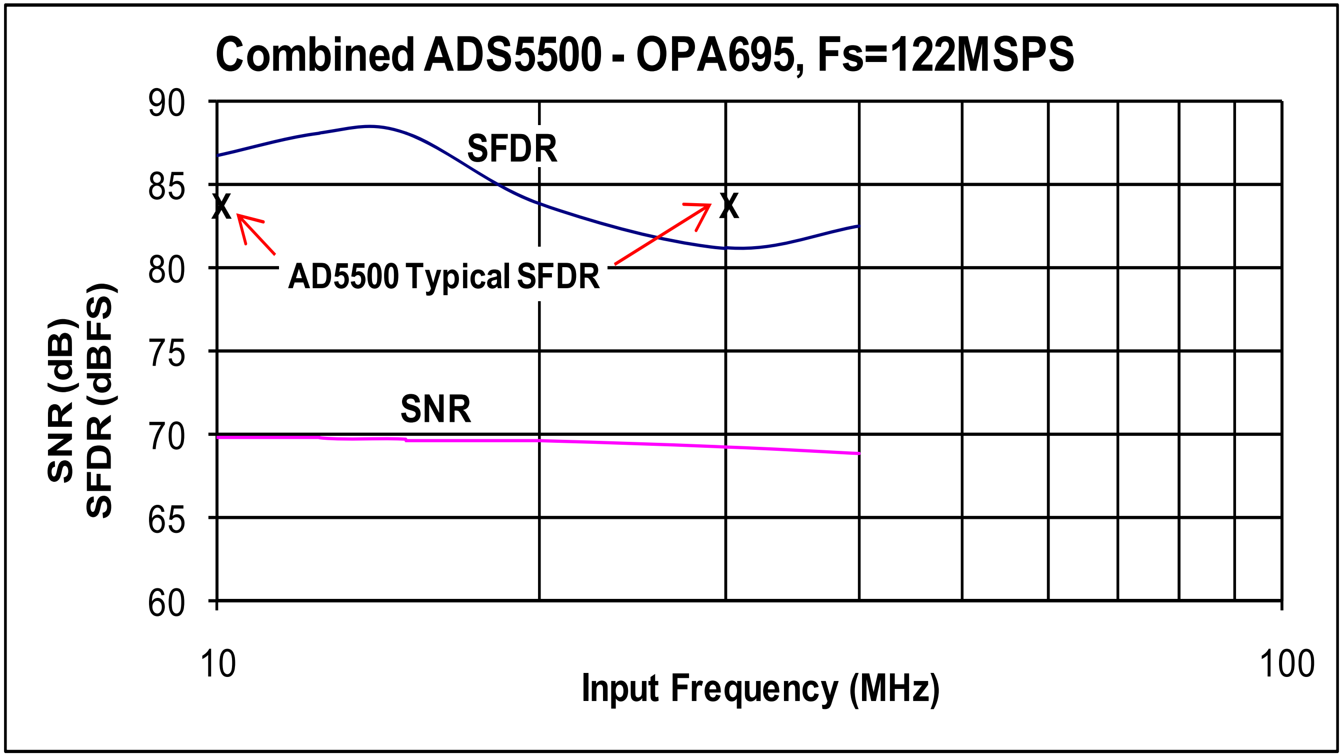
One of the first things we can look at in this interface is the SNR calculation.

The ADS5500 (14bit, 125MSPS) literature specifies a 71.5dB SNR at frequencies up to 50MHz
- 2.3Vpp maximum differential input.

Operating at -1dB below full scale, this would be adjusted to 2.05Vpp differential input and 70.5dB SNR for the converter.

The postfilter is a 54Mhz cutoff Butterworth filter
- This 2nd order filter has a noise power bandwidth that is 1.11*F-3dB which gives a 60Mhz noise power bandwidth for the spot noise being delivered at the amplifier outputs.
- This filter design is discuss in more detail in the application note listed below
- The next slide shows the combined SNR calculations loading in the all the required numbers for this design.
- This interface provides a 75.6dB SNR up to the converter inputs which should result in a combined SNR of 69.3dB.

Combined ADS5500 + OPA695 Performance

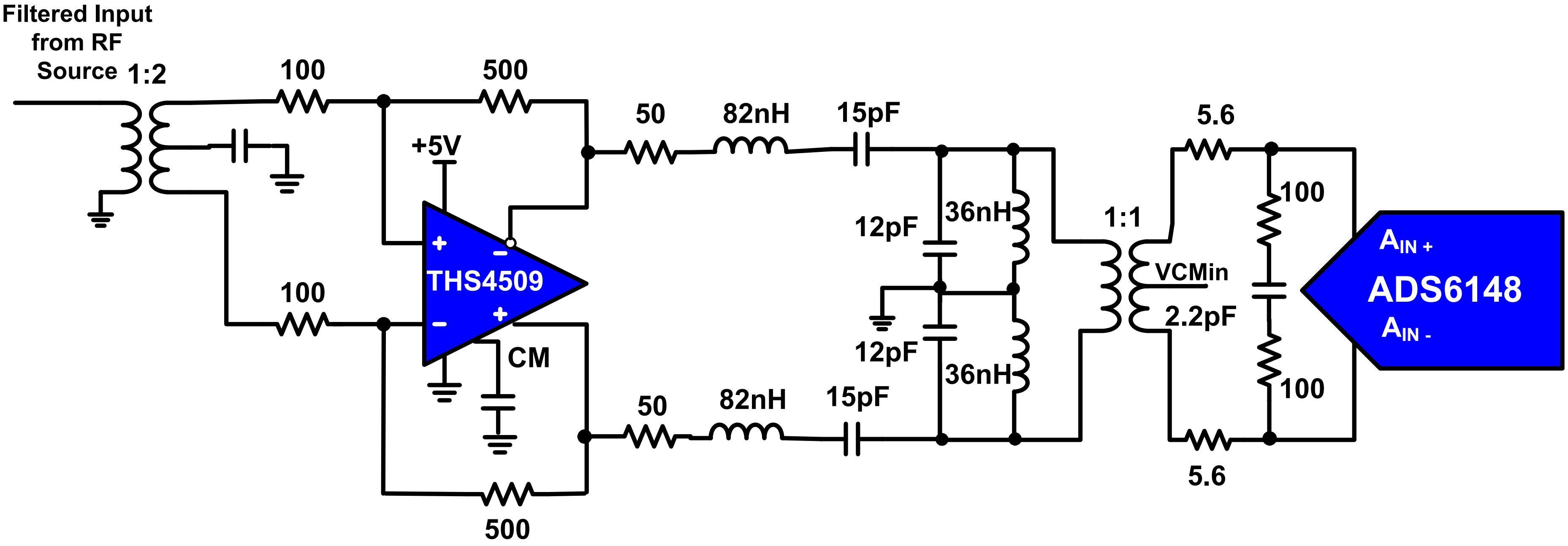


- SFDR did not follow the linear combination as expected, but varied between the amplifier or the higher order converter terms, whichever was dominant
- SNR was slightly better than predicted

Design Example: Narrow Band IF Undersampling Using THS4509 + ADS6148

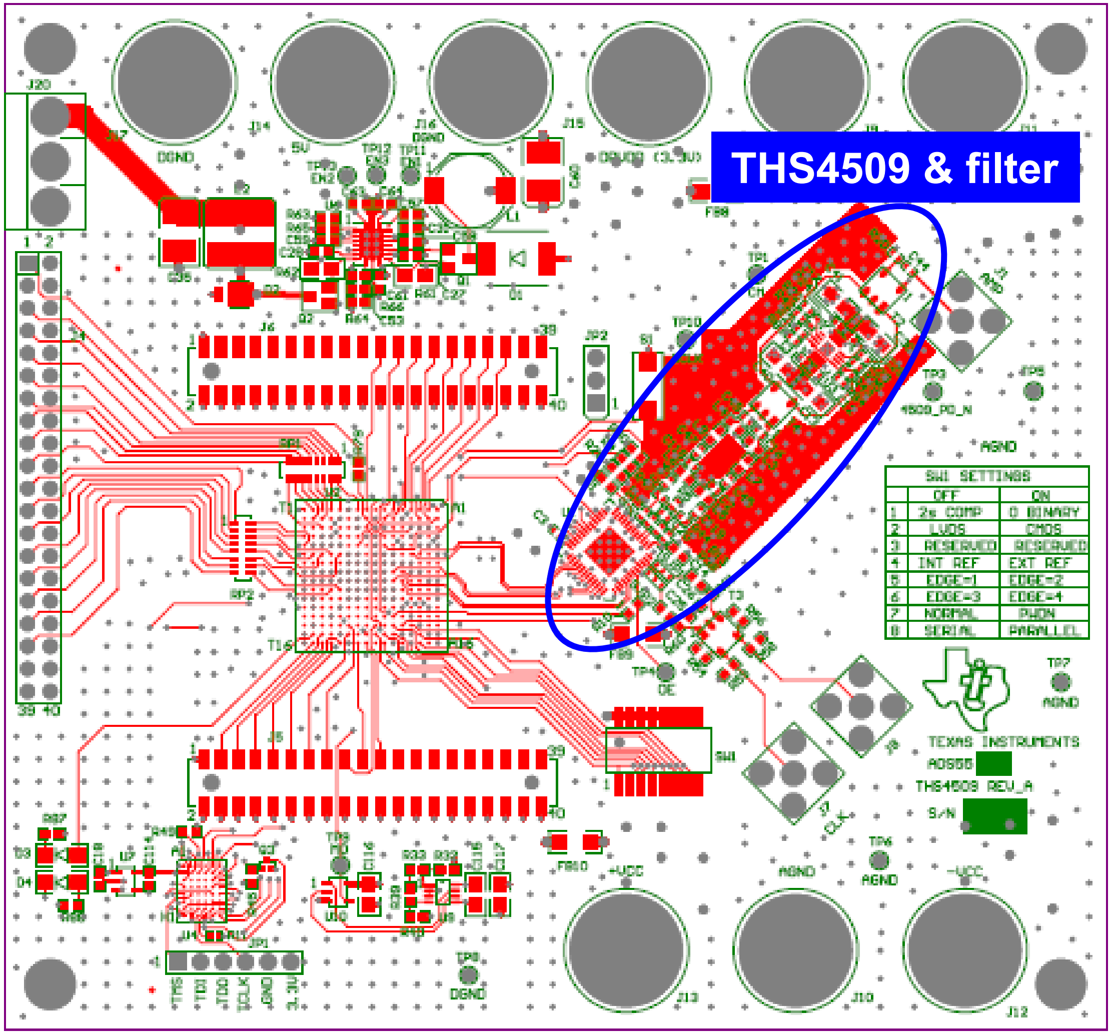
◆ THS4509 driving ADS6148 thru an RLC band-pass filter and transformer.

  - Fs = 190MHz
  - 2nd Nyquist zone



Design Example: Narrow Band IF Undersampling Using THS4509 + ADS6148 (cont'd)

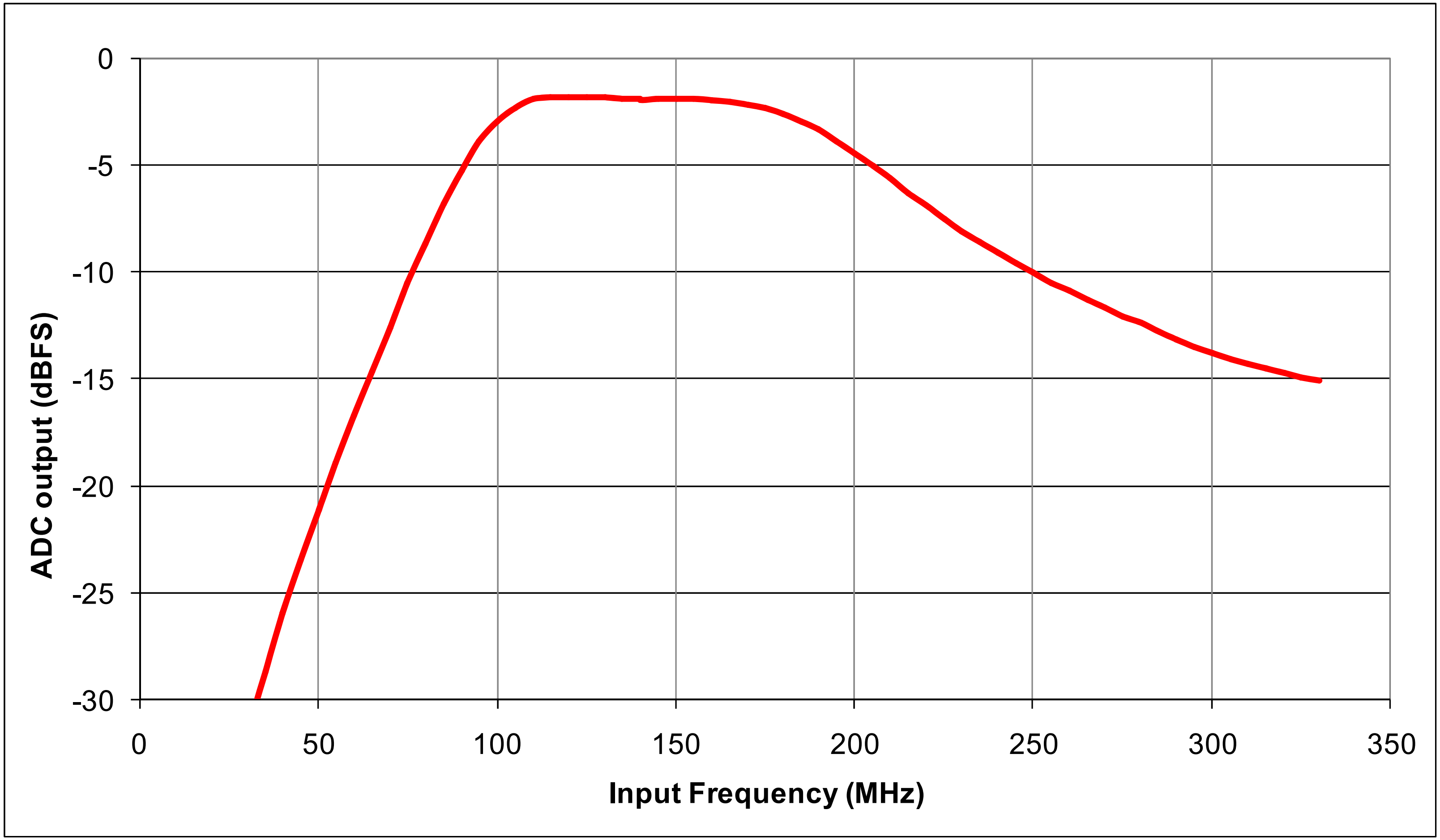
THS4509 & ADS6128 EVM Top Layer


THS4509 & filter

SW1 SETTINGS		
	OFF	ON
1	2s COMP	0 BINARY
2	LVDS	CMOS
3	RESERVED	RESERVED
4	INT REF	EXT REF
5	EDGE=1	EDGE=2
6	EDGE=3	EDGE=4
7	NORMAL	PWDN
8	SERIAL	PARALLEL

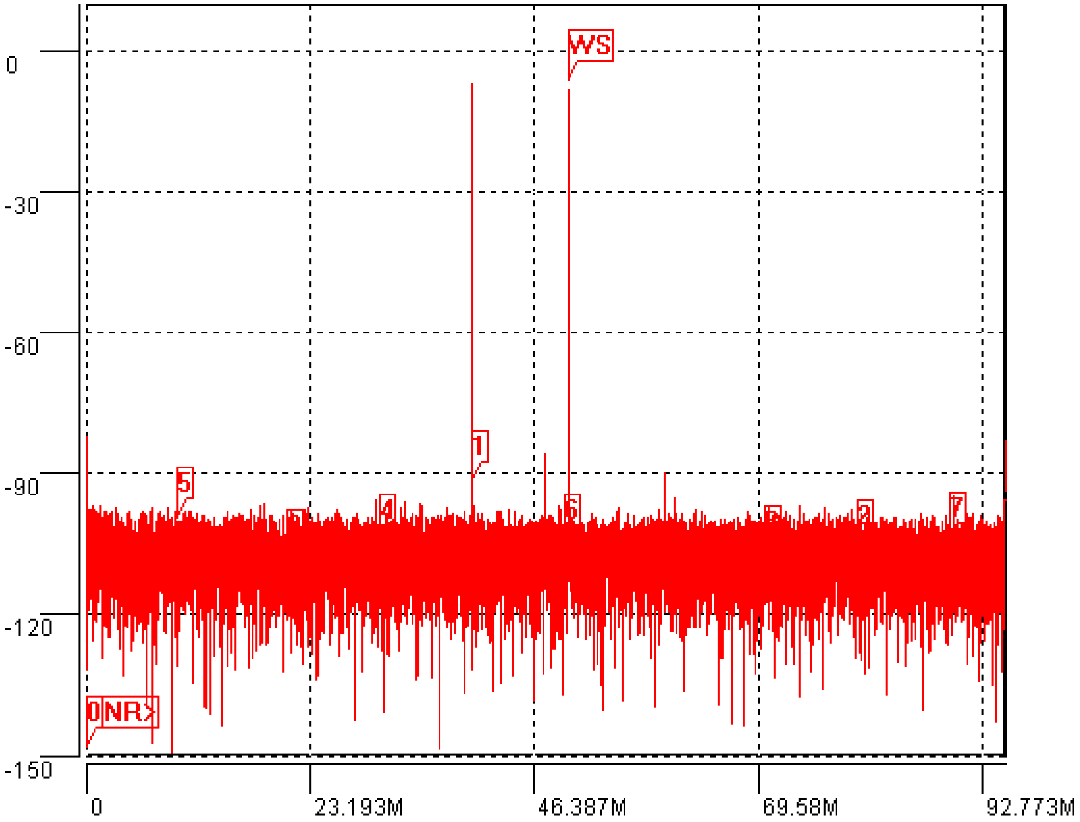
Design Example: Narrow Band IF Undersampling Using THS4509 + ADS6148 (cont'd)

Amp/Filter/ADC Frequency Response



Design Example: Narrow Band IF Undersampling Using THS4509 + ADS6148 (cont'd)

Two-tone FFT Plot
f1 = 140MHz, f2 = 150MHz



Design Example:
High SFDR ADC at 100MHz IF

THS770006 Driving ADS5493 Tests using ADS5493 EVM

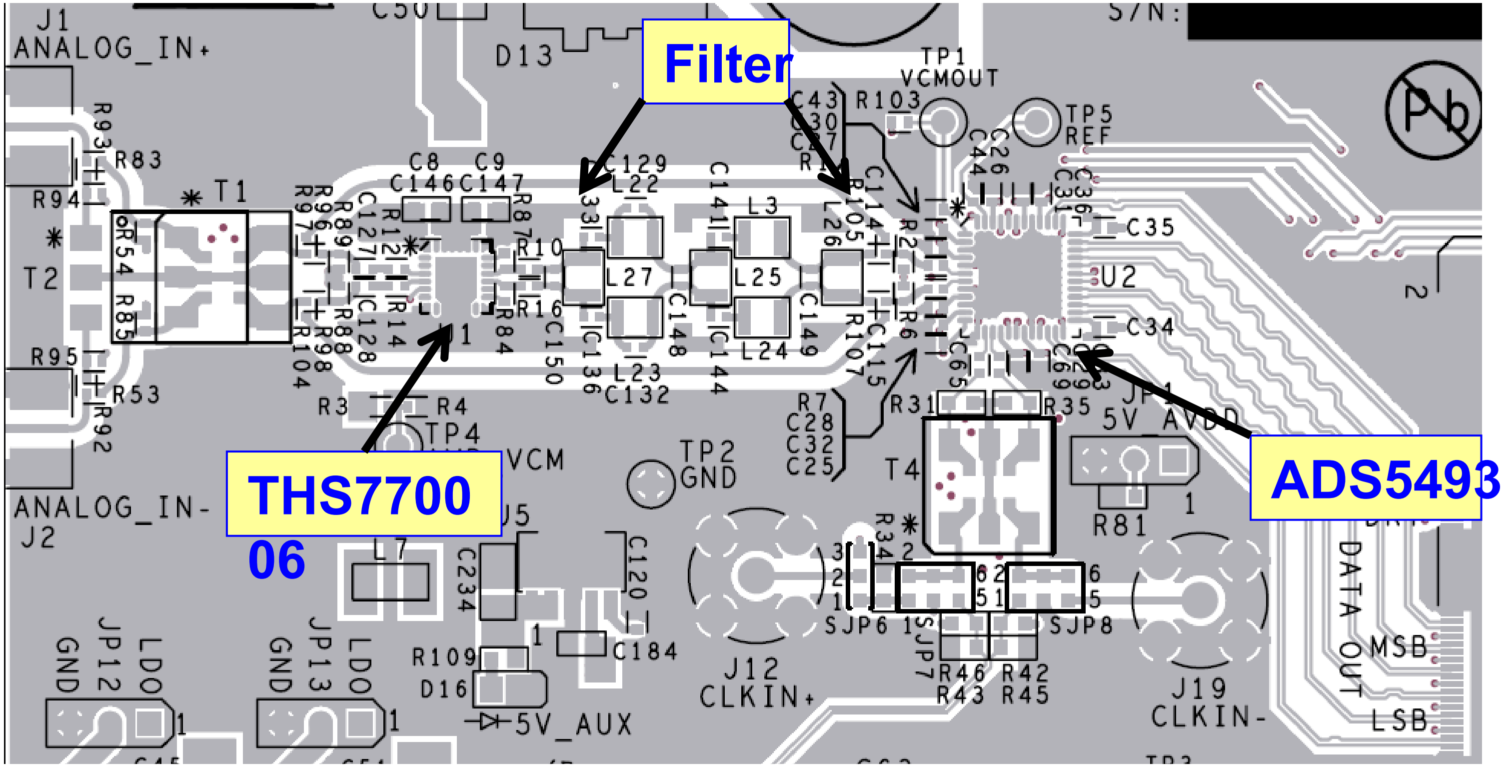
Information presented reflects ongoing work

ADS5493 Key Interface Specs

- ADS5493 Key Interface Specs
  - 16-bit
  - 130MSPS
  - 3.15V analog input common mode
  - 1.5Vpp to 2.5Vpp FS analog input differential mode
  - 2kΩ resistive analog input differential impedance
  - 4.6pF to 5.6pF each analog input to ground (depending on PCB layout)
  - SNR = 75.4dBFS (typ) at F_{IN} = 100MHz
  - SFDR = 100dBc (typ) at F_{IN} = 100MHz
  - HD_2 = 102dBc (typ) at F_{IN} = 100MHz
  - HD_3 = 100dBc (typ) at F_{IN} = 100MHz

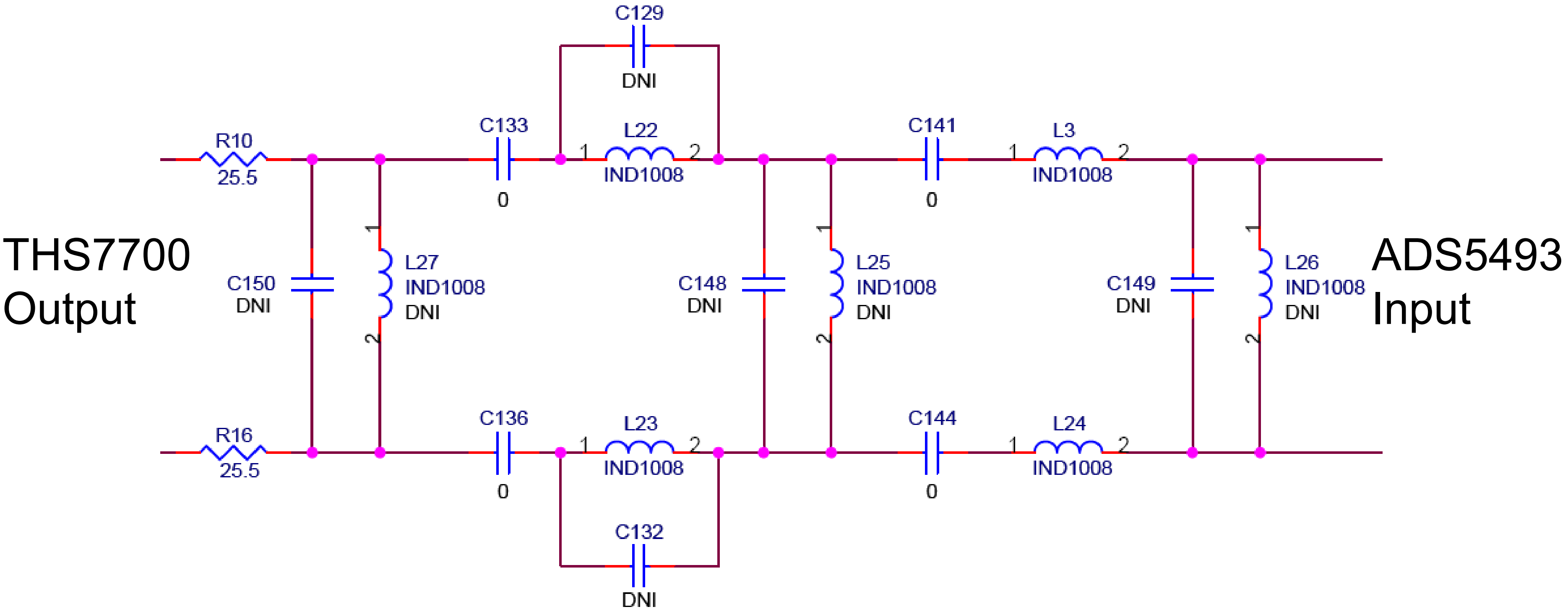
ADS5493 EVM Layout

- Note symmetrical layout of circuit is critical for best differential performance

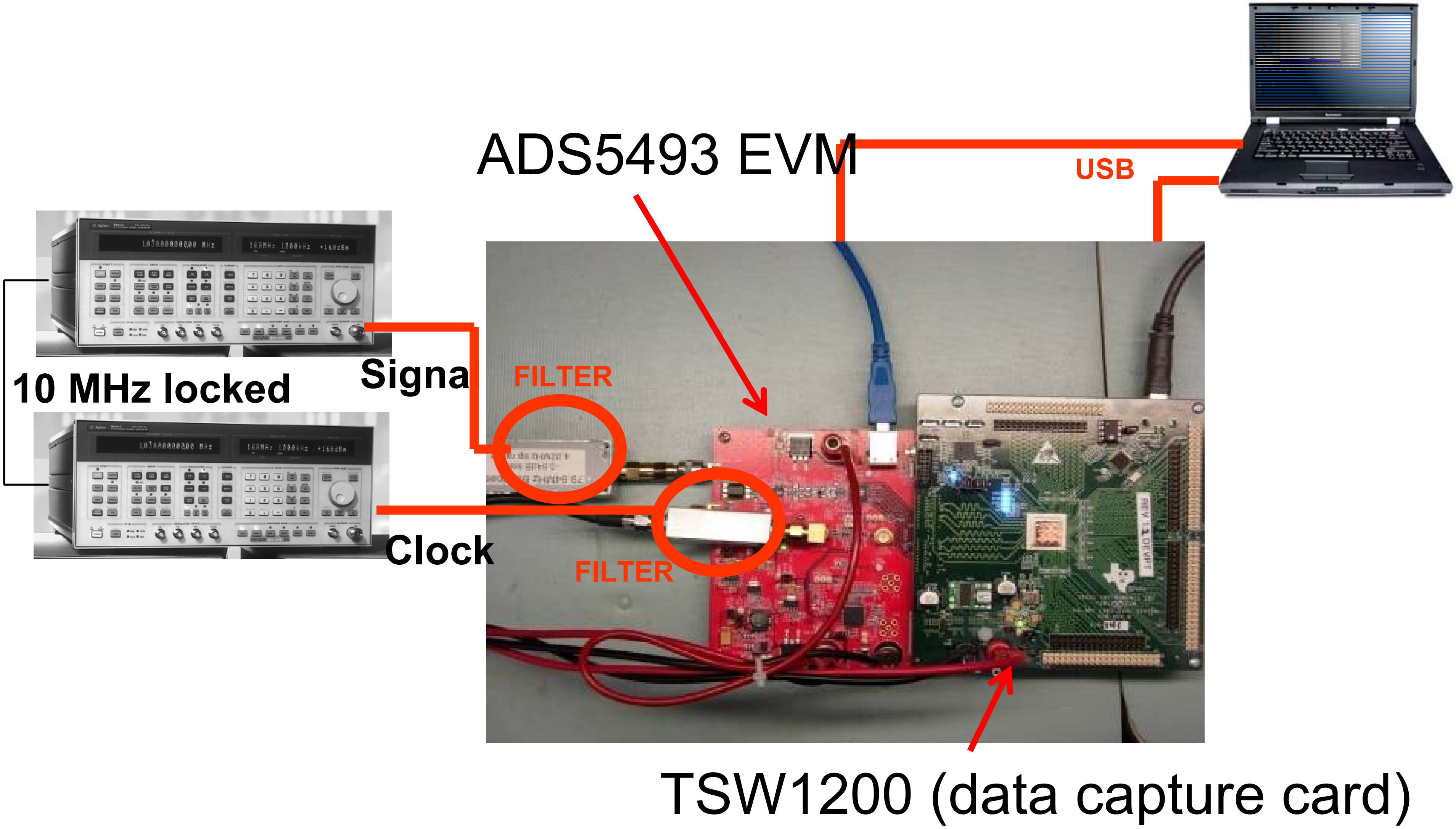


ADS5493 EVM Filter Schematic

- EVM has generic Circuit below for filtering between THS7700 and ADS5493



THS7700 + ADS5493 Test Setup



ADS5493 EVM

USB

10 MHz locked

Signal

FILTER

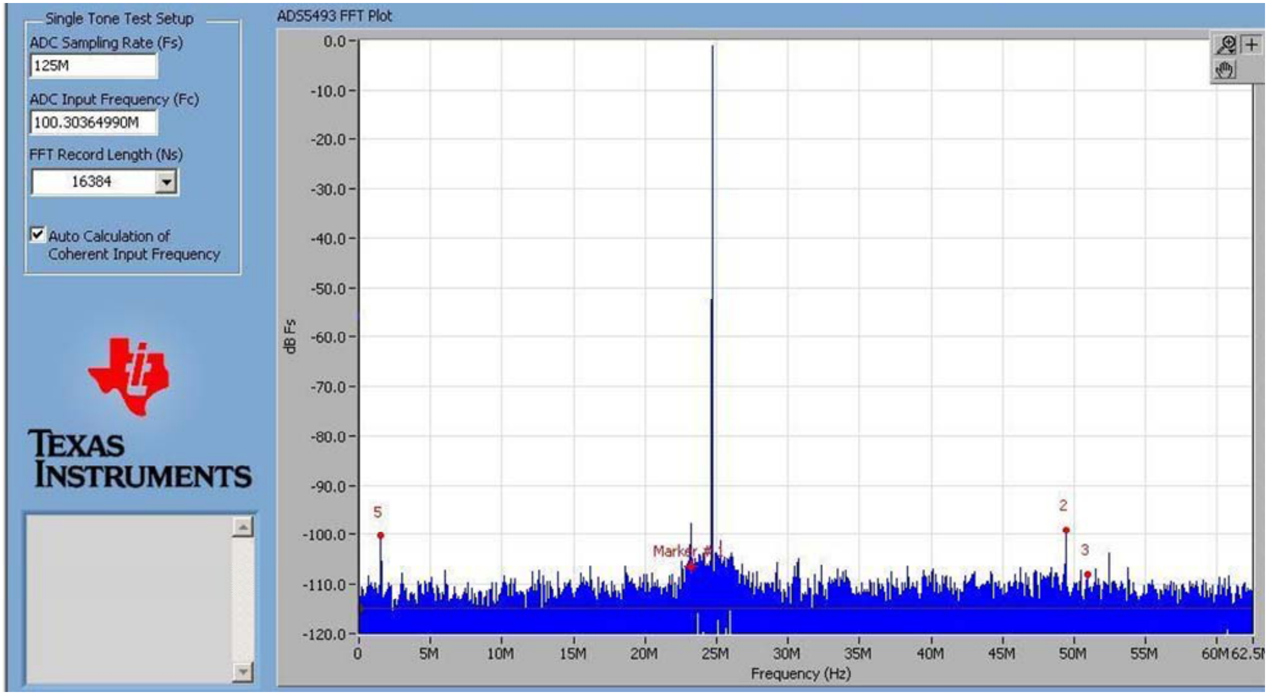
Clock

FILTER

TSW1200 (data capture card)

Single-Tone Performance Test Results:

BPF at 100MHz, F_{IN}=100.3MHz, F_{CLK}=125MHz



Single Tone Test Setup

ADC Sampling Rate (Fs): 125M

ADC Input Frequency (Fc): 100.30364990M

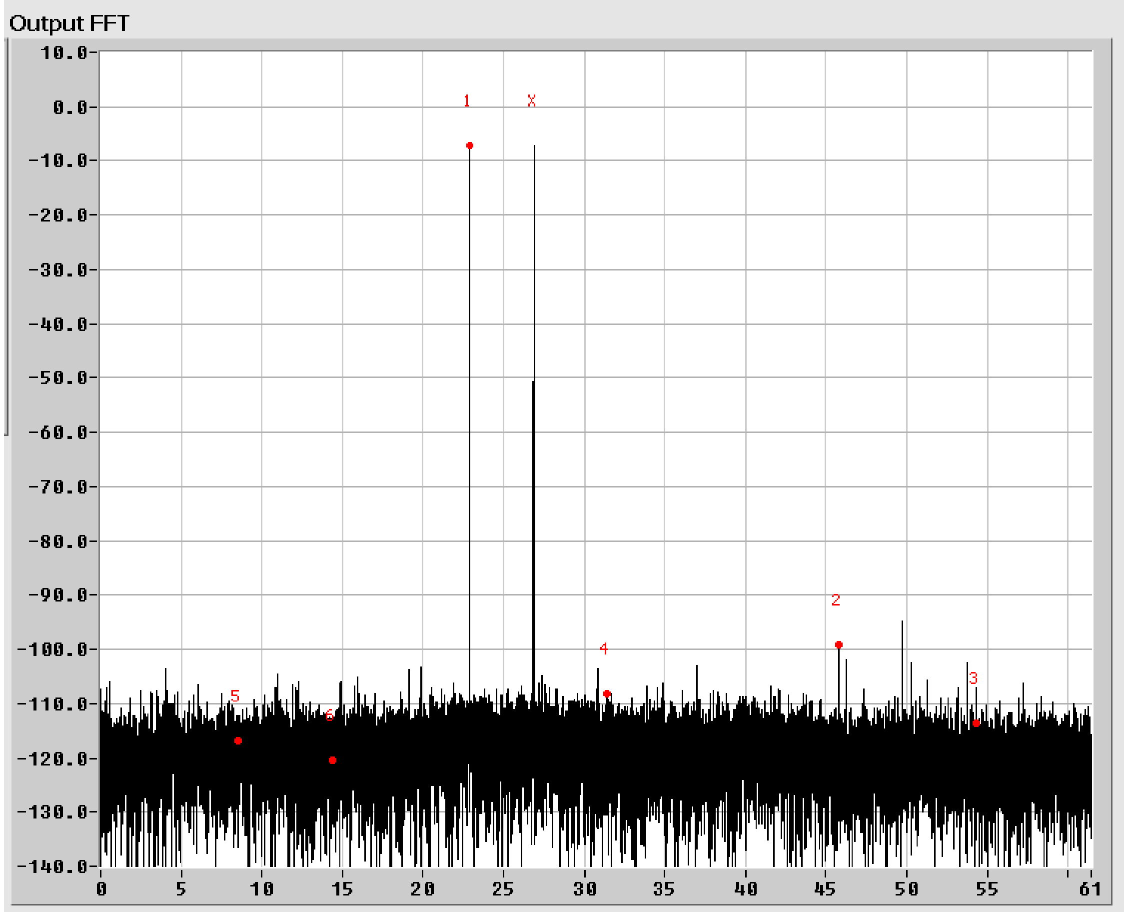
FFT Record Length (Ns): 16384

☑ Auto Calculation of Coherent Input Frequency

	ADC Input	SNR	HD2	HD3
THS770006 + BPF + ADS5493	-1dBFS	75.6dBFS	-98dBc	-107dBc
ADS5493 Spec (typ)	-1dBFS	75.4dBFS	-102dBc	-100dBc

Two-Tone Performance Test Results:

BPF at 100MHz, F_1=96MHz , F_2=100MHz, F_{CLK}=122.88MHz



Near in IMD3 spurs ≈ 100dBc

Thank you!