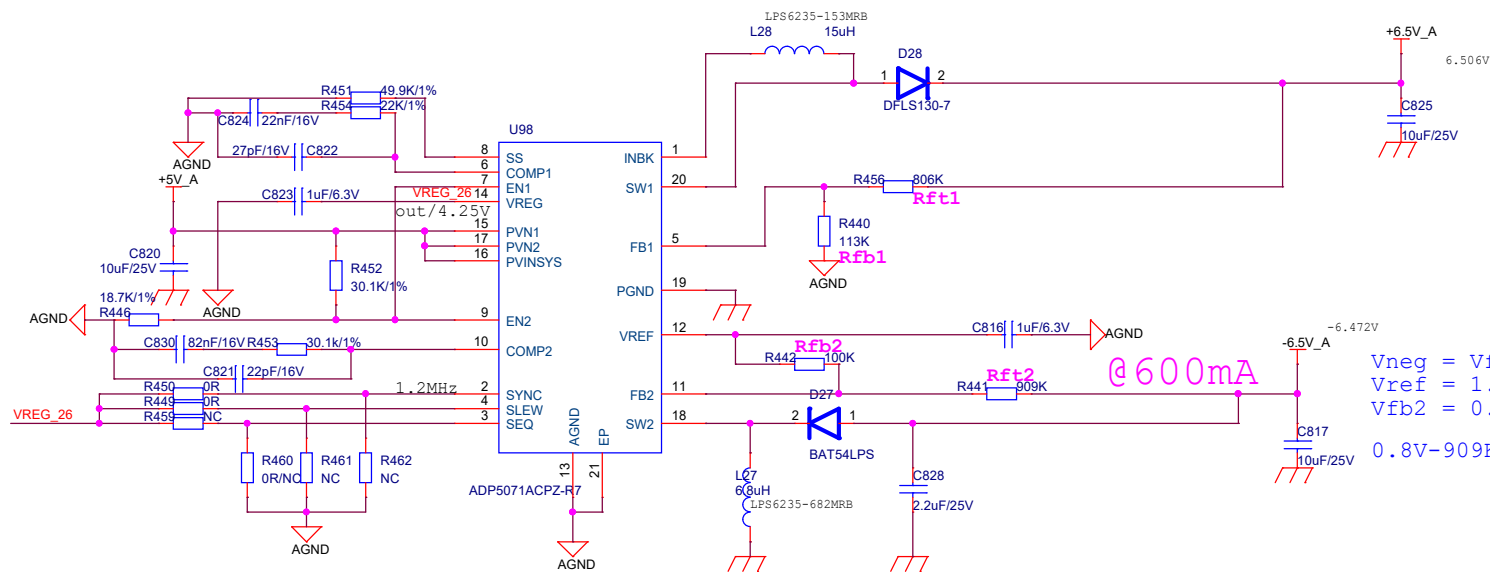


Title		
<Title> POWER_TREE		
Size	Document Number	Rev
B	<Doc>	<RevCode>
Date:	Tuesday, December 02, 2025	Sheet 1 of 19



**@1A**

$$V_{pos} = 0.8V \times (1 + R_{ft1}/R_{fb1})$$

$$0.8V \times (1 + 806K/113K) = 6.5V$$

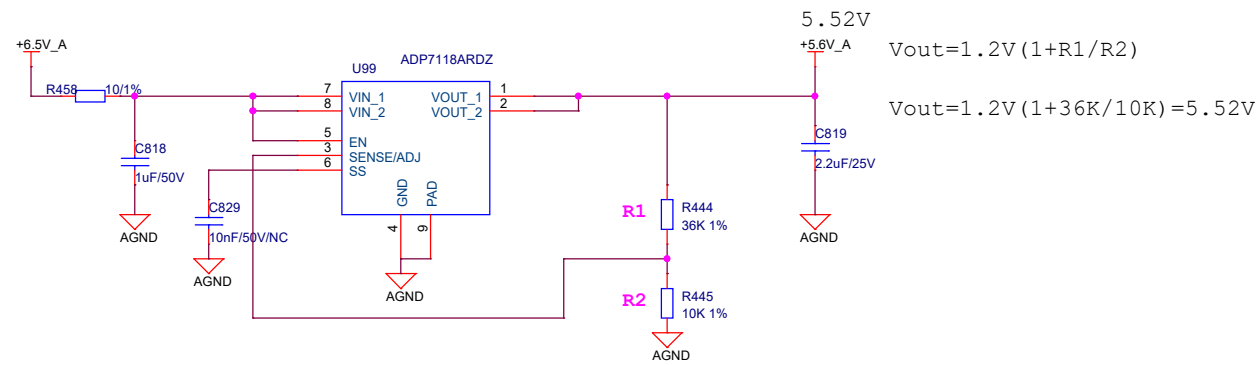
**@600mA**

$$V_{neg} = V_{fb2} - R_{ft2}/R_{fb2} (V_{ref} - V_{fb2})$$

$$V_{ref} = 1.60V$$

$$V_{fb2} = 0.8V$$

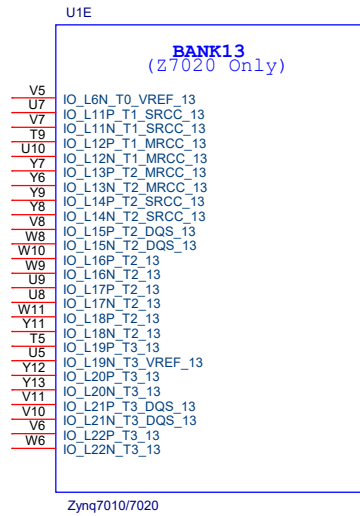
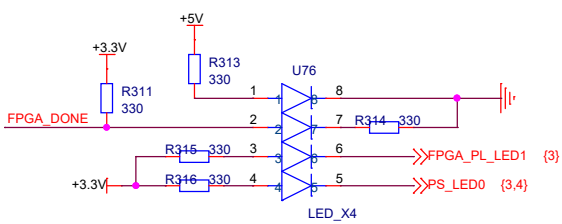
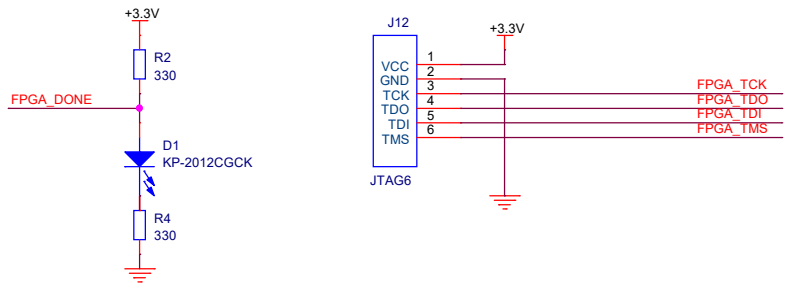
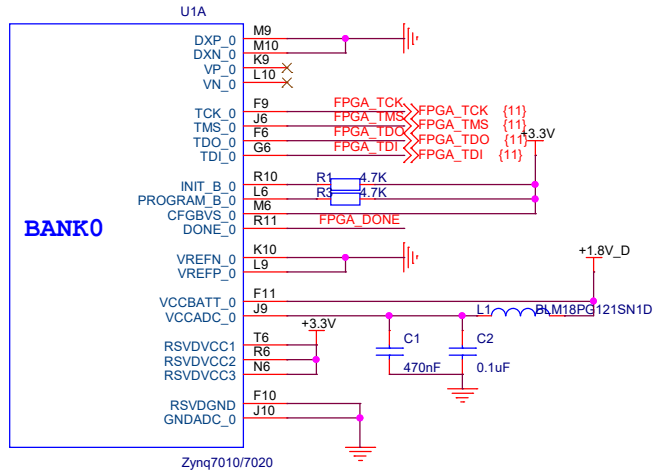
$$0.8V - 909K/100K (1.6 - 0.8) = -6.472V$$



$$V_{out} = 1.2V (1 + R1/R2)$$

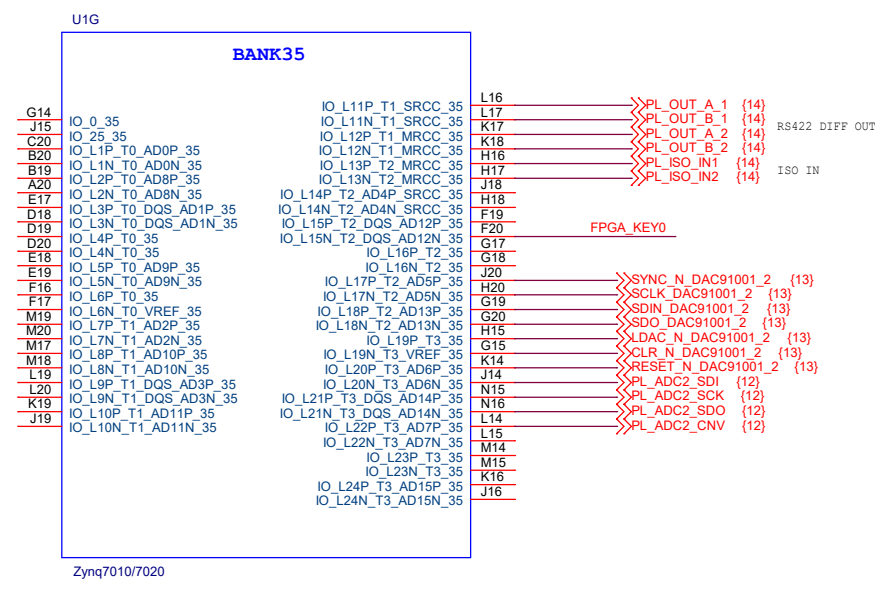
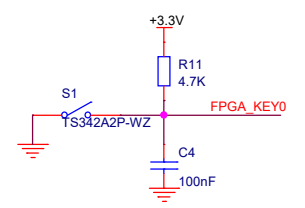
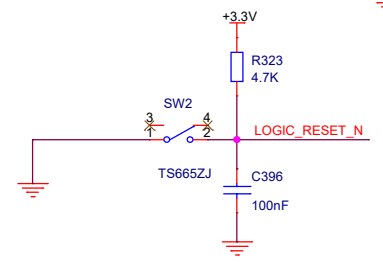
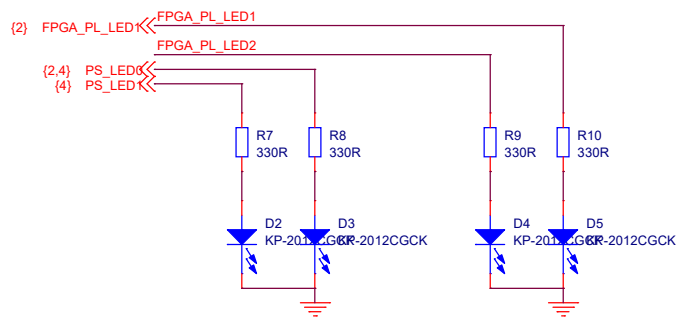
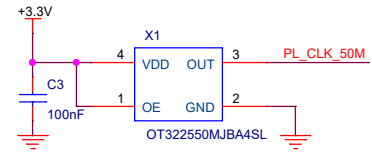
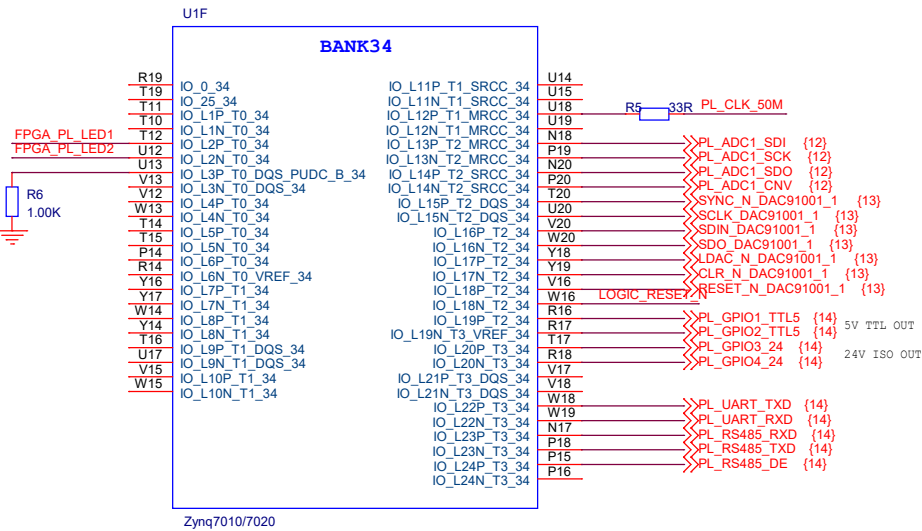
$$V_{out} = 1.2V (1 + 36K/10K) = 5.52V$$

Title			<Title>
Size	Document Number	Rev	
Custom	<Doc>	<RevCode>	
Date:	Tuesday, December 02, 2025	Sheet	17 of 19

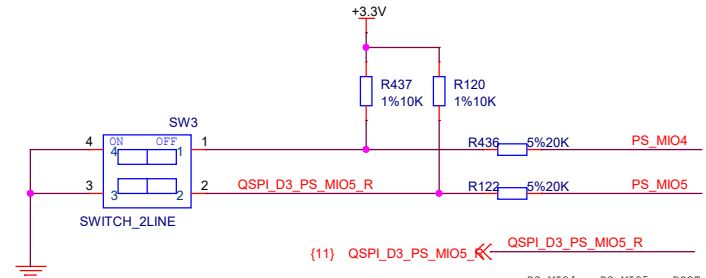
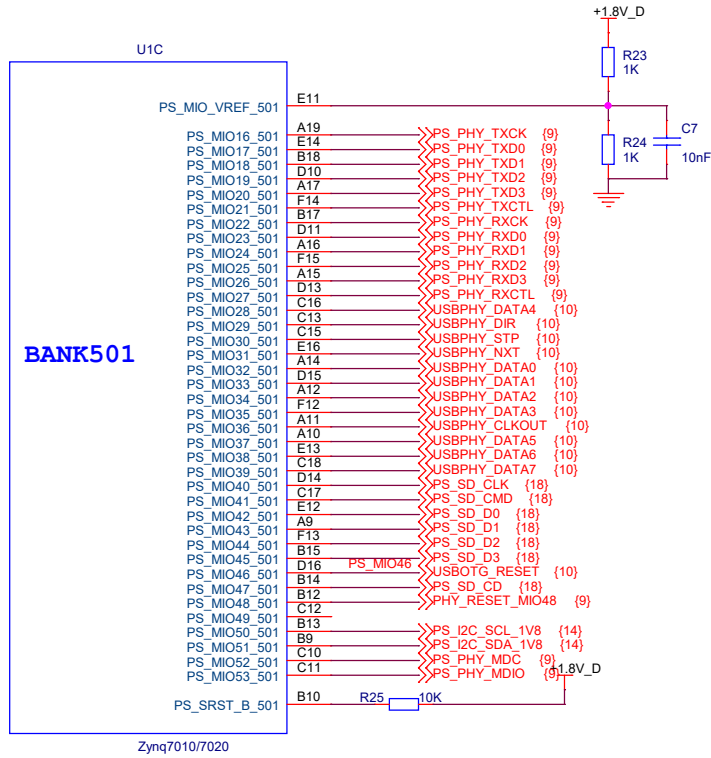
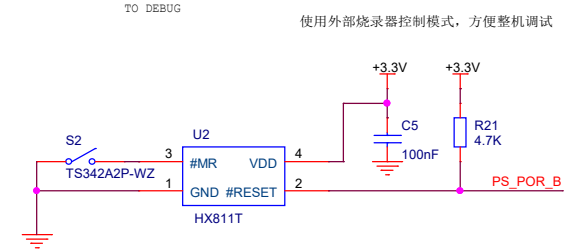
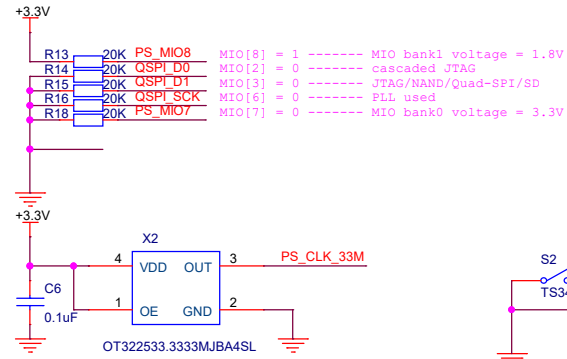
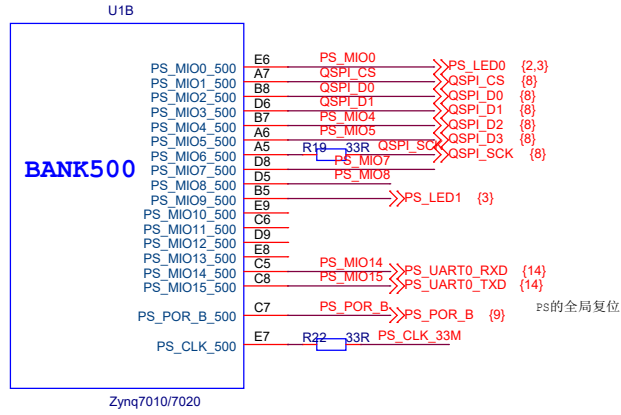


Title		
<Title> FPGA BANK0/BANK13		
Size	Document Number	Rev
B	<Doc>	<RevCode>
Date:	Tuesday, December 02, 2025	Sheet 2 of 19

PL端时钟接入全局时钟输入引脚中的一个



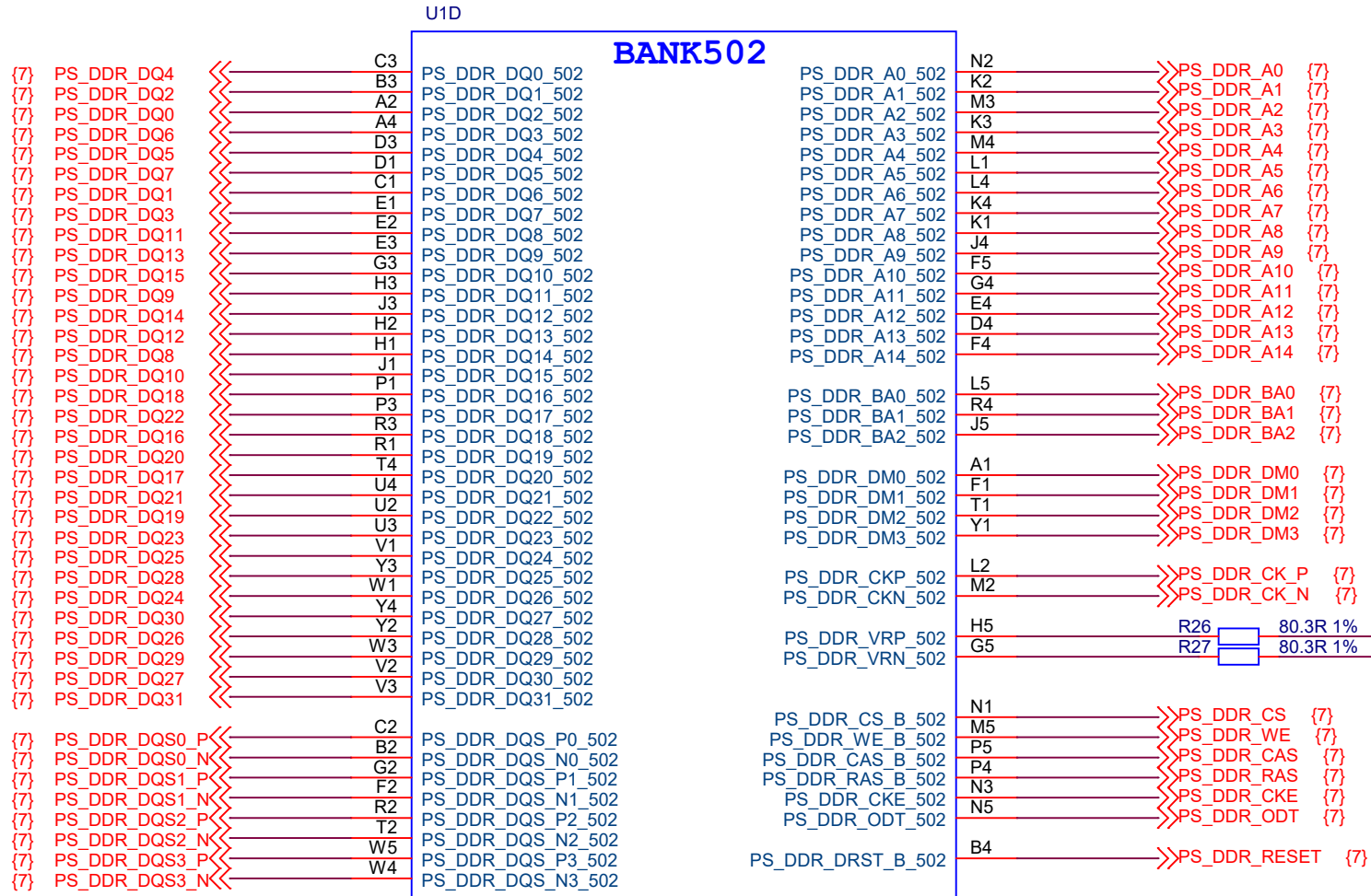
Title		
<Title> FPGA BANK34/BANK35		
Size	Document Number	Rev
B	<Doc>	<RevCode>
Date:	Tuesday, December 02, 2025	Sheet 3 of 19



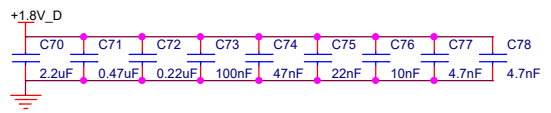
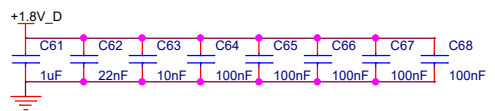
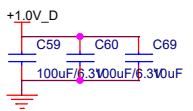
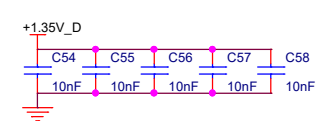
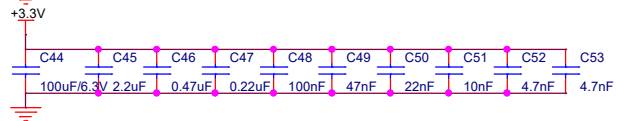
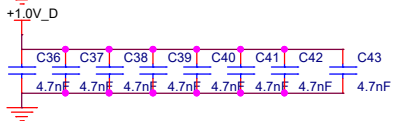
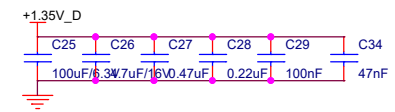
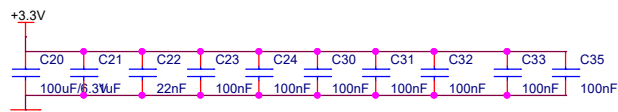
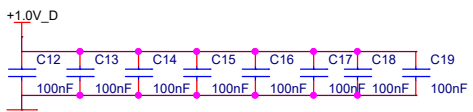
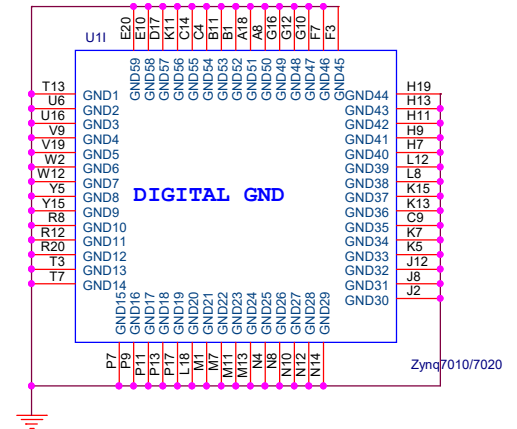
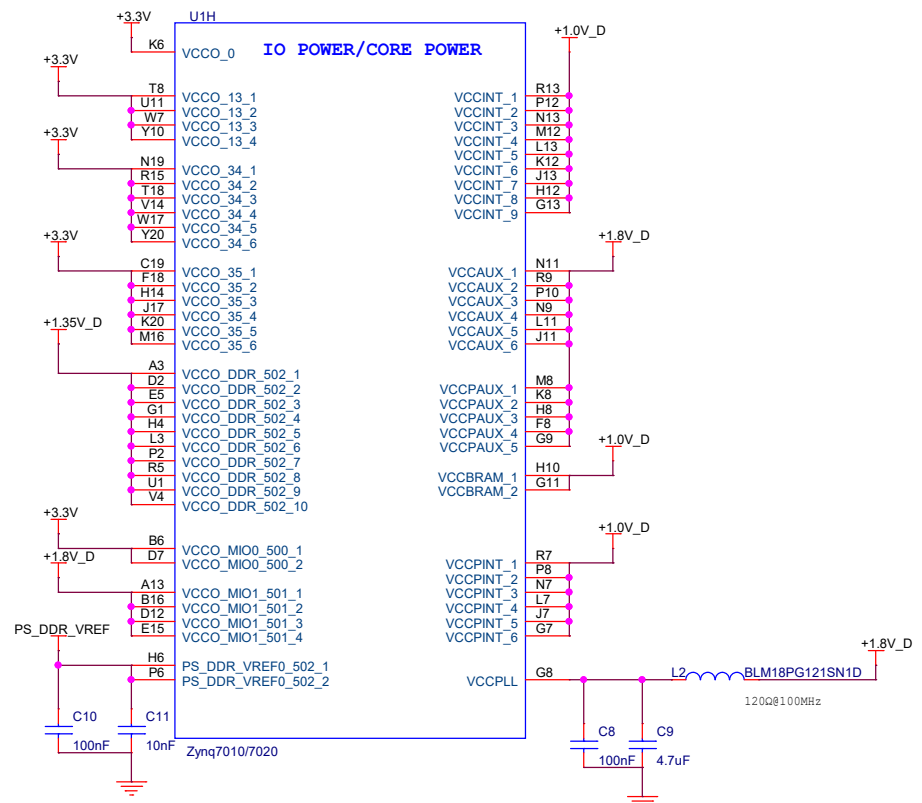
{11} QSPI\_D3\_PS\_MIO5\_R << QSPI\_D3\_PS\_MIO5\_R

PS_MIO4	PS_MIO5	BOOT MODE
0	0	JTAG
0	1	QSPI (default)
1	1	SD CARD

Title		<Title> FPGA BANK500/BANK501
Size	Document Number	Rev
B	<Doc>	<RevCode>
Date:	Tuesday, December 02, 2025	Sheet 4 of 19

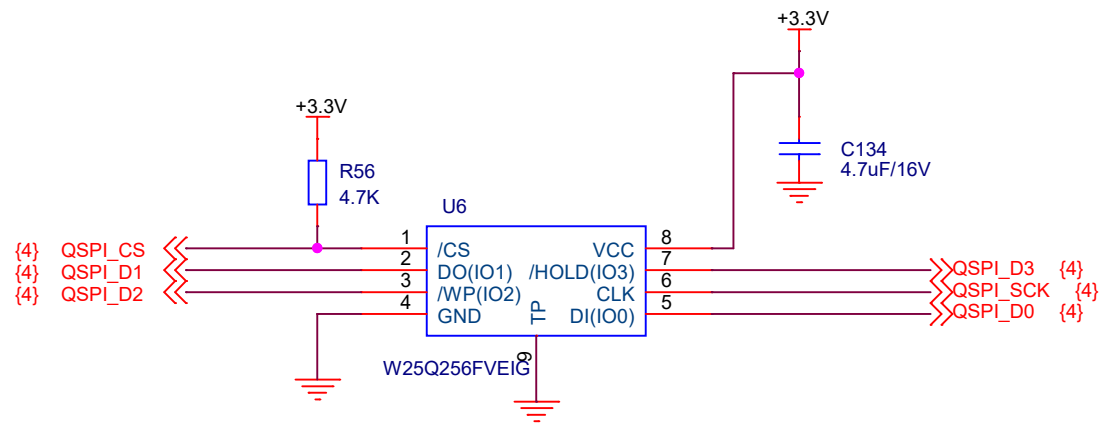


Title		
<Title> FPGA BANK502		
Size	Document Number	Rev
A	<Doc>	<RevCode>
Date: Tuesday, December 02, 2025		
Sheet	5	of 19



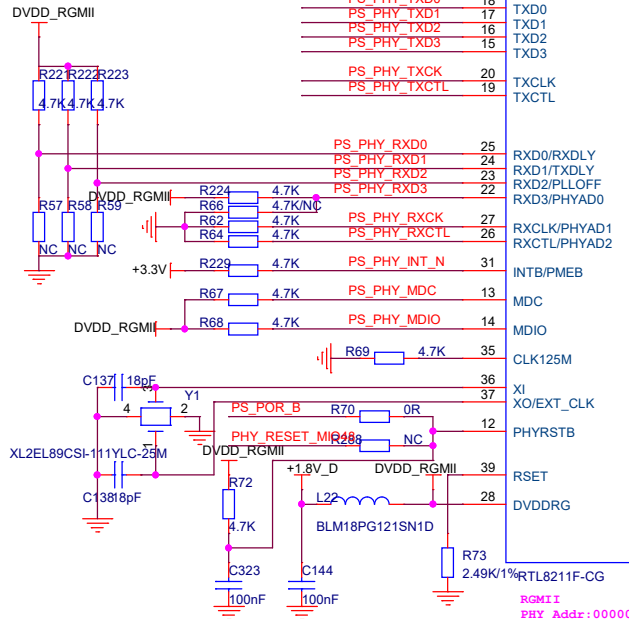
Title		<Title>	CORE/IO POWER
Size	Document Number	Rev	
B	<Doc>	<RevCode>	
Date:	Tuesday, December 02, 2025	Sheet	6 of 19





Title		
<Title> FLASH		
Size	Document Number	Rev
A	<Doc>	<RevCode>
Date:	Tuesday, December 02, 2025	Sheet 8 of 19

stop pll when entering ALDEFS mode  
 add 2ns delay to TXC for TXD latching  
 add 2ns delay to RXC for RXD latching

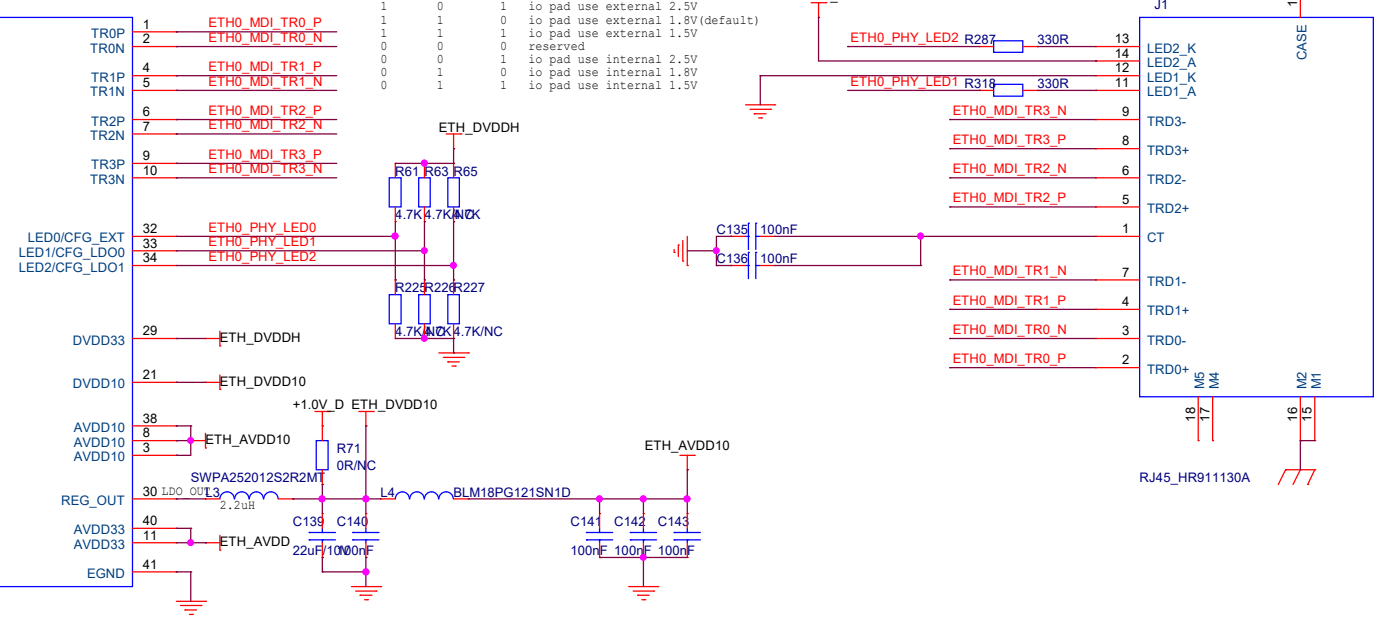


PS\_POR\_B上电之后拉高，然后就一直为高

RGMIID  
 PHY Addr: 00000

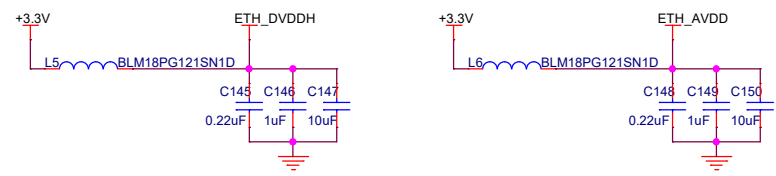
Y78531C 裕泰微代

CFG_EXT	CFG_LD01	CFG_LD00	
1	0	0	io pad use external 3.3V
1	0	1	io pad use external 2.5V
1	1	1	io pad use external 1.8V(default)
0	0	0	reserved
0	0	1	io pad use internal 2.5V
0	1	0	io pad use internal 1.8V
0	1	1	io pad use internal 1.5V

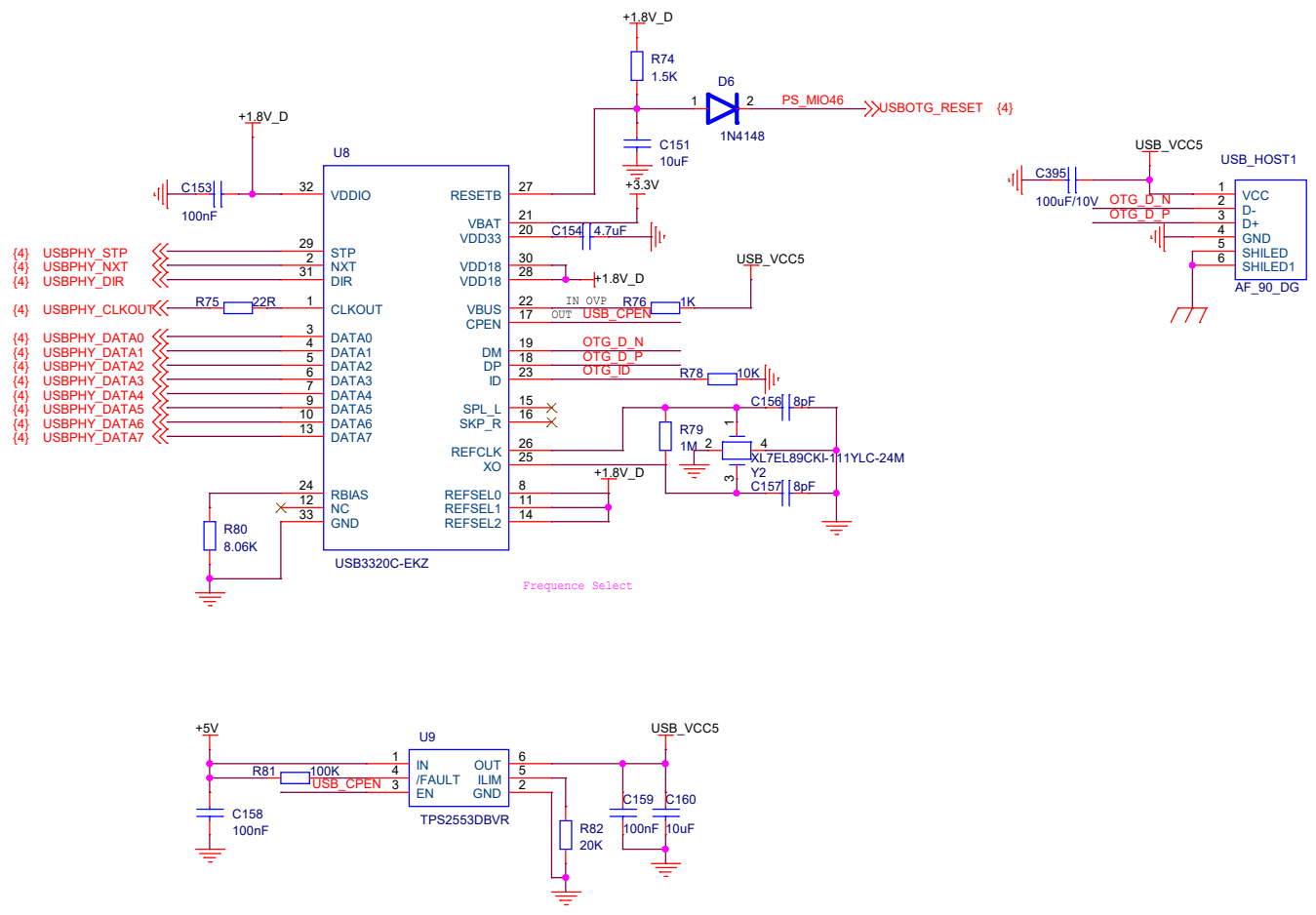


- (4) PS\_PHY\_TXD0 <-> PS\_PHY\_TXD0
- (4) PS\_PHY\_TXD2 <-> PS\_PHY\_TXD2
- (4) PS\_PHY\_TXD1 <-> PS\_PHY\_TXD1
- (4) PS\_PHY\_TXD3 <-> PS\_PHY\_TXD3
- (4) PS\_PHY\_TXCK <-> PS\_PHY\_TXCK
- (4) PS\_PHY\_TXCTL <-> PS\_PHY\_TXCTL
- (4) PS\_PHY\_RXD0 <-> PS\_PHY\_RXD0
- (4) PS\_PHY\_RXD2 <-> PS\_PHY\_RXD2
- (4) PS\_PHY\_RXD1 <-> PS\_PHY\_RXD1
- (4) PS\_PHY\_RXD3 <-> PS\_PHY\_RXD3
- (4) PS\_PHY\_RXCK <-> PS\_PHY\_RXCK
- (4) PS\_PHY\_RXCTL <-> PS\_PHY\_RXCTL
- (4) PS\_PHY\_MDC <-> PS\_PHY\_MDC
- (4) PS\_PHY\_MDIO <-> PS\_PHY\_MDIO
- (4) PHY\_RESET\_MIO48 <-> PHY\_RESET\_MIO48

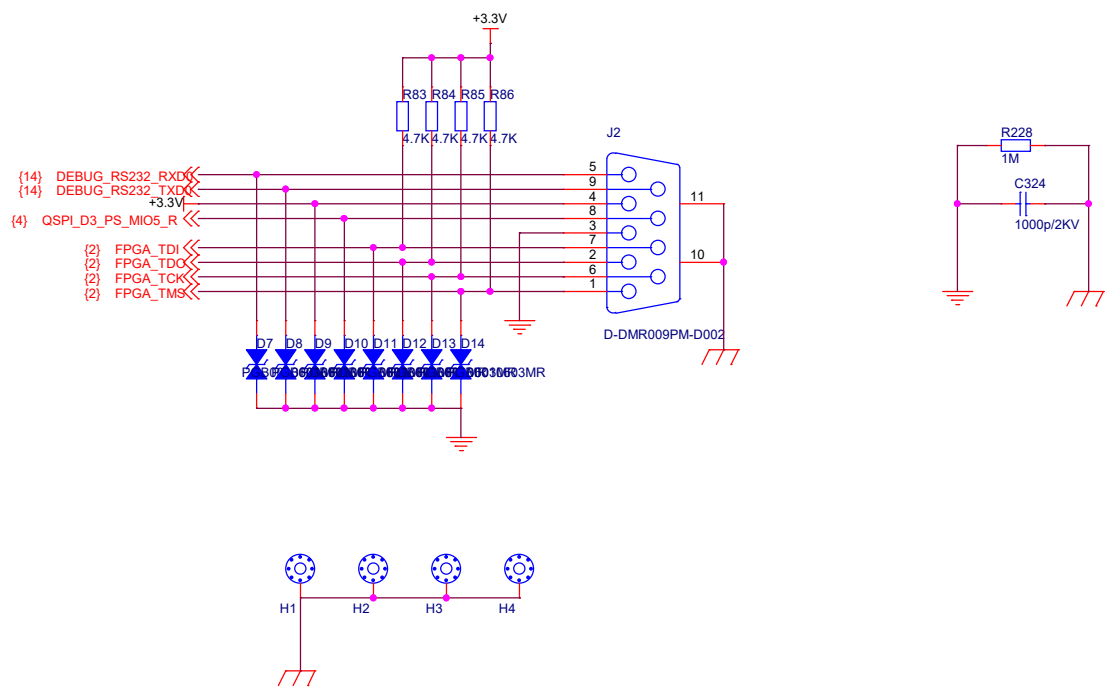
- (4) PS\_POR\_B <-> PS\_POR\_B



Title		<Title> ETH
Size	Document Number	Rev
B	<Doc>	<RevCode>
Date:	Tuesday, December 02, 2025	Sheet 9 of 19

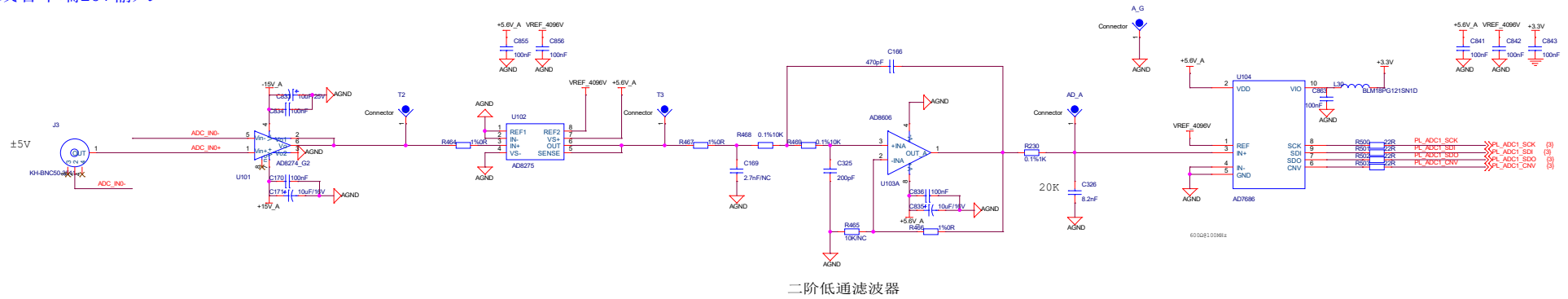


Title		<Title> USB
Size	Document Number	Rev
B	<Doc>	<RevCode>
Date:	Tuesday, December 02, 2025	Sheet 10 of 19



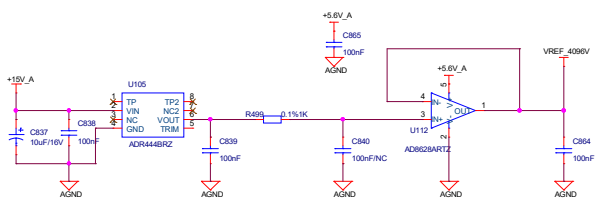
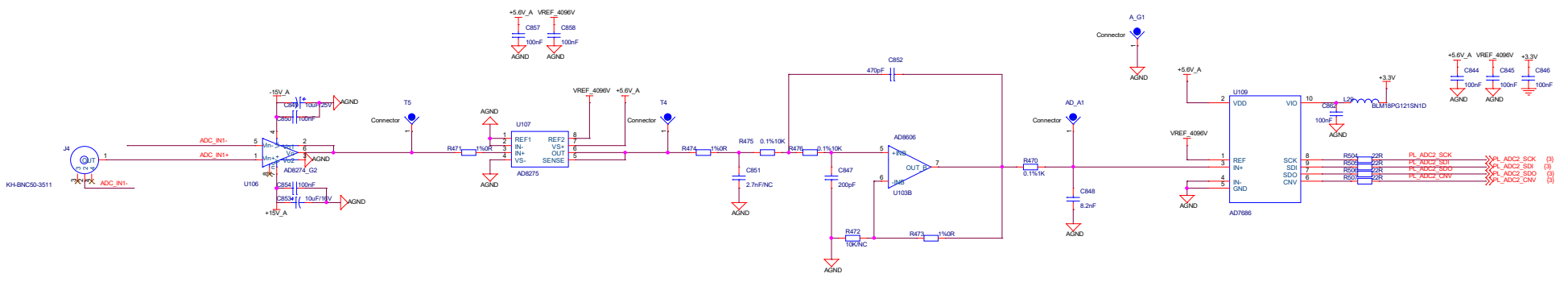
Title		<Title> JTAG
Size	Document Number	Rev
B	<Doc>	<RevCode>
Date:	Tuesday, December 02, 2025	Sheet 11 of 19

差分±5V或者单端±5V输入



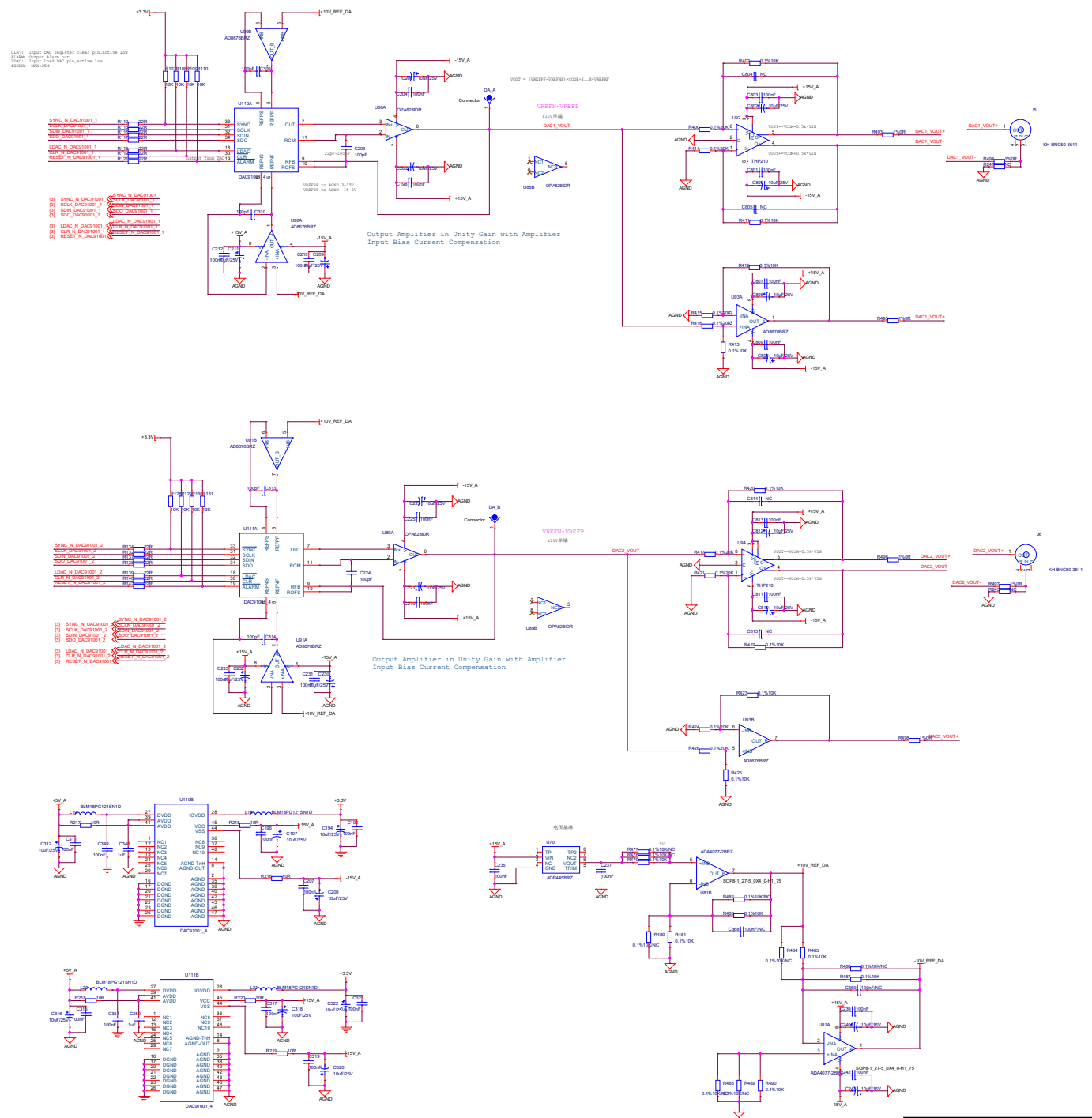
二阶低通滤波器

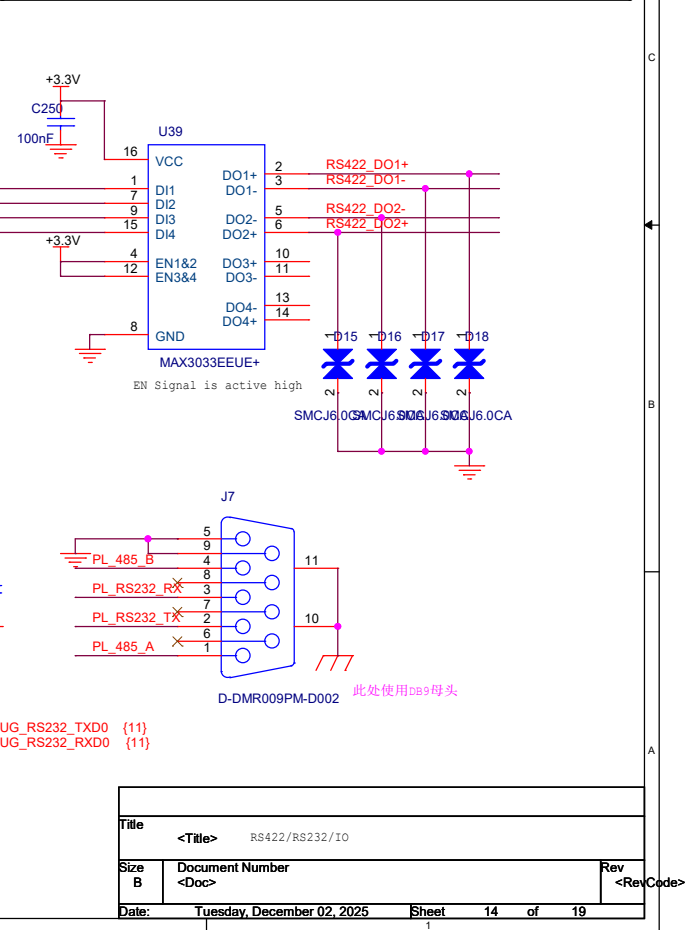
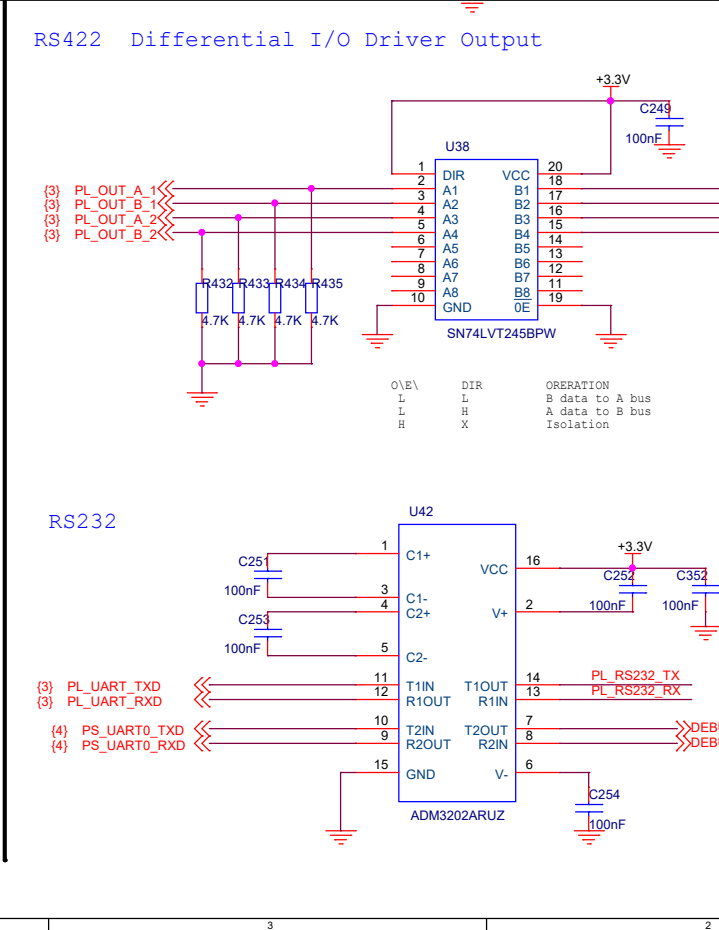
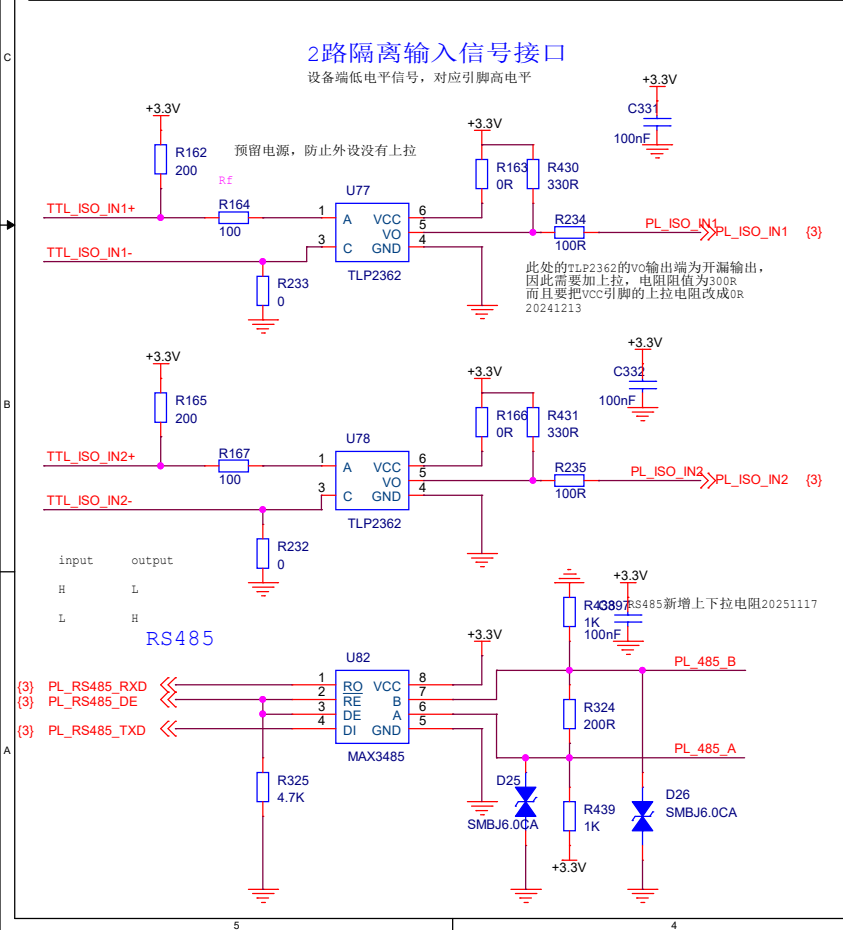
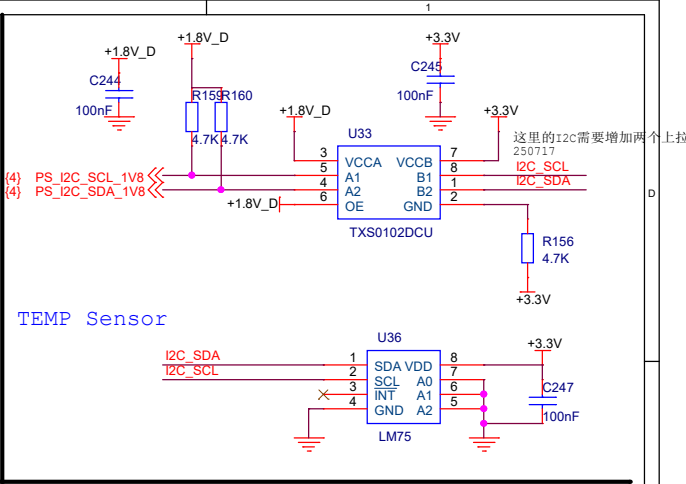
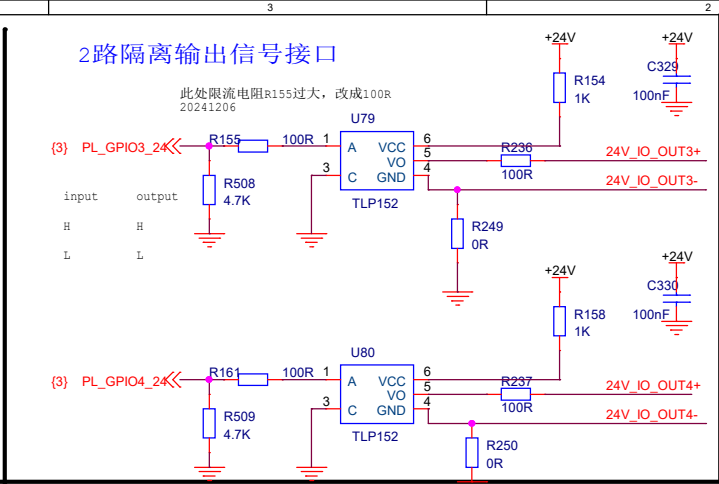
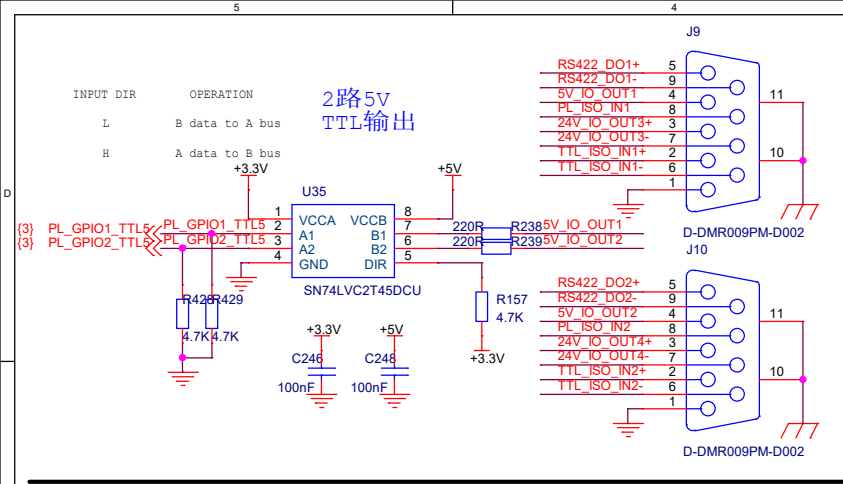
此处参考AGND错误，应该为数字地



File	<Title>_ADC	Rev	
Size	Document Number	Rev	
	Custom-Doc		<Rev Code>
Date	Tuesday, December 02, 2008	Sheet	12 of 19

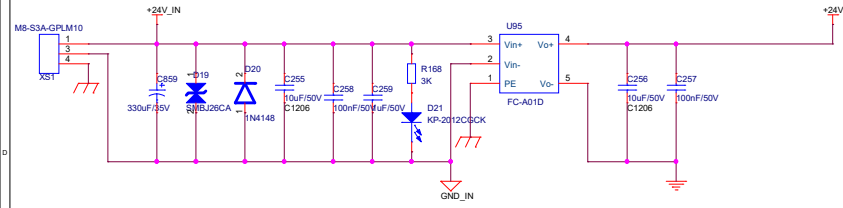
2路DAC接口, 差分输出, 幅度±5V





Title		<Title>	RS422/RS232/I/O
Size	Document Number		
B	<Doc>		
Date:	Tuesday, December 02, 2025	Sheet	14 of 19
		Rev	<RevCode>

POWER IN EMI FILTER

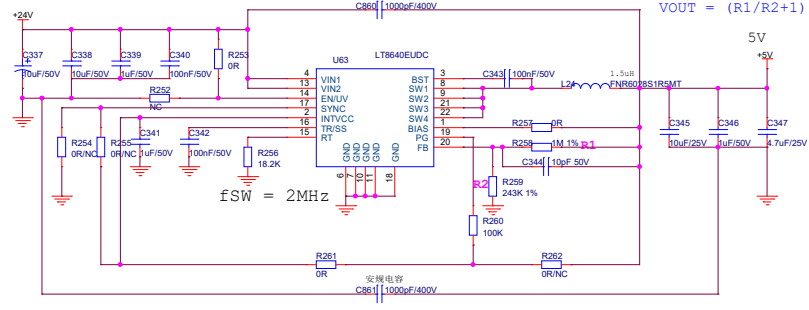


+24V --->> +5V\_P @ 5A max

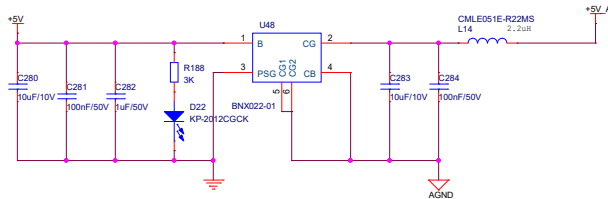
$$R1 = R2 \times (Vout/VFB - 1)$$

$$VFB = 0.97V$$

$$VOUT = (R1/R2 + 1) \times 0.97V$$

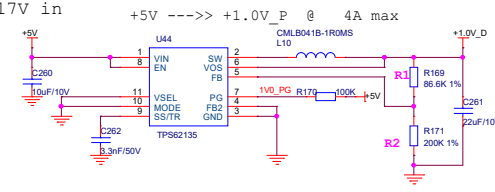


POWER IN EMI FILTER



Power On Sequence:  
1.0V->1.8V->1.5V->3.3V->VCCIO

3~17V in



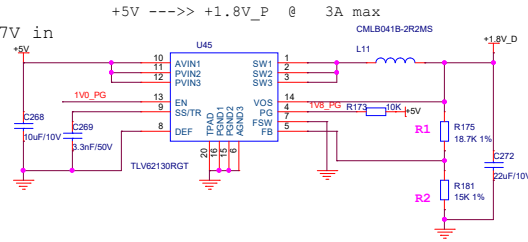
0.8~12V out

$$R1 = R2 \times (Vout/VFB - 1)$$

$$VFB = 0.7V$$

$$Vout = (R1/R2 + 1) \times 0.7V$$

3~17V in

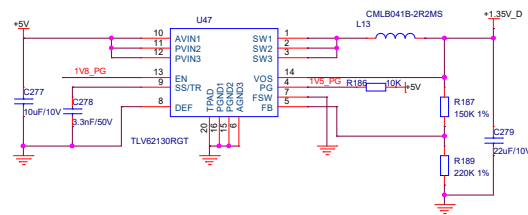


0.9~5.5V out

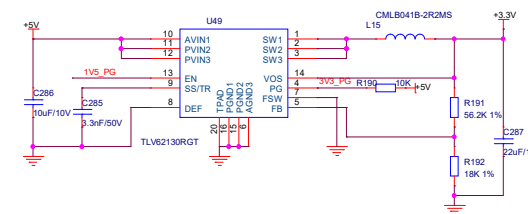
$$R1 = R2 \times (Vout/0.8V - 1)$$

$$Vout = (R1/R2 + 1) \times 0.8V$$

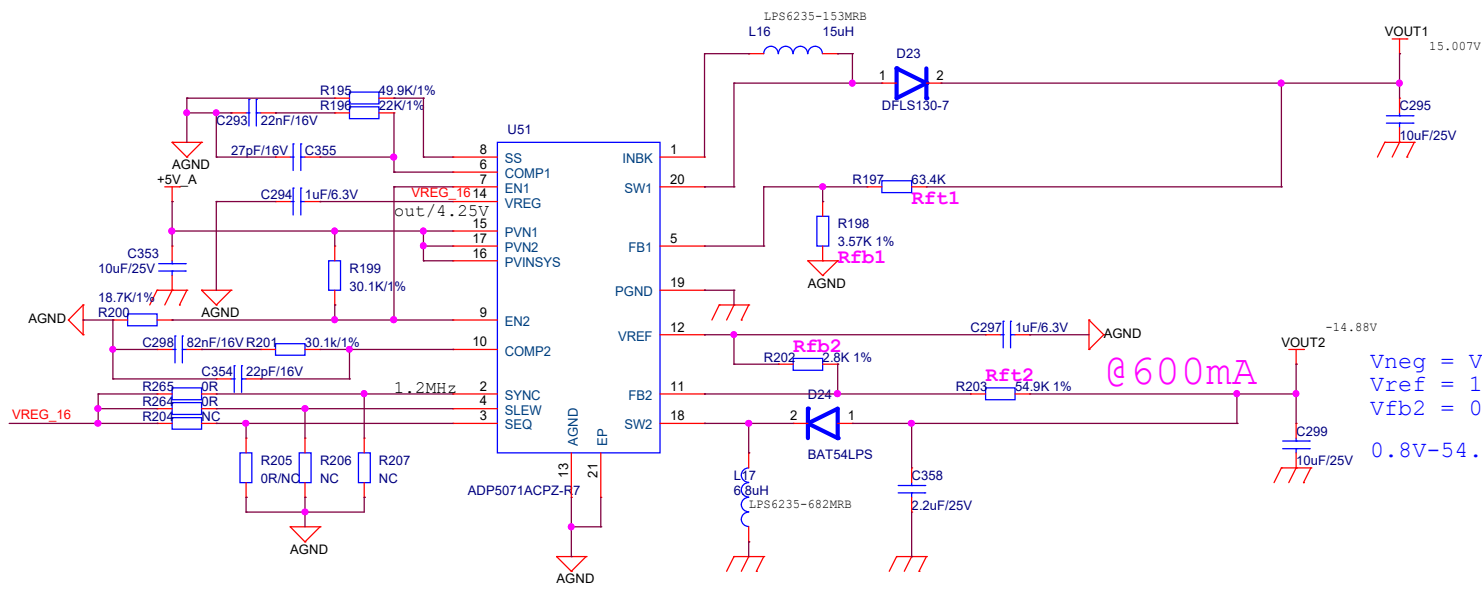
+5V --->> +1.35V\_P @ 3A max



+5V --->> +3.3V\_P @ 3A max



Title	<Title>
Size	Document Number
Customer	<Doc>
Date	Tuesday, December 02, 2025
Sheet	15 of 19



**@1A**

$$V_{pos} = 0.8V \times (1 + R_{ft1}/R_{fb1})$$

$$0.8V \times (1 + 63.4K/3.57K) = 15$$

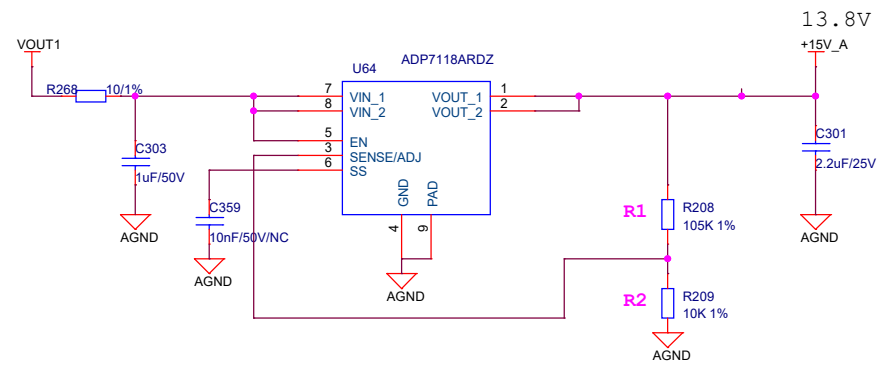
**@600mA**

$$V_{neg} = V_{fb2} - R_{ft2}/R_{fb2} (V_{ref} - V_{fb2})$$

$$V_{ref} = 1.60V$$

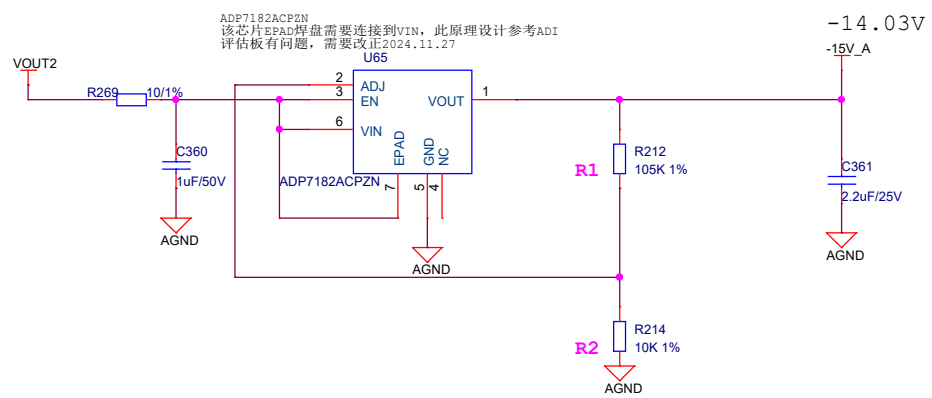
$$V_{fb2} = 0.8V$$

$$0.8V - 54.9K/2.8K (1.6 - 0.8) = -14.88V$$



$$V_{out} = 1.2V (1 + R1/R2)$$

$$1.2V (1 + 105K/10K) = 13.8V$$

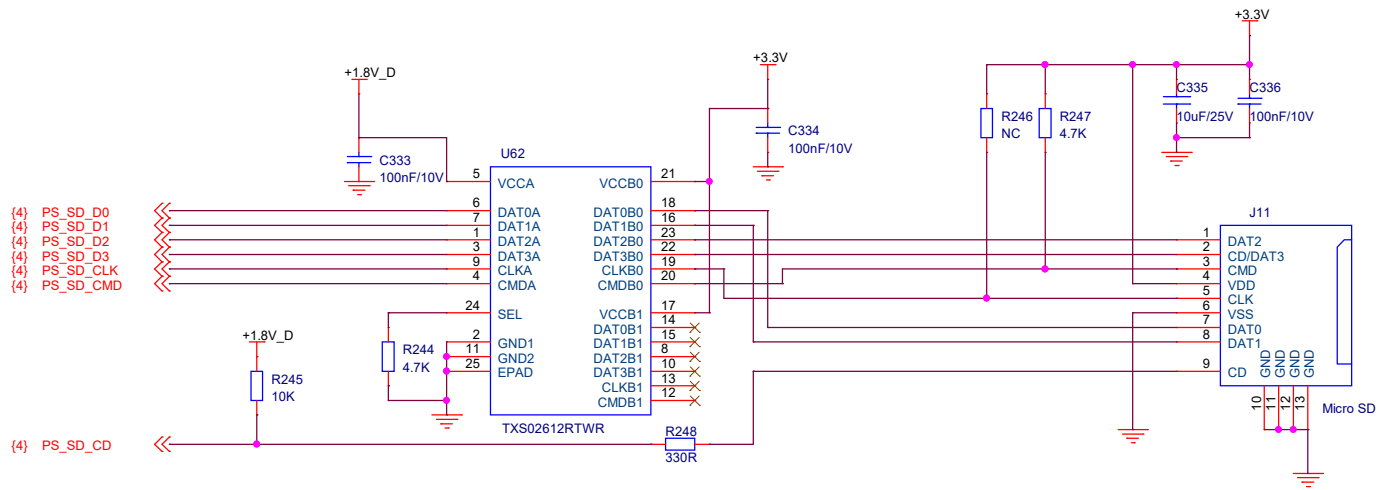


$$-V_{out} = -1.22V (1 + R1/R2)$$

$$-1.22 (1 + 105K/10K) = -14.03V$$

ADP7182ACPZN  
该芯片EPAD焊盘需要连接到VIN，此原理设计参考ADI  
评估极有问题，需要改正2024.11.27

Title		<Title>
Size	Document Number	Rev
Custom	<Doc>	<RevCode>
Date:	Tuesday, December 02, 2025	Sheet 16 of 19



Title		
<Title> SD Card		
Size	Document Number	Rev
B	<Doc>	<RevCode>
Date:	Tuesday, December 02, 2025	Sheet 18 of 19

20251113

1. 针对上一版的AD5791输出，移相过程中会出现最后一次输出有尖峰或者下降台阶，导致多次触发。方案是将DAC的输出改回原来的DAC11001

20251114

1. DAC输出电路优化，使用精密差分运放输出差分信号，使用精密运放搭建单端输出电路。电阻更换为0.1%精度，10ppm温度系数电阻  
2. 针对之前设计中的错误进行更新，比如之前IO输出在系统上电前会触发输出，在引脚加入下拉电阻，规定初始电平  
3. 电源输入部分增加EMC滤波器  
4. 增加zynq上电模式切换的拨码开关，两位拨码

20251117

1. RS485部分增加上下拉电阻

20251118

1. ADC采样电路部分重新设计，原来是按照电流输入进行采样，更换为差分±5V电压输入采样  
2. 2.4V电源输入部分增加EMC模块  
3. 板载增加JTAG接口6pin

20251124

1. 修改元器件封装，匹配之前设计的器件库

20251125

1. EMC滤波器输入新增一个电解电容。DCDC新增两个安规电容。

20251126

1. 数字地和安全地之间连接更换为安规电容，1M电阻  
2. 电源输入连接器更换型号为M8-S3A-GPLM10，带保护接地  
3. ADC采样电路部分ADC芯片的3.3V参考数字地，增加磁珠进入采样芯片  
4. 删除-5.6V\_A这一路电源

20251128

1. 更新器件DAC11001的symbol，原来器件中的NC1脚用的power类型，导致引脚包含网络

20251201

1. ADC电路部分，更新参考电压输出电路，增加RC滤波以及一级运放buffer

20251202

1. ADC采样部分，ADC芯片与FPGA之间的SPI接口串22R电阻隔离  
2. DIO部分，24V隔离输出，FPGA的控制引脚增加下拉电阻，规定初始状态

Title		
<Title>		
Size	Document Number	Rev
A	<Doc>	<RevCode>
Date:	Tuesday, December 02, 2025	Sheet 19 of 19