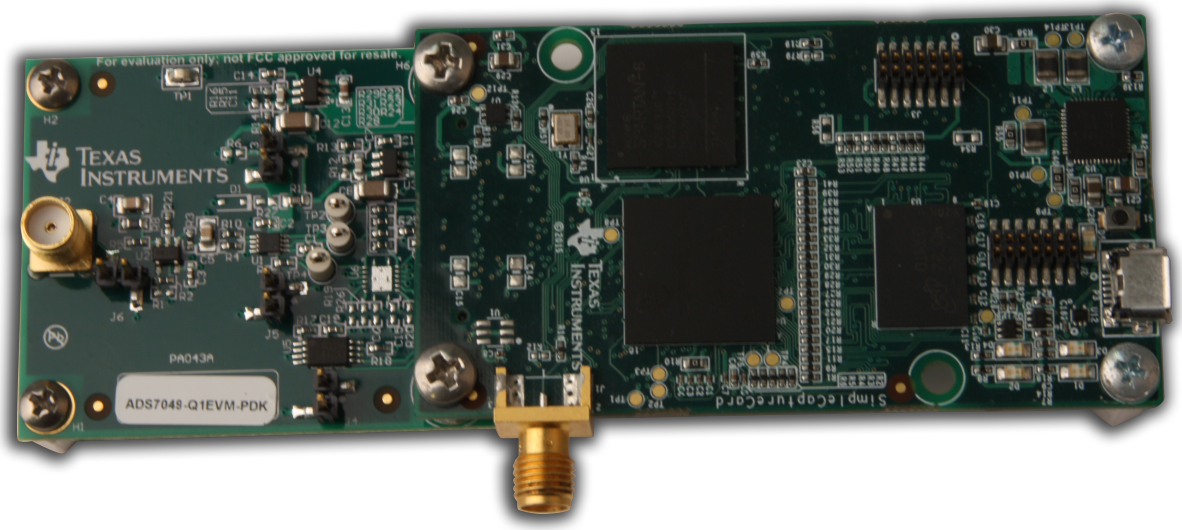
User's Guide
SBAU280–November 2016

ADS7049-Q1EVM-PDK

This user's guide describes the characteristics, operation, and use of the ADS7049-Q1 evaluation module (EVM) performance demonstration kit (PDK). This kit is an evaluation platform for the ADS7049-Q1, which is a 12-bit, 2-MSPS, single-ended analog input, successive approximation register (SAR) analog-to-digital converter (ADC) that features an easy-to-use SPI serial interface. The EVM-PDK eases the evaluation of the ADS7049-Q1 device with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials.



The following related documents are available through the Texas Instruments web site at www.ti.com.

Related Documentation

Device	Literature Number
ADS7049-Q1	SBAS763
OPA365-Q1	SBOS512
TPS791-Q1	SGLS160
SN74AVC4T245-Q1	SCES792

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1 Overview

The ADS7049-Q1EVM-PDK is a platform for evaluating the performance of the ADS7049-Q1 SAR ADC, which is a single-ended analog input, 12-bit, 2-MSPS device. The evaluation kit includes the ADS7049-Q1EVM board and the *Precision Host Interface* (PHI) controller board that enables the accompanying computer software to communicate with the ADC over USB for data capture and analysis.

The ADS7049-Q1EVM board includes the ADS7049-Q1 SAR ADC, all the peripheral analog circuits, and components required to extract optimum performance from the ADC.

The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS7049-Q1
- Supplies power to all active circuitry on the ADS7049-Q1EVM board

Along with the ADS7049-Q1EVM and PHI controller board, this evaluation kit includes an A-to-micro-B USB cable to connect to a computer.

1.1 ADS7049-Q1EVM-PDK Features

The ADS7049-Q1EVM-PDK includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS7049-Q1 ADC
- USB powered—no external power supply is required
- The PHI controller that provides a convenient communication interface to the ADS7049-Q1 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output
- Easy-to-use evaluation software for Microsoft® Windows® 7, Windows 8, 64-bit operating systems

1.2 ADS7049-Q1EVM Features

The ADS7049-Q1EVM includes the following features:

- Onboard low-noise and low distortion ADC input drivers optimized to meet ADC performance
- Onboard ultralow noise low-dropout (LDO) regulators to generate supplies for the operation amplifier and voltage reference.

2 Analog Interface

The ADS7049-Q1 is an low-power, extremely small size ADC that supports single-ended analog inputs. The ADS7049-Q1EVM uses an OPA365-Q1 amplifier to drive the inputs of the ADC. The ADS7049-Q1EVM is designed for easy interface to analog sources. This section covers driver details including jumper configuration for analog input signal source.

2.1 Connectors for Single-Ended Analog Input

The ADS7049-Q1EVM is designed for easy interfacing to an external analog single-ended source via a subminiature version A (SMA) connector or 100-mil headers. J2 is the SMA connector that allows analog source connectivity through coaxial cables. Alternatively, 100-mil jumper cables or mini-grabbers can be used to connect analog sources to the J6:1 pin.

Table 1. Analog Input Connector Description

Pin Number	Signal	Description
J2	INP	Positive single-ended input provided at the SMA
J6:1	INP	Alternate location to provide the positive single-ended input

2.2 ADC Single-Ended Input Signal Driver

SAR ADC inputs terminate in switched-capacitor networks that create large instantaneous current loads when the switches are closed that effectively make the ADC inputs dynamically low impedance. The single-ended input of the ADS7049-Q1 are therefore driven by an OPA365-Q1 used in an non-inverting, unity-gain configuration to maintain ADC performance with maximum loading at full device throughput of 2 MSPS.

2.2.1 Input Signal Path

Figure 1 shows the signal path for positive single-ended input applied to ADS7049-Q1EVM. An OPA365-Q1 is used in buffer configuration drives single-ended input of ADS7049-Q1. An RC filter value of 25.5 Ω and 1.5 nF are selected to achieve SINAD greater than 70 dB and THD less than – 80 dB for 2 kHz sine wave input at full throughput of 2 MSPS.

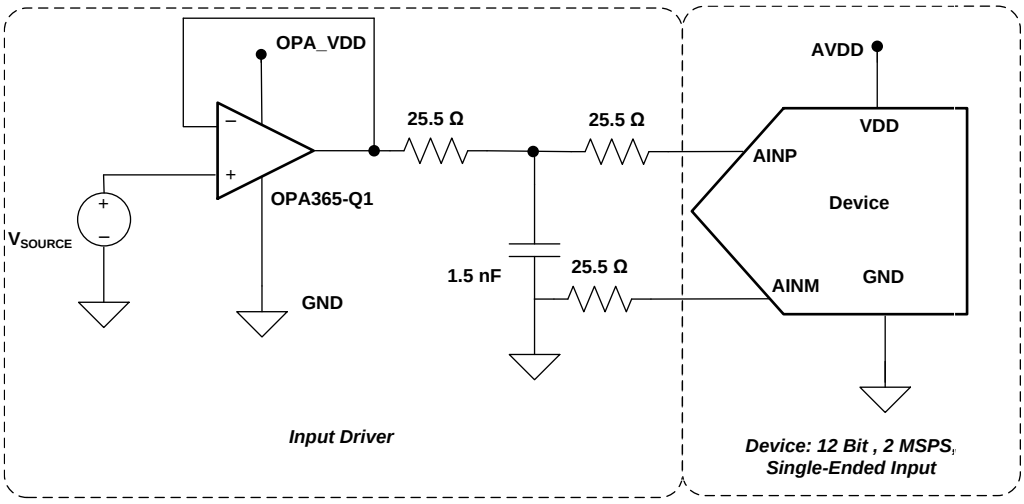

Figure 1. ADS7049-Q1EVM Analog Input Path

3 Digital Interfaces

As noted in Section 1, the EVM interfaces with the PHI that, in turn, communicates with the computer over USB. There are two devices on the EVM with which the PHI communicates: the ADS7049-Q1 ADC (over SPI or multiSPI) and the EEPROM (over I^2C). The EEPROM comes pre-programmed with the information required to configure and initialize the ADS7049-Q1EVM-PDK platform. Once the hardware is initialized, the EEPROM is no longer used.

3.1 SPI Interface for ADC Digital IO

The ADS7049-Q1EVM-PDK supports the interface and calibration modes as detailed in the ADS7049-Q1 datasheet (SBAS763). The PHI is capable of operating at a 3.3 V logic level and is directly connected to the digital I/O lines of the ADC.

The buffer U6 is included in the design to ensure that, if required, the SDO can be driven to a host controller over long cables with minimal distortion. For the normal operating condition with the PHI directly plugged in on connector J1, the U6 buffer is not required and has been bypassed in the factory configuration of the ADS7049-Q1EVM-PDK.

4 Power Supplies

The ADS7049-Q1 supports a wide range of operation on its analog supplies. The AVDD can operate from 2.35 V to 3.6 V. The DVDD operates from 1.65 V to 3.6 V, independent of the AVDD supply. The analog portion of the ADS7049-Q1EVM-PDK operates from a 5.5 V supply, that in turn generates an AVDD supply and an OPA+ supply using low-noise TPS79101 LDOs. The AVDD supply is nominally set to 3.3 V at the factory, but this voltage may be changed to any value within the valid range, by modifying the value of R12 as per Table 2. Similarly, the OPA+ supply is nominally set to 4.83 V at the factory, but this voltage maybe changed by modifying the value of R15 as per Table 2. In case any intermediate values need to be set, the detailed formula to arrive at these values are available in the TPS79101 (SGLS160) datasheet.

Table 2. TPS79101 Voltage Settings for AVDD and OPA+ Supplies

Output Voltage	R12/R15	R13/R16	C7/C11
1.8 V	14.2 kΩ	30.1 kΩ	33 pF
2.0 V	19.1 kΩ	30.1 kΩ	27 pF
2.5 V	31.6 kΩ	30.1 kΩ	22 pF
3.0 V	43.7 kΩ	30.1 kΩ	15 pF
3.3 V	51.1 kΩ	30.1 kΩ	15 pF
3.6 V	59.0 kΩ	30.1 kΩ	15 pF
4.83 V	88.7 kΩ	30.1 kΩ	15 pF

Alternatively, AVDD may be set by connecting an external power source through J3. Table 3 describes the modifications required for on-board or external AVDD supply.

Table 3. AVDD Voltage Selection Settings

AVDD Source	Position	Setting
Onboard regulated AVDD (set to 3.3 V)	J3	Closed
External AVDD	J3	Open
	R11	Disassembled

CAUTION

The external AVDD supply applied to external connector J3 must not exceed 3.6 V as this may damage the device. The external AVDD supply must be in the range of 2.35 V to 3.6 V for proper operation of the ADS7049-Q1EVM.

The digital portion of the ADS7049-Q1 ADC operates from a 3.3 V supply from the PHI.

5 ADS7049-Q1EVM-PDK Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for the proper operation of the ADS7049-Q1EVM-PDK.

5.1 Default Jumper Settings

The silk screen plot shown in Figure 2 details the jumper locations for ADS7049-Q1EVM-PDK.

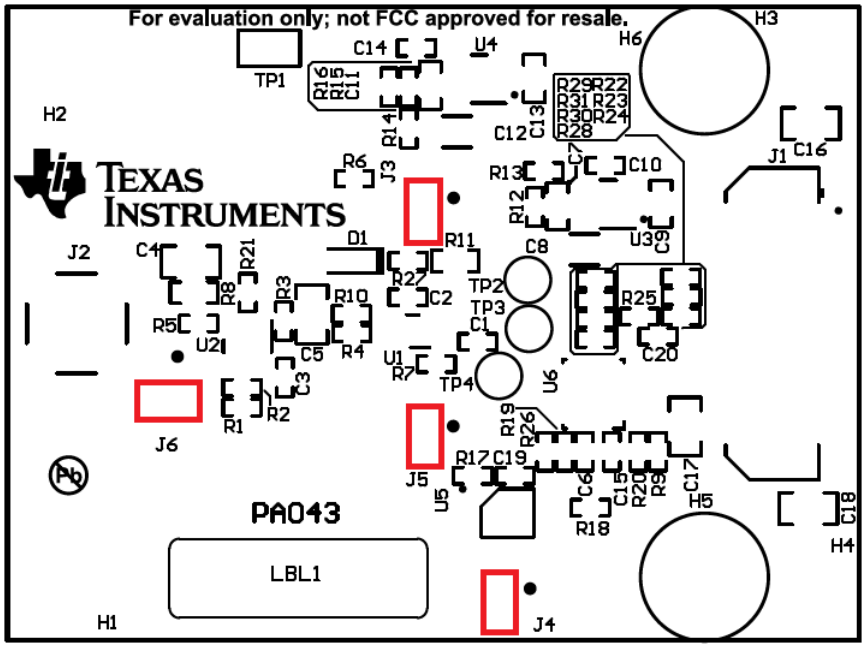

Figure 2. ADS7049-Q1EVM-PDK Jumper Locations

Table 4 explains the functionality of each of these jumpers and their default configurations. No shunts are required on any location at the EVM for normal operation. Remove any shunts that may be present at locations J3 through J6.

Table 4. Default Jumper Configurations

Reference Designator	Default Configuration	Description
J3	Open	Location to feed external AVDD supply to the ADS7049-Q1EVM-PDK
J4	Open	Unassembled by default
J5	Open	Location for external trigger signal (3.3-V logic)
J6	Open	Alternate location for analog input to the ADS7049-Q1EVM-PDK

5.2 EVM Graphical User Interface (GUI) Software Installation

Download the latest version of the EVM GUI installer from the *Tools and Software* folder of the ADS7049-Q1 and run the GUI installer to install the EVM GUI software on the user's computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Otherwise, depending on the antivirus settings, an error message may appear or the *installer.exe* file may be deleted.

Accept the license agreements and follow the on-screen instructions to complete the installation.

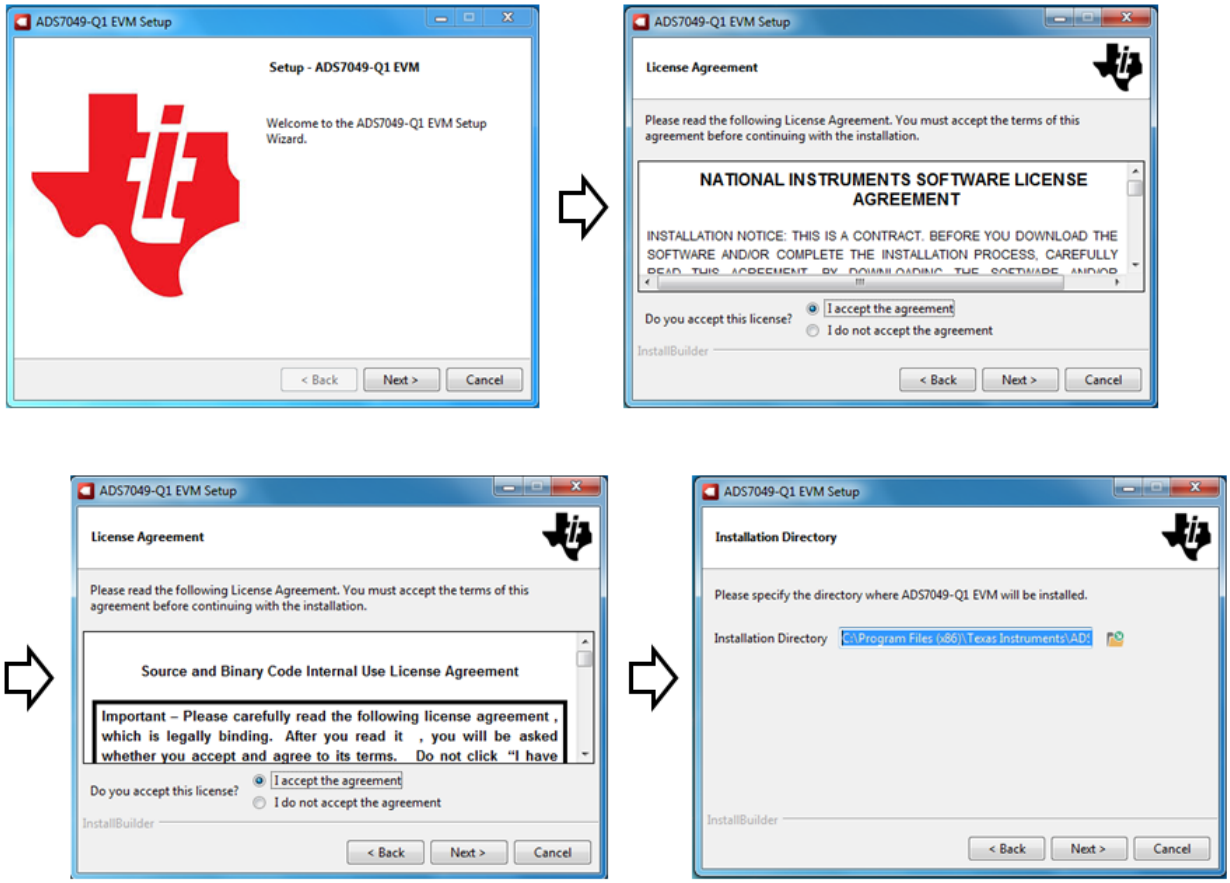

Figure 3. ADS7049-Q1 Software Installation Prompts

As a part of the ADS7049-Q1EVM GUI installation, a prompt with a *Device Driver Installation* will appear on the screen. Click *Next* to proceed.

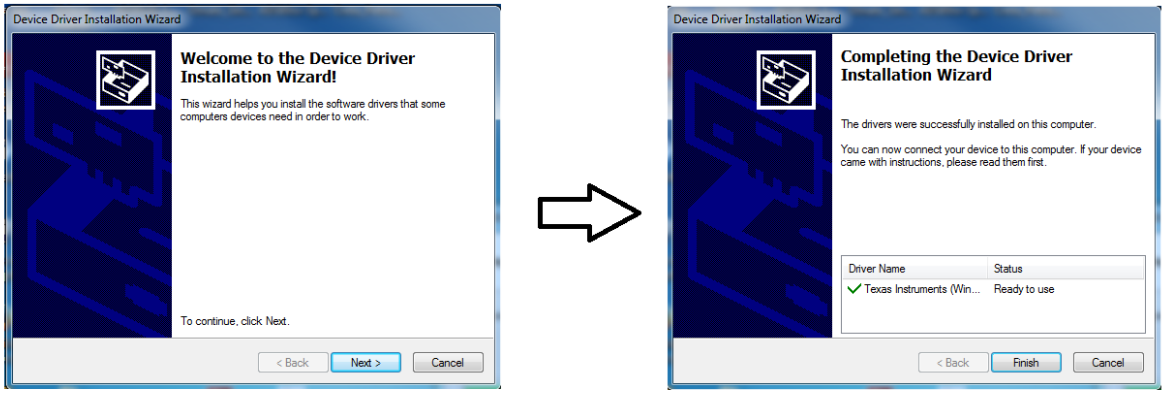

Figure 4. Device Driver Installation Wizard Prompts

NOTE: A notice may appear on the screen stating that Widows cannot verify the publisher of this driver software. Select *Install this driver software anyway*.

The ADS7049-Q1EVM-PDK requires *LabVIEW™ Run-Time Engine* and may prompt for the installation of this software, if not already installed.

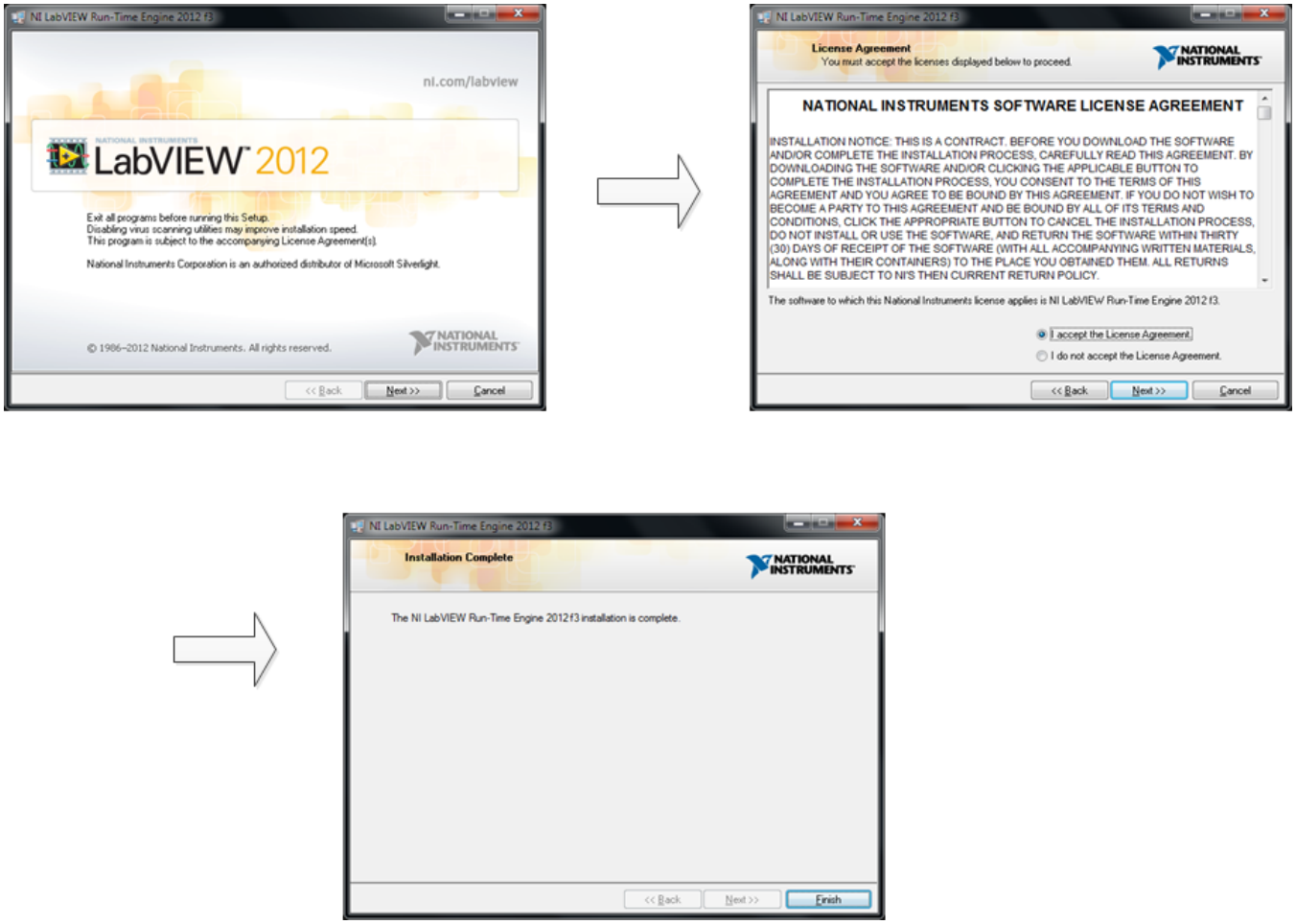

Figure 5. LabVIEW Run-Time Engine Installation

After these installations, check the **Create Desktop Shortcut** as shown in Figure 6.

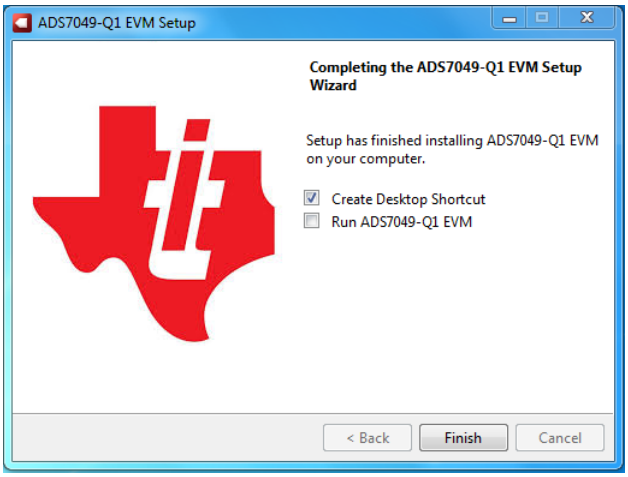

Figure 6. ADS7049-Q1EVM-PDK Installation Final Step

6 ADS7049-Q1EVM-PDK Operation

The following instructions are a step-by-step guide to connecting the ADS7049-Q1EVM-PDK to the computer and evaluating the performance of the ADS7049-Q1:

1. Connect the ADS7049-Q1EVM to the PHI. Install the two screws as indicated in Figure 7.
2. Use the provided USB cable to connect the PHI to the computer.
   - LED D5 on the PHI lights up, indicating that the PHI is powered up.
   - LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC.

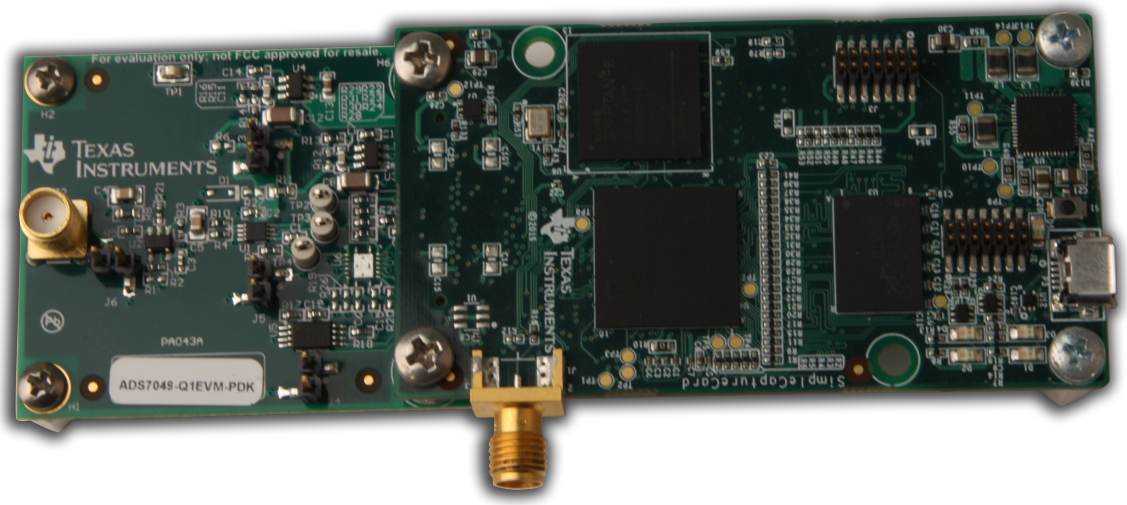

Figure 7. EVM-PDK Hardware Setup and LED Indicators

3. Launch the ADS7049-Q1EVM GUI software from the installed path as shown in Figure 8 or using the desktop shortcut created during installation.

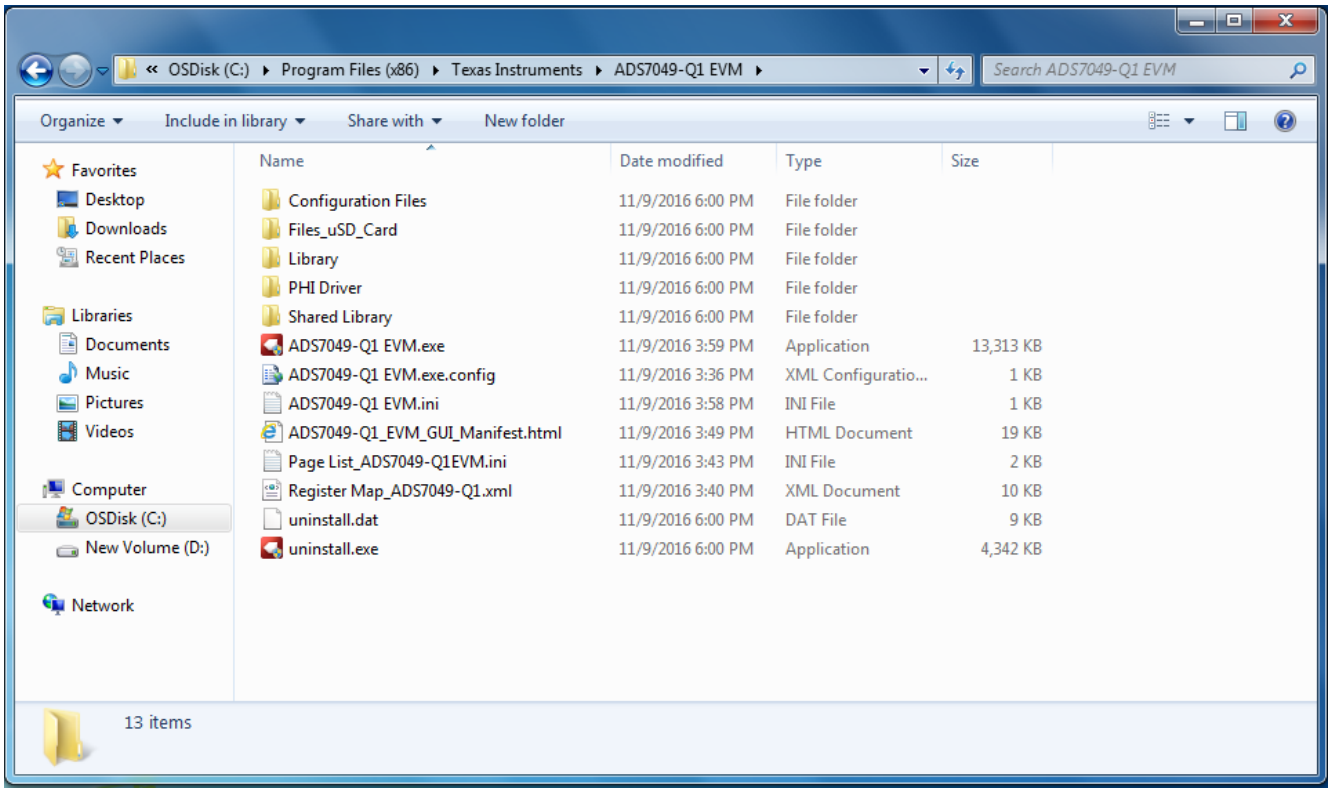

Figure 8. Launch the EVM GUI Software

6.1 EVM GUI Global Settings for ADC Control

Figure 9 identifies the input parameters of the GUI (as well as their default values) through which the various functions of the ADS7049-Q1 can be exercised. These settings are global because they persist across the GUI tools listed in the top left pane (or from one page to another).

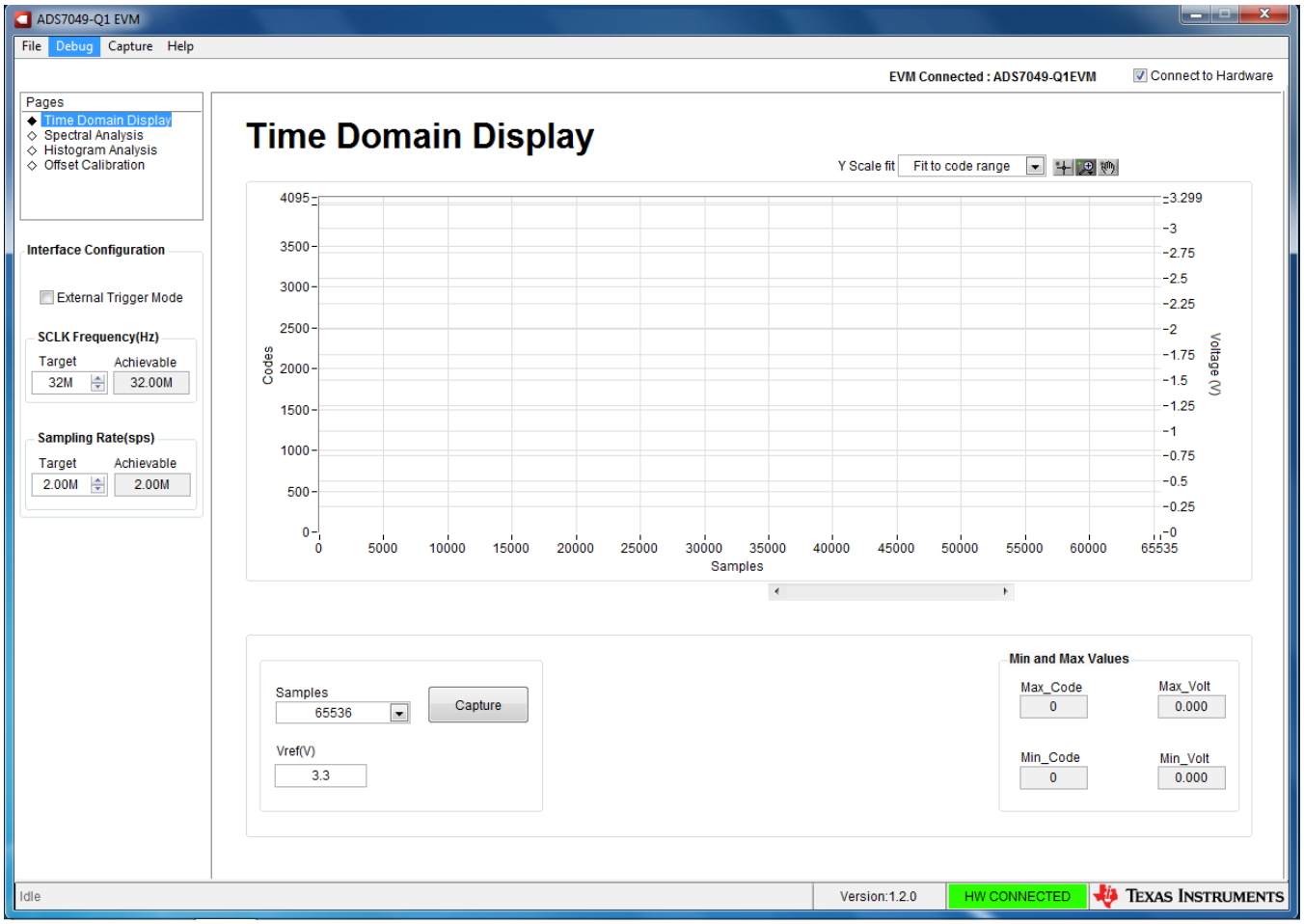

Figure 9. EVM GUI Global Input Parameters

The user can select *SCLK Frequency* and *Sampling Rate* on this pane. The GUI allows the user to enter the targeted values for these two parameters and the GUI computes the best values that can be achieved, considering the timing constraints of the device.

The user can specify a target SCLK frequency (in Hz) and the GUI tries to match this frequency as closely as possible by changing the PHI PLL settings and the achievable frequency may differ from the target value entered. Similarly, the sampling rate of the ADC can be adjusted by modifying the Target Sampling Rate argument (also in Hz). The achievable ADC sampling rate can differ from the target value, depending on the applied SCLK frequency and the closest match achievable is displayed. This pane, therefore, allows the user to try various settings available on the ADS7049-Q1 in an iterative fashion until the user converges to the best settings for the corresponding test scenario.

Located above these controls, is an External Trigger Mode checkbox. When selected this configures the PHI to monitor the signal connected on J5:1 for a low to 3.3 V transition and captures the requested number of samples after this level transition is detected. This is useful in cases when the external analog input is generated or ready for measurement only after an external trigger event.

6.2 Time Domain Display Tool

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits.

The user can trigger a capture of the data of the selected number of samples from the ADS7049-Q1, as per the current interface mode settings using the **Capture** button as indicated in Figure 10. The sample indices are on the x-axis and there are two y-axes showing the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the Analysis tools described in the subsequent sections, triggers calculations to be performed on the same set of data.

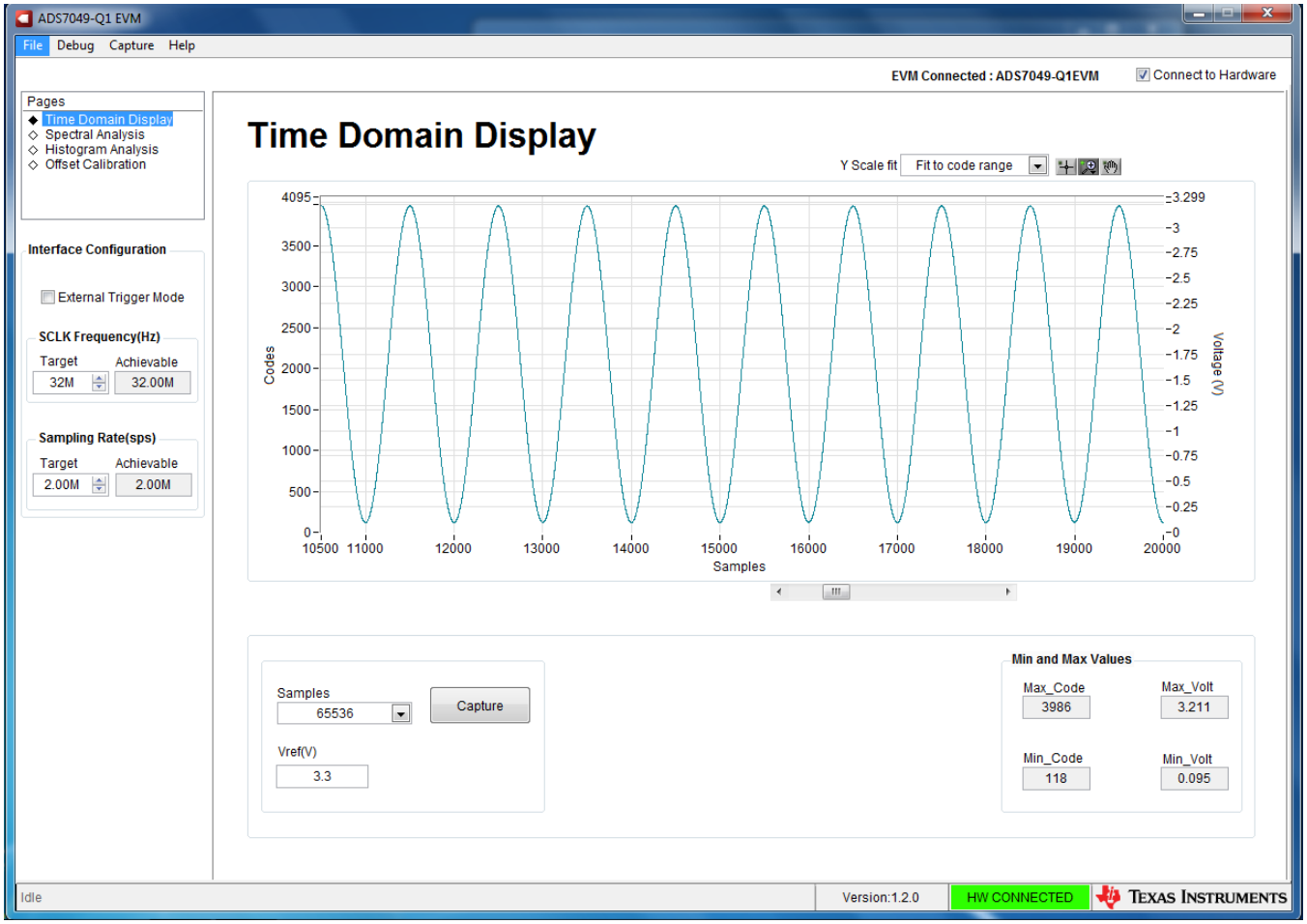

Figure 10. Time Domain Display Tool Options

6.3 Spectral Analysis Tool

The spectral analysis tool is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS7049-Q1 SAR ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. Alternatively, the window setting of *None* can be used to search for noise spurs over frequency in dc inputs.

For dynamic performance evaluation, the external single-ended source must have better specifications than the ADC itself to ensure that the measured system performance is not limited by the performance of the signal source. Therefore, the external reference source must meet the source requirements mentioned in Table 5.

Table 5. External Source Requirements for Evaluation of the ADS7049-Q1

Specification Description	Specification Value
Signal frequency	2 kHz
External source type	Single ended
External source common-mode	1.65 V
Maximum SNR	80 dB
Maximum THD	–100 dB

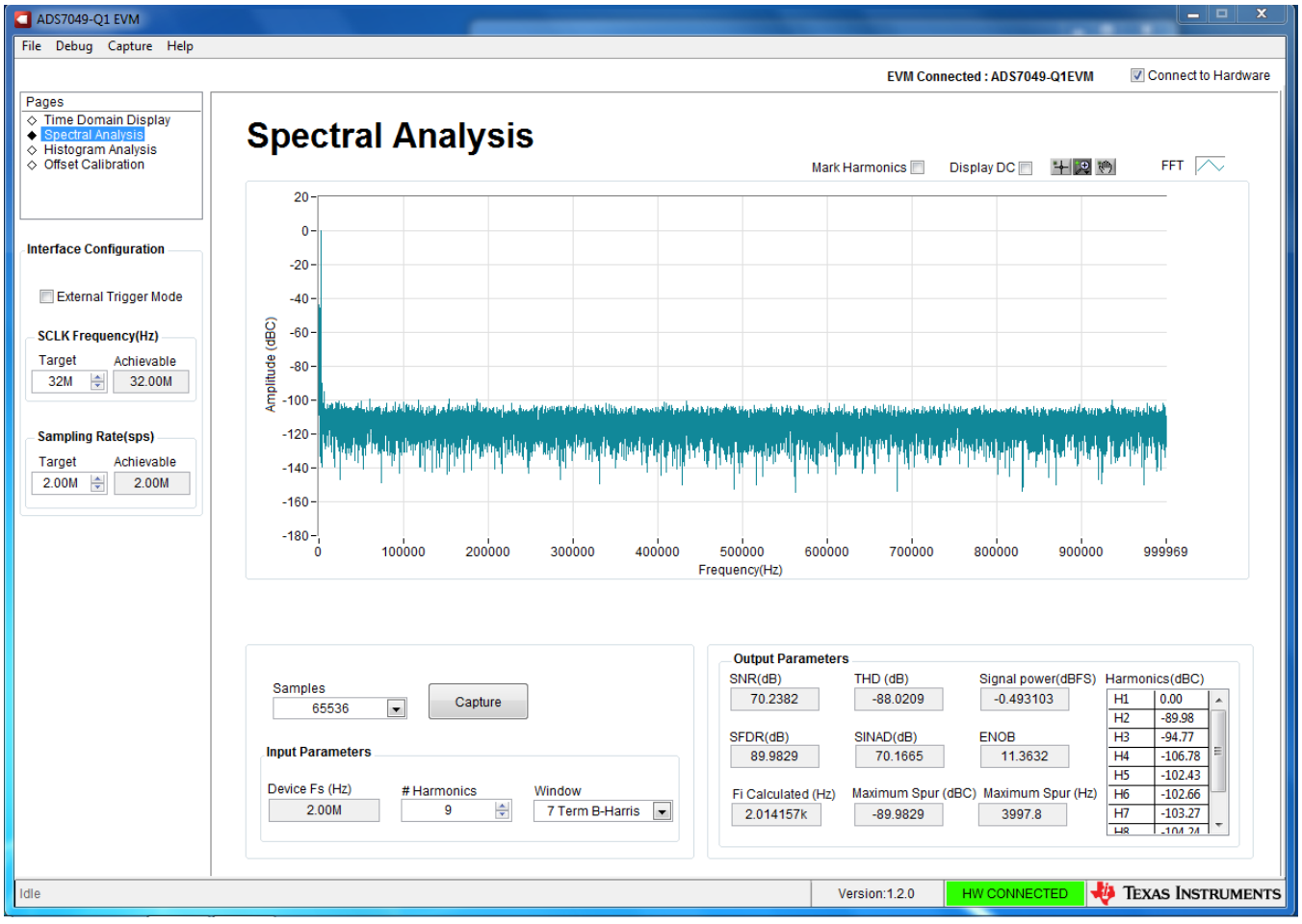

Figure 11. Spectral Analysis Tool

6.4 Histogram Tool

Noise degrades ADC resolution and the histogram tool can be used to estimate *effective resolution*, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a dc signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel.

The histogram corresponding to a dc input is displayed on clicking the **Capture** button, as shown in Figure 12:

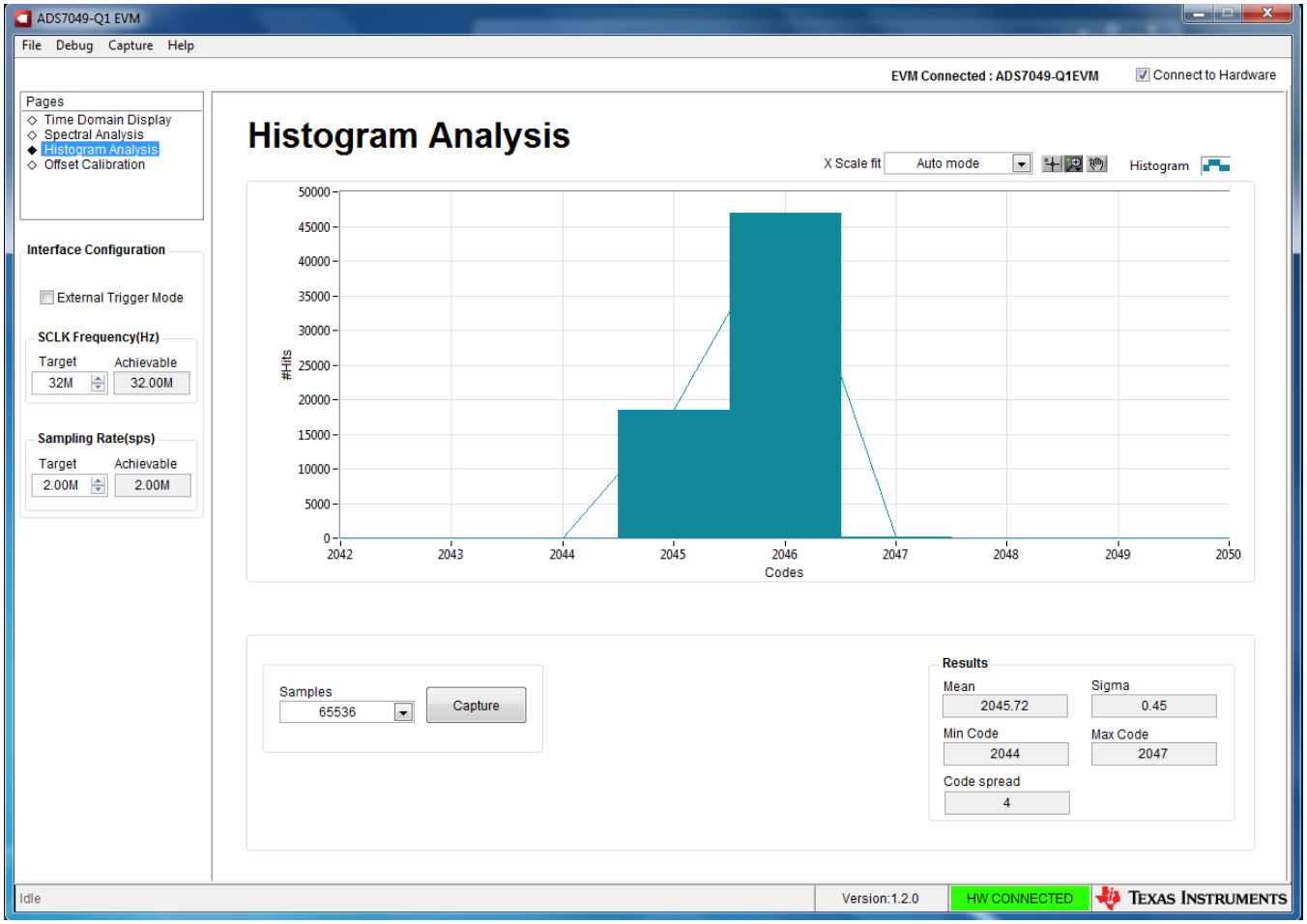

Figure 12. Histogram Analysis Tool

6.5 Offset Calibration

The ADS7049-Q1 device has the ability to calibrate its internal offset. The offset calibration can be initiated by the user either on power-up or during normal operation. During offset calibration, the analog input pins (AINP and AINM) are disconnected from the sampling stage and connected to an internal reference. The result of the offset calibration is stored in an internal register. For subsequent conversions, the device adjusts the conversion results provided on the SDO output with the value stored in this internal register.

The ADS7049-Q1 GUI implements offset calibration as described in the *Offset Calibration During Normal Operation* section of ADS7049-Q1 datasheet (SBAS763). Figure 13 depicts the *Offset Calibration* page of the GUI.

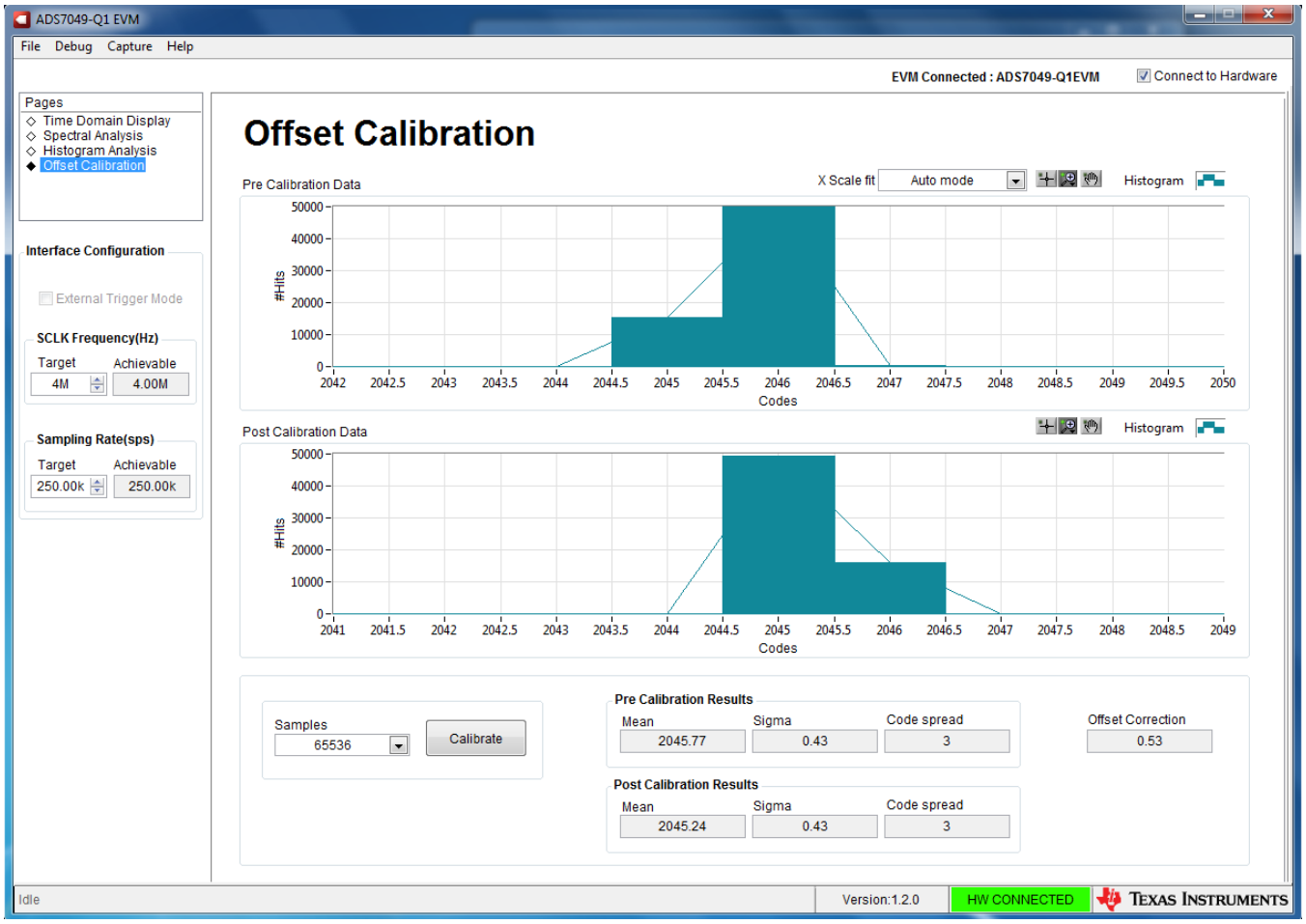

Figure 13. ADS7049-Q1 Calibration

The *Offset Calibration* test is best conducted with a DC input at the *Analog Input Terminal* of the ADS7049-Q1EVM-PDK. Simply click the **Calibrate** button. The GUI first performs a histogram test for the device described in Section 6.4 and populates the first of the two graphs. The pre-calibrated *Mean* code is inserted in the indicator. Next, the calibration frame is sent to the ADS7049-Q1 device that enables the internal offset calibration logic. The GUI performs the histogram test for a second time and the second graph is populated and *Post Calibrated Mean* value computed. Finally, the difference between the first and second computed mean is populated in the *Calculated Offset Correction* indicator.

The computed offset for all subsequent attempts to calibrate the device will always yield a result within the limits specified in the datasheet. This indicates that after the calibration is performed for the first time, the offset is actually being applied on all subsequent conversions. This computed offset will remain fixed, unless the device is reset or there is a significant change in operating temperature or analog supply voltage.

7 Bill of Materials, PCB Layout, and Schematics

This section contains the ADS7049-Q1EVM bill of materials, PCB layout, and the EVM schematics.

7.1 Bill of Materials

Table 6 lists the ADS7049-Q1EVM BOM.

Table 6. ADS7049-Q1EVM Bill of Materials

Manufacturer Part Number	Qty	Reference Designators	Manufacturer	Description
PA043	1	!PCB	Any	Printed Circuit Board
PA007A	1	!PCB2	Any	PHI-EVM-CONTROLLER
1891	4	@H1, @H2, @H3, @H4	Keystone	3/16 Hex Female Standoff
RM3X4MM 2701	2	@H5, @H6	APM HEXSEAL	Machine Screw Pan PHILLIPS M3
GRM155R71C104KA88D	3	C1, C2, C3	Murata	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0402
08051C153KAT2A	2	C4, C5	AVX	CAP, CERM, 0.015 µF, 100 V, +/- 10%, X7R, 0805
GRM1885C1H150JA01D	2	C7, C11	Murata	CAP, CERM, 15 pF, 50 V, +/- 5%, C0G/NP0, 0603
C3216X7R1V106K160AC	2	C8, C12	TDK	CAP, CERM, 10 µF, 35 V, +/- 10%, X7R, 1206_190
C1608X7R1C105K	2	C9, C13	TDK	CAP, CERM, 1 µF, 16 V, +/- 10%, X7R, 0603
GCM155R71H103KA55D	2	C10, C14	Murata	CAP, CERM, 0.01 µF, 50 V, +/- 10%, C0G/NP0, 0402
CGA4J1X7S1C106K125AC	3	C16, C17, C18	TDK	CAP, CERM, 10 µF, 16 V, +/- 10%, X7S, AEC-Q200 Grade 1, 0805
GCM155R71C104KA55D	1	C19	Murata	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0402
PMSSS 440 0025 PH	4	H1, H2, H3, H4	B&F Fastener Supply	MACHINE SCREW PAN PHILLIPS 4-40
9774050360R	2	H5, H6	Wurth Elektronik	ROUND STANDOFF M3 STEEL 5MM
QTH-030-01-L-D-A	1	J1	Samtec	Header(Shrouded), 19.7mil, 30x2, Gold, SMT
5-1814832-1	1	J2	TE Connectivity	SMA Straight PCB Socket Die Cast, 50 Ohm, TH
TSM-102-01-L-SV	4	J3, J4, J5, J6	Samtec	Header, 100mil, 2x1, Gold with Tin Tail, SMT
THT-14-423-10	1	LBL1	Brady	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll
CRCW040249R9FKED	3	R2, R5, R7	Vishay-Dale	RES, 49.9, 1%, 0.063 W, 0402
CRCW040225R5FKED	3	R3, R4, R10	Vishay-Dale	RES, 25.5, 1%, 0.063 W, 0402
CRCW06031M00JNEA	1	R8	Vishay-Dale	RES, 1.0 M, 5%, 0.1 W, 0603
RC0603FR-0710RL	1	R11	Yageo America	RES, 10.0, 1%, 0.1 W, 0603
CRCW040251K1FKED	1	R12	Vishay-Dale	RES, 51.1 k, 1%, 0.063 W, 0402
CRCW040230K1FKED	2	R13, R16	Vishay-Dale	RES, 30.1 k, 1%, 0.063 W, 0402
CRCW04020000Z0ED	5	R14, R28, R29, R30, R31	Vishay-Dale	RES, 0, 5%, 0.063 W, 0402
CRCW040288K7FKED	1	R15	Vishay-Dale	RES, 88.7 k, 1%, 0.063 W, 0402
CRCW040210K0FKED	2	R17, R18	Vishay-Dale	RES, 10.0k ohm, 1%, 0.063W, 0402
ERJ-2GE0R00X	4	R21, R22, R23, R24	Panasonic	RES, 0, 5%, 0.063 W, 0402
CRCW040220R0FKED	1	R25	Vishay-Dale	RES, 20.0, 1%, 0.063 W, 0402
5015	1	TP1	Keystone	Test Point, Miniature, SMT

Table 6. ADS7049-Q1EVM Bill of Materials (continued)

Manufacturer Part Number	Qty	Reference Designators	Manufacturer	Description
5002	3	TP2, TP3, TP4	Keystone	Test Point, Miniature, White, TH
ADS7049IDCUR	1	U1	Texas Instruments	Ultra-Low Power, Ultra-Small Size, 12-Bit, 1-MSPS, SAR ADC, DCU0008A
OPA365AQDBVRQ1	1	U2	Texas Instruments	Automotive Catalog, 50 MHz, Low-Noise, Single-Supply Rail-to-Rail Operational Amplifier, 2.2 to 5.5 V, -40 to 125 degC, 5-pin SOT23 (DBV0005A), Green (RoHS & no Sb/Br)
TPS79101DBVRQ1	2	U3, U4	Texas Instruments	Single Output High PSRR LDO, 100 mA, Adjustable 1.2 to 5.5 V Output, 2.7 to 5.5 V Input, 6-pin SOT-23 (DBV), -40 to 125 degC, Green (RoHS & no Sb/Br)
BR24G32FVT-3AGE2	1	U5	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8
GCM155R71H103KA55D	0	C6, C15	Murata	CAP, CERM, 0.01 µF, 50 V, +/- 10%, C0G/NP0, 0402
GRM1555C1H470FA01D	0	C20	Murata	CAP, CERM, 47 pF, 50 V, +/- 1%, C0G/NP0, 0402
SP4020-01FTG	0	D1	Littelfuse	Diode, TVS, Uni, 3.3 V, 21.8 Vc, SOD-323
N/A	0	FID1, FID2, FID3	N/A	Fiducial mark. There is nothing to buy or mount.
CRCW04020000Z0ED	0	R1, R6, R27	Vishay-Dale	RES, 0, 5%, 0.063 W, 0402
CRCW040210K0FKED	0	R9, R19, R20, R26	Vishay-Dale	RES, 10.0k ohm, 1%, 0.063W, 0402
74AVC4T245QRGYRQ1	0	U6	Texas Instruments	4-Bit Dual-supply Bus Transceiver with Configurable Voltage Translation and 3-State Outputs, RGY0016A

7.2 PCB Layout

Figure 14 through Figure 17 illustrate the EVM PCB layout.

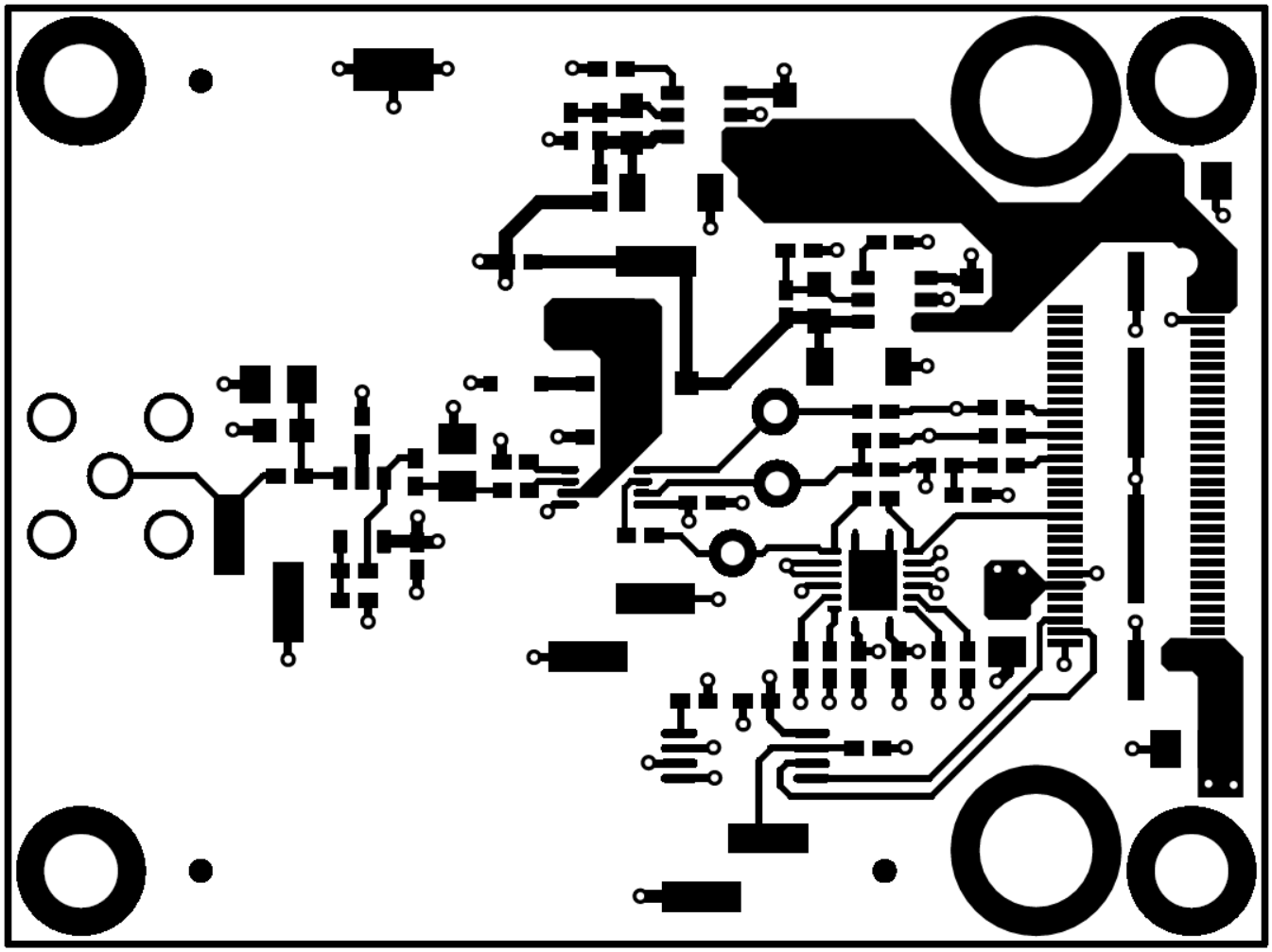

Figure 14. ADS7049-Q1EVM PCB Layer 1: Top Layer

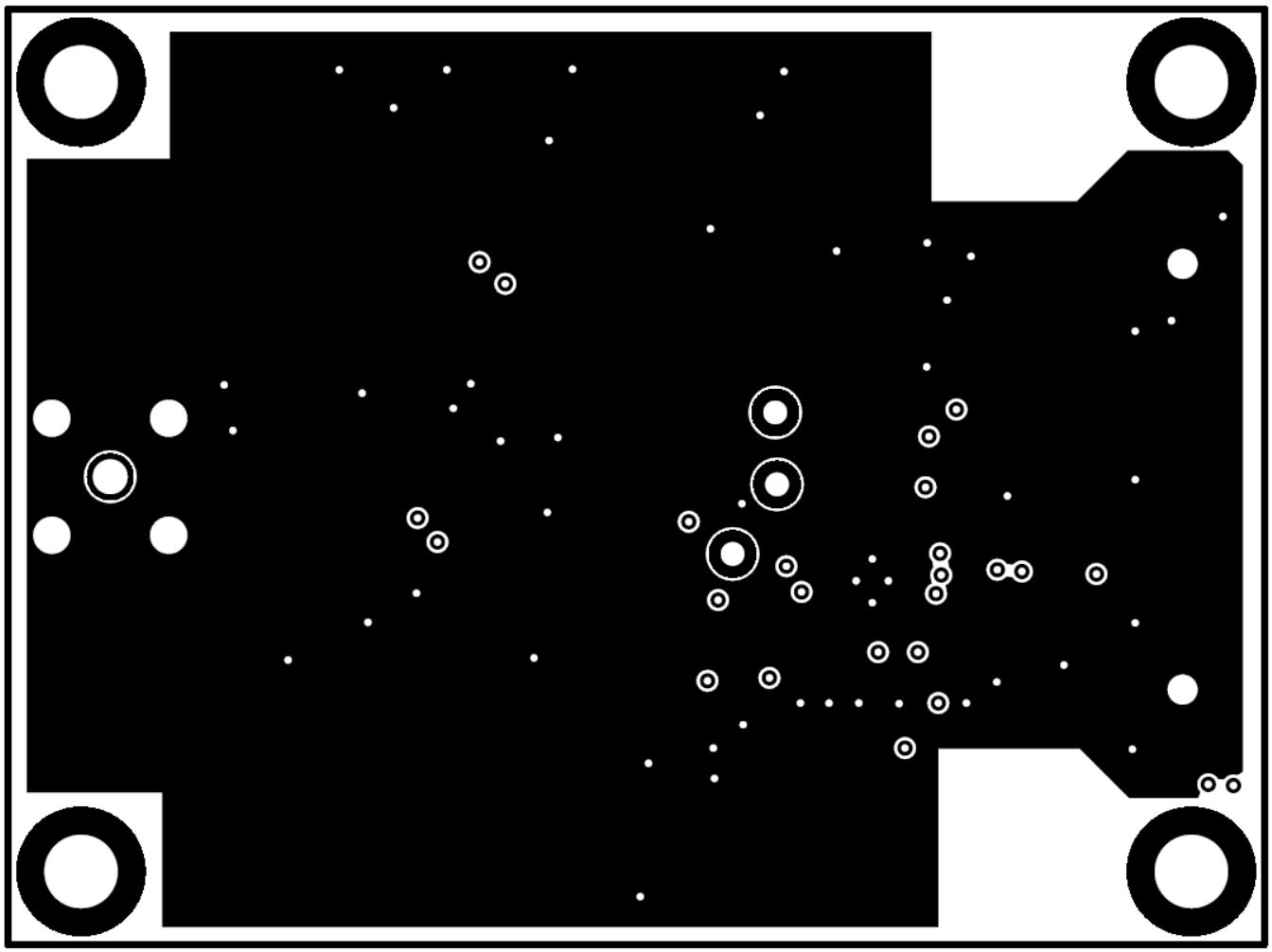

Figure 15. ADS7049-Q1EVM PCB Layer 2: GND Plane

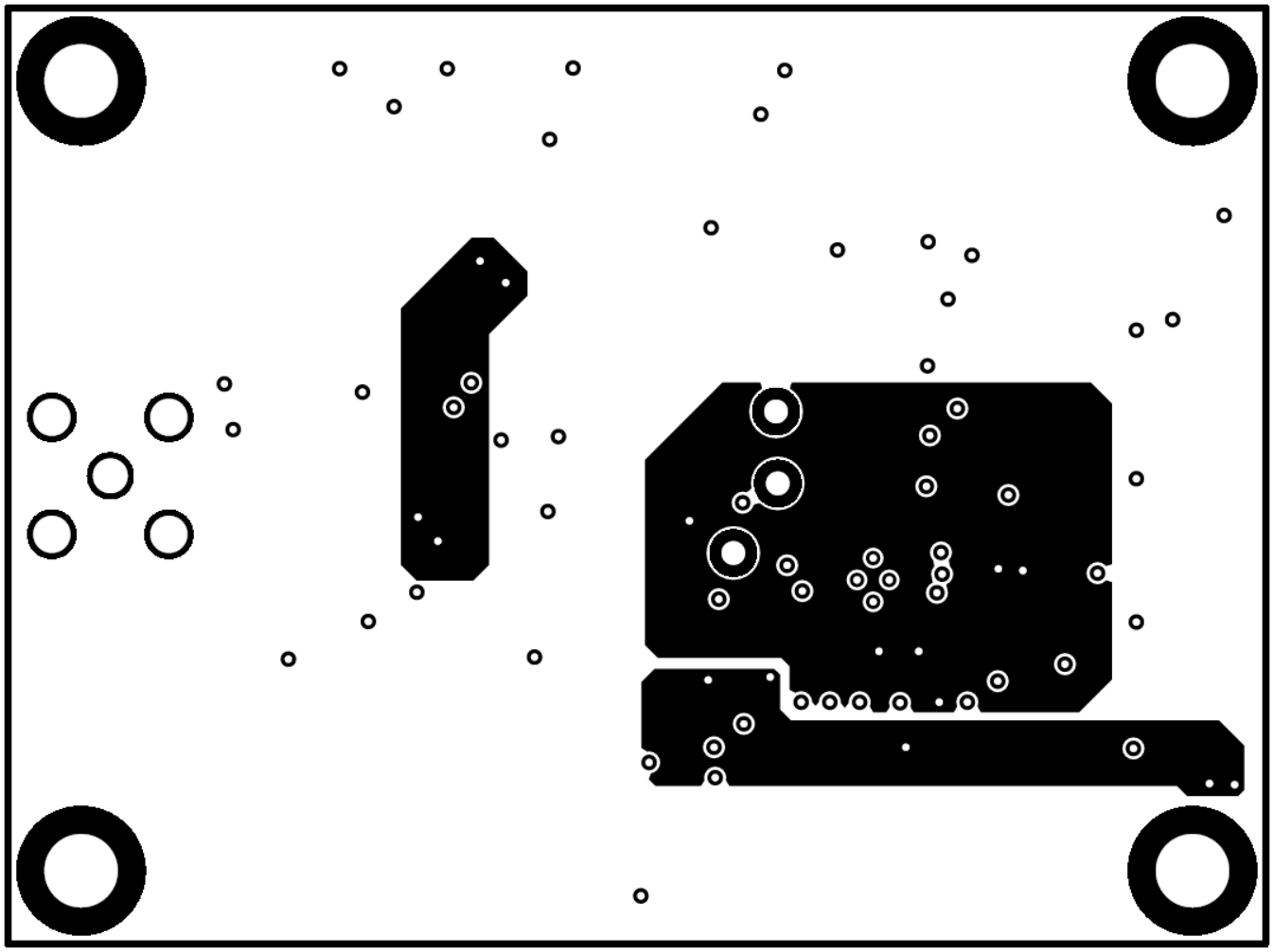

Figure 16. ADS7049-Q1EVM PCB Layer 3: Power Planes

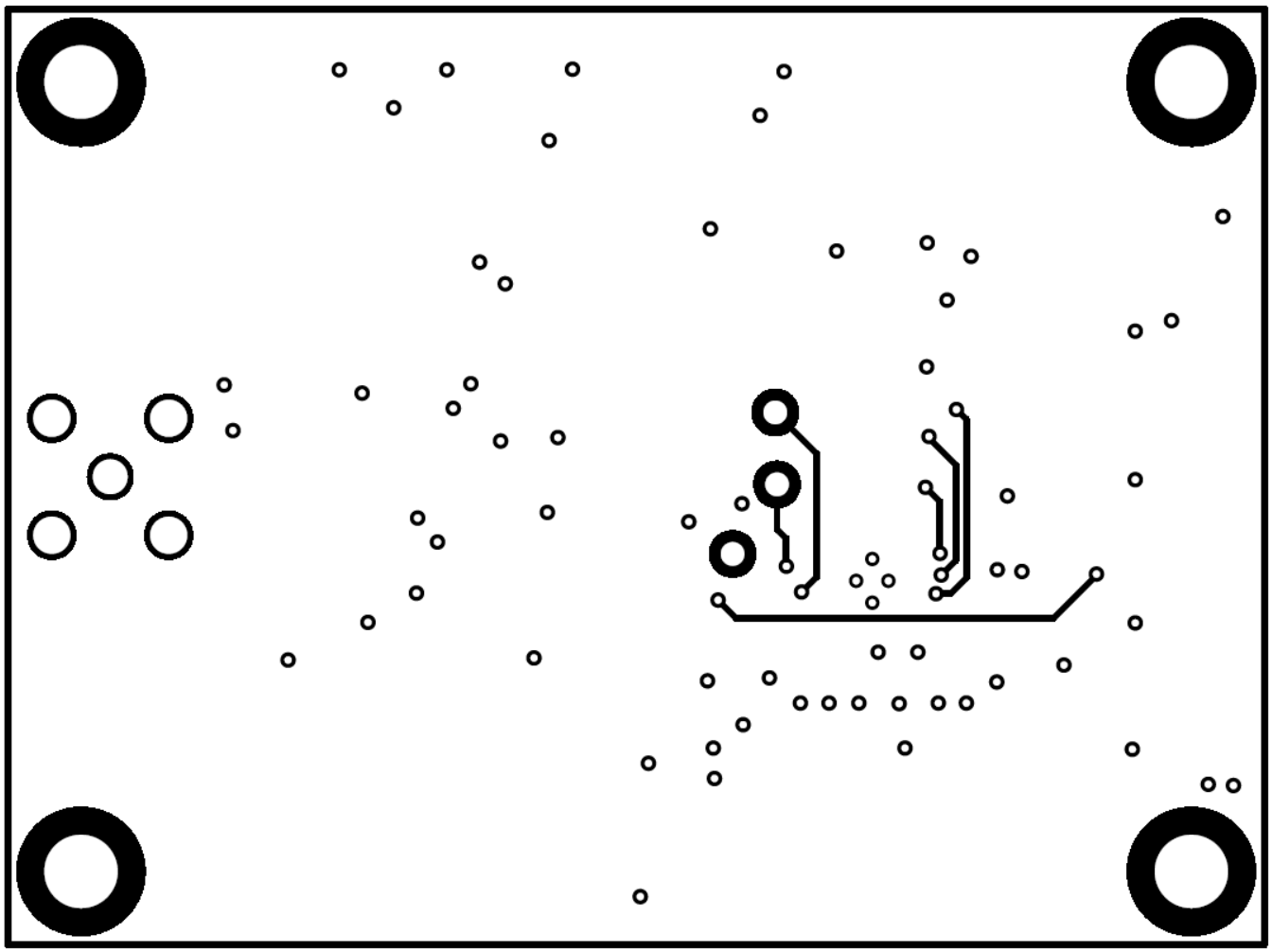

Figure 17. ADS7049-Q1EVM PCB Layer 4: Bottom Layer

7.3 Schematics

Figure 18 and Figure 19 illustrate the EVM schematics.

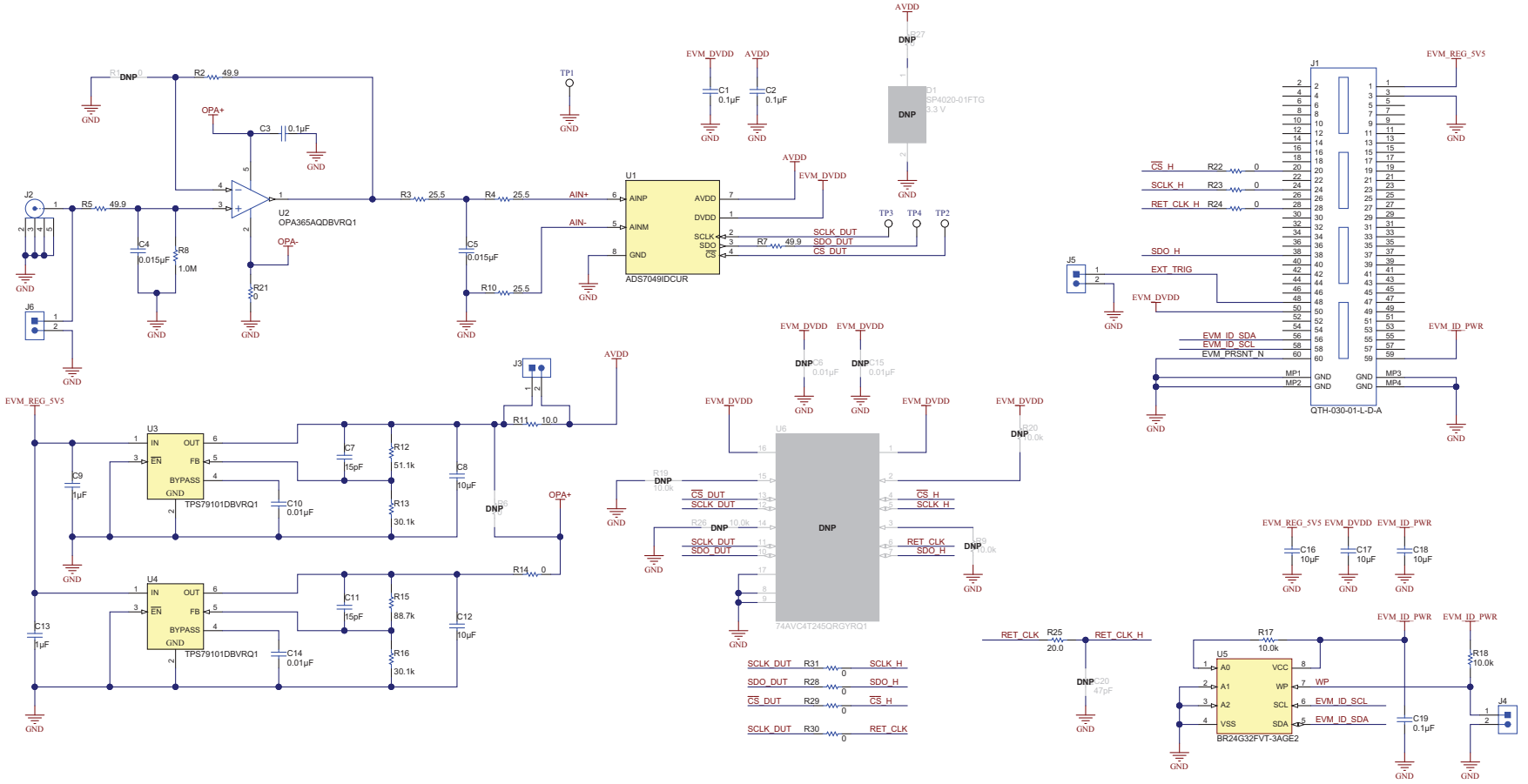

Figure 18. Schematic Diagram (Page 1) of the ADS7049-Q1EVM PCB

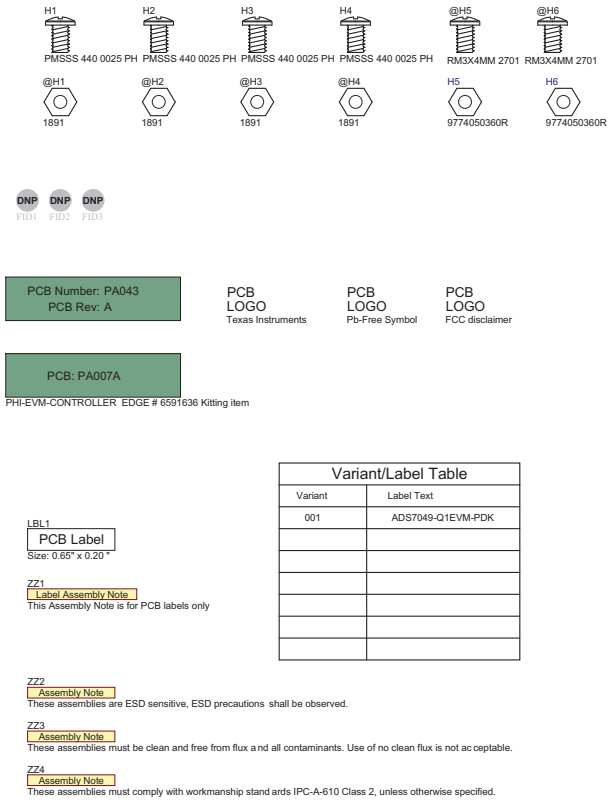

Figure 19. Schematic Diagram (Page 2) of the ADS7049-Q1EVM PCB

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2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

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   2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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