



ENSMB = 1 (SMBUS SLAVE MODE) FLOAT (SMBUS MASTER MODE)			
SCL	50	1. LVCMOS	ENSMB: master or slave mode. SMBUS clock input pin is enabled (slave mode). SMBUS clock output after loading configuration from EEPROM (master mode).
SDA	49	1. LVCMOS	ENSMB: master or slave mode. Two-Wire Interfacing: SDA pin is enabled. Data input or open-drain (pushdown only).
ADDR03	54, 53, 47, 46	1. LVCMOS	ENSMB: Master or Slave mode. SMBus address pins. In SMBus mode, these pins are the user set SMBus slave address pins.
RESET/INT	26	1. LVCMOS	ENSMB: P-CEAT (SMBus master mode). When using an external EEPROM, a transition from high to low starts the load from the external EEPROM.

当ENSMB=1时，
EQ_S0\EQ_S1\DEM_D0\DEM_D1为地址管脚。
DEM_S0\DEM_S1为I2C配置管脚。

CONTROL PINS — BOTH PIN AND SMBUS MODES (LVCMOS)			
MODE	21	1. ALEVEL, LVCMOS	0: Set I2C mode. P-CEAT: Set I2C and I2C+ P-CEAT: Set I2C and I2C+ (I2C+ only).
INPUT_EN	22	1. ALEVEL, LVCMOS	0: Internal operation. FANOUT is disabled. Use SEL0 to select the A or B input/output (use 0:0 to 0:0). 1: External operation. FANOUT is enabled. FANOUT is disabled.
SEL0	23	1. ALEVEL, LVCMOS	0: Select input B. FANOUT is disabled. FANOUT is disabled. 1: Select input B. FANOUT is disabled. FANOUT is disabled.
SEL1	24	1. ALEVEL, LVCMOS	0: Select input B. FANOUT is disabled. FANOUT is disabled. 1: Select input B. FANOUT is disabled. FANOUT is disabled.

- HM21_RX0- << HM21_RX0- [11]
- HM21_RX0+ << HM21_RX0+ [11]
- HM21_RX1- << HM21_RX1- [11]
- HM21_RX1+ << HM21_RX1+ [11]
- HM21_RX2- << HM21_RX2- [11]
- HM21_RX2+ << HM21_RX2+ [11]
- HM21_RX3- << HM21_RX3- [11]
- HM21_RX3+ << HM21_RX3+ [11]
- HM20_RX_RCK- << HM20_RX_RCK- [11]
- HM20_RX_RCK+ << HM20_RX_RCK+ [11]
- RX_SV_N << RX_SV_N [15]
- RX_HPD_N << RX_HPD_N [15]
- HM21_SCL << HM21_SCL [15]
- HM21_SDA << HM21_SDA [15]
- HM_TX_SCL2 << HM_TX_SCL2 [15]
- HM_TX_SDA2 << HM_TX_SDA2 [15]