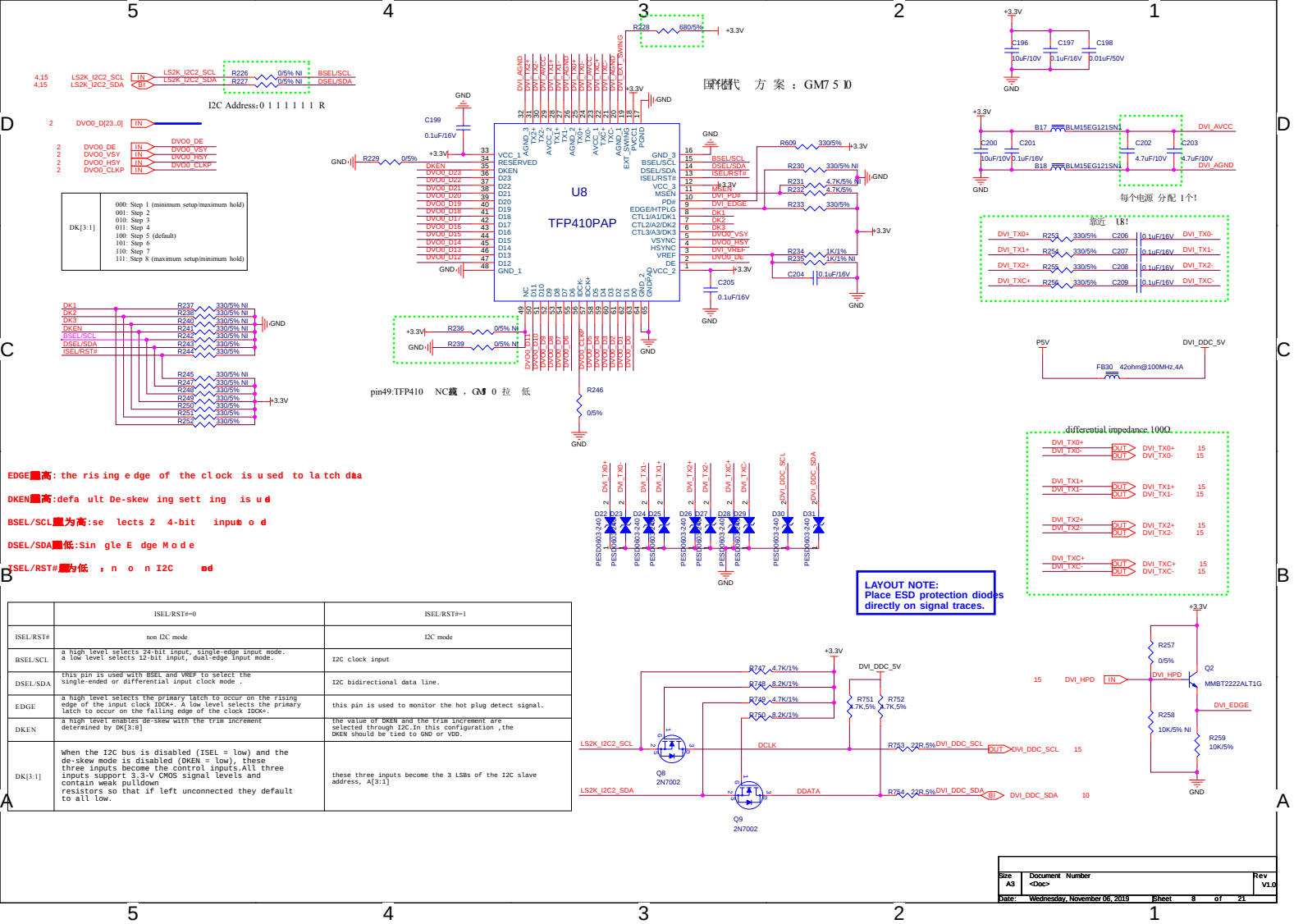

EDGE置高: the ris ing e dge of the cl ock is u sed to la tch data

DKEN置高:defa ult De-skew ing sett ing is u d

BSEL/SCL置为高:se lects 2 4-bit inpu t o d

DSEL/SDA置低:Sin gle E dge M o d e

ISEL/RST#置为低 ： n o n I2C mod

	ISEL/RST#=0	ISEL/RST#=1
ISEL/RST#	non I2C mode	I2C mode
BSEL/SCL	a high level selects 24-bit input, single-edge input mode. a low level selects 12-bit input, dual-edge input mode.	I2C clock input
DSEL/SDA	this pin is used with BSEL and VREF to select the single-ended or differential input clock mode .	I2C bidirectional data line.
EDGE	a high level selects the primary latch to occur on the rising edge of the input clock IDCK+. A low level selects the primary latch to occur on the falling edge of the clock IDCK+.	this pin is used to monitor the hot plug detect signal.
DKEN	a high level enables de-skew with the trim increment determined by DK[3:0]	the value of DKEN and the trim increment are selected through I2C.In this configuration ,the DKEN should be tied to GND or VDD.
DK[3:1]	When the I2C bus is disabled (ISEL = low) and the de-skew mode is disabled (DKEN = low), these three inputs become the control inputs.All three inputs support 3.3-V CMOS signal levels and contain weak pulldown resistors so that if left unconnected they default to all low.	these three inputs become the 3 LSBs of the I2C slave address, A[3:1]

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