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A

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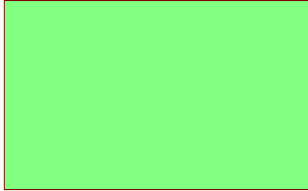
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C

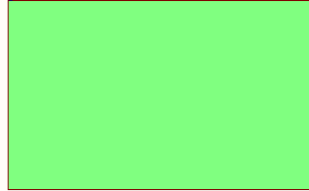
D

D

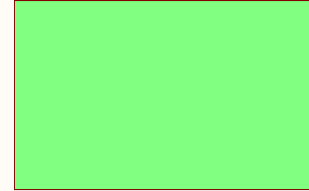
U_ET1100
ET1100.SchDoc



U_greenconn_EBUS
greenconn_EBUS.SchDoc



U_M8_P_OUT
M8_P_OUT.SchDoc



U_DP83822
DP83822.SchDoc



U_M8_P_IN
M8_P_IN.SchDoc



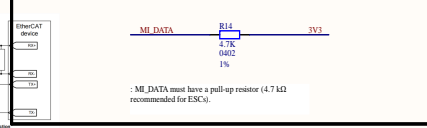
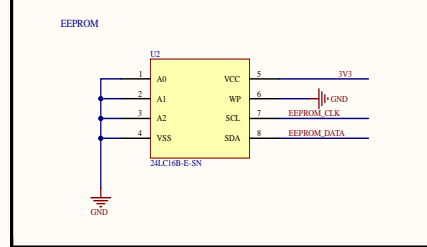
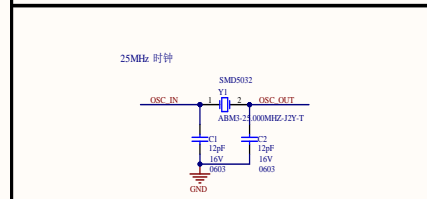
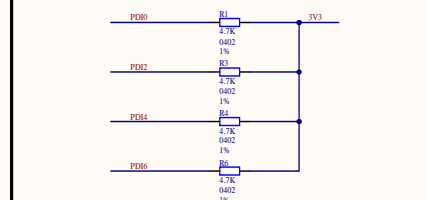
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File:	F:\ketiziliao\main.SchDoc	Drawn By:

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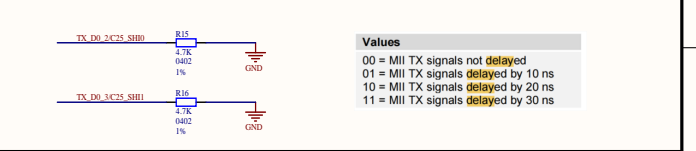
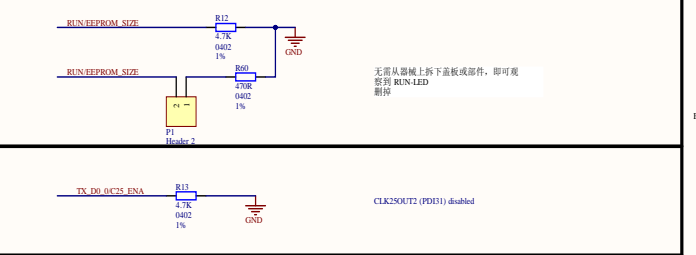
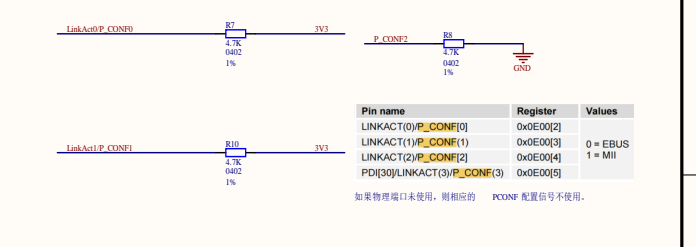
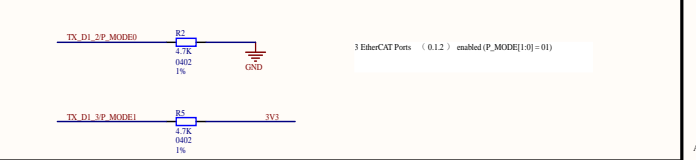
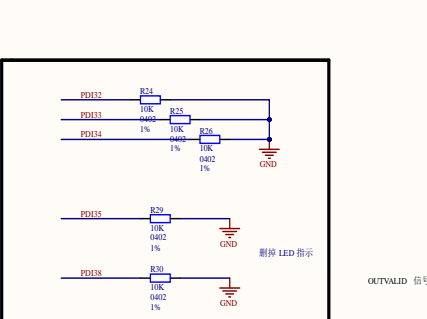


PDIOpin#4	PDIOpin#32n	PDIOpin#32n	PDIOpin#32n	PDIOpin#32n	PDIOpin#32n	PDIOpin#32n	PDIOpin#32n
PDIO[3]	SOFT	OE_EXT	OUTVALID	WD_TRIG	LATCH_IN	OE_CONF	EEPROM_LOADED
PDIO[3]	OE_EXT	OE_EXT	OUTVALID	WD_TRIG	LATCH_IN	OE_CONF	EEPROM_LOADED
PDIO[4]	OUTVALID	OE_EXT	WD_TRIG	LATCH_IN	OE_CONF	OE_CONF	EEPROM_LOADED
PDIO[5]	WD_TRIG	OE_EXT	LATCH_IN	OE_CONF	OE_CONF	OE_CONF	EEPROM_LOADED
PDIO[6]	LATCH_IN	OE_EXT	OE_CONF	OE_CONF	OE_CONF	OE_CONF	EEPROM_LOADED
PDIO[7]	OE_CONF	OE_CONF	OE_CONF	OE_CONF	OE_CONF	OE_CONF	EEPROM_LOADED
PDIO[8]	EEPROM_LOADED	OE_CONF	OE_CONF	OE_CONF	OE_CONF	OE_CONF	EEPROM_LOADED
PDIO[9]	-	OE_CONF	OE_CONF	OE_CONF	OE_CONF	OE_CONF	EEPROM_LOADED

ETH100 具有输出使能信号 OE_EXT 和输出使能信号 OE_CONF。通过 OE_EXT 信号，可清除 I/O 信号并将其置于高阻状态。OE_CONF 控制输出驱动器在输出使能信号 OE_EXT 设置为低电平或 SyncManager 看门狗超时后（且未配置时）复位。

在正常模式下，OE_CONF 被忽略。若 OE_EXT 为 0 或看门狗超时，输出事件期间 IO 将驱动至低电平。

对于外部看门狗实现方案，可采用 WD_TRIG（看门狗触发）信号。当同步管理器的看门狗被触发前，看门狗生成 WD_TRIG 和 OUT 信号。程序可使用内部同步管理器的看门狗功能。当外部看门狗超时后，可通过 OE_EXT 和 OE_CONF 参数配置 I/O 信号。对于未配备 WD_TRIG 信号的设备，可将 OUT VALID 配置为对应 WD_TRIG 信号的功能。



Pin name	Register	Values
LINKACT(0)/P_CONF[0]	0xE00[2]	
LINKACT(1)/P_CONF[1]	0xE00[3]	0 = EBUS 1 = MII
LINKACT(2)/P_CONF[2]	0xE00[4]	
PDIO[30]/LINKACT(3)/P_CONF(3)	0xE00[5]	

Values
00 = MII TX signals not delayed
01 = MII TX signals delayed by 10 ns
10 = MII TX signals delayed by 20 ns
11 = MII TX signals delayed by 30 ns

Values
00 = off
01 = 25 MHz
10 = 20 MHz
11 = 10 MHz

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OUTVALID 信号上的脉冲表示一个输出事件。如果将输出事件配置为工作结果 EEPROM 加载信号表示数字 1 0 接口正常工作

SOFT 表示以太帧的开始

此为 PHY 管理的时钟接口：透明模式禁用时，逻辑性设置为低电平有效（连接 PHY 芯片的管理数据时钟）

Digital-IO 模式下 SYNC_LATCH 完全失效

删除 LED 指示

删除 LED 指示

Transparent Mode disabled (TRANS_MODE_ENA = 0)

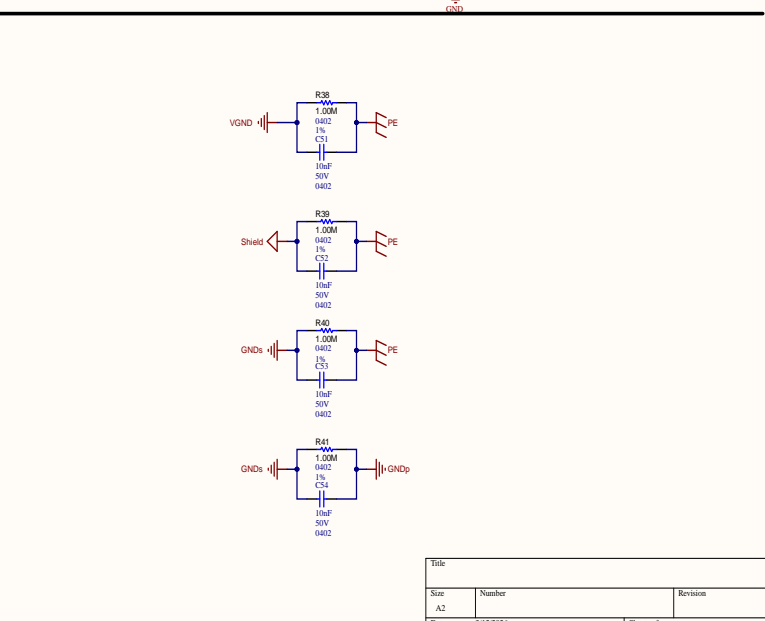
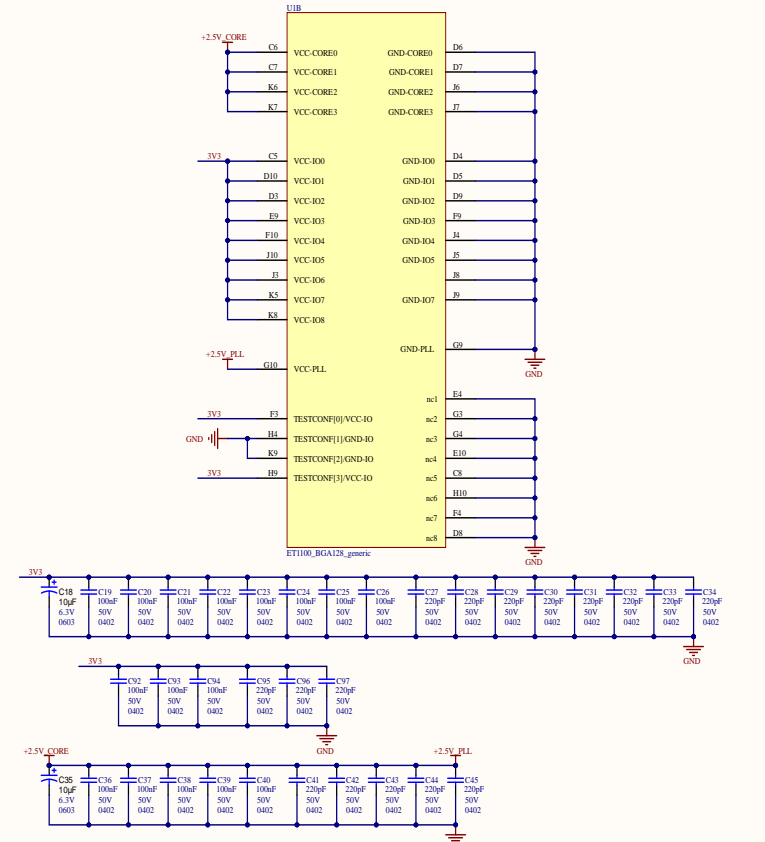
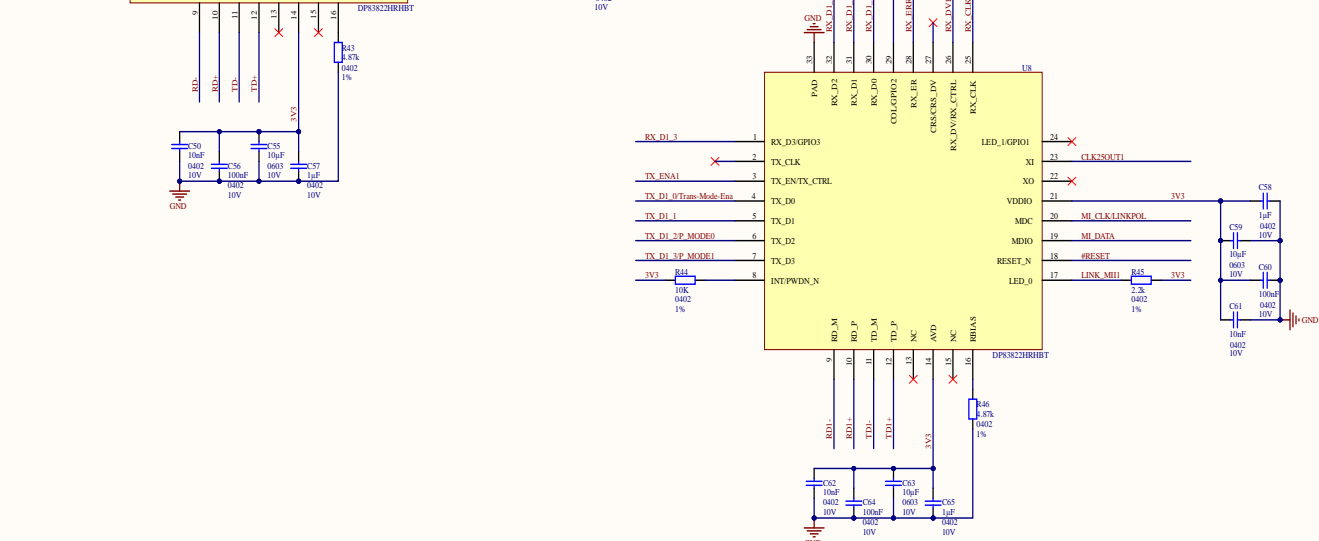
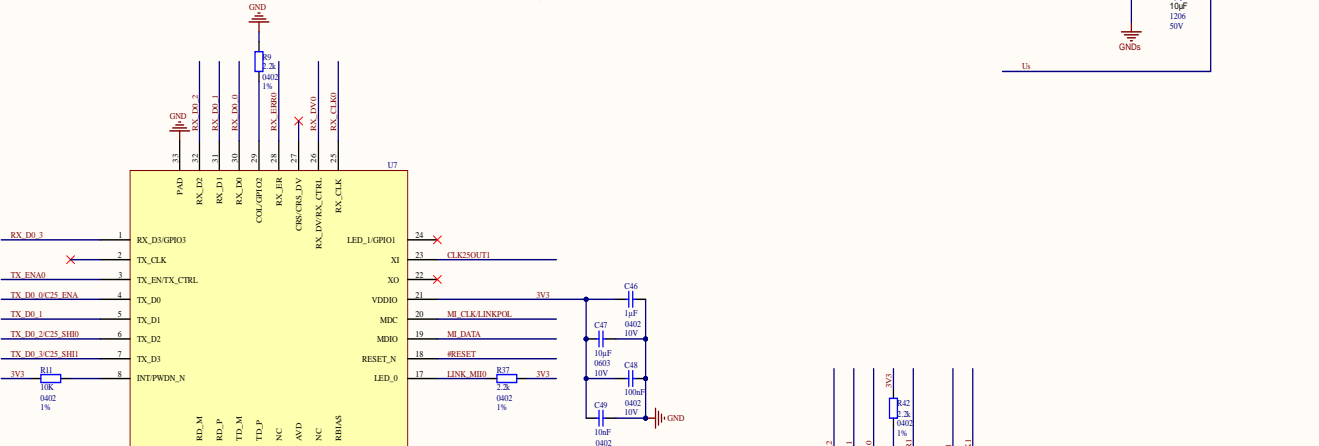
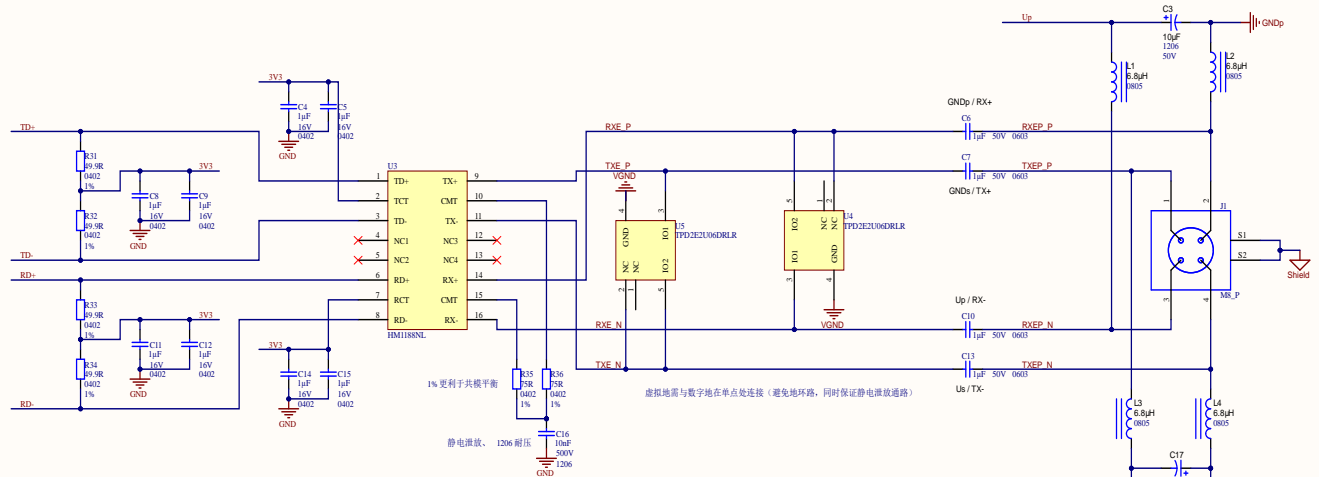
PHY Address Offset = 0

3 EtherCAT Ports (0.1.2) enabled (P_MODE[1:0] = 01)

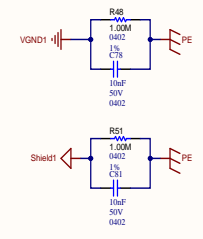
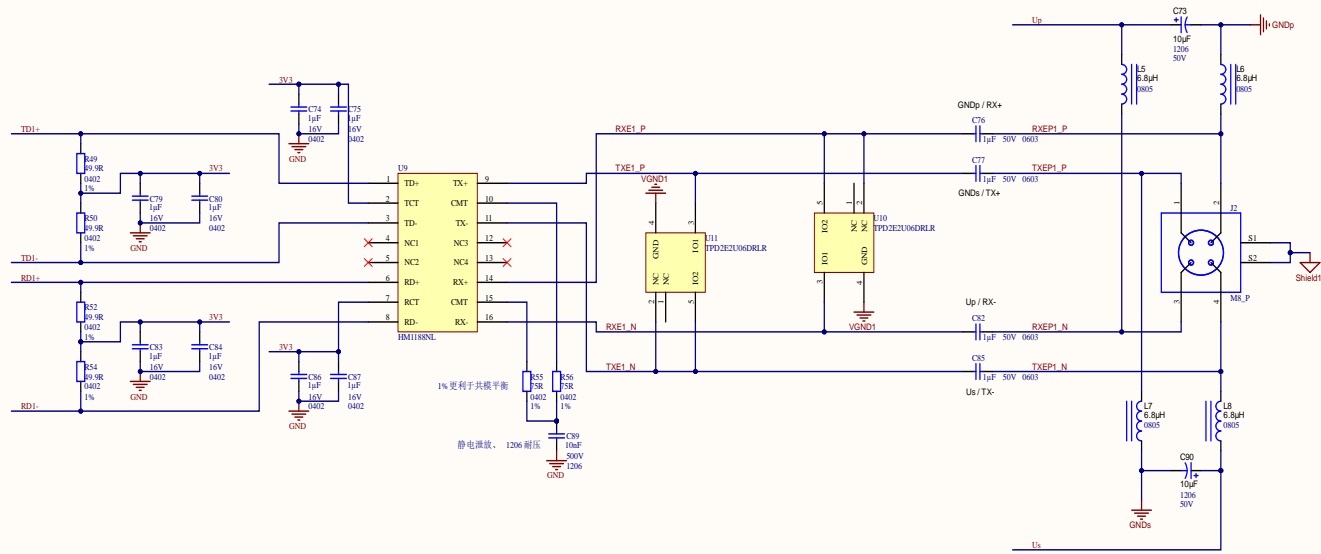
如果物理接口未使用，则相应的 PCONF 配置信号不使用。

无需从器件上拆下盖板或部件，即可观察到 RUN_LED 翻转

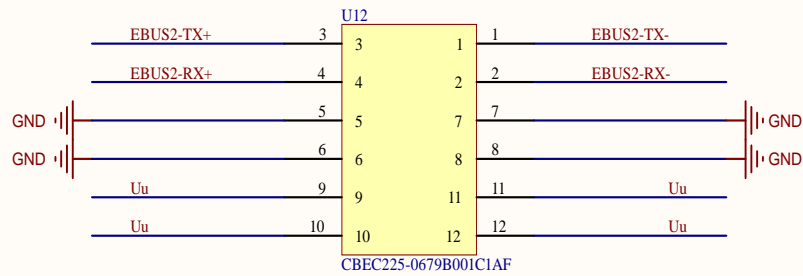
CLK25OUT2 (PDIO13) disabled



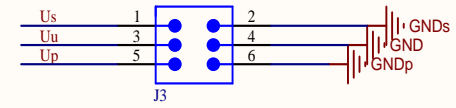
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Date	3/12/2026	Sheet of
File	F:\kernel\mb_p\tn_schDoc	Drawn By:



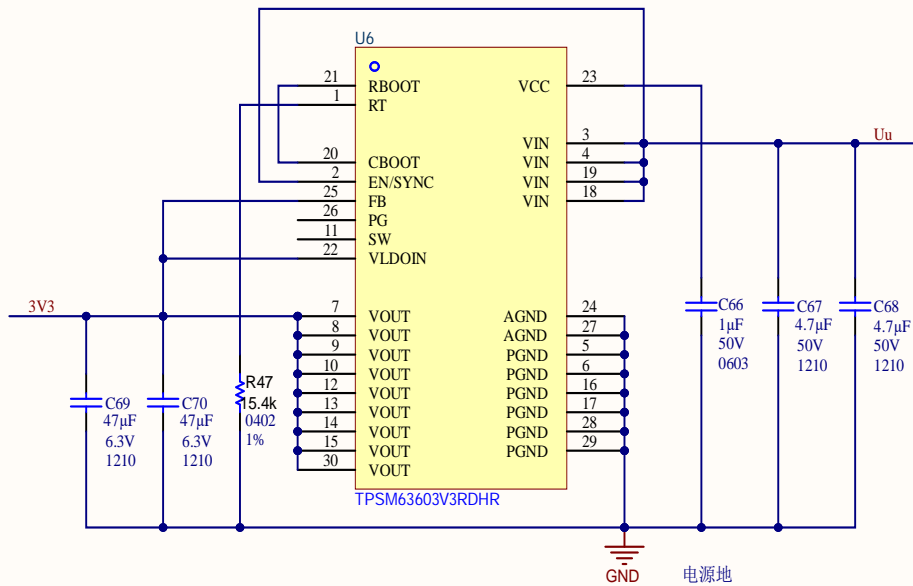
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A2		
Date	3/12/2016	Sheet of
File	F:\test\lib\MS_P_OUT_SchDoc	Drawn By:



GNDs GNDp 用的都是 M8 P 分开的，在第一个屏蔽孔附近



24V-3.3V



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Date:	3/12/2026	Sheet of
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