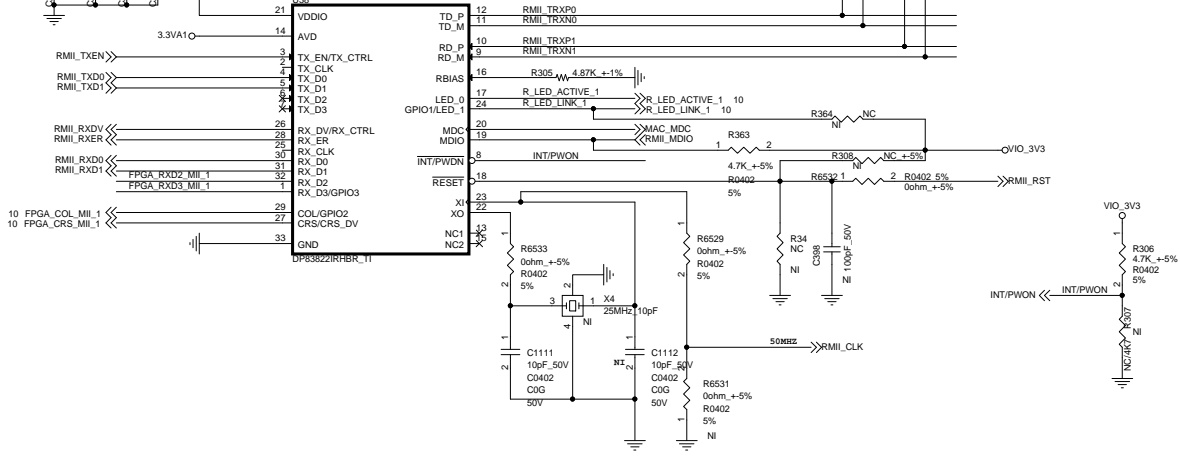
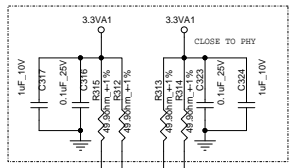
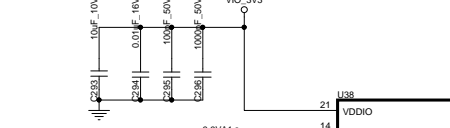
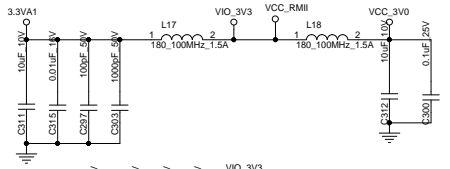
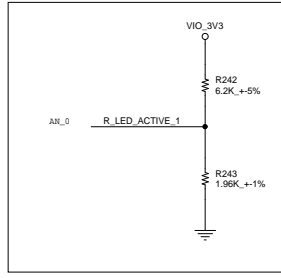
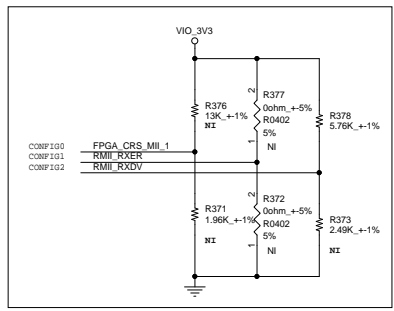
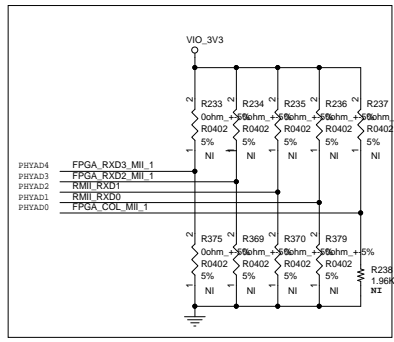


RMII_TRXP0
 RMII_TRXN0
 RMII_TRXP1
 RMII_TRXN1

15 CN_RGMII_LED_100-L << CN_RMII_LED_100-L
 15 CN_RGMII_LED_ACT-L << CN_RMII_LED_ACT-L
 15 RGMII_TRXN1 << RMII_TRXN1
 15 RGMII_TRXP1 << RMII_TRXP1
 15 RGMII_TRXN0 << RMII_TRXN0
 15 RGMII_TRXP0 << RMII_TRXP0

R_LED_ACTIVE_1 R6527 1 0ohm +5% R0402 5% CN_RMII_LED_ACT-L
 NI
 R_LED_LINK_1 R6528 1 0ohm +5% R0402 5% CN_RMII_LED_100-L
 NI

注意: for primary LAN(TI DP83822IRHBR, U38) FPGA_RXD3_MII_1(#1 of U38) 應與 RMII_CLK (#AA6 of PX30) 相接, FPGA_CR_S_MII_1 (#27 of U38) 應與 RMII_RXDV (W5 of PX30) 相接



<< RMII_TXEN
 << RMII_TXD0
 << RMII_TXD1
 << RMII_RXER
 << RMII_RXD0
 << RMII_RXD1
 << RMII_RXDV
 << MAC_MDC
 << RMII_CLK
 << RMII_RST