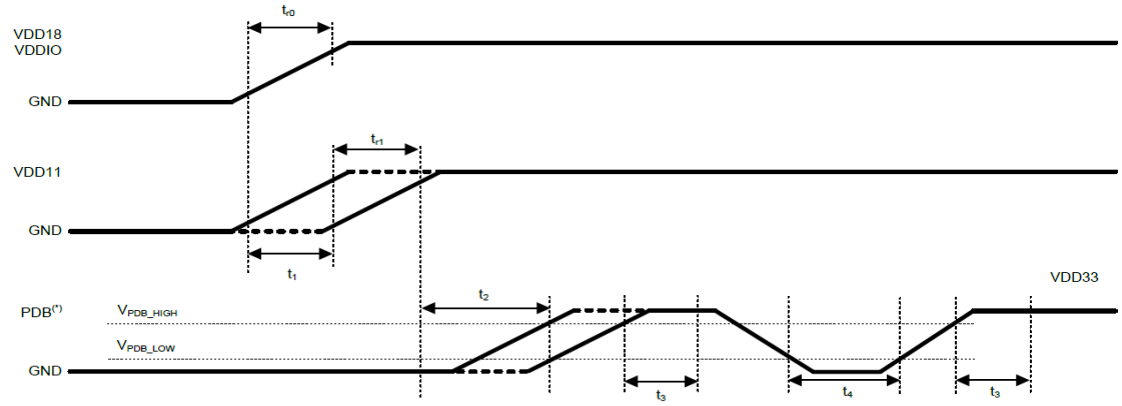
1. **Update power-up sequence: A stable OpenLDI PCLK required before OpenLDI PLL comes out of reset**

Description: In rare instances, the system display can show a pixelated mixed-color screen at power up if the DS90Ux947 device is brought out of reset while the input OpenLDI PCLK is still unstable. Note this symptom has a very low occurrence rate (in the region of ~1/1000 power cycles).

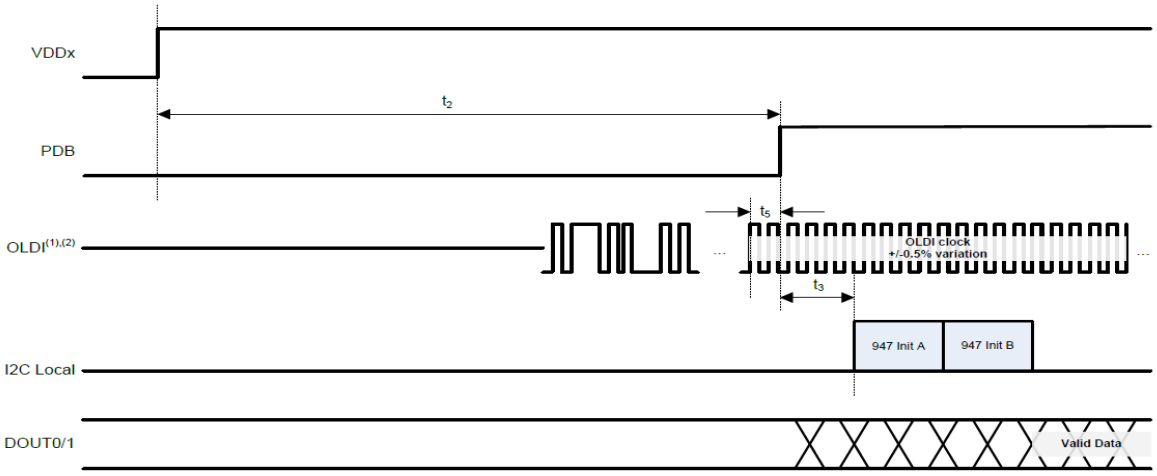
Workaround: Option A: Delay PDB release until after the OpenLDI PCLK has stabilized as shown in Figure 2. Alternatively, the PDB may be toggled again in case it comes up before the PCLK is stable as shown in Figure 3.

Option B: Apply workarounds described in Errata #2 and #3 (947 Init B Sequence) after the OpenLDI PCLK has stabilized as shown in Figure 4.



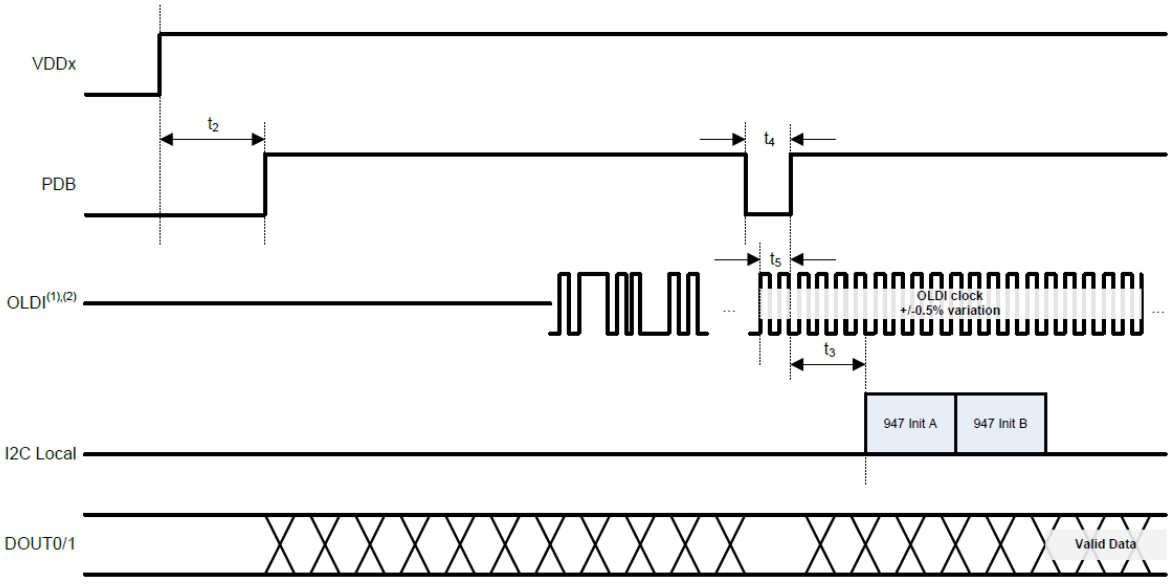
(*) It is recommended to assert PDB (active High) with a microcontroller rather than an RC filter network to help ensure proper sequencing of PDB pin after settling of power supplies.

Figure 1. Power Supply Sequencing Diagram



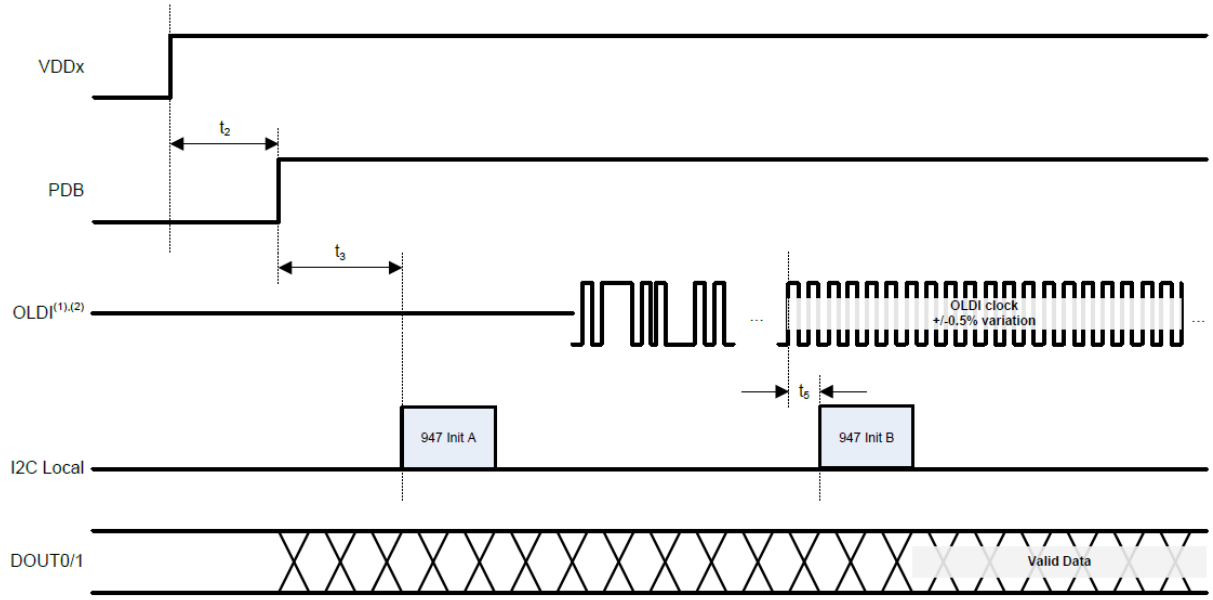
(1) Assumes OpenLDI clock and data arrive simultaneously
(2) Electrical Characteristics of the LVDS should follow TIA/EIA-644-A and OpenLDI specification

Figure 2. Initialization Sequencing Diagram



(1) Assumes OpenLDI clock and data arrive simultaneously
(2) Electrical Characteristics of the LVDS should follow TIA/EIA-644-A and OpenLDI specification

Figure 3. Initialization Sequencing Diagram



(1) Assumes OpenLDI clock and data arrive simultaneously
(2) Electrical Characteristics of the LVDS should follow TIA/EIA-644-A and OpenLDI specification

Figure 4. Initialization Sequencing Diagram

The 947 Init B sequence consists of a programming sequence described in Errata #2 followed by the sequence described in Errata #3.

Symbol	Description	Test Conditions	Min	Typ	Max	Units
tr0	VDDIO, VDD18 Rise time	These time constants are specified for rise time of power supply voltage ramp (10% - 90%)	~~0.2~~		1.5	ms
tr1	VDD11 Rise time		~~0.04~~		1.5	ms
t1	VDD11 Delay time	Power supplies may be ramped simultaneously. If sequenced, VDD18/VDDIO ramps-up first	0			ms
t2	PDB delay time	PDB should be released after all supplies are stable	0			ms
t3	I2C Ready time	Starting from PDB high, the local I2C access is available after this time	2			ms
t4	Hard Reset time	PDB negative pulse width required for the device reset	2			ms
t5	oLDI Clock Stable to Hard (PDB) Reset or PLL Reset (947 Init B) delay time	oLDI Clock must be within 0.5% of the target frequency and stable	1			us

Table 1. Timing Parameters

Status: The updated power-up and initialization sequences will be added in the next revisions of the DS90UB947-Q1 and DS90UH947-Q1 datasheets.

2. VCO frequency in the PLL drifts when Ta around the device changes by ~60C or more

Description: The voltage controlled oscillator (VCO) frequency in the phase locked loop (PLL) drifts when the ambient temperature around the device changes by ~60°C or more. As a result of the frequency drift, the system display may exhibit distortions or flickering.

Workaround: The following programming sequence is required for all systems. It should be written as a part of the 947 Init B sequence as shown in Figures 2, 3 or 4 and before the workaround described in Errata #3.

• Step 1: SoC/MCU reads ambient temperature
– When a system (i.e. a car) is started, read an external temperature sensor (on-board or on-chip on SoC) to determine the starting ambient temperature around the DS90Ux947-Q1 sub-system.

Step 2: Based on ambient temperature, SoC/MCU programs the following sequence to the DS90Ux947-Q1 device registers as a part of the startup configuration.

– Reg0x40=0x10 //set Page to oLDI PLL indirect registers
– Reg0x41=0x4A
– Reg0x42=0x3F
– Reg0x41=0x4B
– //Based on temperature reading from external sensor:
• Reg0x42=0x88 //if ambient temp < 10°C
• Reg0x42=0x89 //if ambient temp is ≥ 10°C

```
Reg0x41=0x49
Reg0x42=0x10   } //Reset oLDI PLL
Reg0x42=0x00
```

– Reg0x40=0x14 //set Page to FPD PLL indirect registers
– Reg0x41=0x4A
– Reg0x42=0x3F
– Reg0x41=0x4B

– //Based on temperature reading from external sensor:
• Reg0x42=0x88 //if ambient temp < 10°C
• Reg0x42=0x89 //if ambient temp is ≥ 10°C

```
Reg0x41=0x49
Reg0x42=0x10   } //Reset FPD PLL
Reg0x42=0x00
```

The software workaround above ensures device operation over a continuous temperature drift of -20°C to 80°C in cold-start conditions and 80°C to 25°C in hot-start conditions. If device operation is desired over a larger temperature range in hot-start conditions, the software workaround below should be implemented instead.

– Reg0x40=0x10 //set Page to oLDI PLL indirect registers
– Reg0x41=0x4A
– Reg0x42=0x3F
– Reg0x41=0x4B
– //Based on temperature reading from external sensor:
• Reg0x42=0x88 //if ambient temp < -10°C
• Reg0x42=0x89 //if -10°C ≤ ambient temp is < 60°C
• Reg0x42=0x8A //if ambient temp is ≥ 60°C

Reg0x41=0x49
Reg0x42=0x10
Reg0x42=0x00
} //Reset oLDI PLL

– Reg0x40=0x14 //set Page to FPD PLL indirect registers
– Reg0x41=0x4A
– Reg0x42=0x3F
– Reg0x41=0x4B
– //Based on temperature reading from external sensor:
• Reg0x42=0x89 // if ambient temp < -10°C
• Reg0x42=0x8A //if -10°C ≤ ambient temp is < 60°C
• Reg0x42=0x8B //if ambient temp is ≥ 60degC

Reg0x41=0x49
Reg0x42=0x10
Reg0x42=0x00
} //Reset FPD PLL

Note: This software workaround should be reprogrammed after any device reset. The software workaround resets the input (oLDI) PLL and the output (FPD) PLL at the end of their respective reconfiguration steps. If the Serializer had already established a lock with a companion Deserializer device, each of the PLL reset steps will cause a brief period of unlock in this link. The oLDI PLL may be reset just before the FPD PLL reset step.

Status: The required recommendations and programming sequences will be added in the next revisions of the DS90UB947-Q1 and DS90UH947-Q1 datasheets.

3. Reset the OLDI clock generation block after PLL lock at power-up when using dual-OLDI mode

Description: The system display has a red or blue background with flicker imposed on the video image at power up. Note this symptom has a very low occurrence rate (in the region of ~1/1000 power cycles). A reset of the PLL divider block is required.
Work-around: The following programming sequence is required for all systems. It should be written as a part of the 947 Init B sequence as shown in Figures 2, 3 or 4 and after the workaround described in Errata #2.

Reg0x40=0x10

Reg0x41=0x49

Reg0x42=0x16

Reg0x41=0x47

Reg0x42=0x20

Reg0x42=0xA0

Reg0x42=0x20

- ~~Reg0x42=0x20~~
- ~~Reg0x42=0x20~~
- ~~Reg0x42=0x20~~
- ~~Reg0x42=0x20~~

Reg0x42=0x00

Reg0x41=0x49

Reg0x42=0x00

Note: This software workaround should be reprogrammed after any device reset. The software workaround resets the input (oLDI) PLL at the end of the reconfiguration steps. If the Serializer had already established a lock with a companion Deserializer device, the PLL reset steps will cause a brief period of unlock in this link.

Status: The required programming sequences will be added in the next revisions of the DS90UB947-Q1 and DS90UH947-Q1 datasheets.

4. Add Prevention of AV Mute Info

Description: When using DS90UB947-Q1, it is possible to send video data during the blanking period (DE = L). If a specific pattern is sent during the blanking period, the companion Deserializer will enter AVMUTE mode. The pattern that the Deserializer is looking for is 24'h666666. If the last pixel of the frame is 24'h666666, and the video transmission extends into the DE = L period, then AVMUTE mode will be enabled.

Work-around: Setting DE_GATE_RGB register bit (0x04[4] = "1") on the DS90UB947 will prevent video from being sent during the blanking interval. This will ensure AVMUTE mode is not entered during normal operation.

Any device configuration including this one should be written as a part of the 947 Init A sequence as shown in Figures 2, 3 or 4.

5. **Indirect access registers information omitted in the datasheet**

Description: Some analog controls are located in the indirect access register space. Access to these controls is provided via an indirect access mechanism through the Analog Indirect Access registers (ANA_IA_CTL, ANA_IA_ADDR, and ANA_IA_DATA). These registers are located at offsets 0x40-0x42 in the main register space. The following are their descriptions: The indirect address mechanism involves setting the control register to select the desired block, setting the register offset address, and reading or writing the data register.

ADDRESS	REGISTER NAME	BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0x40	ANA_IA_CTL					
		7:5	reserved	RW	0	Reserved
		4:2	ANA_IA_SEL	RW	0	Analog Register Select: Selects target for register access 000 : Disabled 001 - 011 : Reserved 100 : OLDI Registers 101 : FPD3 TX Registers 11x : Reserved
		1	reserved	RW	0	Reserved
		0	ANA_IA_R/W_SEL	RW	0	Read / Write Select 0 : Write 1 : Read
0x41	ANA_IA_ADDR					
		7:0	ANA_IA_ADDR	RW	0	Analog Register Offset: This regiser contains the 8-bit register offset for the indirect access.
0x42	ANA_IA_DATA					
		7:0	ANA_IA_DATA	RW	0	Analog Register Data: Writing this register will cause an indirect write of the ANA_IA_DATA value to the selected analog block register. Reading this register will return the value of the selected analog block register

For writes, the process is as follows:
1. Write to the ANA_IA_CTL register to select the desired register block and Write operation
2. Write to the ANA_IA_ADDR register to set the register offset
3. Write the data value to the ANA_IA_DATA register

For reads, the process is as follows:
1. Write to the ANA_IA_CTL register to select the desired register block and Read operation
2. Write to the ANA_IA_ADDR register to set the register offset
3. Read from the ANA_IA_DATA register

The following are the oLDI PLL Analog Indirect Access Registers (ANA_AI_SEL=100):

ADDRESS	REGISTER NAME	BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0x49	oLDI_PLL_STATE_MC_CTL					
		7:5	RESERVED	R	0	Reserved
		4	OLDI_STATE_MC_RESET	RW	0	Enable oLDI PLL reset state: 0 : Disable state machine reset (normal operation) 1 : Enable state machine reset
		3:0	OLDI_STATE_MC_CTLS	RW	0	0000 = RESET 0001 = INITIAL_VCO_SETTLING 0010 = SELECT_DIVIDER_PPM 0011 = FREQ_DAC_TIMER 0100 = FREQ_DAC_PPM 0101 = FREQ_DAC_SELECT 0110 = PFD_CLOSE_LOOP_TIMER 0111 = MONITOR_FREQ_LOCK 1000 = CHECK_FREQ_LOCK 1001 = FREQ_LOCK_TIMER
0x4A	oLDI_PLL_PPM_COUNTER					
		7:0	OLDI_PPM_CNTER_DPTH	RW	7	oLDI PLL reference clock to feedback clock frequency skew parts-per-million (PPM) counter depth 00: 8-bit counters 01: 9-bit counters 03:10-bit counters 07:11-bit counters 0F:12-bit counters 1F:13-bit counters 3F 14-bit counters 7F:15-bit counters FF:16-bit coutners
0x4B	oLDI_PLL_SETTING					
		7	RESERVED	RW	1	
		6:4	RESERVED	RW	0	
		3:0	oLDI_INIT_LOOP_FLTR_VLTG	RW	0xA	oLDI PLL loop filter initial charge voltage setting 0: 0.244 1: 0.325 2: 0.407 3: 0.488 4: 0.569 5: 0.651 6: 0.732 7: 0.813 8: 0.895 9: 0.976 A: 1.057 B: 1.139 C: 1.22 D: 1.301 E: 1.383 F: 1.464

The following are the FPD PLL Analog Indirect Access Registers (ANA_AI_SEL=101):

ADDRESS	REGISTER NAME	BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0x49	FPD_PLL_STATE_MC_CTL					
		7:5	RESERVED	R	0	Reserved
		4	FPD_STATE_MC_RESET	RW	0	Enable FPD PLL reset state: 0 : Disable state machine reset (normal operation) 1 : Enable state machine reset
		3:0	RESERVED	RW	0	Always write '0000b' to this field
0x4A	FPD_PLL_PPM_COUNTER					
		7:0	FPD_PPM_CNTER_DPTH	RW	7	FPD PLL reference clock to feedback clock frequency skew parts-per-million (PPM) counter depth 00: 8-bit counters 01: 9-bit counters 03:10-bit counters 07:11-bit counters 0F:12-bit counters 1F:13-bit counters 3F 14-bit counters 7F:15-bit counters FF:16-bit coutners
0x4B	FPD_PLL_SETTING					
		7	RESERVED	RW	1	
		6:4	RESERVED	RW	0	
		3:0	FPD_INIT_LOOP_FLTR_VLTG	RW	0xA	FPD PLL loop filter initial charge voltage setting 0: 0.244 1: 0.325 2: 0.407 3: 0.488 4: 0.569 5: 0.651 6: 0.732 7: 0.813 8: 0.895 9: 0.976 A: 1.057 B: 1.139 C: 1.22 D: 1.301 E: 1.383 F: 1.464

Status: The required information will be added in the next revisions of the DS90UB947-Q1 and DS90UH947-Q1 datasheets.