8.3 Feature Description

8.3.1 4-Level Inputs

The TDP0604 has 4-level inputs pins that control the receiver equalization gain, transmitter voltage swing, and pre-emphasis, and place TDP0604 into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings. There are internal pull-up and a pull-down resistors. These resistors are combined with the external resistor connection to achieve the desired voltage level.

Table 8-1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Tie 1-kΩ 5% to GND.
R	Tie 20-kΩ 5% to GND.
F	Float (leave pin open)
1	Tie 1-kΩ 5% to V_{CC}.

MODE (Default set to I2C Mode)

Table 8-15. MODE Pin Function

MODE Pin Level	Description
0	Pin Strap with DDC Buffer enabled
R	Pin Strap with DDC Buffer disabled
F	I2C mode
1	Reserved

8.4.1 MODE Control

The MODE pin provides four modes of operation. There are three pin-strap modes and one I²C mode. In all three pin strap modes, DDC snooping feature is enabled. In I²C mode, DDC snoop feature is enabled by default but can be disabled by a register.

8.4.1.1 I²C Mode (MODE = "F")

In I²C mode, all settings of the TDP0604 can be controlled through the registers. The TDP0604 7-bit I2C address is determined by the ADDR/EQ0 pin. All other 4-level and 2-level pins are not used in I²C mode since the functions exist in a register. The SCL/CFG0 pin will function as the I²C clock and the SDA/CFG1 pin will function as the I²C data.

The TDP0604 defaults to power down in I²C mode. Upon completion of initialization of the TDP0604, software must clear the PD_EN field to exit the power down state. The HPD_OUT pin will be asserted low while the PD_EN register is set.

The TDP0604 supports 1.2-V, 1.8-V, and 3.3-V I²C signaling levels. Selection of 1.2-V, 1.8-V, or 3.3-V is determined by the VIO pin as provided in Table 8-2.

ADDR=0x10111100 / BC or 0x10111101 / BD

8.5.2 TDP0604 I²C Address Options

For further programmability, the TDP0604 can be controlled using I²C. The SCL/CFG0 and SDA/CFG1 terminals are used for I²C clock and I²C data respectively.

Table 8-18. TDP0604 I²C Device Address Description

ADDR/EQ0 pin	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)	HEX
0	1	0	1	1	1	1	0	0/1	BC/BD
R	1	0	1	1	1	0	1	0/1	BA/BB
F	1	0	1	1	1	0	0	0/1	B8/B9
1	1	0	1	1	0	1	1	0/1	B6/B7

EQ

8.3.8 Receiver Equalizer

The equalizer is used to clean up inter-symbol interference (ISI) jitter or loss from the bandwidth-limited board traces or cables. TDP0604 supports fixed receiver equalizer by setting the EQ0 and EQ1 pins or through I²C register.

The TDP0604 has two sets of CTLE curves (3 Gbps CTLE and 6 Gbps CTLE) with each curve having 16 ac gain settings and 3 dc gain settings. The 16 ac gain settings with GLOBAL_DCG = 0x2 is detailed in Table 8-5.

The TDP0604 in pin-strap mode has two CTLE HDMI Datarate Maps: Map B and Map C. These maps are detailed in Table 8-6. The expectation is Map B or C should be used if TDP0604 is used in a source application and Map B for a sink application.

When the TDP0604 is configured for pin-strap mode, the default CTLE HDMI data rate map will be determined by the sampled state of the CTLEMAP_SEL pin as detailed in Table 8-7.

In the I²C mode, the default CTLE (3 Gbps or 6 Gbps) used for each HDMI mode can be controlled from a register.

Table 8-5. Receiver EQ Settings when GLOBAL_DCG = 0x2

EQ Setting[1]	RX EQ Level for 3Gbps CTLE (Gain at 1.5 GHz - Gain at 10 MHz)	RX EQ Level for 6Gbps CTLE (Gain at 3 GHz - Gain at 10 MHz)	EQ1 PIN	EQ0 PIN
0[2]	1.0	0.5	0	0
1	2.0	1.0	0	R
2	3.2	2.4	0	F
3	4.2	3.3	0	1
4	5.3	4.4	R	0
5	6.0	5.2	R	R
6	7.0	6.0	R	F
7	7.7	6.8	R	1
8	9.0	7.5	F	0
9	9.5	8.2	F	R
10	10.0	8.8	F	F
11	10.5	9.3	F	1
12	11.0	10.0	1	0
13	11.5	10.5	1	R
14	12.0	11.0	1	F
15	12.3	11.8	1	1

(1) In I2C mode, the receiver EQ setting is determined by D0_EQ, D1_EQ, and D2_EQ registers.
(2) When CTLEBYP_EN = 1 and dcGAIN = 0-dB, EQ settings 0 will be 0-dB due to the CTLE is bypassed.

LINEAR_EN

Table 8-4. Pin-Strap Mode LINEAR_EN Pin Function

LINEAR_EN Pin Level	Description
1	Limited Enabled
F	Linear Enabled. Recommended for HDMI sink application.
R	Reserved
0	Limited Enabled. Recommended for HDMI source application

AC_EN (Default set to AC coupled)

8.3.11 Main Link Outputs

8.3.11.1 Transmitter Bias

The TDP0604 transmitter supports both external (DC-coupled) and internal bias (AC-coupled) to a receiver. Selection between DC and AC-coupled is done through use of the AC_EN pin in pin-strap mode and TX_AC_EN register in I²C mode. The AC_EN pin informs the TDP0604 whether or not an external AC-coupling capacitor is present. When AC_EN is greater than VIH, then TDP0604 transmitters are internally biased to approximately V_{CC}. For AC-coupled application, the AC_EN pin should be connected to greater than VIH and an external AC-coupling capacitor should be placed on each of the OUT_D[2:0] pins and the OUT_CLK pin. If the AC_EN pin is connected to less than VIL, then the AC_EN pin will inform TDP0604 that AC_EN pin is DC-coupled (externally biased) to the far-end HDMI compliant receiver.

HPDOUT_SEL

HPDOUT_SEL	2	I 2-Level (PD)	HPDOUT_SEL. Selects whether HPD_OUT pin is push/pull, or open-drain. Open-drain is not supported in pin-strap mode. Therefore this pin should be left floating or pull-down to GND.

CTLEMAP_SEL

The TDP0604 in pin-strap mode has two CTLE HDMI Datarate Maps: Map B and Map C. These maps are detailed in Table 8-6. The expectation is Map B or C should be used if TDP0604 is used in a source application and Map B for a sink application.

When the TDP0604 is configured for pin-strap mode, the default CTLE HDMI data rate map will be determined by the sampled state of the CTLEMAP_SEL pin as detailed in Table 8-7.

Table 8-6. CTLE HDMI Datarate Map B and C

HDMI Mode	Map B	Map C
1.4	3 Gbps CTLE	6 Gbps CTLE
2.0	6 Gbps CTLE	6 Gbps CTLE

Table 8-7. Pin-Strap Mode CTLE HDMI Datarate Mapping

	Sampled State of CTLEMAP_SEL Pin			
	"0"	"R"	"F"	"1"
CTLE HDMI Datarate Map	Reserved	Map C	Reserved	Map B

Note

The clock lane EQ when operating in HDMI 1.4 or 2.0 will use the 3-Gbps CTLE and will be set to the zero EQ setting.

TXPRE

8.3.11.4 TX Pre-Emphasis and De-Emphasis Control

The TDP0604 provides pre-emphasis and de-emphasis on the data lanes allowing the output signal pre-conditioning to offset interconnect losses between the TDP0604 outputs and a TMDS receiver. Pre-emphasis and de-emphasis is not implemented on the clock lane. There are two methods to implement pre-emphasis, pin strapping or through I²C programming. TX pre-emphasis and de-emphasis control is only supported in limited mode.

When using pin strap mode, the TXPRE pin controls four different global pre-emphasis and de-emphasis values for all data lanes when TDP0604 is operating in HDMI 1.4 or HDMI 2.0. These pre-emphasis and de-emphasis values are described in Table 8-11.

Table 8-11. Pin-Strap TXPRE Pin Function

TXPRE Pin	HDMI 1.4 or HDMI 2.0
0	3.5 dB pre-emphasis
R	-2.5 dB de-emphasis
F	0 dB
1	6.0 dB pre-emphasis

TXSWG

8.3.11.5 TX Swing Control

The TDP0604 transmitter swing level can be adjusted in both pin strap and I²C mode. In I²C mode, TX swing settings are controlled independently for each lane (both clock and data) through registers.

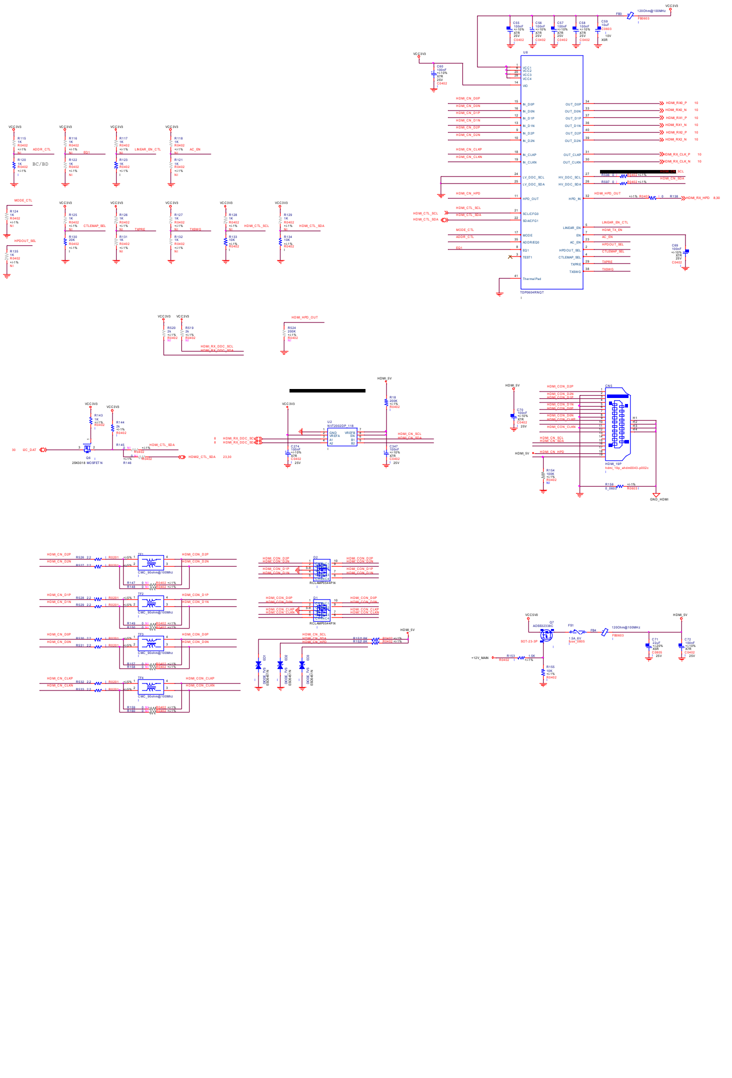
In I2C mode, the TX swing used when operating in HDMI 1.4 and HDMI 2.0 can be independently controlled through HDMI14_VOD and HDMI20_VOD registers.

In pin strap mode with limited enabled, the TXSWG pin adjusts the default 1000 mV swing as detailed in Table 8-12. In HDMI 1.4 the TXSWG pin controls the swing for both the data and clock lanes. In HDMI 2.0, the TXSWG pin controls the swing for data lanes while the clock lane will remain at default value.

In pin-strap mode with linear enabled, the linearity range is fixed at the highest level (1200 mVpp) and therefore TXSWG pin is not used. In I²C mode, the linearity range can be adjusted from a register.

Table 8-12. Pin Strap TXSWG Control

TXSWG pin	Limited Mode for HDMI 1.4	Limited Mode for HDMI 2.0	Linear Mode
0	Default (1000 mVpp)	Default (1000 mVpp)	1200 mVpp
R	Default - 5%	Default - 5%	1200 mVpp
F	Default (1000 mVpp)	Default (1000 mVpp)	1200 mVpp
1	Default (1000 mVpp)	Default + 5%	1200 mVpp



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8.3 Feature Description

8.3.1 4-Level Inputs

The TDP0604 has 4-level inputs pins that control the receiver equalization gain, transmitter voltage swing, and pre-emphasis, and place TDP0604 into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings. There are internal pull-up and a pull-down resistors. These resistors are combined with the external resistor connection to achieve the desired voltage level.

Table 8-1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Tie 1-kΩ 5% to GND.
R	Tie 20-kΩ 5% to GND.
F	Float (leave pin open)
1	Tie 1-kΩ 5% to V_{CC}.

MODE (Default set to I2C Mode)

Table 8-15. MODE Pin Function

MODE Pin Level	Description
0	Pin Strap with DDC Buffer enabled
R	Pin Strap with DDC Buffer disabled
F	I2C mode
1	Reserved

8.4.1 MODE Control

The MODE pin provides four modes of operation. There are three pin-strap modes and one I²C mode. In all three pin strap modes, DDC snooping feature is enabled. In I²C mode, DDC snoop feature is enabled by default but can be disabled by a register.

8.4.1.1 I²C Mode (MODE = "F")

In I²C mode, all settings of the TDP0604 can be controlled through the registers. The TDP0604 7-bit I2C address is determined by the ADDR/EQ0 pin. All other 4-level and 2-level pins are not used in I²C mode since the functions exist in a register. The SCL/CFG0 pin will function as the I²C clock and the SDA/CFG1 pin will function as the I²C data.

The TDP0604 defaults to power down in I²C mode. Upon completion of initialization of the TDP0604, software must clear the PD_EN field to exit the power down state. The HPD_OUT pin will be asserted low while the PD_EN register is set.

The TDP0604 supports 1.2-V, 1.8-V, and 3.3-V I²C signaling levels. Selection of 1.2-V, 1.8-V, or 3.3-V is determined by the VIO pin as provided in Table 8-2.

ADDR=0x10111100 / BC or 0x10111101 / BD

8.5.2 TDP0604 I²C Address Options

For further programmability, the TDP0604 can be controlled using I²C. The SCL/CFG0 and SDA/CFG1 terminals are used for I²C clock and I²C data respectively.

Table 8-18. TDP0604 I²C Device Address Description

ADDR/EQ0 pin	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)	HEX
0	1	0	1	1	1	1	0	0/1	BC/BD
R	1	0	1	1	1	0	1	0/1	BA/BB
F	1	0	1	1	1	0	0	0/1	B8/B9
1	1	0	1	1	0	1	1	0/1	B6/B7

EQ

8.3.8 Receiver Equalizer

The equalizer is used to clean up inter-symbol interference (ISI) jitter or loss from the bandwidth-limited board traces or cables. TDP0604 supports fixed receiver equalizer by setting the EQ0 and EQ1 pins or through I²C register.

The TDP0604 has two sets of CTLE curves (3 Gbps CTLE and 6 Gbps CTLE) with each curve having 16 ac gain settings and 3 dc gain settings. The 16 ac gain settings with GLOBAL_DCG = 0x2 is detailed in Table 8-5.

The TDP0604 in pin-strap mode has two CTLE HDMI Datarate Maps: Map B and Map C. These maps are detailed in Table 8-6. The expectation is Map B or C should be used if TDP0604 is used in a source application and Map B for a sink application.

When the TDP0604 is configured for pin-strap mode, the default CTLE HDMI data rate map will be determined by the sampled state of the CTLEMAP_SEL pin as detailed in Table 8-7.

In the I²C mode, the default CTLE (3 Gbps or 6 Gbps) used for each HDMI mode can be controlled from a register.

Table 8-5. Receiver EQ Settings when GLOBAL_DCG = 0x2

EQ Setting(1)	RX EQ Level for 3Gbps CTLE (Gain at 1.5 GHz - Gain at 10 MHz)	RX EQ Level for 6Gbps CTLE (Gain at 3 GHz - Gain at 10 MHz)	EQ1 PIN	EQ0 PIN
0(2)	1.0	0.5	0	0
1	2.0	1.0	0	R
2	3.2	2.4	0	F
3	4.2	3.3	0	1
4	5.3	4.4	R	0
5	6.0	5.2	R	R
6	7.0	6.0	R	F
7	7.7	6.8	R	1
8	9.0	7.5	F	0
9	9.5	8.2	F	R
10	10.0	8.8	F	F
11	10.5	9.3	F	1
12	11.0	10.0	1	0
13	11.5	10.5	1	R
14	12.0	11.0	1	F
15	12.3	11.8	1	1

(1) In I2C mode, the receiver EQ setting is determined by D0_EQ, D1_EQ, and D2_EQ registers.
(2) When CTLEBYP_EN = 1 and dcGAIN = 0-dB, EQ settings 0 will be 0-dB due to the CTLE is bypassed.

LINEAR_EN

Table 8-4. Pin-Strap Mode LINEAR_EN Pin Function

LINEAR_EN Pin Level	Description
1	Limited Enabled
F	Linear Enabled. Recommended for HDMI sink application.
R	Reserved
0	Limited Enabled. Recommended for HDMI source application

AC_EN (Default set to AC coupled)

8.3.11 Main Link Outputs

8.3.11.1 Transmitter Bias

The TDP0604 transmitter supports both external (DC-coupled) and internal bias (AC-coupled) to a receiver. Selection between DC and AC-coupled is done through use of the AC_EN pin in pin-strap mode and TX_AC_EN register in I²C mode. The AC_EN pin informs the TDP0604 whether or not an external AC-coupling capacitor is present. When AC_EN is greater than VIH, then TDP0604 transmitters are internally biased to approximately V_{CC}. For AC-coupled application, the AC_EN pin should be connected to greater than VIH and an external AC-coupling capacitor should be placed on each of the OUT_D[2:0] pins and the OUT_CLK pin. If the AC_EN pin is connected to less than VIL, then the AC_EN pin will inform TDP0604 that AC_EN pin is DC-coupled (externally biased) to the far-end HDMI compliant receiver.

CTLEMAP_SEL

The TDP0604 in pin-strap mode has two CTLE HDMI Datarate Maps: Map B and Map C. These maps are detailed in Table 8-6. The expectation is Map B or C should be used if TDP0604 is used in a source application and Map B for a sink application.

When the TDP0604 is configured for pin-strap mode, the default CTLE HDMI data rate map will be determined by the sampled state of the CTLEMAP_SEL pin as detailed in Table 8-7.

Table 8-6. CTLE HDMI Datarate Map B and C

HDMI Mode	Map B	Map C
1.4	3 Gbps CTLE	6 Gbps CTLE
2.0	6 Gbps CTLE	6 Gbps CTLE

Table 8-7. Pin-Strap Mode CTLE HDMI Datarate Mapping

	Sampled State of CTLEMAP_SEL Pin			
	"0"	"R"	"F"	"1"
CTLE HDMI Datarate Map	Reserved	Map C	Reserved	Map B

Note

The clock lane EQ when operating in HDMI 1.4 or 2.0 will use the 3-Gbps CTLE and will be set to the zero EQ setting.

TXPRE

8.3.11.4 TX Pre-Emphasis and De-Emphasis Control

The TDP0604 provides pre-emphasis and de-emphasis on the data lanes allowing the output signal pre-conditioning to offset interconnect losses between the TDP0604 outputs and a TMDS receiver. Pre-emphasis and de-emphasis is not implemented on the clock lane. There are two methods to implement pre-emphasis, pin strapping or through I²C programming. TX pre-emphasis and de-emphasis control is only supported in limited mode.

When using pin strap mode, the TXPRE pin controls four different global pre-emphasis and de-emphasis values for all data lanes when TDP0604 is operating in HDMI 1.4 or HDMI 2.0. These pre-emphasis and de-emphasis values are described in Table 8-11.

Table 8-11. Pin-Strap TXPRE Pin Function

TXPRE Pin	HDMI 1.4 or HDMI 2.0
0	3.5 dB pre-emphasis
R	-2.5 dB de-emphasis
F	0 dB
1	6.0 dB pre-emphasis

TXSWG

8.3.11.5 TX Swing Control

The TDP0604 transmitter swing level can be adjusted in both pin strap and I²C mode. In I²C mode, TX swing settings are controlled independently for each lane (both clock and data) through registers.

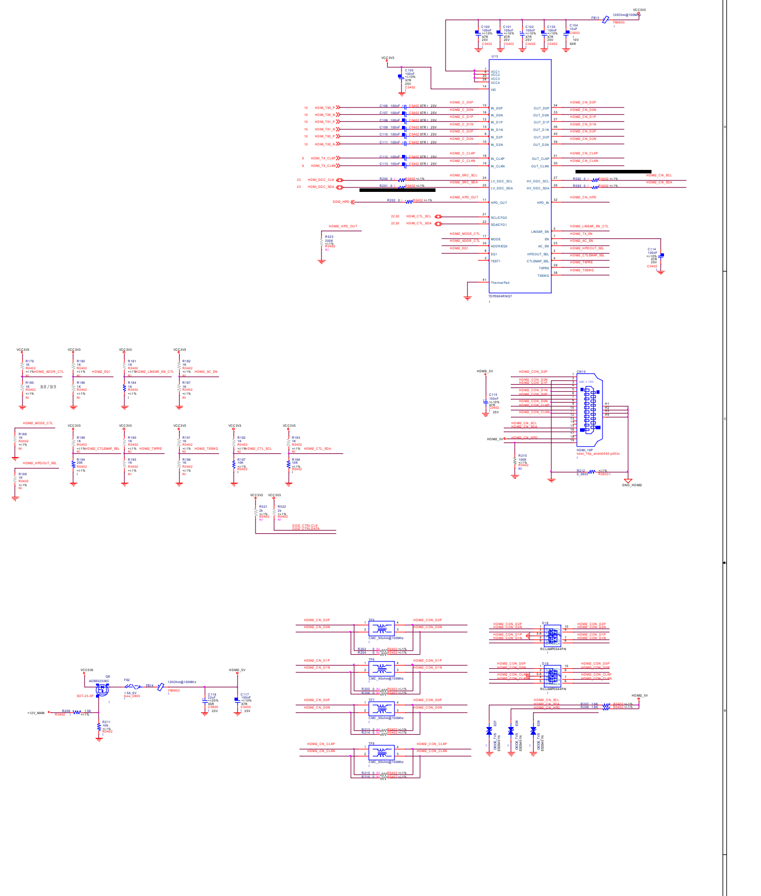
In I2C mode, the TX swing used when operating in HDMI 1.4 and HDMI 2.0 can be independently controlled through HDMI14_VOD and HDMI20_VOD registers.

In pin strap mode with limited enabled, the TXSWG pin adjusts the default 1000 mV swing as detailed in Table 8-12. In HDMI 1.4 the TXSWG pin controls the swing for both the data and clock lanes. In HDMI 2.0, the TXSWG pin controls the swing for data lanes while the clock lane will remain at default value.

In pin-strap mode with linear enabled, the linearity range is fixed at the highest level (1200 mVpp) and therefore TXSWG pin is not used. In I²C mode, the linearity range can be adjusted from a register.

Table 8-12. Pin Strap TXSWG Control

TXSWG pin	Limited Mode for HDMI 1.4	Limited Mode for HDMI 2.0	Linear Mode
0	Default (1000 mVpp)	Default (1000 mVpp)	1200 mVpp
R	Default - 5%	Default - 5%	1200 mVpp
F	Default (1000 mVpp)	Default (1000 mVpp)	1200 mVpp
1	Default (1000 mVpp)	Default + 5%	1200 mVpp



Title: **HDMI OUT**
Size: E | Document Number: **MPSOCX** | Rev: V100
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8.3 Feature Description

8.3.1 4-Level Inputs

The TDP0604 has 4-level inputs pins that control the receiver equalization gain, transmitter voltage swing, and pre-emphasis, and place TDP0604 into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings. There are internal pull-up and a pull-down resistors. These resistors are combined with the external resistor connection to achieve the desired voltage level.

Table 8-1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Tie 1-kΩ 5% to GND.
R	Tie 20-kΩ 5% to GND.
F	Float (leave pin open)
1	Tie 1-kΩ 5% to V_{CC}.

MODE (Default set to I2C Mode)

Table 8-15. MODE Pin Function

MODE Pin Level	Description
0	Pin Strap with DDC Buffer enabled
R	Pin Strap with DDC Buffer disabled
F	I2C mode
1	Reserved

8.4.1 MODE Control

The MODE pin provides four modes of operation. There are three pin-strap modes and one I^2C mode. In all three pin strap modes, DDC snooping feature is enabled. In I^2C mode, DDC snoop feature is enabled by default but can be disabled by a register.

8.4.1.1 I^2C Mode (MODE = "F")

In I^2C mode, all settings of the TDP0604 can be controlled through the registers. The TDP0604 7-bit I2C address is determined by the ADDR/EQ0 pin. All other 4-level and 2-level pins are not used in I^2C mode since the functions exist in a register. The SCL/CFG0 pin will function as the I^2C clock and the SDA/CFG1 pin will function as the I^2C data.

The TDP0604 defaults to power down in I^2C mode. Upon completion of initialization of the TDP0604, software must clear the PD_EN field to exit the power down state. The HPD_OUT pin will be asserted low while the PD_EN register is set.

The TDP0604 supports 1.2-V, 1.8-V, and 3.3-V I^2C signaling levels. Selection of 1.2-V, 1.8-V, or 3.3-V is determined by the VIO pin as provided in Table 8-2.

ADDR=0x10111100 / BC or 0x10111101 / BD

8.5.2 TDP0604 I^2C Address Options

For further programmability, the TDP0604 can be controlled using I^2C. The SCL/CFG0 and SDA/CFG1 terminals are used for I^2C clock and I^2C data respectively.

Table 8-18. TDP0604 I^2C Device Address Description

ADDR/EQ0 pin	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)	HEX
0	1	0	1	1	1	1	0	0/1	BC/BD
R	1	0	1	1	1	0	1	0/1	BA/BB
F	1	0	1	1	1	0	0	0/1	B8/B9
1	1	0	1	1	0	1	1	0/1	B6/B7

EQ

8.3.8 Receiver Equalizer

The equalizer is used to clean up inter-symbol interference (ISI) jitter or loss from the bandwidth-limited board traces or cables. TDP0604 supports fixed receiver equalizer by setting the EQ0 and EQ1 pins or through I^2C register.

The TDP0604 has two sets of CTLE curves (3 Gbps CTLE and 6 Gbps CTLE) with each curve having 16 ac gain settings and 3 dc gain settings. The 16 ac gain settings with GLOBAL_DCG = 0x2 is detailed in Table 8-5.

The TDP0604 in pin-strap mode has two CTLE HDMI Datarate Maps: Map B and Map C. These maps are detailed in Table 8-6. The expectation is Map B or C should be used if TDP0604 is used in a source application and Map B for a sink application.

When the TDP0604 is configured for pin-strap mode, the default CTLE HDMI data rate map will be determined by the sampled state of the CTLEMAP_SEL pin as detailed in Table 8-7.

In the I^2C mode, the default CTLE (3 Gbps or 6 Gbps) used for each HDMI mode can be controlled from a register.

Table 8-5. Receiver EQ Settings when GLOBAL_DCG = 0x2

EQ Setting(1)	RX EQ Level for 3Gbps CTLE (Gain at 1.5 GHz - Gain at 10 MHz)	RX EQ Level for 6Gbps CTLE (Gain at 3 GHz - Gain at 10 MHz)	EQ1 PIN	EQ0 PIN
0(2)	1.0	0.5	0	0
1	2.0	1.0	0	R
2	3.2	2.4	0	F
3	4.2	3.3	0	1
4	5.3	4.4	R	0
5	6.0	5.2	R	R
6	7.0	6.0	R	F
7	7.7	6.8	R	1
8	9.0	7.5	F	0
9	9.5	8.2	F	R
10	10.0	8.8	F	F
11	10.5	9.3	F	1
12	11.0	10.0	1	0
13	11.5	10.5	1	R
14	12.0	11.0	1	F
15	12.3	11.8	1	1

(1) In I2C mode, the receiver EQ setting is determined by D0_EQ, D1_EQ, and D2_EQ registers.
(2) When CTLEBYP_EN = 1 and dcGAIN = 0-dB, EQ settings 0 will be 0-dB due to the CTLE is bypassed.

LINEAR_EN

Table 8-4. Pin-Strap Mode LINEAR_EN Pin Function

LINEAR_EN Pin Level	Description
1	Limited Enabled
F	Linear Enabled. Recommended for HDMI sink application.
R	Reserved
0	Limited Enabled. Recommended for HDMI source application

AC_EN (Default set to AC coupled)

8.3.11 Main Link Outputs

8.3.11.1 Transmitter Bias

The TDP0604 transmitter supports both external (DC-coupled) and internal bias (AC-coupled) to a receiver. Selection between DC and AC-coupled is done through use of the AC_EN pin in pin-strap mode and TX_AC_EN register in I^2C mode. The AC_EN pin informs the TDP0604 whether or not an external AC-coupling capacitor is present. When AC_EN is greater than VIH, then TDP0604 transmitters are internally biased to approximately V_{CC}. For AC-coupled application, the AC_EN pin should be connected to greater than VIH and an external AC-coupling capacitor should be placed on each of the OUT_D[2:0] pins and the OUT_CLK pin. If the AC_EN pin is connected to less than VIL, then the AC_EN pin will inform TDP0604 that AC_EN pin is DC-coupled (externally biased) to the far-end HDMI compliant receiver.

HPDOUT_SEL

HPDOUT_SEL	2	I 2-Level (PD)	HPDOUT_SEL. Selects whether HPD_OUT pin is push/pull, or open-drain. Open-drain is not supported in pin-strap mode. Therefore this pin should be left floating or pull-down to GND.

CTLEMAP_SEL

The TDP0604 in pin-strap mode has two CTLE HDMI Datarate Maps: Map B and Map C. These maps are detailed in Table 8-6. The expectation is Map B or C should be used if TDP0604 is used in a source application and Map B for a sink application.

When the TDP0604 is configured for pin-strap mode, the default CTLE HDMI data rate map will be determined by the sampled state of the CTLEMAP_SEL pin as detailed in Table 8-7.

Table 8-6. CTLE HDMI Datarate Map B and C

HDMI Mode	Map B	Map C
1.4	3 Gbps CTLE	6 Gbps CTLE
2.0	6 Gbps CTLE	6 Gbps CTLE

Table 8-7. Pin-Strap Mode CTLE HDMI Datarate Mapping

	Sampled State of CTLEMAP_SEL Pin			
	"0"	"R"	"F"	"1"
CTLE HDMI Datarate Map	Reserved	Map C	Reserved	Map B

Note

The clock lane EQ when operating in HDMI 1.4 or 2.0 will use the 3-Gbps CTLE and will be set to the zero EQ setting.

TXPRE

8.3.11.4 TX Pre-Emphasis and De-Emphasis Control

The TDP0604 provides pre-emphasis and de-emphasis on the data lanes allowing the output signal pre-conditioning to offset interconnect losses between the TDP0604 outputs and a TMDS receiver. Pre-emphasis and de-emphasis is not implemented on the clock lane. There are two methods to implement pre-emphasis, pin strapping or through I^2C programming. TX pre-emphasis and de-emphasis control is only supported in limited mode.

When using pin strap mode, the TXPRE pin controls four different global pre-emphasis and de-emphasis values for all data lanes when TDP0604 is operating in HDMI 1.4 or HDMI 2.0. These pre-emphasis and de-emphasis values are described in Table 8-11.

Table 8-11. Pin-Strap TXPRE Pin Function

TXPRE Pin	HDMI 1.4 or HDMI 2.0
0	3.5 dB pre-emphasis
R	-2.5 dB de-emphasis
F	0 dB
1	6.0 dB pre-emphasis

TXSWG

8.3.11.5 TX Swing Control

The TDP0604 transmitter swing level can be adjusted in both pin strap and I^2C mode. In I^2C mode, TX swing settings are controlled independently for each lane (both clock and data) through registers.

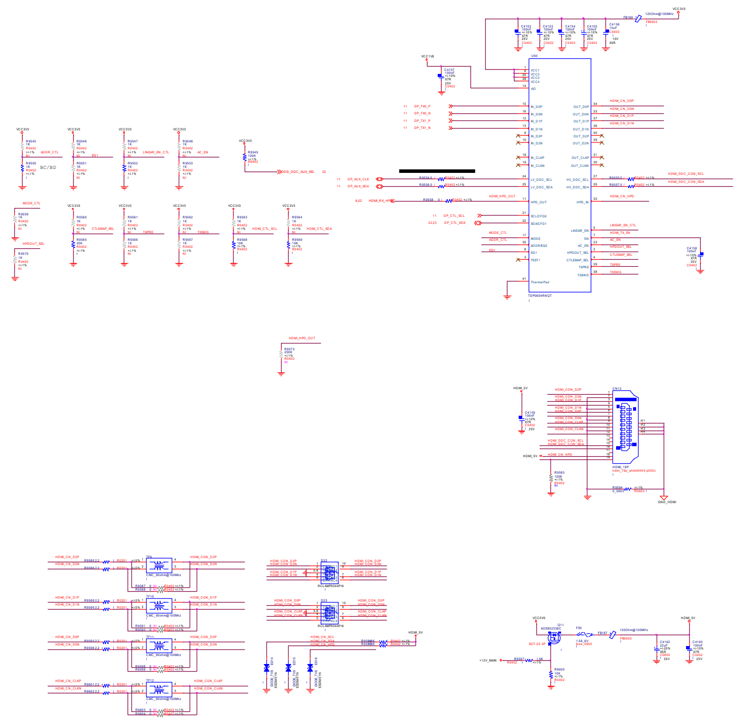
In I2C mode, the TX swing used when operating in HDMI 1.4 and HDMI 2.0 can be independently controlled through HDMI14_VOD and HDMI20_VOD registers.

In pin strap mode with limited enabled, the TXSWG pin adjusts the default 1000 mV swing as detailed in Table 8-12. In HDMI 1.4 the TXSWG pin controls the swing for both the data and clock lanes. In HDMI 2.0, the TXSWG pin controls the swing for data lanes while the clock lane will remain at default value.

In pin-strap mode with linear enabled, the linearity range is fixed at the highest level (1200 mVpp) and therefore TXSWG pin is not used. In I^2C mode, the linearity range can be adjusted from a register.

Table 8-12. Pin Strap TXSWG Control

TXSWG pin	Limited Mode for HDMI 1.4	Limited Mode for HDMI 2.0	Linear Mode
0	Default (1000 mVpp)	Default (1000 mVpp)	1200 mVpp
R	Default - 5%	Default - 5%	1200 mVpp
F	Default (1000 mVpp)	Default (1000 mVpp)	1200 mVpp
1	Default (1000 mVpp)	Default + 5%	1200 mVpp



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