

### 8.3.1.4-Level Inputs

The TDP0604 has 4-level inputs pins that control the receiver equalization gain, transmitter voltage swing, and pre-emphasis, and place TDP0604 into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4-level levels and provide a wider range of control settings. There are internal pull-up and pull-down resistors. These resistors are combined with the external resistor connection to achieve the desired voltage level.

LEVEL	SETTINGS
0	The IAD 5% to GND
R	The 20kΩ 5% to GND
F	Flow (never pin open)
1	The IAD 5% to VCC

### MODE (Default set to IC2 Mode)

Table 8-15. MODE Pin Function

MODE Pin Level	Description
0	Pin Strip with DDC Buffer enabled
R	Pin Strip with DDC Buffer disabled
F	IC2 mode
1	Reserved

### 8.4.1 MODE Control

The **MODE** pin provides four modes of operation. There are three pin-strip modes and one IC mode. In all three pin-strip modes, DDC snooping feature is enabled. In IC mode, DDC snooping feature is disabled by default but can be disabled by a register.

In IC mode, all settings of the TDP0604 can be controlled through the registers. The TDP0604 7-bit I2C address is determined by the ADDR0604 pin. All other 4-level and 2-level pins are not used in IC mode since the functions exist in a register. The SCLCFG0 pin will function as the IC clock and the SDAICFG1 pin will function as the IC data.

The TDP0604 defaults to power down in IC mode. Upon completion of initialization of the TDP0604, software must clear the PD\_EN field to exit the power-down state. The HPD\_OUT pin will be asserted low while the PD\_EN register is set.

The TDP0604 supports 1.2V, 1.8V, and 3.3V V<sub>CC</sub> signaling levels. Selection of 1.2V, 1.8V, or 3.3V is determined by the VCC pin as provided in Table 8-2.

### ADDR=0x1011100 / BC or 0x1011101 / BD

**8.4.2 TDP0604 IC Address Options**  
For further programmability, the TDP0604 can be controlled using IC. The SCLCFG0 and SDAICFG1 terminals are used for IC clock and IC data respectively.

ADDRESS pin	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Address	Pin
0	0	0	0	0	0	0	0	0	0x1011100	BC
0	0	0	0	0	0	0	1	0	0x1011101	BD
1	0	0	0	0	0	1	0	0	0x1011102	BE
1	0	0	0	0	0	1	1	0	0x1011103	BF
1	0	0	0	0	1	0	1	0	0x1011104	CG
1	0	0	0	0	1	1	1	0	0x1011105	CH
1	0	0	0	1	0	0	0	0	0x1011106	CI
1	0	0	0	1	0	0	1	0	0x1011107	CJ
1	0	0	0	1	0	1	0	0	0x1011108	CK
1	0	0	0	1	0	1	1	0	0x1011109	CL
1	0	0	0	1	1	0	0	0	0x101110A	CM
1	0	0	0	1	1	0	1	0	0x101110B	CN
1	0	0	0	1	1	1	0	0	0x101110C	CO
1	0	0	0	1	1	1	1	0	0x101110D	CP
1	0	0	1	0	0	0	0	0	0x101110E	CQ
1	0	0	1	0	0	0	1	0	0x101110F	CR
1	0	0	1	0	0	1	0	0	0x1011110	CS
1	0	0	1	0	0	1	1	0	0x1011111	CT
1	0	0	1	0	1	0	0	0	0x1011112	CU
1	0	0	1	0	1	0	1	0	0x1011113	CV
1	0	0	1	0	1	1	0	0	0x1011114	CW
1	0	0	1	0	1	1	1	0	0x1011115	CX
1	0	0	1	1	0	0	0	0	0x1011116	CY
1	0	0	1	1	0	0	1	0	0x1011117	CZ
1	0	0	1	1	0	1	0	0	0x1011118	CA
1	0	0	1	1	0	1	1	0	0x1011119	CB
1	0	0	1	1	1	0	0	0	0x101111A	CC
1	0	0	1	1	1	0	1	0	0x101111B	CD
1	0	0	1	1	1	1	0	0	0x101111C	CE
1	0	0	1	1	1	1	1	0	0x101111D	CF
1	0	1	0	0	0	0	0	0	0x101111E	CG
1	0	1	0	0	0	0	1	0	0x101111F	CH
1	0	1	0	0	0	1	0	0	0x1011120	CI
1	0	1	0	0	0	1	1	0	0x1011121	CJ
1	0	1	0	0	1	0	0	0	0x1011122	CK
1	0	1	0	0	1	0	1	0	0x1011123	CL
1	0	1	0	0	1	1	0	0	0x1011124	CM
1	0	1	0	0	1	1	1	0	0x1011125	CN
1	0	1	0	1	0	0	0	0	0x1011126	CO
1	0	1	0	1	0	0	1	0	0x1011127	CP
1	0	1	0	1	0	1	0	0	0x1011128	CQ
1	0	1	0	1	0	1	1	0	0x1011129	CR
1	0	1	0	1	1	0	0	0	0x101112A	CS
1	0	1	0	1	1	0	1	0	0x101112B	CT
1	0	1	0	1	1	1	0	0	0x101112C	CU
1	0	1	0	1	1	1	1	0	0x101112D	CV
1	0	1	1	0	0	0	0	0	0x101112E	CW
1	0	1	1	0	0	0	1	0	0x101112F	CX
1	0	1	1	0	0	1	0	0	0x1011130	CY
1	0	1	1	0	0	1	1	0	0x1011131	CZ
1	0	1	1	0	1	0	0	0	0x1011132	CA
1	0	1	1	0	1	0	1	0	0x1011133	CB
1	0	1	1	0	1	1	0	0	0x1011134	CC
1	0	1	1	0	1	1	1	0	0x1011135	CD
1	0	1	1	1	0	0	0	0	0x1011136	CE
1	0	1	1	1	0	0	1	0	0x1011137	CF
1	0	1	1	1	0	1	0	0	0x1011138	CG
1	0	1	1	1	0	1	1	0	0x1011139	CH
1	0	1	1	1	1	0	0	0	0x101113A	CI
1	0	1	1	1	1	0	1	0	0x101113B	CJ
1	0	1	1	1	1	1	0	0	0x101113C	CK
1	0	1	1	1	1	1	1	0	0x101113D	CL
1	1	0	0	0	0	0	0	0	0x101113E	CM
1	1	0	0	0	0	0	1	0	0x101113F	CN
1	1	0	0	0	0	1	0	0	0x1011140	CO
1	1	0	0	0	0	1	1	0	0x1011141	CP
1	1	0	0	0	1	0	0	0	0x1011142	CQ
1	1	0	0	0	1	0	1	0	0x1011143	CR
1	1	0	0	0	1	1	0	0	0x1011144	CS
1	1	0	0	0	1	1	1	0	0x1011145	CT
1	1	0	0	1	0	0	0	0	0x1011146	CU
1	1	0	0	1	0	0	1	0	0x1011147	CV
1	1	0	0	1	0	1	0	0	0x1011148	CW
1	1	0	0	1	0	1	1	0	0x1011149	CX
1	1	0	0	1	1	0	0	0	0x101114A	CY
1	1	0	0	1	1	0	1	0	0x101114B	CZ
1	1	0	0	1	1	1	0	0	0x101114C	CA
1	1	0	0	1	1	1	1	0	0x101114D	CB
1	1	0	1	0	0	0	0	0	0x101114E	CC
1	1	0	1	0	0	0	1	0	0x101114F	CD
1	1	0	1	0	0	1	0	0	0x1011150	CE
1	1	0	1	0	0	1	1	0	0x1011151	CF
1	1	0	1	0	1	0	0	0	0x1011152	CG
1	1	0	1	0	1	0	1	0	0x1011153	CH
1	1	0	1	0	1	1	0	0	0x1011154	CI
1	1	0	1	0	1	1	1	0	0x1011155	CJ
1	1	0	1	1	0	0	0	0	0x1011156	CK
1	1	0	1	1	0	0	1	0	0x1011157	CL
1	1	0	1	1	0	1	0	0	0x1011158	CM
1	1	0	1	1	0	1	1	0	0x1011159	CN
1	1	0	1	1	1	0	0	0	0x101115A	CO
1	1	0	1	1	1	0	1	0	0x101115B	CP
1	1	0	1	1	1	1	0	0	0x101115C	CQ
1	1	0	1	1	1	1	1	0	0x101115D	CR
1	1	1	0	0	0	0	0	0	0x101115E	CS
1	1	1	0	0	0	0	1	0	0x101115F	CT
1	1	1	0	0	0	1	0	0	0x1011160	CU
1	1	1	0	0	0	1	1	0	0x1011161	CV
1	1	1	0	0	1	0	0	0	0x1011162	CW
1	1	1	0	0	1	0	1	0	0x1011163	CX
1	1	1	0	0	1	1	0	0	0x1011164	CY
1	1	1	0	0	1	1	1	0	0x1011165	CZ
1	1	1	0	1	0	0	0	0	0x1011166	CA
1	1	1	0	1	0	0	1	0	0x1011167	CB
1	1	1	0	1	0	1	0	0	0x1011168	CC
1	1	1	0	1	0	1	1	0	0x1011169	CD
1	1	1	0	1	1	0	0	0	0x101116A	CE
1	1	1	0	1	1	0	1	0	0x101116B	CF
1	1	1	0	1	1	1	0	0	0x101116C	CG
1	1	1	0	1	1	1	1	0	0x101116D	CH
1	1	1	1	0	0	0	0	0	0x101116E	CI
1	1	1	1	0	0	0	1	0	0x101116F	CJ
1	1	1	1	0	0	1	0	0	0x1011170	CK
1	1	1	1	0	0	1	1	0	0x1011171	CL
1	1	1	1	0	1	0	0	0	0x1011172	CM
1	1	1	1	0	1	0	1	0	0x1011173	CN
1	1	1	1	0	1	1	0	0	0x1011174	CO
1	1	1	1	0	1	1	1	0	0x1011175	CP
1	1	1	1	1	0	0	0	0	0x1011176	CQ

### 8.3 Feature Description

#### 8.3.1.4 Level Inputs

The TDP0604 has 4-level inputs pins that control the receiver equalization gain, transmitter voltage swing, and pre-emphasis, and place TDP0604 into different modes of operation. These 4-level inputs utilize a resistor divider to hold set the 4 valid levels and provide a wider range of control settings. There are internal pull-up and pull-down resistors. These resistors are combined with the external resistor connection to achieve the desired voltage level.

Table 8-4. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	The 1.4D 5% to GND.
R	The 204D 5% to GND.
F	Fixed (never pin open)
1	The 1.4D 5% to V <sub>DD</sub> .

### MODE (Default set to I2C Mode)

Table 8-15. MODE Pin Function

MODE Pin Level	Description
0	Pin Strap with DDC Buffer enabled
R	Pin Strap with DDC Buffer disabled
F	Reserved
1	Reserved

#### 8.4.1 MODE Control

The MODE pin provides four modes of operation. There are three pin-strap modes and one PC mode. In all three pin strap modes, DDC snooping feature is enabled. In PC mode, DDC snooping feature is enabled by default but can be disabled by a register.

##### 8.4.1.1 PC Mode (MODE = "F")

In PC mode, all settings of the TDP0604 can be controlled through the registers. The TDP0604 744d I2C address is determined by the ADDR020 pin. All other 4-level and 2-level pins are not used in PC mode since the functions exist in a register. The SCLCFG0 pin will function as the PC clock and the SDA/CFG1 pin will function as the PC data.

The TDP0604 defaults to power down in PC mode. Upon completion of initialization of the TDP0604, software must clear the PD\_EN field to exit the power down state. The HFD\_OUT pin will be asserted low while the P0\_EN register is set.

The TDP0604 supports 1.2V, 1.8V, and 3.3V I2C signaling levels. Selection of 1.2V, 1.8V, or 3.3V is determined by the VIO pin as provided in Table 8-2.

### ADDR=0x10111100 / BC or 0x10111101 / BD

#### 8.6.2 TDP0604 PC Address Options

For further programmability, the TDP0604 can be controlled using PC. The SCLCFG0 and SDA/CFG1 terminals are used for PC clock and PC data respectively.

Table 8-18. TDP0604 PC Device Address Description

ADDRESS pin	ADDR020 pin	ADDR01 pin	ADDR00 pin	ADDR03 pin	ADDR02 pin	ADDR01 pin	ADDR00 pin	ADDR03 pin	ADDR02 pin	ADDR01 pin	ADDR00 pin
0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	4	4	4	4	4
5	5	5	5	5	5	5	5	5	5	5	5
6	6	6	6	6	6	6	6	6	6	6	6
7	7	7	7	7	7	7	7	7	7	7	7
8	8	8	8	8	8	8	8	8	8	8	8
9	9	9	9	9	9	9	9	9	9	9	9
10	10	10	10	10	10	10	10	10	10	10	10
11	11	11	11	11	11	11	11	11	11	11	11
12	12	12	12	12	12	12	12	12	12	12	12
13	13	13	13	13	13	13	13	13	13	13	13
14	14	14	14	14	14	14	14	14	14	14	14
15	15	15	15	15	15	15	15	15	15	15	15
16	16	16	16	16	16	16	16	16	16	16	16
17	17	17	17	17	17	17	17	17	17	17	17
18	18	18	18	18	18	18	18	18	18	18	18
19	19	19	19	19	19	19	19	19	19	19	19
20	20	20	20	20	20	20	20	20	20	20	20
21	21	21	21	21	21	21	21	21	21	21	21
22	22	22	22	22	22	22	22	22	22	22	22
23	23	23	23	23	23	23	23	23	23	23	23
24	24	24	24	24	24	24	24	24	24	24	24
25	25	25	25	25	25	25	25	25	25	25	25
26	26	26	26	26	26	26	26	26	26	26	26
27	27	27	27	27	27	27	27	27	27	27	27
28	28	28	28	28	28	28	28	28	28	28	28
29	29	29	29	29	29	29	29	29	29	29	29
30	30	30	30	30	30	30	30	30	30	30	30
31	31	31	31	31	31	31	31	31	31	31	31

### EQ

#### 8.2.6 Receiver Equalizer

The equalizer is used to clean up inter-symbol interference (ISI) after or loss from the bandwidth-limited board traces or cables. TDP0604 supports full receiver equalizer by setting the EQ0 and EQ1 pins or through PC register.

The TDP0604 has two sets of CTLE control (3 Gbps CTLE and 6 Gbps CTLE) with each one having 16 bit gain settings and 3 bit gain straps. The 16 bit gain settings with GLOBAL\_DCC = 0D is detailed in Table 8-5. The TDP0604 pin-strap mode has two CTLE (3 Gbps and 6 Gbps) data rate maps. Map B and Map C. These maps are detailed in Table 8-6. The expectation is Map B or C should be used if TDP0604 is used in a source application and Map B for a sink application.

When the TDP0604 is configured for pin-strap mode, the default CTLE HDMI data rate map will be determined by the sampled state of the CTLEMAP\_SEL pin as detailed in Table 8-7.

In the PC mode, the default CTLE (3 Gbps or 6 Gbps) used for each HDMI mode can be controlled from a register.

Table 8-5. Receiver EQ Settings when GLOBAL\_DCC = 0D

EQ Setting	ADDR020 pin	ADDR01 pin	ADDR00 pin	EQ0 pin	EQ1 pin
0	0	0	0	0	0
1	1	1	1	1	1
2	2	2	2	2	2
3	3	3	3	3	3
4	4	4	4	4	4
5	5	5	5	5	5
6	6	6	6	6	6
7	7	7	7	7	7
8	8	8	8	8	8
9	9	9	9	9	9
10	10	10	10	10	10
11	11	11	11	11	11
12	12	12	12	12	12
13	13	13	13	13	13
14	14	14	14	14	14
15	15	15	15	15	15
16	16	16	16	16	16
17	17	17	17	17	17
18	18	18	18	18	18
19	19	19	19	19	19
20	20	20	20	20	20
21	21	21	21	21	21
22	22	22	22	22	22
23	23	23	23	23	23
24	24	24	24	24	24
25	25	25	25	25	25
26	26	26	26	26	26
27	27	27	27	27	27
28	28	28	28	28	28
29	29	29	29	29	29
30	30	30	30	30	30
31	31	31	31	31	31

### LINEAR\_EN

Table 8-4. Pin-Strap Mode LINEAR\_EN Pin Function

LINEAR_EN Pin Level	Description
0	Limited Enabled
R	Limited Enabled
F	Recommended for HDMI sink application.
1	Limited Enabled
2	Recommended for HDMI sink application.

### AC\_EN (Default set to AC coupled)

#### 8.3.1.7 Transmitter Bias

The TDP0604 transmitter supports both external (DC-coupled) and internal bias (AC-coupled) to a receiver. Selection between DC and AC-coupled is done through one of the AC\_EN pin or through mode and V<sub>DD</sub>AC\_EN pin. When AC\_EN is greater than V<sub>DD</sub>, then TDP0604 transmitters are internally biased to approximately V<sub>DD</sub>. The AC-coupled application, the AC\_EN pin should be connected to ground through a 100 pF or an external AC-coupling capacitor should be placed on each of the OUT<sub>0</sub> (EQ0) pins and the OUT<sub>1</sub> (EQ1) pin. If the AC\_EN pin is connected to bias than V<sub>DD</sub>, then the AC\_EN pin will assert TDP0604 that AC\_EN pin is DC-coupled (externally biased) to the far-end HDMI compliant receiver.

### CTLEMAP\_SEL

The TDP0604 in pin-strap mode has two CTLE HDMI Datarate Maps: Map B and Map C. These maps are detailed in Table 8-6. The expectation is Map B or C should be used in a source application and Map B for a sink application.

When the TDP0604 is configured for pin-strap mode, the default CTLE HDMI data rate map will be determined by the sampled state of the CTLEMAP\_SEL pin as detailed in Table 8-7.

Table 8-6. CTLE HDMI Datarate Map B and C

HDMI Mode	Map B	Map C
1.4	3 Gbps CTLE	6 Gbps CTLE
2.0	6 Gbps CTLE	6 Gbps CTLE

Table 8-7. Pin-Strap Mode CTLE HDMI Datarate Mapping

CTLE HDMI Datarate Map	Sampled State of CTLEMAP_SEL Pin			
	"0"	"R"	"F"	"1"
Reserved	Reserved	Map B	Reserved	Map B

Note  
The clock lane EQ when operating in HDMI 1.4 or 2.0 will use the 3-Gbps CTLE and will be set to the zero EQ setting.

### TXPRE

#### 8.3.11.4 TX Pre-Emphasis and De-Emphasis Control

The TDP0604 provides pre-emphasis and de-emphasis on the data lanes allowing the output signal pre-conditioning to offset interconnect losses between the TDP0604 outputs and a TMSD receiver. Pre-emphasis and de-emphasis is not implemented on the clock lanes. There are two methods to implement pre-emphasis, pin strapping or through PC programming. TX pre-emphasis and de-emphasis control is only supported in limited mode.

When using pin strap mode, the TXPRE pin controls four different global pre-emphasis and de-emphasis values for all data lanes when TDP0604 is operating in HDMI 1.4 or HDMI 2.0. These pre-emphasis and de-emphasis values are described in Table 8-11.

Table 8-11. Pin-Strap TXPRE Pin Function

TXPRE Pin	HDMI 1.4/HDMI 2.0
0	3.0 dB pre-emphasis
R	2.5 dB de-emphasis
F	0 dB
1	6.0 dB pre-emphasis

### TXSWG

#### 8.3.11.5 TX Swing Control

The TDP0604 transmitter swing level can be adjusted in both pin strap and PC mode. In PC mode, TX swing settings are controlled independently for each lane (both clock and data) through registers.

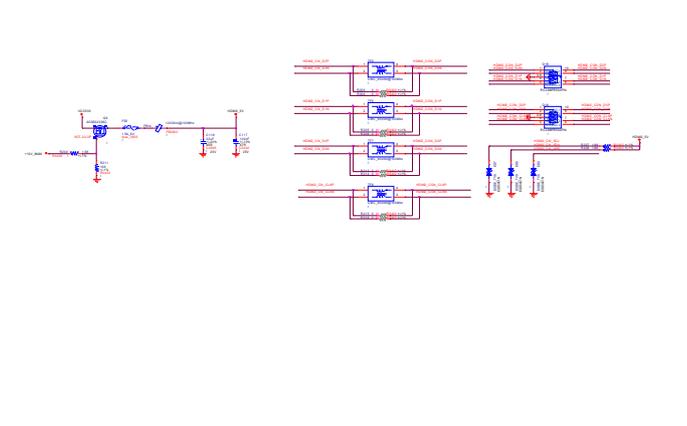
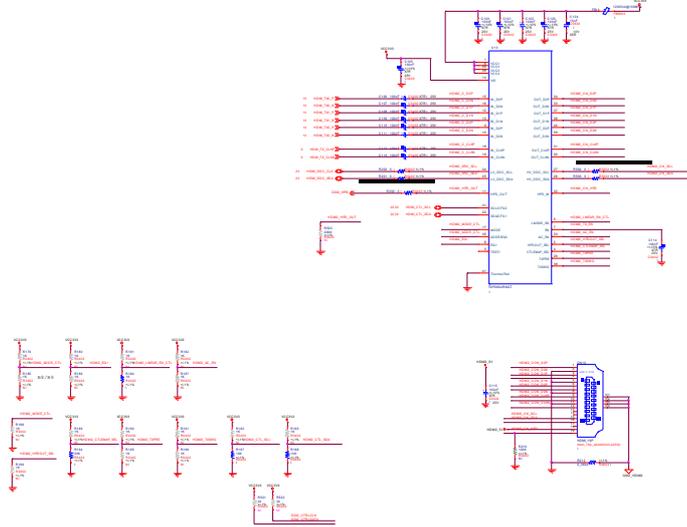
In I2C mode, the TX swing used when operating in HDMI 1.4 and HDMI 2.0 can be independently controlled through HDMI14\_VOD and HDMI20\_VOD registers.

In HDMI 1.4 the TXSWG pin controls the swing for both the data and clock lanes. In HDMI 2.0, the TXSWG pin controls the swing for data lanes while the clock lane will remain at default value.

In pin-strap mode with linear enabled, the linearity range is fixed at the highest level (1200 mV) and therefore TXSWG pin is not used. In PC mode, the linearity range can be adjusted from a register.

Table 8-12. Pin Strap TXSWG Control

TXSWG pin	Linearity Range for HDMI 1.4	Linearity Range for HDMI 2.0	Linear Mode
0	Default (1200 mVpp)	Default (1200 mVpp)	1200 mVpp
R	Default (3N)	Default (3N)	1200 mVpp
F	Default (1200 mVpp)	Default (1200 mVpp)	1200 mVpp
1	Default (1200 mVpp)	Default (3N)	1200 mVpp



### 8.3.1.4 Feature Description

The TDP0604 has 4-level inputs pins that control the receiver equalization gain, transmitter voltage swing, and pre-emphasis, and place TDP0604 into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4-level inputs and provide a wider range of control settings. There are internal pull-up and pull-down resistors. These resistors are combined with the external resistor to achieve the desired voltage level.

Table 8-1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	1k 140Ω to GND
0	2k 140Ω to GND
F	Float (leave pin open)
1	1k 140Ω to VCC

### MODE (Default set to I2C Mode)

Table 8-15. MODE Pin Function

MODE Pin Level	Description
0	Pin Strap with DDC Buffer enabled
0	Pin Strap with DDC Buffer disabled
F	I2C mode
1	Reserved

#### 8.4.1 MODE Control

The **MODE** pin provides four modes of operation. There are three pin-strap modes and one PC mode. In all three pin-strap modes, DDC snooping feature is enabled. In PC mode, DDC snoop feature is enabled by default but can be disabled by a register.

#### 8.4.1.1 PC Mode (MODE = "F")

In PC mode, all settings of the TDP0604 can be controlled through the registers. The TDP0604 7-bit I2C address is determined by the ADDR[0:2] pins. All other 4-level and 3-level pins are not used in PC mode since the functions exist in a register. The SCLCFG0 pin will function as the PC clock and the SDACFG1 pin will function as the PC data.

The TDP0604 defaults to power down in PC mode. Upon completion of initialization of the TDP0604, software must clear the PD\_EN field to exit the power down state. The HPD\_OUT pin will be asserted low while the PD\_EN register is set.

The TDP0604 supports 1.2V, 1.8V, and 3.3V I<sup>2</sup>C signaling levels. Selection of 1.2V, 1.8V, or 3.3V is determined by the VIO pin as provided in Table 8-2.

### ADDR=0x10111100 / BC or 0x10111101 / BD

#### 8.5.2 TDP0604 PC Address Options

For further programmability, the TDP0604 can be controlled using PC. The SCLCFG0 and SDACFG1 terminals are used for PC clock and PC data respectively.

Table 8-16. TDP0604 PC Device Address Description

ADDRESS	ADDR[2]	ADDR[1]	ADDR[0]	PC Mode	PC Mode	PC Mode	PC Mode
0	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
2	0	1	0	0	1	0	0
3	0	1	1	0	1	1	0
4	1	0	0	1	0	0	0
5	1	0	1	1	0	1	0
6	1	1	0	1	1	0	0
7	1	1	1	1	1	1	0

### EQ

#### 8.3.3 Receiver Equalizer

The equalizer is used to clean up inter-symbol interference (ISI) prior to bias from the bandwidth-limited board traces or cables. TDP0604 supports fixed receiver equalizer by setting the EQ0 and EQ1 pins or through PC register.

The TDP0604 has two sets of CTLE curves (3-Gbps CTLE and 6-Gbps CTLE) with each curve having 16 ac gain settings and 3 dc gain settings. The 16 ac gain settings with GLOBAL\_DCC = 0 is detailed in Table 8-5.

The TDP0604 in pin-strap mode has two CTLE HDMI Data Rate Maps: Map B and Map C. These maps are detailed in Table 8-6. The operation in Map B or C should be used if TDP0604 is used in a source application and Map B for a sink application.

When the TDP0604 is configured for pin-strap mode, the default CTLE HDMI data rate map will be determined by the sampled state of the CTLEMAP\_SEL pin as detailed in Table 8-7.

In the PC mode, the default CTLE (3-Gbps or 6-Gbps) used for each HDMI mode can be controlled from a register.

Table 8-5. Receiver EQ Settings when GLOBAL\_DCC = 0x0

| EQ Setting |
|------------|------------|------------|------------|------------|------------|
| 0          | 1          | 2          | 3          | 4          | 5          |
| 6          | 7          | 8          | 9          | 10         | 11         |
| 12         | 13         | 14         | 15         | 16         | 17         |
| 18         | 19         | 20         | 21         | 22         | 23         |
| 24         | 25         | 26         | 27         | 28         | 29         |
| 30         | 31         | 32         | 33         | 34         | 35         |
| 36         | 37         | 38         | 39         | 40         | 41         |
| 42         | 43         | 44         | 45         | 46         | 47         |
| 48         | 49         | 50         | 51         | 52         | 53         |
| 54         | 55         | 56         | 57         | 58         | 59         |
| 60         | 61         | 62         | 63         | 64         | 65         |
| 66         | 67         | 68         | 69         | 70         | 71         |
| 72         | 73         | 74         | 75         | 76         | 77         |
| 78         | 79         | 80         | 81         | 82         | 83         |
| 84         | 85         | 86         | 87         | 88         | 89         |
| 90         | 91         | 92         | 93         | 94         | 95         |
| 96         | 97         | 98         | 99         | 100        | 101        |
| 102        | 103        | 104        | 105        | 106        | 107        |
| 108        | 109        | 110        | 111        | 112        | 113        |
| 114        | 115        | 116        | 117        | 118        | 119        |
| 120        | 121        | 122        | 123        | 124        | 125        |
| 126        | 127        | 128        | 129        | 130        | 131        |
| 132        | 133        | 134        | 135        | 136        | 137        |
| 138        | 139        | 140        | 141        | 142        | 143        |
| 144        | 145        | 146        | 147        | 148        | 149        |
| 150        | 151        | 152        | 153        | 154        | 155        |
| 156        | 157        | 158        | 159        | 160        | 161        |
| 162        | 163        | 164        | 165        | 166        | 167        |
| 168        | 169        | 170        | 171        | 172        | 173        |
| 174        | 175        | 176        | 177        | 178        | 179        |
| 180        | 181        | 182        | 183        | 184        | 185        |
| 186        | 187        | 188        | 189        | 190        | 191        |
| 192        | 193        | 194        | 195        | 196        | 197        |
| 198        | 199        | 200        | 201        | 202        | 203        |
| 204        | 205        | 206        | 207        | 208        | 209        |
| 210        | 211        | 212        | 213        | 214        | 215        |
| 216        | 217        | 218        | 219        | 220        | 221        |
| 222        | 223        | 224        | 225        | 226        | 227        |
| 228        | 229        | 230        | 231        | 232        | 233        |
| 234        | 235        | 236        | 237        | 238        | 239        |
| 240        | 241        | 242        | 243        | 244        | 245        |
| 246        | 247        | 248        | 249        | 250        | 251        |
| 252        | 253        | 254        | 255        | 256        | 257        |
| 258        | 259        | 260        | 261        | 262        | 263        |
| 264        | 265        | 266        | 267        | 268        | 269        |
| 270        | 271        | 272        | 273        | 274        | 275        |
| 276        | 277        | 278        | 279        | 280        | 281        |
| 282        | 283        | 284        | 285        | 286        | 287        |
| 288        | 289        | 290        | 291        | 292        | 293        |
| 294        | 295        | 296        | 297        | 298        | 299        |
| 300        | 301        | 302        | 303        | 304        | 305        |
| 306        | 307        | 308        | 309        | 310        | 311        |
| 312        | 313        | 314        | 315        | 316        | 317        |
| 318        | 319        | 320        | 321        | 322        | 323        |
| 324        | 325        | 326        | 327        | 328        | 329        |
| 330        | 331        | 332        | 333        | 334        | 335        |
| 336        | 337        | 338        | 339        | 340        | 341        |
| 342        | 343        | 344        | 345        | 346        | 347        |
| 348        | 349        | 350        | 351        | 352        | 353        |
| 354        | 355        | 356        | 357        | 358        | 359        |
| 360        | 361        | 362        | 363        | 364        | 365        |
| 366        | 367        | 368        | 369        | 370        | 371        |
| 372        | 373        | 374        | 375        | 376        | 377        |
| 378        | 379        | 380        | 381        | 382        | 383        |
| 384        | 385        | 386        | 387        | 388        | 389        |
| 390        | 391        | 392        | 393        | 394        | 395        |
| 396        | 397        | 398        | 399        | 400        | 401        |
| 402        | 403        | 404        | 405        | 406        | 407        |
| 408        | 409        | 410        | 411        | 412        | 413        |
| 414        | 415        | 416        | 417        | 418        | 419        |
| 420        | 421        | 422        | 423        | 424        | 425        |
| 426        | 427        | 428        | 429        | 430        | 431        |
| 432        | 433        | 434        | 435        | 436        | 437        |
| 438        | 439        | 440        | 441        | 442        | 443        |
| 444        | 445        | 446        | 447        | 448        | 449        |
| 450        | 451        | 452        | 453        | 454        | 455        |
| 456        | 457        | 458        | 459        | 460        | 461        |
| 462        | 463        | 464        | 465        | 466        | 467        |
| 468        | 469        | 470        | 471        | 472        | 473        |
| 474        | 475        | 476        | 477        | 478        | 479        |
| 480        | 481        | 482        | 483        | 484        | 485        |
| 486        | 487        | 488        | 489        | 490        | 491        |
| 492        | 493        | 494        | 495        | 496        | 497        |
| 498        | 499        | 500        | 501        | 502        | 503        |
| 504        | 505        | 506        | 507        | 508        | 509        |
| 510        | 511        | 512        | 513        | 514        | 515        |
| 516        | 517        | 518        | 519        | 520        | 521        |
| 522        | 523        | 524        | 525        | 526        | 527        |
| 528        | 529        | 530        | 531        | 532        | 533        |
| 534        | 535        | 536        | 537        | 538        | 539        |
| 540        | 541        | 542        | 543        | 544        | 545        |
| 546        | 547        | 548        | 549        | 550        | 551        |
| 552        | 553        | 554        | 555        | 556        | 557        |
| 558        | 559        | 560        | 561        | 562        | 563        |
| 564        | 565        | 566        | 567        | 568        | 569        |
| 570        | 571        | 572        | 573        | 574        | 575        |
| 576        | 577        | 578        | 579        | 580        | 581        |
| 582        | 583        | 584        | 585        | 586        | 587        |
| 588        | 589        | 590        | 591        | 592        | 593        |
| 594        | 595        | 596        | 597        | 598        | 599        |
| 600        | 601        | 602        | 603        | 604        | 605        |
| 606        | 607        | 608        | 609        | 610        | 611        |
| 612        | 613        | 614        | 615        | 616        | 617        |
| 618        | 619        | 620        | 621        | 622        | 623        |
| 624        | 625        | 626        | 627        | 628        | 629        |
| 630        | 631        | 632        | 633        | 634        | 635        |
| 636        | 637        | 638        | 639        | 640        | 641        |
| 642        | 643        | 644        | 645        | 646        | 647        |
| 648        | 649        | 650        | 651        | 652        | 653        |
| 654        | 655        | 656        | 657        | 658        | 659        |
| 660        | 661        | 662        | 663        | 664        | 665        |
| 666        | 667        | 668        | 669        | 670        | 671        |
| 672        | 673        | 674        | 675        | 676        | 677        |
| 678        | 679        | 680        | 681        | 682        | 683        |
| 684        | 685        | 686        | 687        | 688        | 689        |
| 690        | 691        | 692        | 693        | 694        | 695        |
| 696        | 697        | 698        | 699        | 700        | 701        |
| 702        | 703        | 704        | 705        | 706        | 707        |
| 708        | 709        | 710        | 711        | 712        | 713        |
| 714        | 715        | 716        | 717        | 718        | 719        |
| 720        | 721        | 722        | 723        | 724        | 725        |
| 726        | 727        | 728        | 729        | 730        | 731        |
| 732        | 733        | 734        | 735        | 736        | 737        |
| 738        | 739        | 740        | 741        | 742        | 743        |
| 744        | 745        | 746        | 747        | 748        | 749        |
| 750        | 751        | 752        | 753        | 754        | 755        |
| 756        | 757        | 758        | 759        | 760        | 761        |
| 762        | 763        | 764        | 765        | 766        | 767        |
| 768        | 769        | 770        | 771        | 772        | 773        |
| 774        | 775        | 776        | 777        | 778        | 779        |
| 780        | 781        | 782        | 783        | 784        | 785        |
| 786        | 787        | 788        | 789        | 790        | 791        |
| 792        | 793        | 794        | 795        | 796        | 797        |
| 798        | 799        | 800        | 801        | 802        | 803        |
| 804        | 805        | 806        | 807        | 808        | 809        |
| 810        | 811        | 812        | 813        | 814        | 815        |
| 816        | 817        | 818        | 819        | 820        | 821        |
| 822        | 823        | 824        | 825        | 826        | 827        |
| 828        | 829        | 830        | 831        | 832        | 833        |
| 834        | 835        | 836        | 837        | 838        | 839        |
| 840        | 841        | 842        | 843        | 844        | 845        |
| 846        | 847        | 848        | 849        | 850        | 851        |
| 852        | 853        | 854        | 855        | 856        | 857        |
| 858        | 859        | 860        | 861        | 862        | 863        |
| 864        | 865        | 866        | 867        | 868        | 869        |
| 870        | 871        | 872        | 873        | 874        | 875        |
| 876        | 877        | 878        | 879        | 880        | 881        |
| 882        | 883        | 884        | 885        | 886        | 887        |
| 888        | 889        | 890        | 891        | 892        | 893        |
| 894        | 895        | 896        | 897        | 898        | 899        |
| 900        | 901        | 902        | 903        | 904        | 905        |
| 906        | 907        | 908        | 909        | 910        | 911        |
| 912        | 913        | 914        | 915        | 916        | 917        |
| 918        | 919        | 920        | 921        | 922        | 923        |
| 924        | 925        | 926        | 927        | 928        | 929        |
| 930        | 931        | 932        | 933        | 934        | 935        |
| 936        | 937        | 938        | 939        | 940        | 941        |
| 942        | 943        | 944        | 945        | 946        | 947        |
| 948        | 949        | 950        | 951        | 952        | 953        |
| 954        | 955        | 956        | 957        |            |            |