

# Test Report

## Pass

Test Configuration Details	
<b>Application</b>	
Name	D9020DPHC MIPI D-PHY Test
Version	4.0.0.0
<b>Device Description</b>	
High Speed Data Rate(Mbps)	167.4
CTS Version	v1.2
ZID	100 ohm
Cload	50pF
Fixture Setup	Auto Load Switching
<b>Test Session Details</b>	
Infiniium SW Version	06.74.00701
Infiniium Model Number	DSOX92504A
Infiniium Serial Number	MY53450102
Debug Mode Used	No
Compliance Limits	MIPI D-PHY Test Limit v1.2 (official)
Probe (Channel 1)	Model: 1169A Serial: US55013282 Head: N5381A/B Atten: Calibrated (3 APR 2024 09:11:16), Using Cal Atten (3.2114E+00) Skew: Calibrated (3 APR 2024 09:11:46), Using Cal Skew
Probe (Channel 2)	Model: 1169A Serial: US55013283 Head: N5381A/B Atten: Calibrated (3 APR 2024 09:13:19), Using Cal Atten (3.3176E+00) Skew: Calibrated (3 APR 2024 09:13:37), Using Cal Skew
Probe (Channel 3)	Model: 1169A Serial: US55013281 Head: N5381A/B Atten: Calibrated (3 APR 2024 09:16:01), Using Cal Atten (3.2185E+00) Skew: Calibrated (3 APR 2024 09:18:15), Using Cal Skew
Probe (Channel 4)	Model: 1169A Serial: US55013275 Head: N5381A/B Atten: Calibrated (3 APR 2024 09:19:43), Using Cal Atten (3.2109E+00) Skew: Calibrated (3 APR 2024 09:20:12), Using Cal Skew
Last Test Date	2024-04-08 19:38:06 UTC +08:00

## Summary of Results

Test Statistics		Margin Thresholds	
Failed	0	Warning	< 5 %
Passed	25	Critical	< 0 %
Total	25		

Pass	# Failed	# Trials	Test Name (click to jump)	Actual Value	Margin	Pass Limits
✓	0	1	<a href="#">1.3.10 HS Data TX Common-Level Variations Above 450MHz (VCMTX(HF))</a>	6.37 mV	57.5 %	VALUE < 15.00 mV
✓	0	1	<a href="#">1.3.9 HS Data TX Common-Level Variations Between 50-450MHz (VCMTX(LF))</a>	8.42 mV	66.3 %	VALUE < 25.00 mV
✓	0	1	<a href="#">1.4.9 HS Clock TX Common-Level Variations Between 50-450MHz (VCMTX(LF))</a>	7.30 mV	70.8 %	VALUE < 25.00 mV
✓	0	1	<a href="#">1.4.7 HS Clock TX Static Common Mode Voltage(Vcmtx)</a>	213.22 mV	36.8 %	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	<a href="#">1.4.8 HS Clock TX Vcmtx Mismatch</a>	1.72 mV	65.6 %	VALUE < 5.00 mV
✓	0	1	<a href="#">1.4.10 HS Clock TX Common-Level Variations Above 450MHz (VCMTX(HF))</a>	3.07 mV	79.5 %	VALUE < 15.00 mV
✓	0	1	<a href="#">1.4.4 HS Clock TX Differential Voltage(VOD0 Pulse)</a>	-235.64 mV	26.4 %	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	<a href="#">1.4.4 HS Clock TX Differential Voltage(VOD1 Pulse)</a>	236.05 mV	26.1 %	140.00 mV <= VALUE <= 270.00 mV
✓	0	1	<a href="#">1.4.5 HS Clock TX Differential Voltage Mismatch (Pulse)</a>	400 µV	97.1 %	VALUE < 14.00 mV
✓	0	1	<a href="#">1.4.6 HS Clock TX Single Ended Output High Voltage(VOHHS Pulse)</a>	329.04 mV	8.6 %	VALUE <= 360.00 mV
✓	0	1	<a href="#">1.4.17 HS Clock Instantaneous (UIinst)(Min)</a>	5.897 ns	590E+01 %	VALUE >= UIinst_Min_Limit s
✓	0	1	<a href="#">1.4.18 Clock Lane HS Clock Delta UI (UI variation)</a>	-1.36 %	43.2 %	UIVariant_Limit_Min % <= VALUE <= UIVariant_Limit_Max %
✓	0	1	<a href="#">1.5.3 HS Clock Rising Edge Alignment to First Payload Bit</a>	Pass	100.0 %	VALUE <= 500.000000000 m
✓	0	1	<a href="#">1.5.4 Data-to-Clock Skew (TSKEW(TX))(Max,Min)</a>	19 mUIinst	43.7 %	MinMaxTSkewTest_LimitMin UIinst <= VALUE <= MinMaxTSkewTest_LimitMax UIinst
✓	0	1	<a href="#">1.5.4 Data-to-Clock Skew (TSKEW(TX))(Mean)</a>	12 mUIinst	46.0 %	MeanTSkewTest_LimitMin UIinst <= VALUE <= MeanTSkewTest_LimitMax UIinst
✓	0	1	<a href="#">HS Data Eye Height (Informative)</a>	371 mVpp	165.0 %	VALUE >= Eye_Height_limit_Vpp
✓	0	1	<a href="#">HS Data Eye Width (Informative)</a>	992 mUI	98.4 %	VALUE >= Eye_Width_limit UI
✓	0	1	<a href="#">1.3.7 HS Data TX Static Common Mode Voltage(Vcmtx)</a>	208.72 mV	41.3 %	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	<a href="#">1.3.8 HS Data TX Vcmtx Mismatch</a>	2.30 mV	54.0 %	VALUE < 5.00 mV

✓	0	1	1.3.4 HS Data TX Differential Voltage(VOD0 Pulse)	-232.26 mV	29.0 %	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.3.13 HS Exit: DATA TX THS-TRAIL	140.27 ns	67.2 %	VALUE >= TXTHSTrail_LimitMin s
✓	0	1	1.3.14 HS Exit: DATA TX TREOT	8.82 ns	74.8 %	VALUE <= 35.00 ns
✓	0	1	1.4.17 HS Clock Instantaneous (UIinst)(Max)	6.044 ns	51.6 %	VALUE < 12.500 ns
✓	0	1	1.3.15 HS Exit: DATA TX TEOT	149.08 ns	15.7 %	VALUE <= TXTEOT_LimitMax s
✓	0	1	1.3.16 HS Exit: DATA TX THS-EXIT	253.27 ns	153.3 %	VALUE >= 100.00 ns

## Report Detail

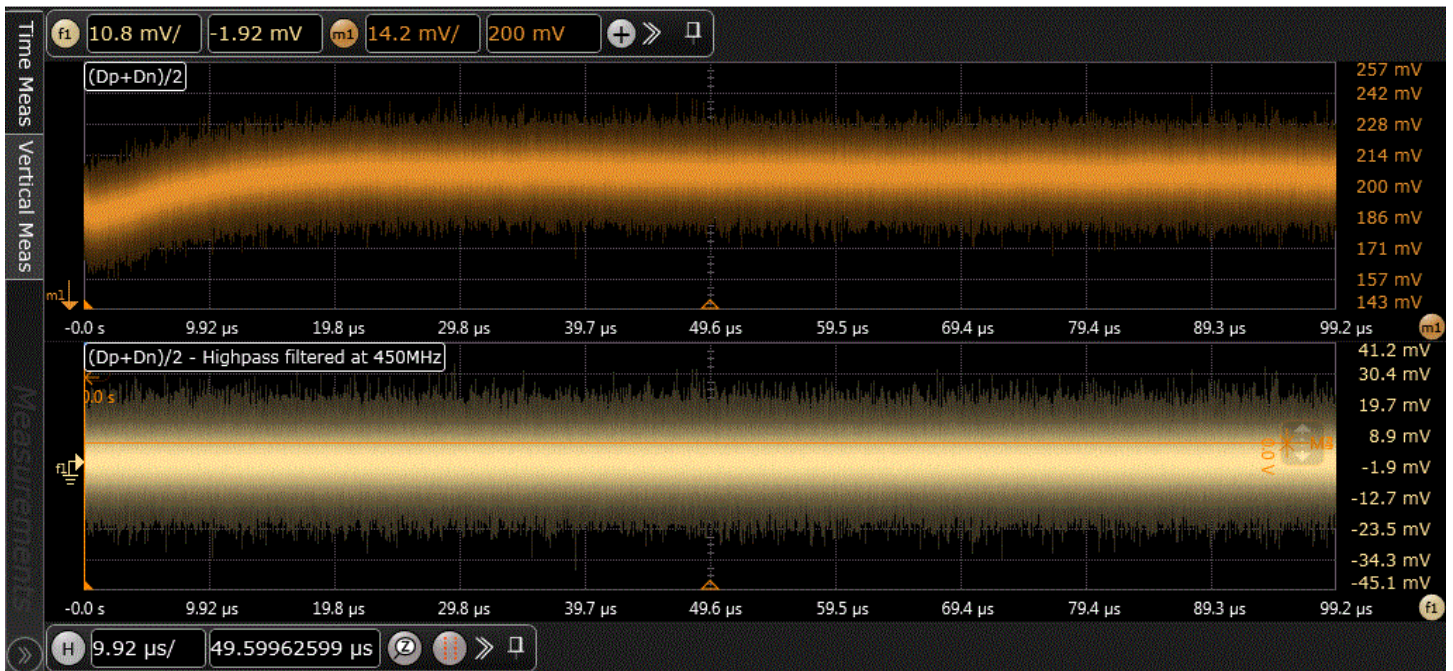
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✓	<b>1.3.10 HS Data TX Common-Level Variations Above 450MHz (VCMTX(HF))</b>	D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.3.10)
Common-level variations above 450MHz. Actual Value Measurement Name: 818_Vcmtx(HF) Pass Limits: VALUE < 15.00 mV		

Actual Value	Margin	Common Level Variations(>450MHz)	ZID	DataLane	Number of HS Burst
6.37 mV	57.5 %	(See image)	100 ohm	Lane0	1

Common Level Variations(>450MHz)

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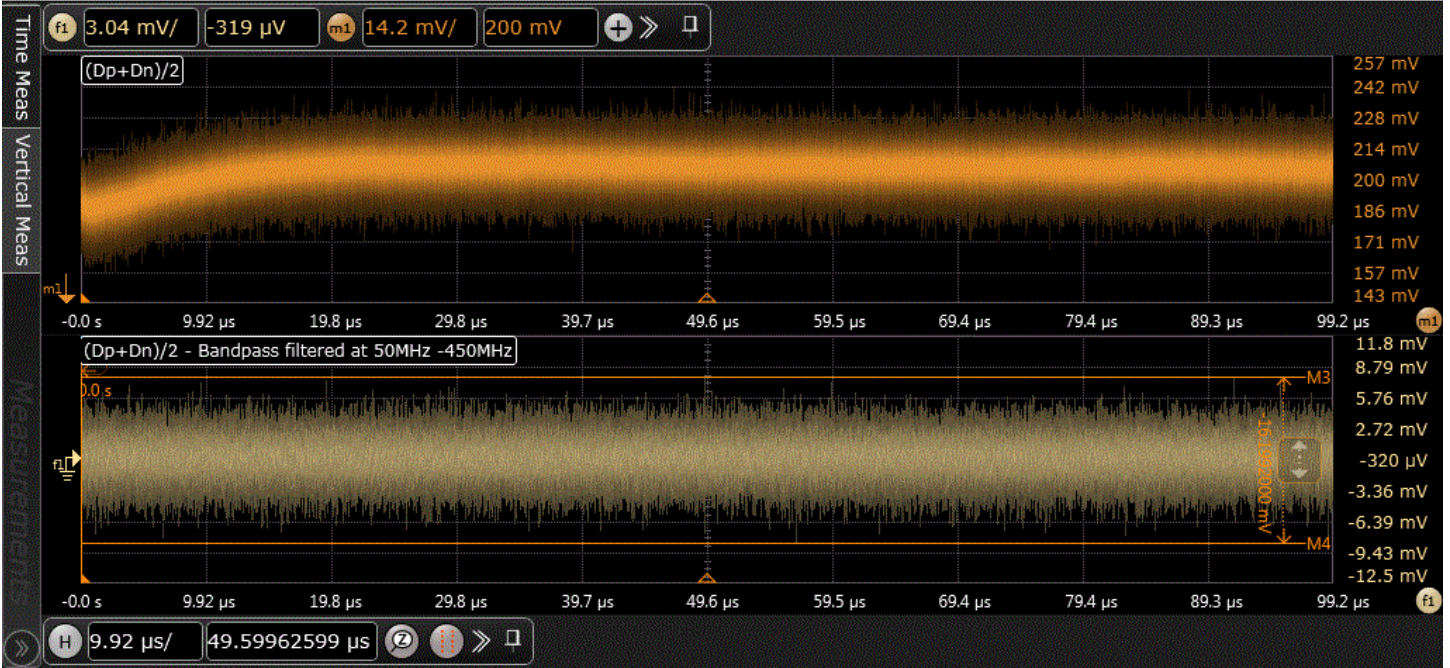


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✓	<b>1.3.9 HS Data TX Common-Level Variations Between 50-450MHz (VCMTX(LF))</b>	D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.3.9)
Common-level variation between 50-450MHz. Actual Value Measurement Name: 819_Vcmtx(LF) Pass Limits: VALUE < 25.00 mV		

Actual Value	Margin	Common Level Variations(50-450MHz)	ZID	DataLane	Number of HS Burst
8.42 mV	66.3 %	(See image)	100 ohm	Lane0	1

Common Level Variations(50-450MHz)



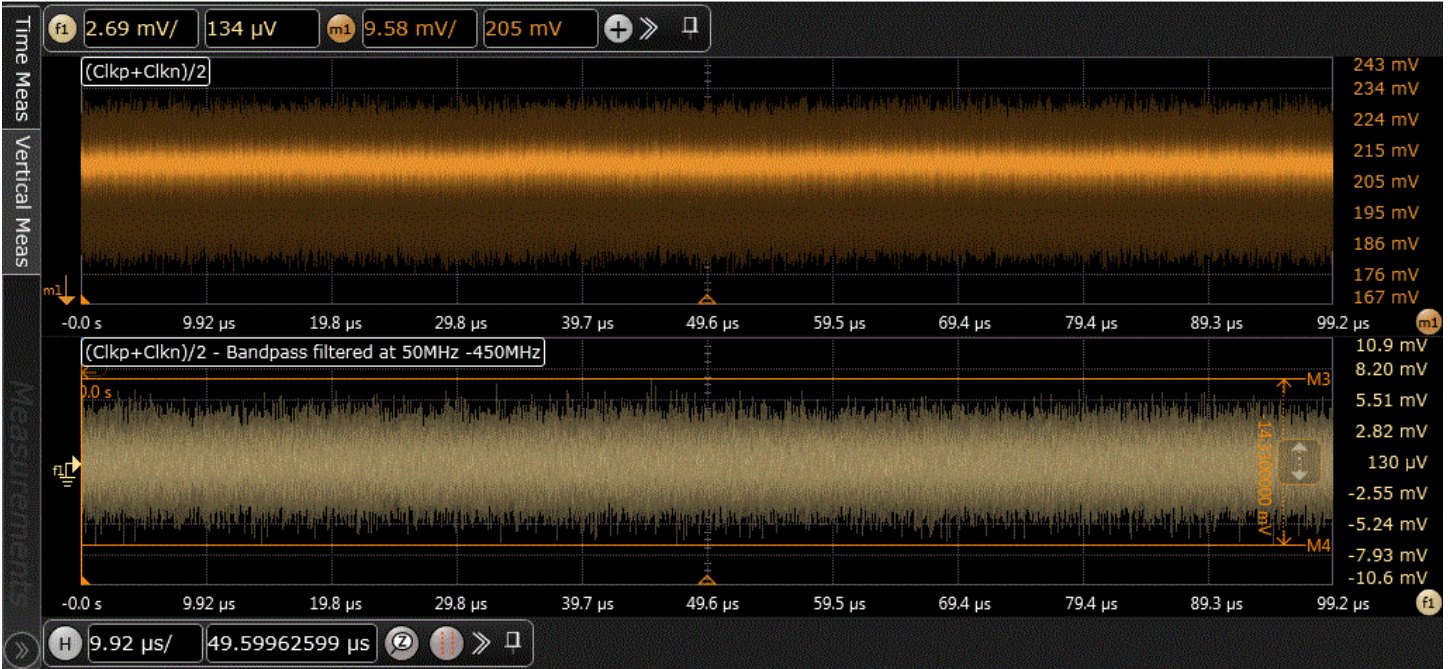
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**1.4.9 HS Clock TX Common-Level Variations Between 50-450MHz (VCMTX(LF))** D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.4.9)

Common-level variation between 50-450MHz. This test is only available for CTS v1.2 and CTS v2.0 and v2.1.  
Actual Value Measurement Name: 1820\_Vcmtx(LF)  
Pass Limits: VALUE < 25.00 mV

Actual Value	Margin	Common Level Variations(50-450MHz)	ZID	Number of HS Burst
7.30 mV	70.8 %	(See image)	100 ohm	1

Common Level Variations(50-450MHz)  
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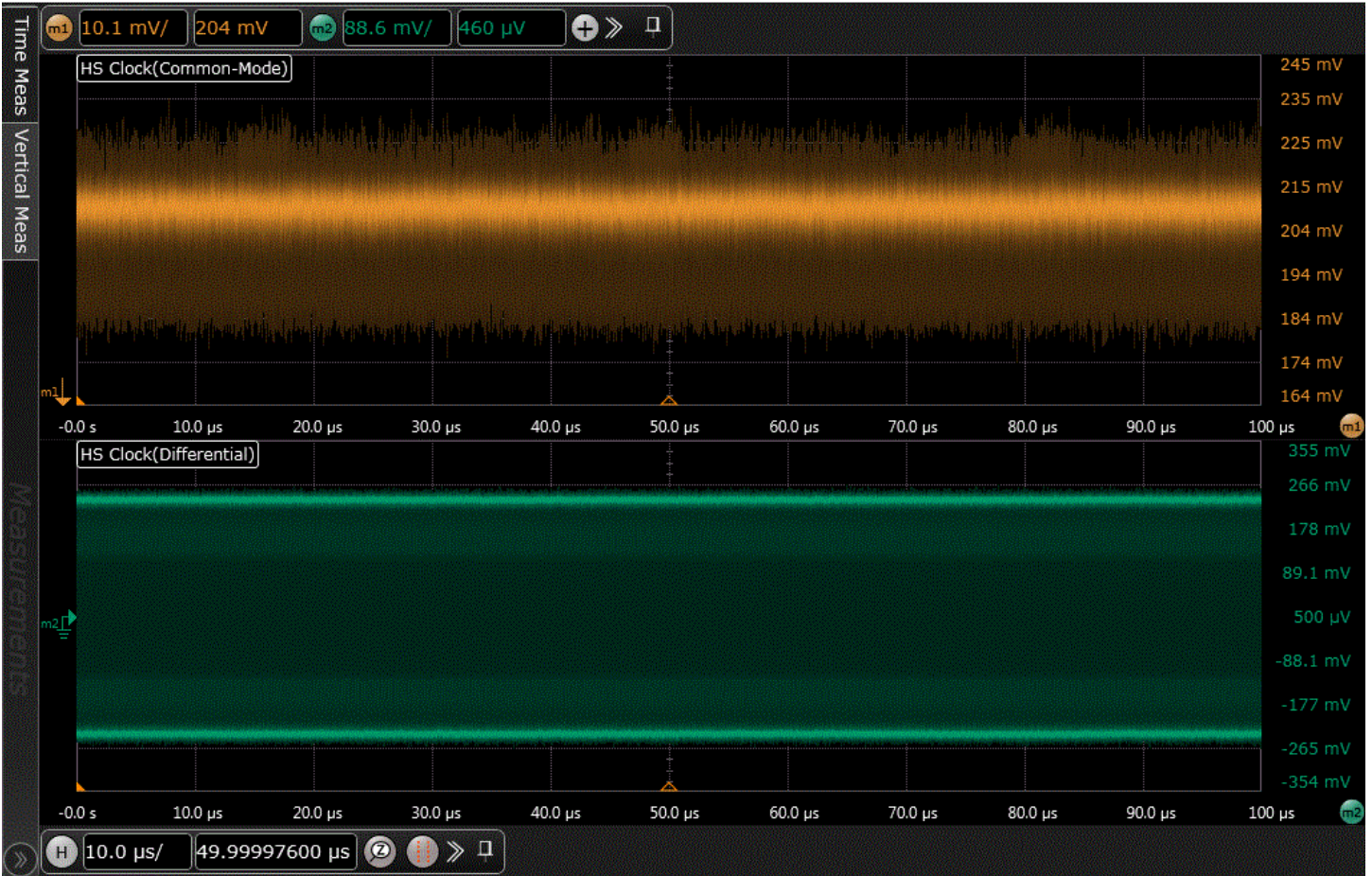
**1.4.7 HS Clock TX Static Common Mode Voltage(Vcmtx)** D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.7)

HS transmit static common-mode voltage for Clock.  
Actual Value Measurement Name: 1811\_Vcmtx(Worst)  
Pass Limits: 150.00 mV <= VALUE <= 250.00 mV

Actual Value	Margin	HS Clock TX Common Mode Voltage	Vcmtx(Differential-1)	Number of Vcmtx(Differential-1) Measured	Vcmtx(Differential-0)
213.22 mV	36.8 %	(See image)	209.78 mV	8.363000 k	213.22 mV

Number of Vcmtx(Differential-0) Measured	ZID	Number of HS Burst
8.364000 k	100 ohm	1

HS Clock TX Common Mode Voltage



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	<b>1.4.8 HS Clock TX Vcmtx Mismatch</b>	D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.8)
VCMTX mismatch when output is Differential-1 or Differential-0. Actual Value Measurement Name: 1812_Vcmtx Mismatch Pass Limits: VALUE < 5.00 mV		

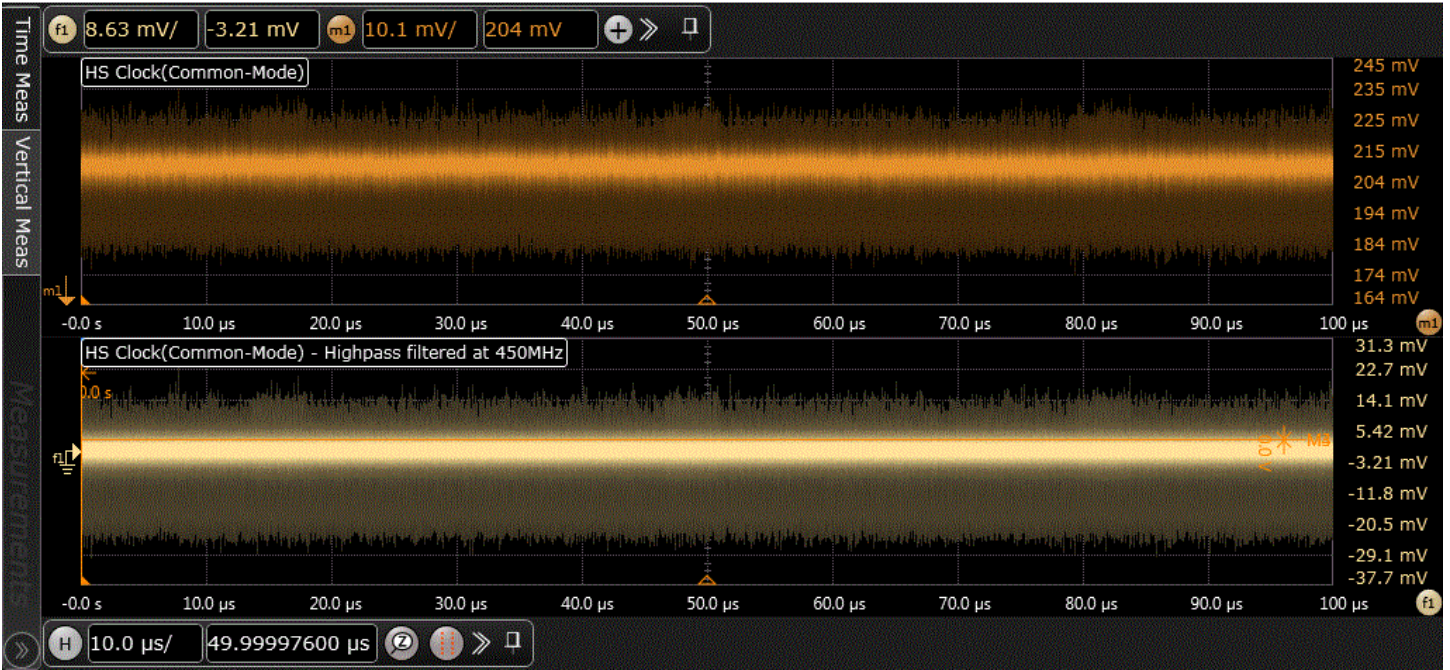
Actual Value	Margin	Vcmtx(Differential-1)	Vcmtx(Differential-0)	ZID	Number of HS Burst
1.72 mV	65.6 %	209.78 mV	213.22 mV	100 ohm	1

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	<b>1.4.10 HS Clock TX Common-Level Variations Above 450MHz (VCMTX(HF))</b>	D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.4.10)
Common-level variations above 450MHz. Actual Value Measurement Name: 1818_Vcmtx(HF) Pass Limits: VALUE < 15.00 mV		

Actual Value	Margin	Common Level Variations(>450Mhz)	ZID	Number of HS Burst
3.07 mV	79.5 %	(See image)	100 ohm	1

Common Level Variations(>450Mhz)



**1.4.4 HS Clock TX Differential Voltage(VOD0 Pulse)** Summary Previous Next  
 D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.4)  
 HS clock transmitter differential voltage.  
 Actual Value Measurement Name: 18131\_Vod0(Mean)  
 Pass Limits: -270.00 mV <= VALUE <= -140.00 mV

Actual Value	Margin	Clock VOD0 (10)	Vod(Differential-0)	Number of measurement	ZID	Number of HS Burst
-235.64 mV	26.4 %	(See image)	-235.64 mV	8.364000 k	100 ohm	1

Clock VOD0 (10)



**1.4.4 HS Clock TX Differential Voltage(VOD1 Pulse)** Summary Previous Next  
 D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.4)  
 HS clock transmitter differential voltage.  
 Actual Value Measurement Name: 18132\_Vod1(Mean)  
 Pass Limits: 140.00 mV <= VALUE <= 270.00 mV

Actual Value	Margin	Clock VOD1 (01)	Vod(Differential-1)	Number of measurement	ZID	Number of HS Burst
236.05 mV	26.1 %	(See image)	236.05 mV	8.364000 k	100 ohm	1

Clock VOD1 (01)



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	<b>1.4.5 HS Clock TX Differential Voltage Mismatch (Pulse)</b>	D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.5)
VOD mismatch when output is Differential-1 or Differential-0. Actual Value Measurement Name: 18141_Vod Mismatch Pass Limits: VALUE < 14.00 mV		

Actual Value	Margin	Vod(Differential-1)	Vod(Differential-0)	ZID	Number of HS Burst
400 $\mu$ V	97.1 %	236.05 mV	-235.64 mV	100 ohm	1

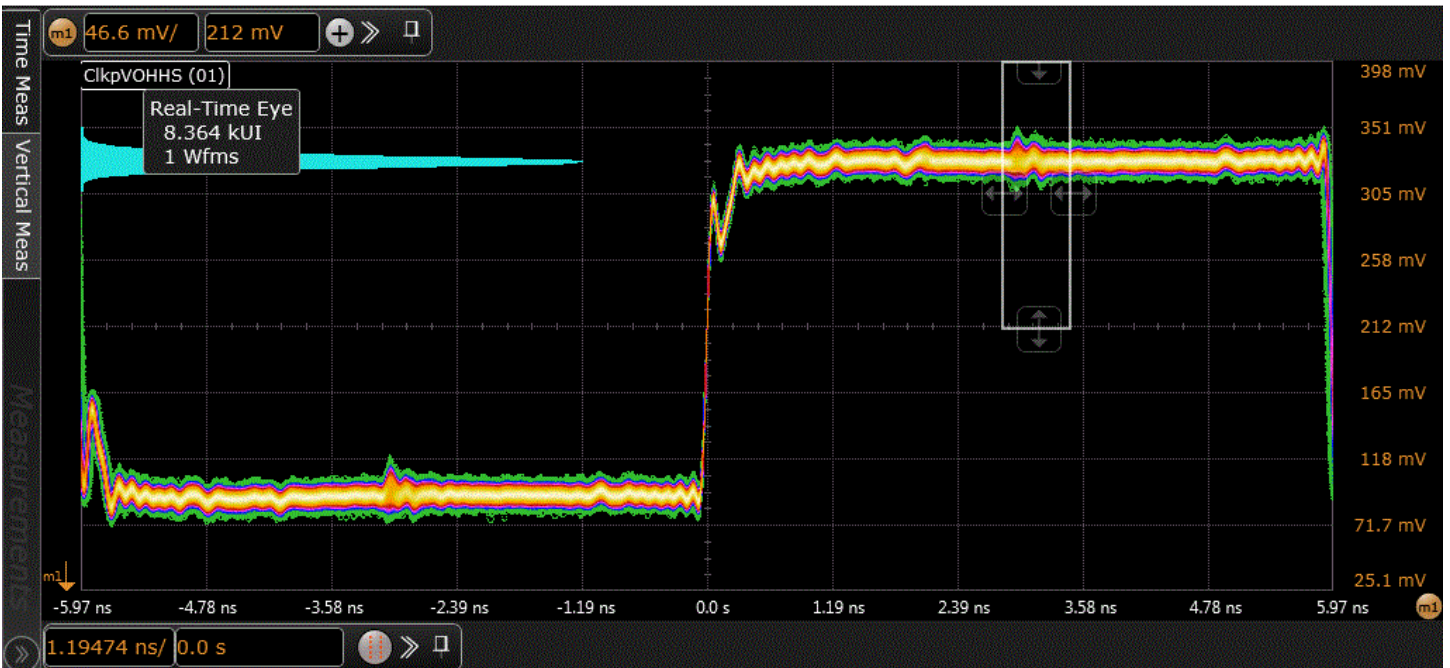
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	<b>1.4.6 HS Clock TX Single Ended Output High Voltage(VOHHS Pulse)</b>	D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.6)
HS Single Ended output high voltage. Actual Value Measurement Name: 18151_Vohhs(Worst) Pass Limits: VALUE <= 360.00 mV		

Actual Value	Margin	ClkpVOHHS (01)	ClknVOHHS (01)	Vohhs(Clkp)	Vohhs(Clkn)	Number of measurement Vohhs(Clkn)
329.04 mV	8.6 %	(See image)	(See image)	327.57 mV	329.04 mV	8.364000 k

Number of measurement Vohhs(Clkn)	ZID	Number of HS Burst
8.364000 k	100 ohm	1

ClkpVOHHS (01)



ClknVOHHS (01)



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**1.4.17 HS Clock Instantaneous (UInst)(Min)** D-PHY Specification v1.2 Section 10.1 Table 29, CTS v1.2(Test 1.4.17)

Minimum UI instantaneous (Min) of HS Clock.  
 Actual Value Measurement Name: 914\_UInst(Min)  
 Pass Limits: VALUE >= UInst\_Min\_Limit s

Actual Value	Margin	UIINST(Min)	UIINST(Mean)	Number of UI	ZID	DataLane	PassLimit Min (UInst_Min_Limit)	Number of HS Burst
5.897 ns	590E+01 %	5.896890 ns	5.978013 ns	16.727000 k	100 ohm	Lane0	0.000000000000 s	1

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**1.4.18 Clock Lane HS Clock Delta UI (UI variation)** D-PHY Specification v1.2 Section 10.1 Table 29, CTS v1.2(Test 1.4.18)

This test is to verify that the Clock lane HS Clock Delta UI is in between the minimum conformance limit(UIVariant\_Limit\_Min) and the maximum conformance limit(UIVariant\_Limit\_Max). For CTS v1.1, UIVariant\_Limit\_Min is -10% and UIVariant\_Limit\_Max is 10% for Datarate = 1Gbps, UIVariant\_Limit\_Min is -5% and UIVariant\_Limit\_Max is 5% for Datarate > 1Gbps. For CTS v1.2, UIVariant\_Limit\_Min is -10% and UIVariant\_Limit\_Max is 10% for Datarate = 1Gbps, UIVariant\_Limit\_Min is -5% and UIVariant\_Limit\_Max is 5% for Datarate > 1Gbps and = 1.5Gbps .  
 Actual Value Measurement Name: 1911\_UIVariant(Min)  
 Pass Limits: UIVariant\_Limit\_Min % <= VALUE <= UIVariant\_Limit\_Max %

Actual Value	Margin	UIINST(Min)	UIINST(Max)	UIINST(Mean)	Number of UI	DataLane	UIVariant_min	UIVariant_max	ZID
-1.36 %	43.2 %	5.896890 ns	6.045260 ns	5.978013 ns	16.727000 k	Lane0	-1.357 %	1.125 %	100 ohm

PassLimit Min (UIVariant_Limit_Min)	PassLimit Max (UIVariant_Limit_Max)	Number of HS Burst
-10.00 %	10.00 %	1

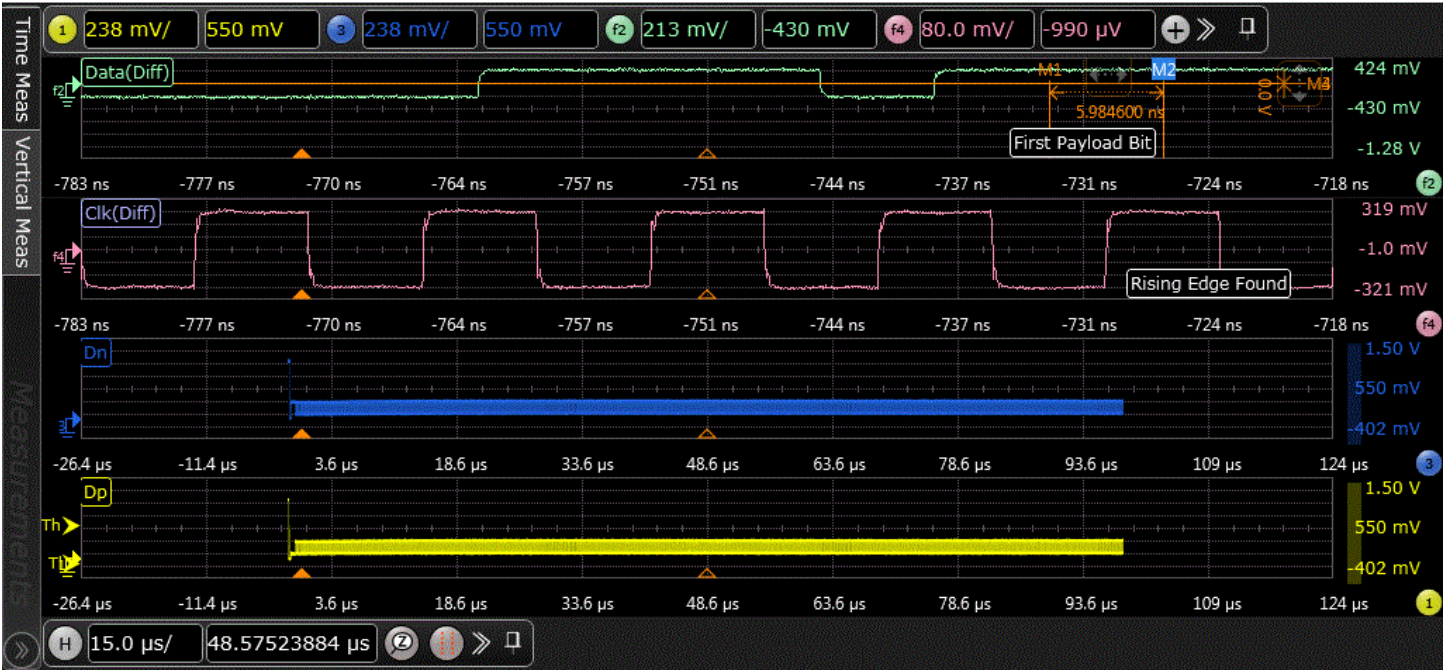
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**1.5.3 HS Clock Rising Edge Alignment to First Payload Bit** D-PHY Specification v1.2 Section 10.2, CTS v1.2(Test 1.5.3)

Test will pass when there is a rising edge during the first payload bit.  
 "First Payload Bit Alignment" will be set to "PASS" ONLY when a rising edge is detected during the first payload bit.  
 Actual Value Measurement Name: 912\_First Payload Bit Alignment  
 Pass Limits: VALUE <= 500.000000000 m

Actual Value	Margin	First Payload Bit Clock Alignment	ZID	DataLane	Number of HS Burst
Pass	100.0 %	(See image)	100 ohm	Lane0	1

First Payload Bit Clock Alignment



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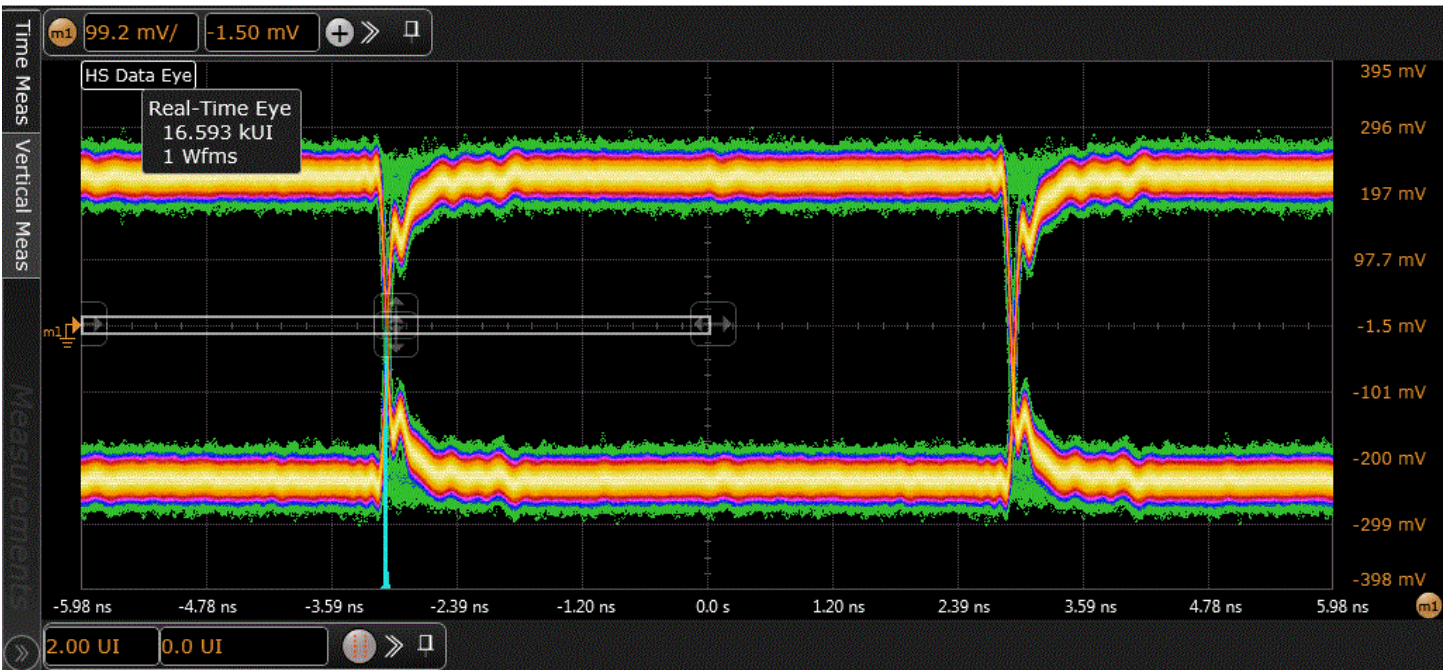
**1.5.4 Data-to-Clock Skew (TSKEW(TX))(Max,Min)** D-PHY Specification v1.2 Section 10.2.1 Table 30, CTS v1.2(Test 1.5.4)

Data to Clock Skew [measured at transmitter].  
 Actual Value Measurement Name: 913\_Tskew(Worst)  
 Pass Limits: MinMaxTSkewTest\_LimitMin Ulinst <= VALUE <= MinMaxTSkewTest\_LimitMax Ulinst

Actual Value	Margin	LeftCrossing	UIINST(Mean)	TSkew(Min)	TSkew(Max)	No Of Measurement	ZID	DataLane
19 mUIinst	43.7 %	(See image)	5.9780 ns	28.0 ps	112.1 ps	16.593000 k	100 ohm	Lane0

PassLimit Min (MinMaxTSkewTest_LimitMin)	PassLimit Max (MinMaxTSkewTest_LimitMax)	Number of HS Burst
-150 mUIinst	150 mUIinst	1

LeftCrossing



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**1.5.4 Data-to-Clock Skew (TSKEW(TX))(Mean)** D-PHY Specification v1.2 Section 10.2.1 Table 30, CTS v1.2(Test 1.5.4)

Data to Clock Skew [measured at transmitter].  
 Actual Value Measurement Name: 9131\_Tskew(Mean)  
 Pass Limits: MeanTSkewTest\_LimitMin Ulinst <= VALUE <= MeanTSkewTest\_LimitMax Ulinst

Actual Value	Margin	UIINST(Mean)	TSkew(Mean)	No Of Measurement	ZID	DataLane	PassLimit Min (MeanTSkewTest_LimitMin)
12 mUIinst	46.0 %	5.9780 ns	71.2 ps	16.593000 k	100 ohm	Lane0	-150 mUIinst

PassLimit Max (MeanTSkewTest_LimitMax)	Number of HS Burst
150 mUIinst	1

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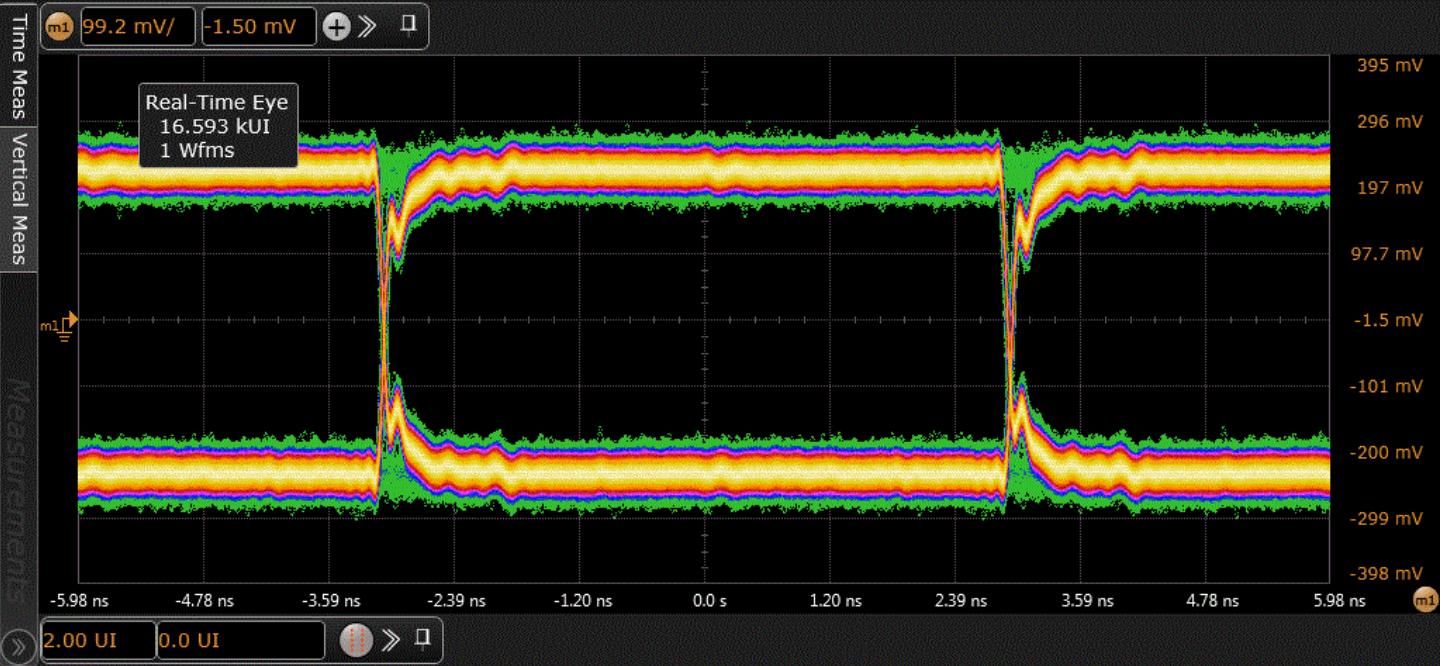
**HS Data Eye Height (Informative)** Informative



HS Data Eye Height  
 Actual Value Measurement Name: 915\_Eye Height  
 Pass Limits: VALUE >= Eye\_Height\_limit Vpp

Actual Value	Margin	UI	ZID	DataLane	EyeHeight	PassLimit Min (Eye_Height_limit)	Number of HS Burst
371 mVpp	165.0 %	5.978016 ns	100 ohm	Lane0	(See image)	140 mVpp	1

EyeHeight  
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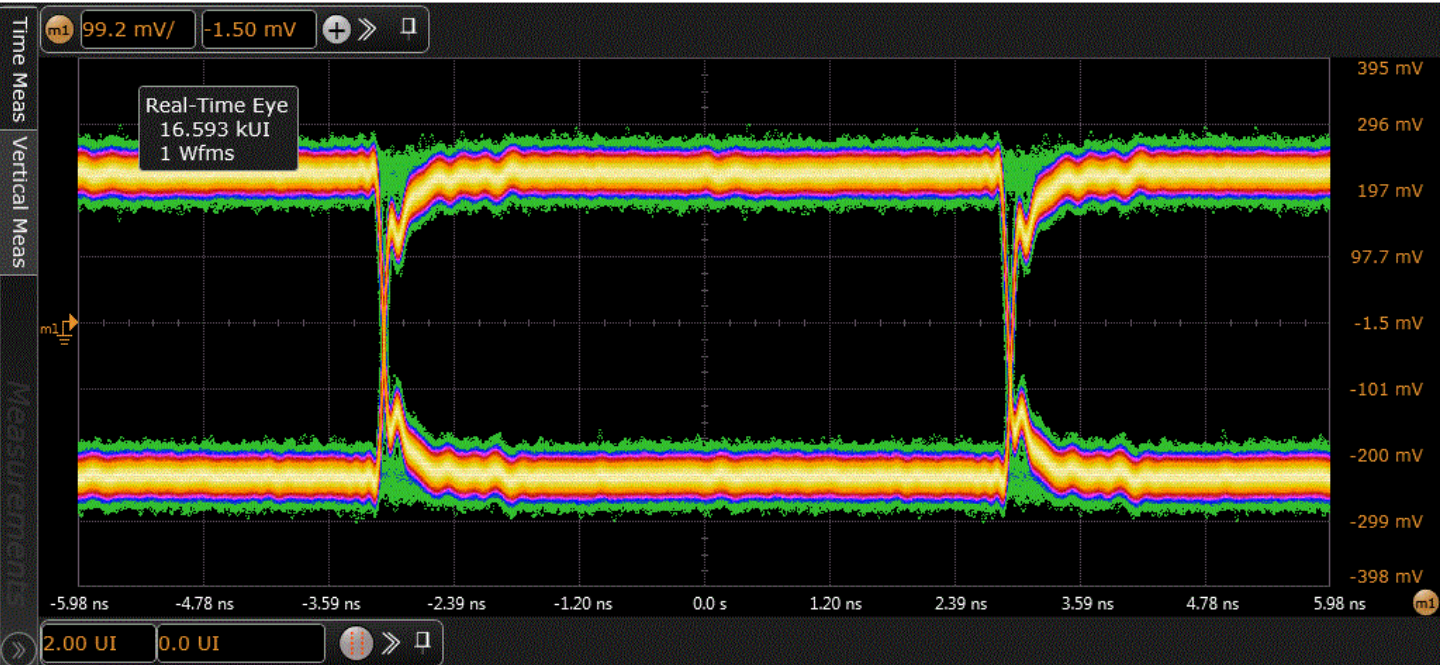
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**HS Data Eye Width (Informative)** Informative

HS Data Eye Width.  
 Actual Value Measurement Name: 916\_Eye Width  
 Pass Limits: VALUE >= Eye\_Width\_limit UI

Actual Value	Margin	UI	ZID	DataLane	EyeWidth	PassLimit Min (Eye_Width_limit)	Number of HS Burst
992 mUI	98.4 %	5.978016 ns	100 ohm	Lane0	(See image)	500 mUI	1

EyeWidth  
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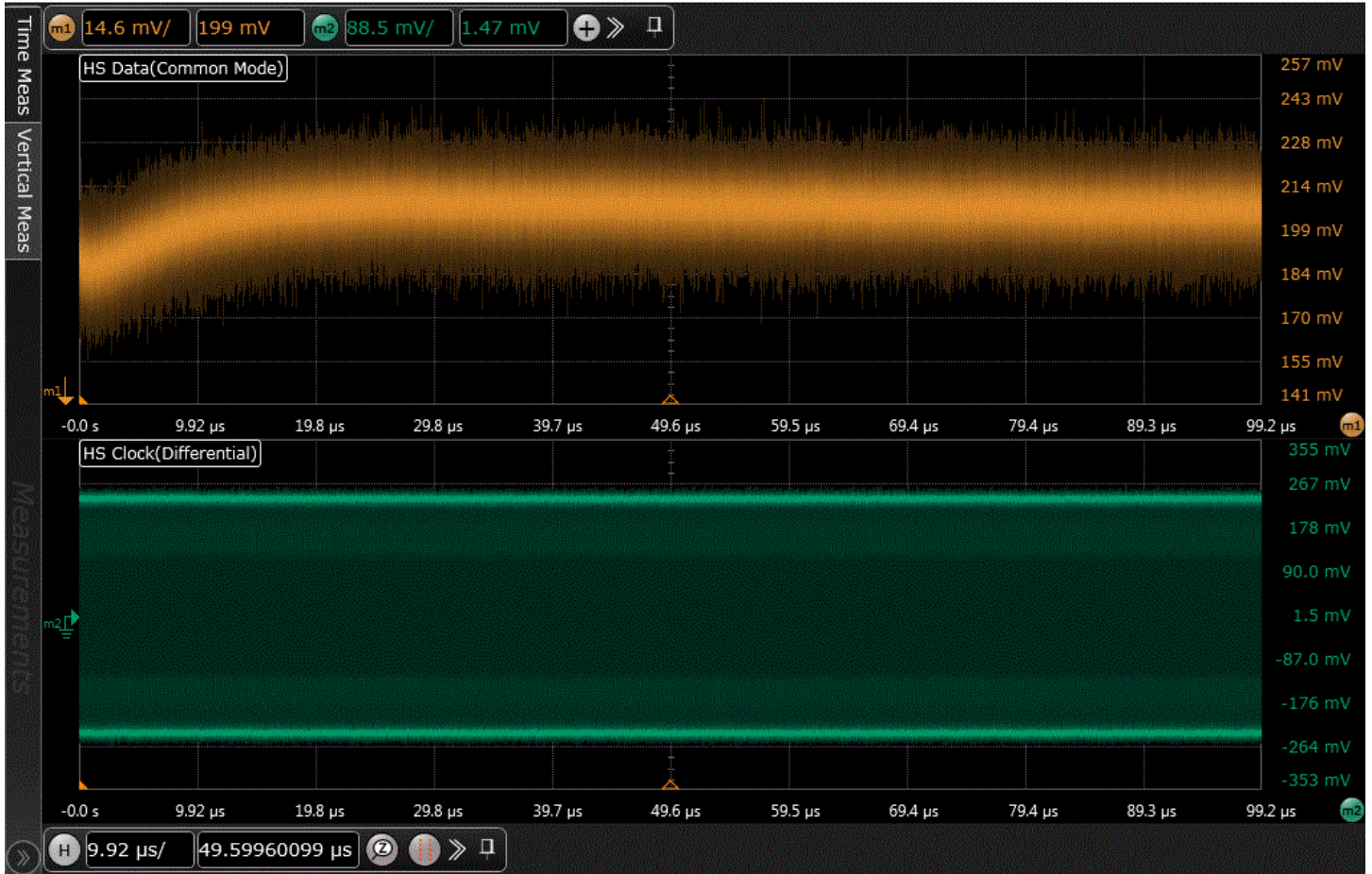
**1.3.7 HS Data TX Static Common Mode Voltage(Vcmtx)** D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.3.7)

HS transmit static common-mode voltage.  
 Actual Value Measurement Name: 811\_Vcmtx(Worst)  
 Pass Limits: 150.00 mV <= VALUE <= 250.00 mV

Actual Value	Margin	HS Data TX Common Mode Voltage	Vcmtx(Differential-1)	Number of Vcmtx(Differential-1) Measured	Vcmtx(Differential-0)
208.72 mV	41.3 %	(See image)	208.72 mV	8.282000 k	204.12 mV

Number of Vcmtx(Differential-0) Measured	ZID	DataLane	Number of HS Burst
8.312000 k	100 ohm	Lane0	1

HS Data TX Common Mode Voltage



**1.3.8 HS Data TX Vcmtx Mismatch** [Summary](#) [Previous](#) [Next](#)

D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.3.8)

VCMTX mismatch when output is Differential-1 or Differential-0.  
 Actual Value Measurement Name: 812\_Vcmtx Mismatch  
 Pass Limits: VALUE < 5.00 mV

Actual Value	Margin	Vcmtx(Differential-1)	Vcmtx(Differential-0)	ZID	DataLane	Number of HS Burst
2.30 mV	54.0 %	208.72 mV	204.12 mV	100 ohm	Lane0	1

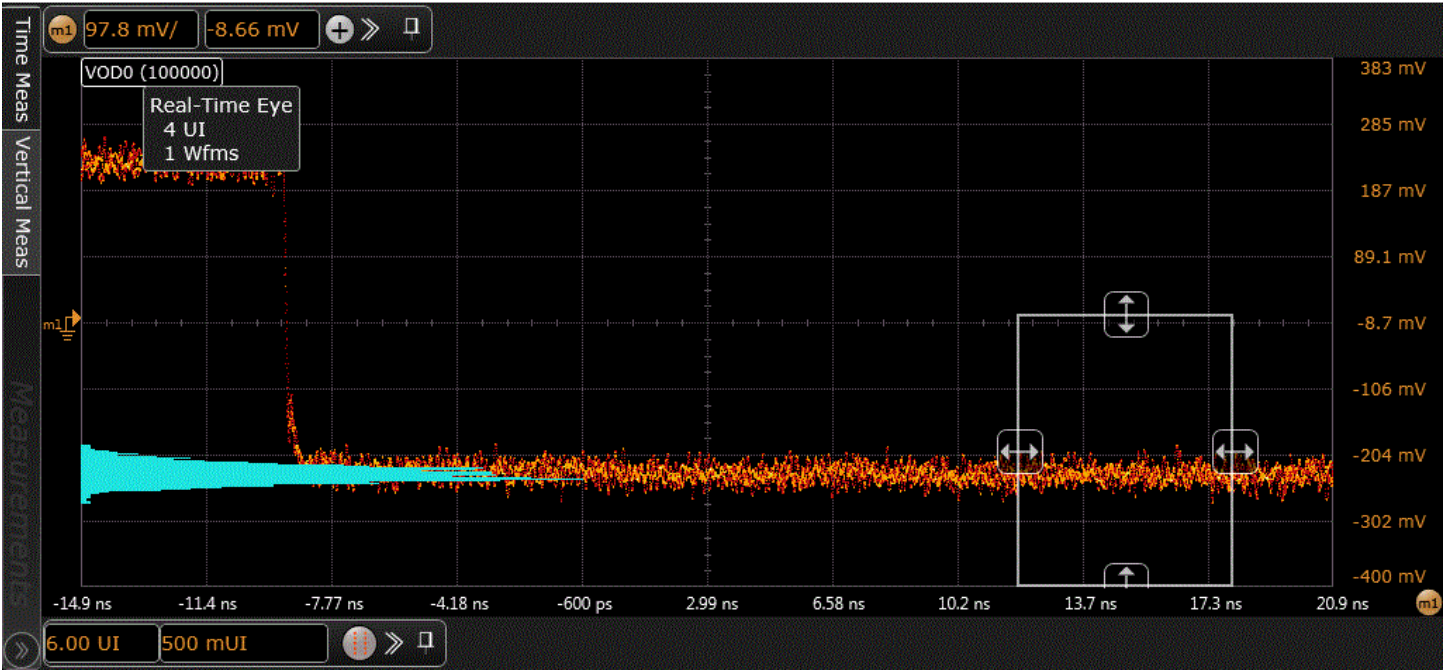
**1.3.4 HS Data TX Differential Voltage(VOD0 Pulse)** [Summary](#) [Previous](#) [Next](#)

D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.3.4)

HS transmit differential voltage.  
 This test will measure the VOD0 based on the reference data patterns(100000) of differential signal.  
 Actual Value Measurement Name: 8131\_Vod0(Mean)  
 Pass Limits: -270.00 mV <= VALUE <= -140.00 mV

Actual Value	Margin	VOD0 (100000)	Vod(Differential-0)	Number of measurement	ZID	DataLane	Number of HS Burst
-232.26 mV	29.0 %	(See image)	-232.26 mV	4.000	100 ohm	Lane0	1

VOD0 (100000)



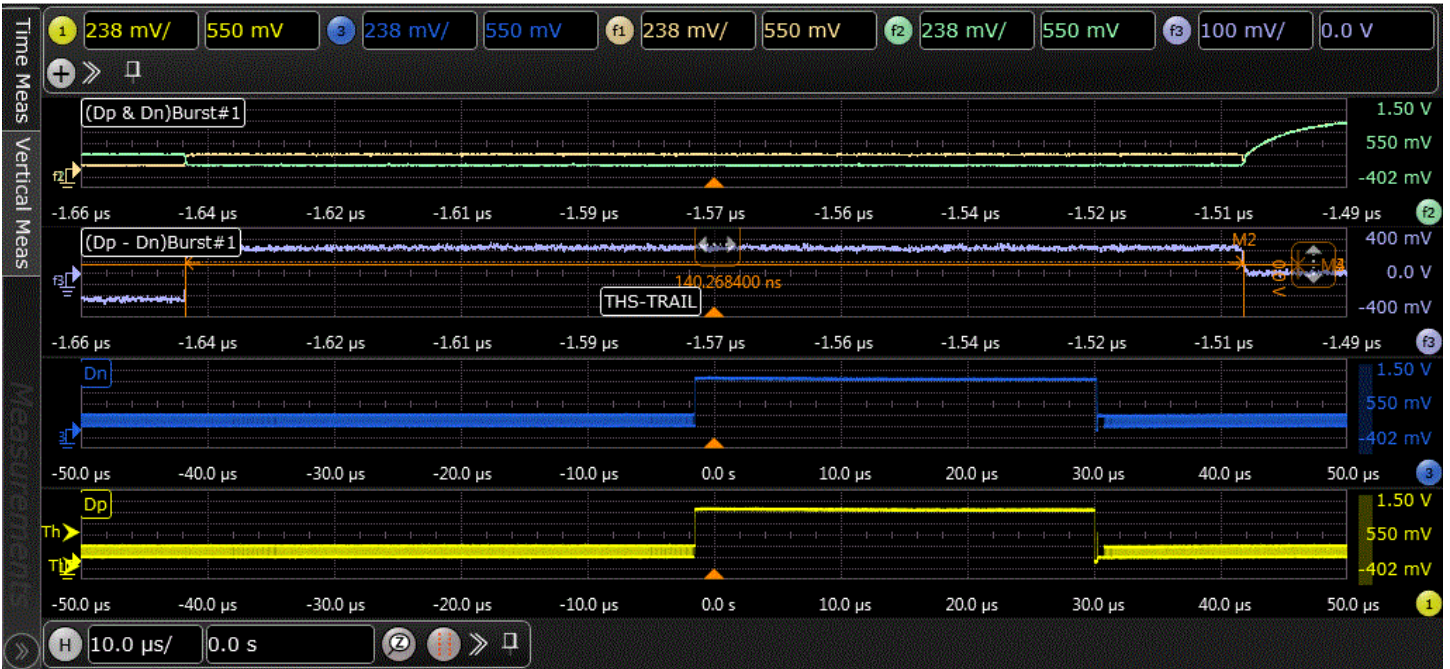
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**1.3.13 HS Exit: DATA TX THS-TRAIL** D-PHY Specification v1.2 Section 6.9 Table 14, CTS v1.2(Test 1.3.13)

Time to drive flipped differential state after last payload data bit of a HS transmission burst.  
 TXTHSTrail\_LimitMin is based on  $60ns+n*4*UI$ .  
 The THS-SKIP parameter is useful to avoid glitch problem during THS-TRAIL measurement.  
 Any transition on the Data Lane in THS-SKIP time interval will be ignored when finding last payload data bit of HS transmission burst.  
 The default value of THS-SKIP is set to 0s to prevent invalid THS-TRAIL measurement.  
 Actual Value Measurement Name: 546\_THS-TRAIL  
 Pass Limits: VALUE  $\geq$  TXTHSTrail\_LimitMin s

Actual Value	Margin	THSTRAIL	THS-SKIP(s)	ZID	DataLane	PassLimit Min (TXTHSTrail_LimitMin)	Number of HS burst
140.27 ns	67.2 %	(See image)	0.000000000000 s	100 ohm	Lane0	83.89 ns	1

THSTRAIL



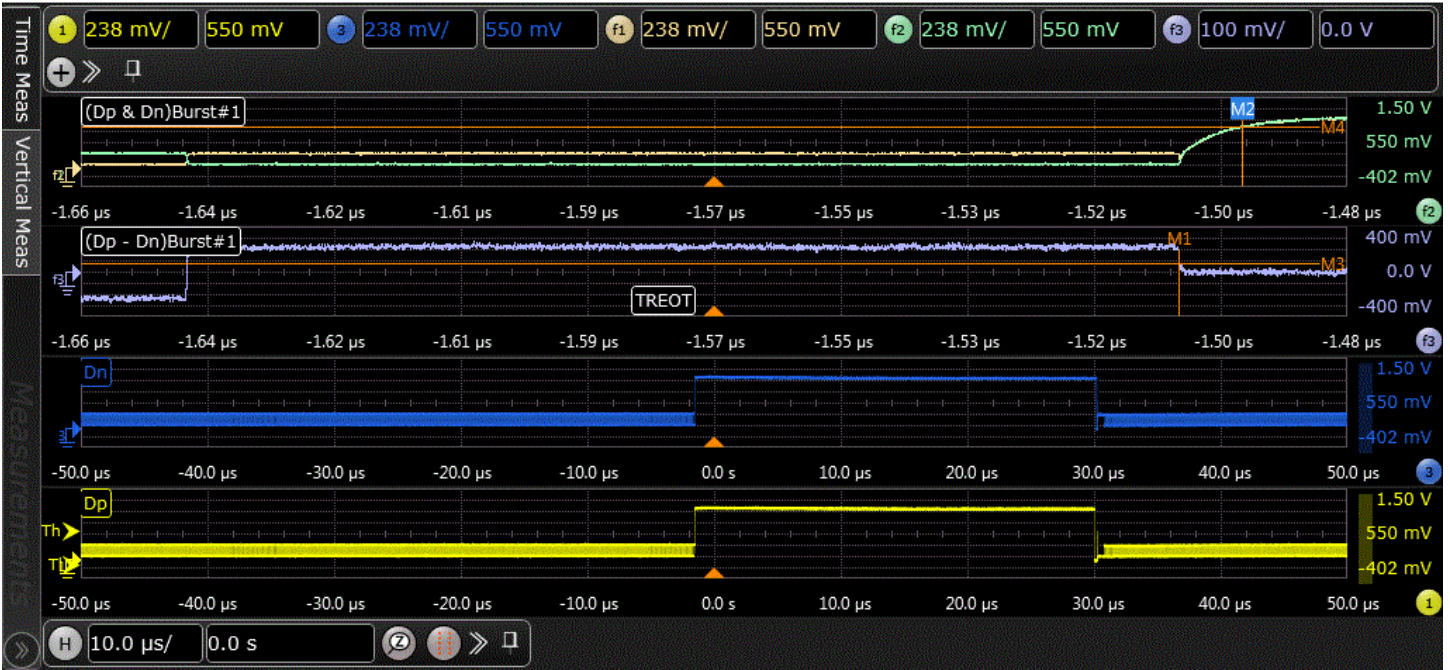
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**1.3.14 HS Exit: DATA TX TREOT** D-PHY Specification v1.2 Section 9.1.2 Table 22, CTS v1.2(Test 1.3.14)

30%-85% rise time and fall time  
 Actual Value Measurement Name: 549\_TREOT  
 Pass Limits: VALUE  $\leq$  35.00 ns

Actual Value	Margin	TREOT	ZID	DataLane	Number of HS burst
8.82 ns	74.8 %	(See image)	100 ohm	Lane0	1

TREOT

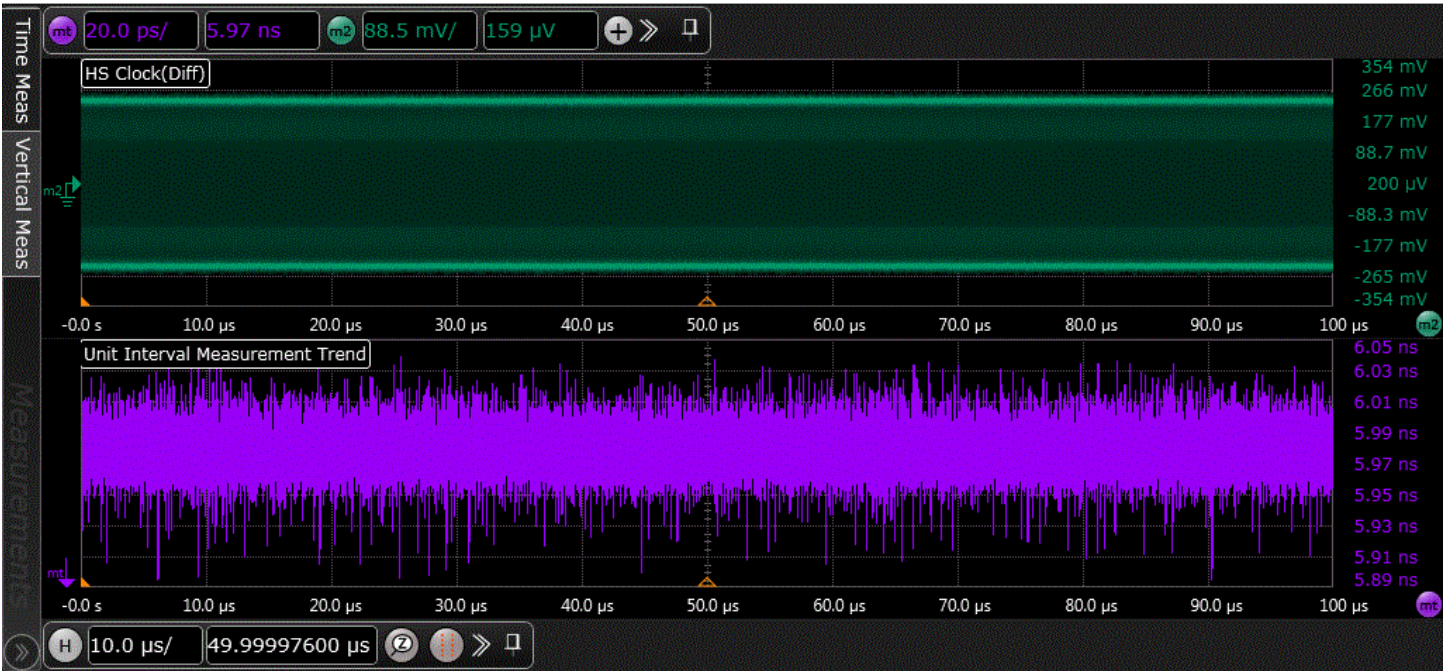


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**1.4.17 HS Clock Instantaneous (UIInst)(Max)** D-PHY Specification v1.2 Section 10.1 Table 29, CTS v1.2(Test 1.4.17)

Maximum UI instantaneous of HS Clock.  
 Actual Value Measurement Name: 911\_UIInst(Max)  
 Pass Limits: VALUE < 12.500 ns

Actual Value	Margin	UIInst	UIINST(Max)	UIINST(Mean)	Number of UI	ZID	DataLane	Number of HS Burst
6.044 ns	51.6 %	(See image)	6.043970 ns	5.978012 ns	16.727000 k	100 ohm	Lane0	1



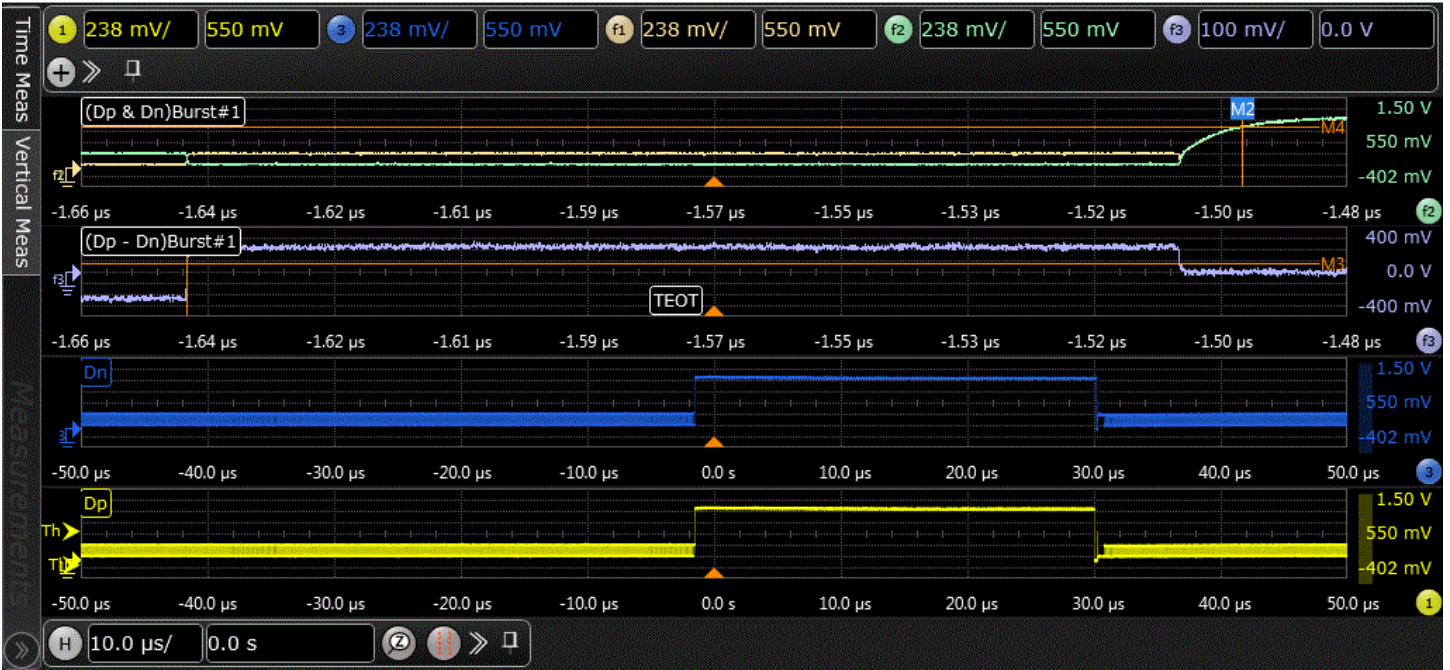
Summary Previous Next

**1.3.15 HS Exit: DATA TX TEOT** D-PHY Specification v1.2 Section 6.9 Table 14, CTS v1.2(Test 1.3.15)

Time from start of THS-TRAIL period to start of LP-11 state.  
 TXTEOT\_LimitMax is based on 105ns+n\*12\*UI.  
 Actual Value Measurement Name: 547\_TEOT  
 Pass Limits: VALUE <= TXTEOT\_LimitMax s

Actual Value	Margin	TEOT	UIINST(Mean)	ZID	DataLane	PassLimit Max (TXTEOT_LimitMax)	Number of HS burst
149.08 ns	15.7 %	(See image)	5.978012 ns	100 ohm	Lane0	176.74 ns	1

TEOT



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	<b>1.3.16 HS Exit: DATA TX THS-EXIT</b>	D-PHY Specification v1.2 Section 6.9 Table 14, CTS v1.2(Test 1.3.16)
Time to drive LP-11 after HS burst. Actual Value Measurement Name: 548_THS-EXIT Pass Limits: VALUE >= 100.00 ns		

Actual Value	Margin	THSEXIT	Notes:	ZID	DataLane	Number of HS burst
253.27 ns	153.3 %	(See image)	The actual THS-EXIT value is greater than the result shown.	100 ohm	Lane0	1

THSEXIT

