datasheet

PRELIMINARY SPECIFICATION

1/2.6" color CMOS (1920 x 1280) high dynamic range (HDR) image sensor with PureCel®Plus-S technology

OX03C10

color CMOS (1920x1280) high dynamic range (HDR) image sensor with PureCel®Plus-S technology

datasheet (a-CSP™)
PRELIMINARY SPECIFICATION

version 1.1
november 2020

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applications

- automotive
  - SVS
  - rear view camera
  - autonomous driving
  - e-Mirror

ordering information

- **OX03C10-E66Y-001B-Z** (color, lead-free)
  66-pin a-CSP™ packed in tray without protective film

features

- support for image size: 1920x1280 and any cropped size
- PureCel®Plus-S technology
- HDR readout modes, with up to 4x captures and on-chip combination:
  - on-chip line buffers (alignment with staggered readout)
  - DCG (LPD) + SPD + staggered (VS)
  - DCG (LPD) + staggered (VS)
  - LFM support (SPD)
  - PWL mapping from 24-bit to 20, 16, 14, and 12-bit
- motion free HDR (3 capture), 4 capture HDR optimized to minimize motion artifacts
- SCCB for register programming
- high speed serial data transfer with MIPI CSI-2
- image signal processor functions: lens shading correction, defective pixel cancellation, HDR combination, automatic black level correction, PWL compression, etc.
- safety features for supporting ASIL C applications
- parallel 12-bit DVP output
- external frame synchronization capability
- embedded temperature sensor
- embedded supply voltage monitor
- one-time programmable (OTP) memory

note To reduce image artifacts from infrared light and provide the best image quality, OmniVision recommends an IR-cut filter

key specifications (typical)

- **active array size:** 1920 x 1280
- **power supply:**
  analog: 2.9V
  digital: 1.1V
  I/O pads: 1.8V/3.3V
- **power requirements:**
  active: streaming @ 1280p60: 390 mW (HDR4 combined 24b), streaming @ 1280p30: 290 mW (HDR4 combined 24b)
- **temperature range:**
  operating: -40°C to 105°C sensor ambient temperature and -40°C to 125°C junction temperature (see **table 9-2**)
- **output interfaces:** up to 4-lane MIPI CSI-2, 12-bit DVP
- **input clock frequency:** 18~27 MHz
- **lens size:** 1/2.6"
- **lens chief ray angle:** 20° (see **figure 11-3**)
- **SCCB speed**: up to 1 MHz
- **max S/N ratio:** 41.6 dB
- **sensitivity:** 25,100 e^-/Lux-sec
- **output formats:** uncompressed 24-bit, 20/16/14/12-bit (PWL) combined HDR (4 captures)
- **maximum image transfer rate:**
  60 fps @ 1280p
- **dynamic range:**
  140 dB HDR4 (DCG + SPD + VS),
  120 dB HDR3 (DCG + VS)
- **pixel size:** 3 µm x 3 µm
- **image array area:** 5814 µm x 3894 µm
- **package cover glass type:** double sided anti-reflective (AR/AR) coating
- **package dimensions:** 6862 µm x 4936 µm

note Pixel performance and power requirements are estimates. Values may change based on real measurements.

note The OX03C10 will be qualified to AEC-Q100 grade-2 specifications.

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1 application system

1.1 overview

The OX03C10 is a 1/2.6" optical format, 1920x1280 stacked-chip, 3.0 µm split-diode DCG pixel, digital high dynamic range sensor, intended for high-end CMS and SVS applications for the automotive market.

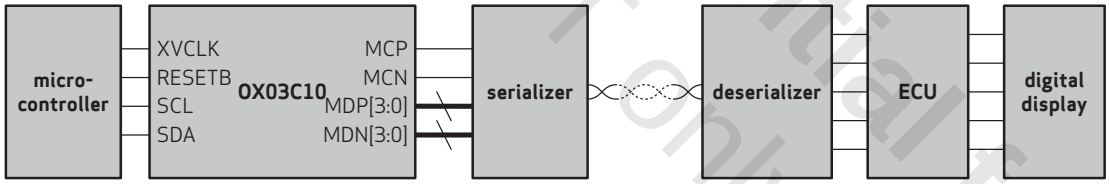
The OX03C10 can output 24-bit HDR combined video featuring LFM (LED flicker mitigation), triple exposure staggered HDR (DCG+SPD+VS), 20-bit HDR combined video featuring LFM, and dual exposure staggered HDR (DCG+VS). The sensor can also output 4x10-bit RAW video (only supported for MIPI output) for off-chip/external combine, output triple exposure staggered HDR, and dual exposure staggered HDR with SPD on a separate channel.

The OX03C10 performs sophisticated camera functions on-chip controlled via the serial camera control bus (SCCB) interface with optional CRC and packet error check (PEC) enabling. These functions include black level correction (BLC), HDR combination, defect pixel correction (DPC), and piecewise linear (PWL) image compression. The OX03C10 enables advanced HDR imaging in a simple, cost effective system.

1.1.1 typical OX03C10 standalone camera

figure 1-1 shows the block diagram of a standalone OX03C10 camera for automotive applications. The microcontroller programs the register settings and controls the OX03C10 based on the application requirements. The serializer and deserializer (SerDes) pair is for transferring video from the camera to the display unit over a long distance.

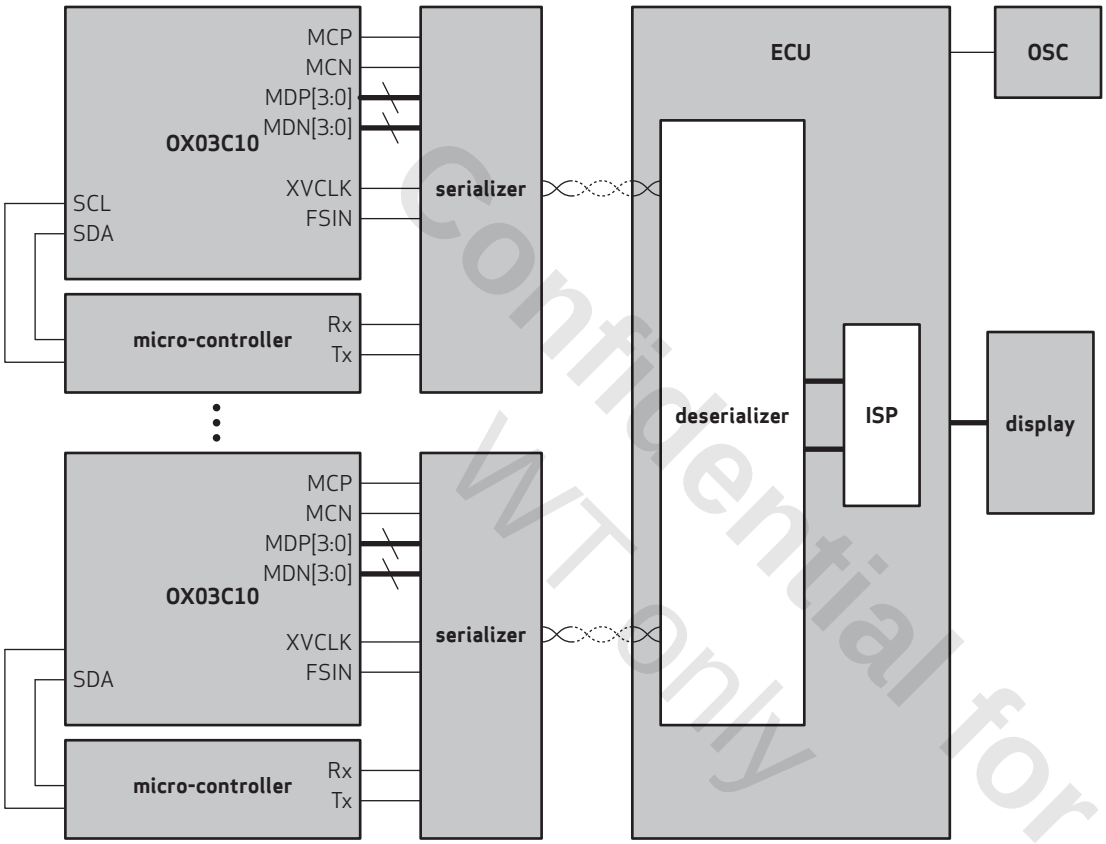
figure 1-1 standalone camera block diagram for automotive applications



1.1.2 typical OX03C10 multi-camera system

The OX03C10 features frame sync input to synchronize the video streaming timing between multiple sensors in a multi-camera system. **figure 1-2** shows the block diagram of a typical multi-camera system using the OX03C10. The sensor registers are programmed by the processor from the back channel.

figure 1-2 multi-camera block diagram



1.2 signal description and pin assignment

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OX03C10 image sensor. The package information is shown in **section 10**. NC labeled pins are not connected to any other electrical net. For better thermal conduction, they can be tied to the ground plane.

figure 1-3 pin diagram

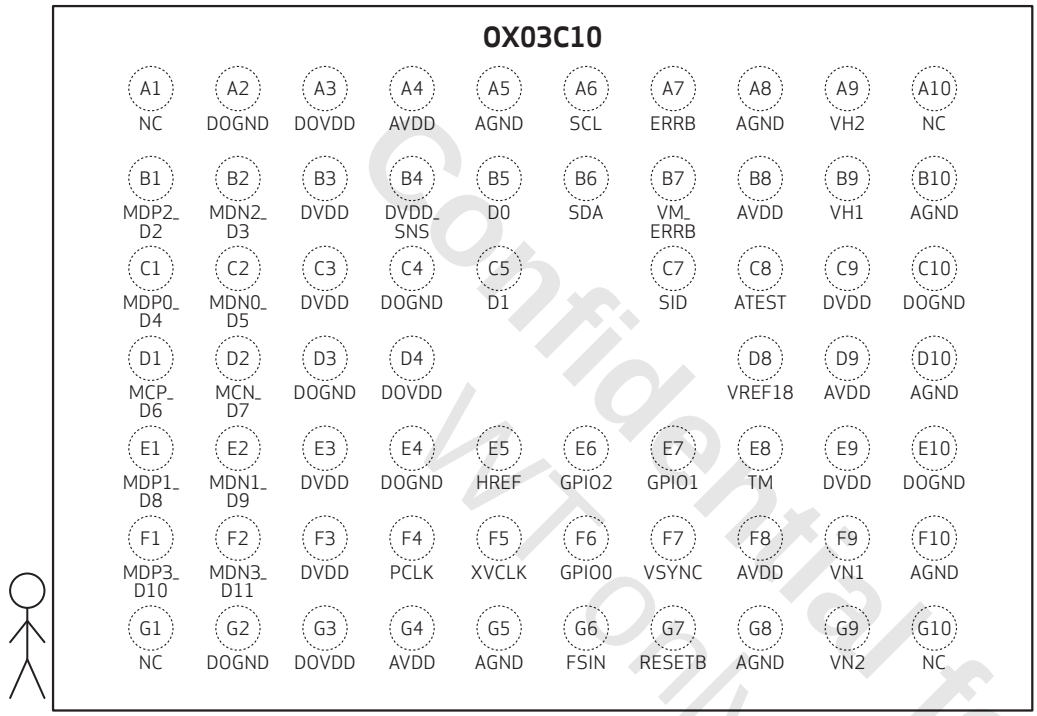


table 1-1 signal descriptions (sheet 1 of 3)

pin number	signal name	pin type	description
A1	NC	–	no connect
A2	DOGND	ground	digital I/O/core ground
A3	DOVDD	power	digital I/O power supply
A4	AVDD	power	analog power supply
A5	AGND	ground	analog ground
A6	**SCL**	input	SCCB input clock

table 1-1 signal descriptions (sheet 2 of 3)

pin number	signal name	pin type	description
A7	**ERRB**	output	fail state error flag (active low)
A8	AGND	ground	analog ground
A9	VH2	analog I/O	analog voltage reference
A10	NC	–	no connect
B1	**MDP2_D2**	output	MIPI data positive output 2/DVP output data 2
B2	**MDN2_D3**	output	MIPI data negative output 2/DVP output data 3
B3	DVDD	power	digital core power supply
B4	DVDD_SNS	sense	power supply sense (DVDD)
B5	**D0**	output	DVP output data 0
B6	**SDA**	I/O	SCCB data (bi-directional)
B7	**VM_ERRB**	output	voltage error flag (active low)
B8	AVDD	power	analog power supply
B9	VH1	analog I/O	analog voltage reference
B10	AGND	ground	analog ground
C1	**MDP0_D4**	output	MIPI data positive output 0/DVP output data 4
C2	**MDN0_D5**	output	MIPI data negative output 0/DVP output data 5
C3	DVDD	power	digital core power supply
C4	DOGND	ground	digital I/O/core ground
C5	**D1**	output	DVP output data 1
C7	**SID**	input	SCCB address
C8	**ATEST**	analog I/O	analog test pad
C9	DVDD	power	digital core power supply
C10	DOGND	ground	digital I/O/core ground
D1	**MCP_D6**	output	MIPI clock positive output/DVP output data 6
D2	**MCN_D7**	output	MIPI clock negative output/DVP output data 7
D3	DOGND	ground	digital I/O/core ground
D4	DOVDD	power	digital I/O power supply
D8	VREF18	analog I/O	analog voltage reference
D9	AVDD	power	analog power supply
D10	AGND	ground	analog ground

table 1-1 signal descriptions (sheet 3 of 3)

pin number	signal name	pin type	description
E1	**MDP1_D8**	output	MIPI data positive output 1/DVP output data 8
E2	**MDN1_D9**	output	MIPI data negative output 1/DVP output data 9
E3	DVDD	power	digital core power supply
E4	DOGND	ground	digital I/O/core ground
E5	**HREF**	output	DVP horizontal sync signal
E6	**GPIO2**	I/O	general purpose I/O 2
E7	**GPIO1**	I/O	general purpose I/O 1
E8	**TM**	input	test mode
E9	DVDD	power	digital core power supply
E10	DOGND	ground	digital I/O/core ground
F1	**MDP3_D10**	output	MIPI data positive output 3/DVP output data 10
F2	**MDN3_D11**	output	MIPI data negative output 3/DVP output data 11
F3	DVDD	power	digital core power supply
F4	**PCLK**	output	DVP output clock
F5	**XVCLK**	input	reference clock input
F6	**GPIO0**	I/O	general purpose I/O 0
F7	**VSYNC**	I/O	vertical sync signal
F8	AVDD	power	analog power supply
F9	VN1	analog I/O	analog voltage reference
F10	AGND	ground	analog ground
G1	NC	–	no connect
G2	DOGND	ground	digital I/O/core ground
G3	DOVDD	power	digital I/O power supply
G4	AVDD	power	analog power supply
G5	AGND	ground	analog ground
G6	**FSIN**	I/O	frame sync input
G7	**RESETB**	input	reset (active low)
G8	AGND	ground	analog ground
G9	VN2	analog I/O	analog voltage reference
G10	NC	–	no connect

table 1-2 pin states under various conditions

pin number	signal name	RESETB mode	SW_STANDBY mode (MIPI, default)	SW_STANDBY mode (DVP)
A6	SCL	high-z	input	input
A7	ERRB	low	low[a]	low[a]
B1	MDP2_D2	high-z	high	low
B2	MDN2_D3	high-z	high	low
B5	D0	low	high[a]	low
B6	SDA	open drain	I/O	I/O
B7	VM_ERRB	low	low	low
C1	MDP0_D4	high-z	high	low
C2	MDN0_D5	high-z	high	low
C5	D1	high-z	high-z	low
C7	SID	input	input	input
C8	ATEST	high-z	high-z	high-z
D1	MCP_D6	high-z	high	low
D2	MCN_D7	high-z	high	low
E1	MDP1_D8	high-z	high	low
E2	MDN1_D9	high-z	high	low
E5	HREF	low	high[a]	low
E6	GPIO2	low	high	low
E7	GPIO1	low	high	low
E8	TM	input (0)[b]	input (0)[b]	input (0)[b]
F1	MDP3_D10	high-z	high	low
F2	MDN3_D11	high-z	high	low
F4	PCLK	low	low	high
F5	XVCLK	input	input	input
F6	GPIO0	low	low	low
F7	VSYNC	high-z	high-z	low
G6	FSIN	high-z	high-z	input (configurable)
G7	RESETB	input (0)[b]	input (1)[c]	input (1)[c]

a. state will be different when entering SW_standby after streaming

b. input (0) externally driven low

c. input (1) externally driven high

table 1-3 pad equivalent circuit (sheet 1 of 2)

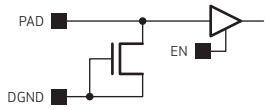
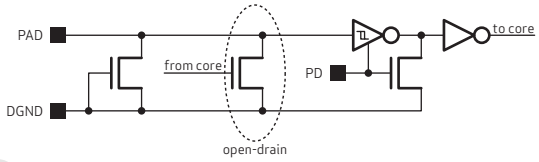
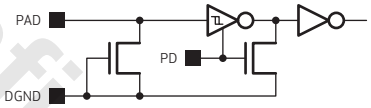
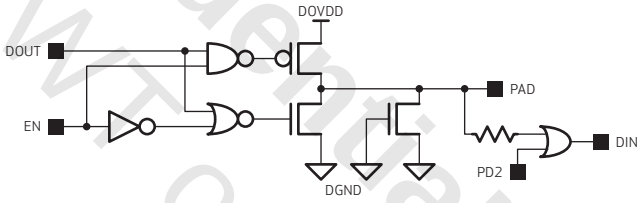
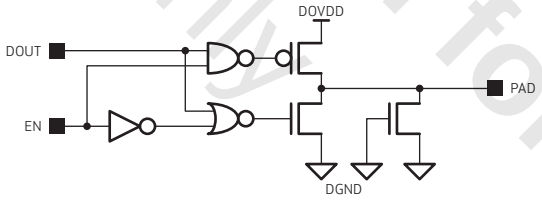
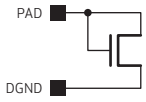
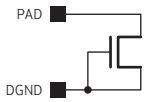
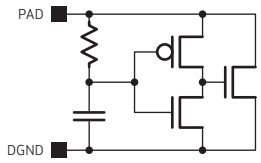
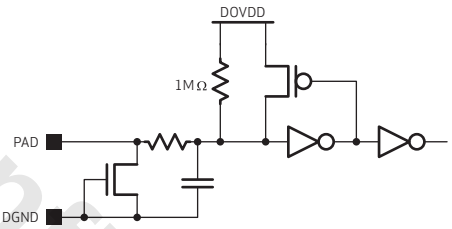
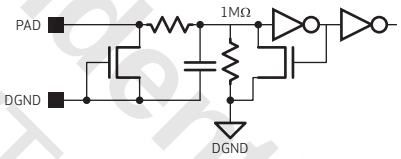
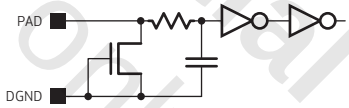
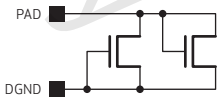
signal name	equivalent circuit
XVCLK	
SDA	
SCL	
VSYNC, FSIN, GPIO0~GPIO2, PCLK, HREF, D0~D11, ERRB	
VM_ERRB	
VN1, VN2	
ATEST, MDP2, MDN2, MDP0, MDN0, MCP, MCN, MDP1, MDN1, MDP3, MDN3, DVDD_SNS, VH1, VH2, DGND	

table 1-3 pad equivalent circuit (sheet 2 of 2)

signal name	equivalent circuit
AVDD, DVDD, DOVDD	
RESETB	
TM	
SID	
AGND	

1.3 I/O control

The OX03C10 can configure its I/O pins as an input or output. This is only applicable when operating in MIPI mode, as all the configurable pins, except for PCLK, HREF, D0, and D1 will be used by the DVP interface in DVP mode. For the output signal, it follows one of two paths; either from the data path or from register control.

table 1-4 GPIO control registers

signal	IO_PAD_OEN[a]	IO_PAD_OUT_SEL[b]	IO_PAD_OUT_VAL[c]	IO_PAD_IEN[d]	IO_PAD_IN_VAL (RO)[e]
FSIN	0x3002[1]	0x3008[1]	0x3005[1]	0x3015[1]	0x303F[1]
VSYNC	0x3002[2]	0x3008[2]	0x3005[2]	0x3015[2]	0x303F[2]
GPIO0	0x3002[4]	0x3008[4]	0x3005[4]	0x3015[4]	0x303F[4]
GPIO1	0x3002[5]	0x3008[5]	0x3005[5]	0x3015[5]	0x303F[5]
GPIO2	0x3002[6]	0x3008[6]	0x3005[6]	0x3015[6]	0x303F[6]
GPIO3/PCLK	0x3002[7]	0x3008[7]	0x3005[7]	0x3015[7]	0x303F[7]
GPIO4/HREF	0x3001[0]	0x3007[0]	0x3004[0]	0x3014[0]	0x303E[0]
GPIO5/D0	0x3001[1]	0x3007[1]	0x3004[1]	0x3014[1]	0x303E[1]
GPIO6/D1	0x3001[2]	0x3007[2]	0x3004[2]	0x3014[2]	0x303E[2]

a. output enable

b. set bit to 1 for GPIO, set bit to 0 for data path

c. output value

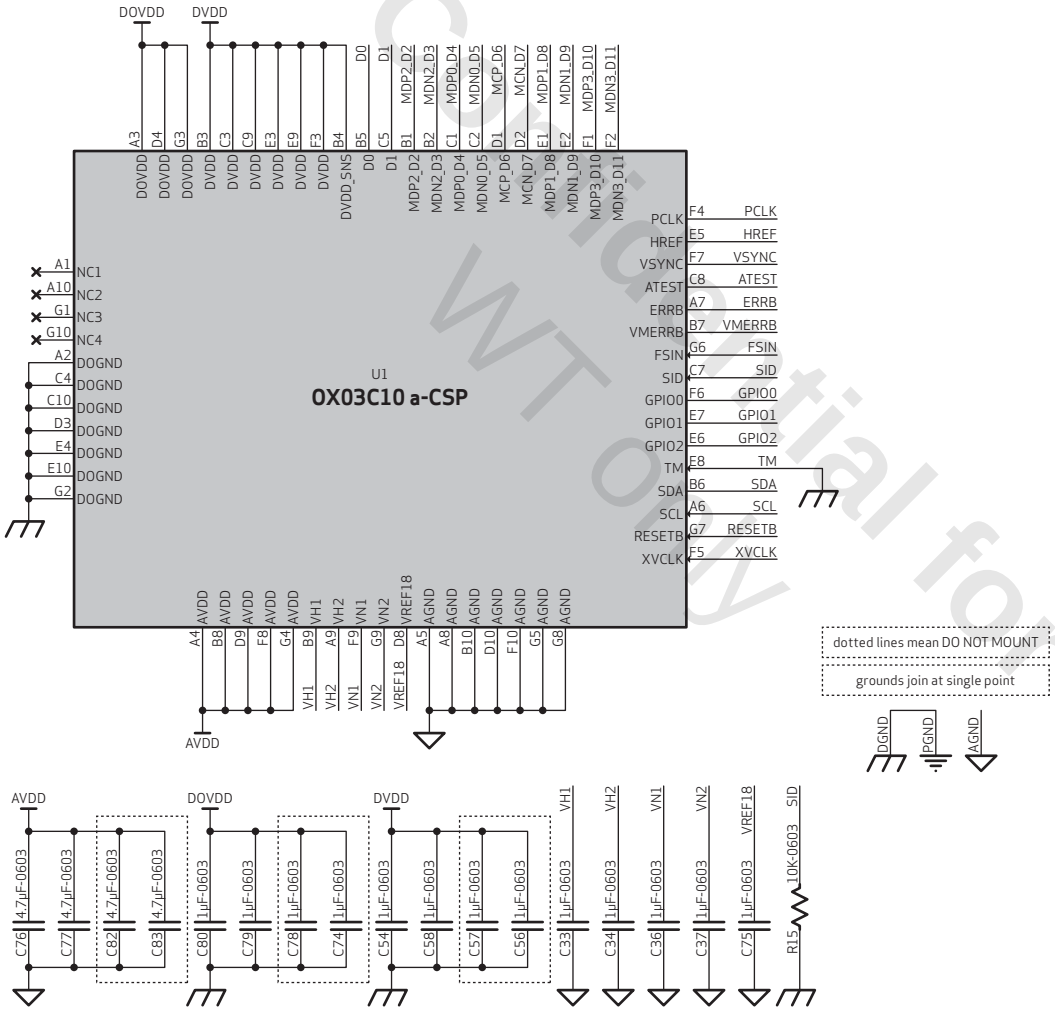
d. input enable (high: configure pad as input pad)

e. read only registers; when IO_PAD_IEN = 1, IO_PAD_IN_VAL indicates measurement of input value

1.4 reference design

figure 1-4 shows the power supply and signal connection of the OX03C10. The silicon (chip) revision of the sensor can be read from register 0x302A. The SCCB ID of the sensor is controlled by the SID pin at power up and after hardware reset (RESETB pin low). If SID is low, the sensor's default SCCB ID is 0x6C. If SID is high, the sensor's default SCCB ID is 0x20. Those two ID values are stored and correspond to two registers 0x3035 (SID = '0') and 0x3037 (SID = '1'). They can be changed either by SCCB command or by an OTP command, thus allowing the ID of the sensor to be altered arbitrarily. The SID pin cannot be left floating and either should be pulled or tied to GND or DOVDD. TM pin must be tied to GND.

figure 1-4 OX03C10 reference schematic



1.4.1 external components

The pixel array and analog readout circuits are powered from 2.9V (AVDD). The I/O pad power supply voltage level is 1.8V or optionally 3.3V (DOVDD). The digital core logic and the MIPI core logic operate on 1.1V (DVDD) power supply.

The OX03C10 must use external power de-coupling capacitors to reduce noise on the supply lines and for proper operation of its reference voltages. These de-coupling capacitors should be connected as close as possible to the different power supply pins of the chip. For the core power supplies, a nominal capacitance of >1 µF is recommended. A minimum capacitance of 1 µF should be used for the output pins from the reference voltages VH1, VH2, VREF18, VN1, and VN2. At power up, the power supplies should ramp up in 50 µs or more to avoid in-rush current during ramp-up.

1.4.2 power management

Power supplies can be turned on in any sequence without causing damage to the chip. This also applies to powering down the chip. When powering up the sensor, it is recommended to assert the RESETB pin low, until the voltage supplies levels rise to stable nominal values. In order to conserve power to the fullest, the sensor could be shut down completely by asserting the RESETB pin to GND.

When AVDD voltage is lower than DOVDD and the impedance on AVDD is low, there could be a large current spike from DOVDD towards AVDD. This is most significant during the power up stage, so ensure that AVDD is always up earlier than DOVDD.

1.4.3 reset

The whole chip will be reset during power up.

1.4.4 power on reset (POR) generation

Reset can be controlled from the external pin. However, inside this chip, there is a power on reset generation circuit that will generate an internal reset pulse when supplies are applied. As the POR does not detect absolute voltage levels, it is recommended to keep the RESETB pin asserted low during power up in order to avoid issues with improper reset with very slow rise time on the supplies

1.4.5 software reset

When register 0x0103[0] is configured as 1, all registers are reset to default values, but OTP data is not loaded.

1.4.6 software reset to hardware standby

When register 0x0107[0] is configured as 1, the sensor is brought to hardware standby, all registers are reset to default values, and the sensor will go through startup state before entering software standby. This will enable OTP configuration to be automatically reloaded.

1.5 power management

1.5.1 power up sequence/ boot sequence

When power is applied to the chip, the POR module resets the chip by generating an internal reset pulse. That pulse will last for approximately t1, during which the voltage supplies are expected to have reached nominal stable levels. After this period, the POR will be released and the sensor will begin its operation. If it takes longer than t1 for supplies to reach minimum operating voltage, the sensor may not be reset correctly by POR. This is more critical for DVDD. Holding RESETB low until all supplies settle is required in this case. Upon RESETB release, a delay of t2 = 6 ms (@ 24 MHz

XVCLK) is required for system internal start up (ROM load, OTP load, MBIST, etc.). The chip will then enter software standby state.

The EERB pin will be held low until after the end of the first frame when all safety checks have been run at least once. If an error occurs during start up phase, the EERB pin will stay low at the end of the first frame.

T2 starts from RESETB going high or when XVCLK is present, whichever is last, entering the start-up state. The XVCLK must be stable before reset mode is released since reset mode release is clocked by XVCLK. When it is finished, the software standby state is reached and the sensor can be programmed over SCCB. It is important to mention that for any SCCB communication to be valid, the sensor must have passed the start up stage (t2 period must have passed).

figure 1-5 power up sequence timing diagram

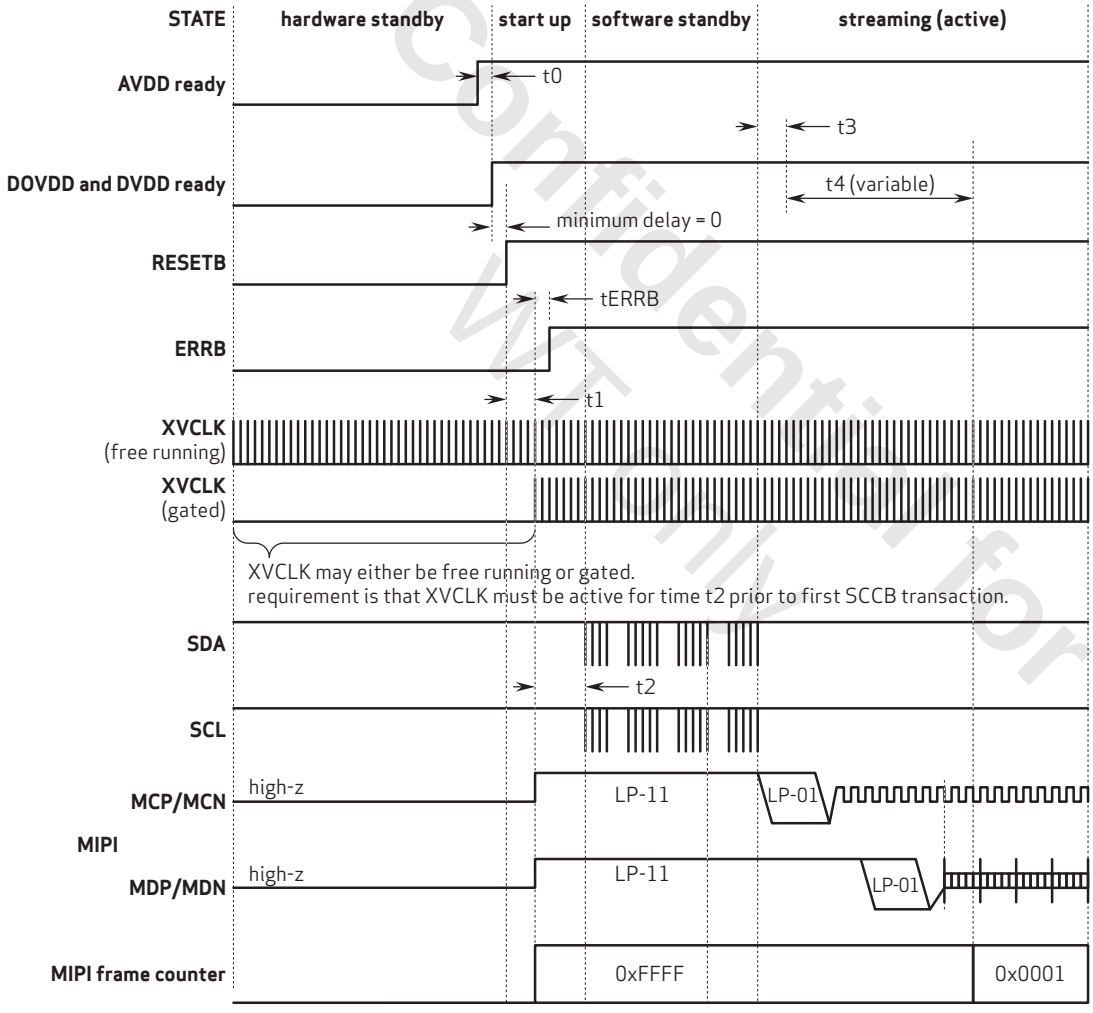


table 1-5 power up sequence timing restraints[a]

constraint	label	min	max	unit
delay period for applying rest of supplies, after AVDD is stable	t0	>0		µs
RESETB rising - system ready	t1		0.5	ms
ERRB pin rise time	tERRB		1	ms
start-up delay prior to first SCCB transaction, SCCB unreliable during this period, wait until it ends to issue SCCB commands	t2[b]	6[c]		ms
entering streaming mode - first frame start sequence (fixed part)	t3[d]	0.7[c]		ms
entering streaming mode - first frame start sequence (variable part)	t4	delay is exposure time value		lines

a. if not used, tie RESETB to DOVDD via pull-up resistor

b. t2 (ms) = 144 / XVCLK (MHz)

c. with 24MHz XVCLK

d. t3 (ms) = 16.4 / XVCLK (MHz)

1.5.2 power down sequence

When in software standby, hardware standby can be entered by pulling RESETB pin low. In order to avoid corrupted frames from the MIPI, it is recommended to use group hold to send the sleep (software standby) SCCB command before exerting the hardware standby to sensor. Any power cut is equivalent to RESETB being driven low.

figure 1-6 software standby sequence

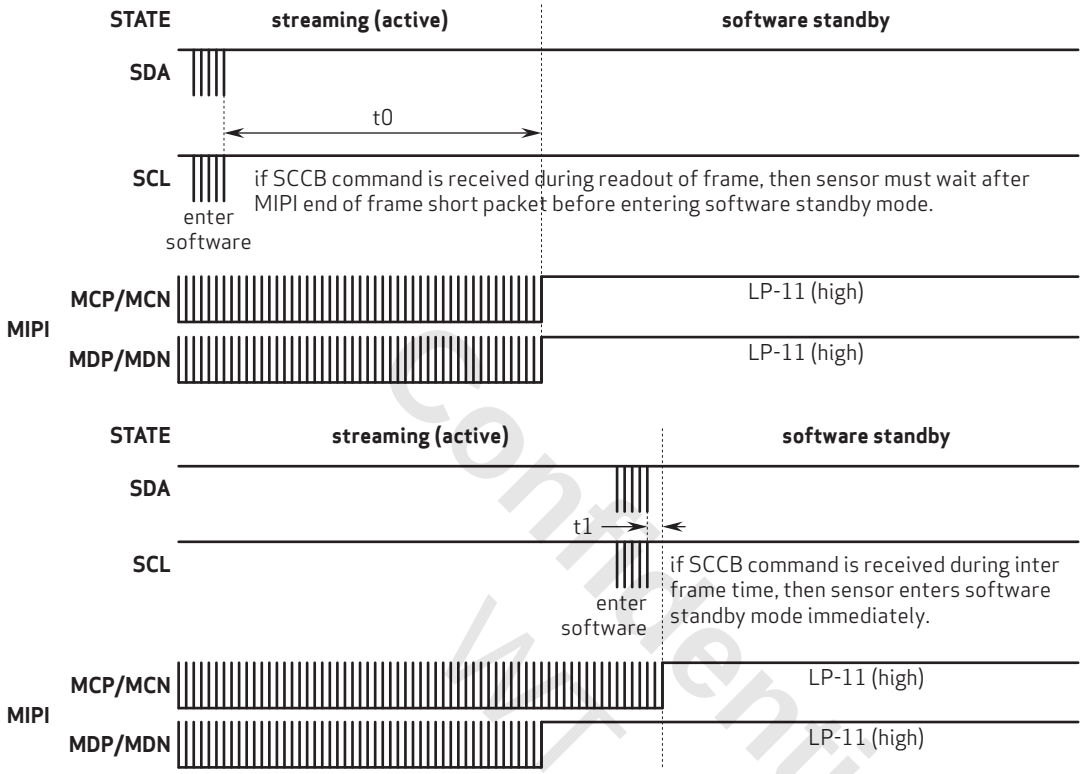


figure 1-7 power down sequence

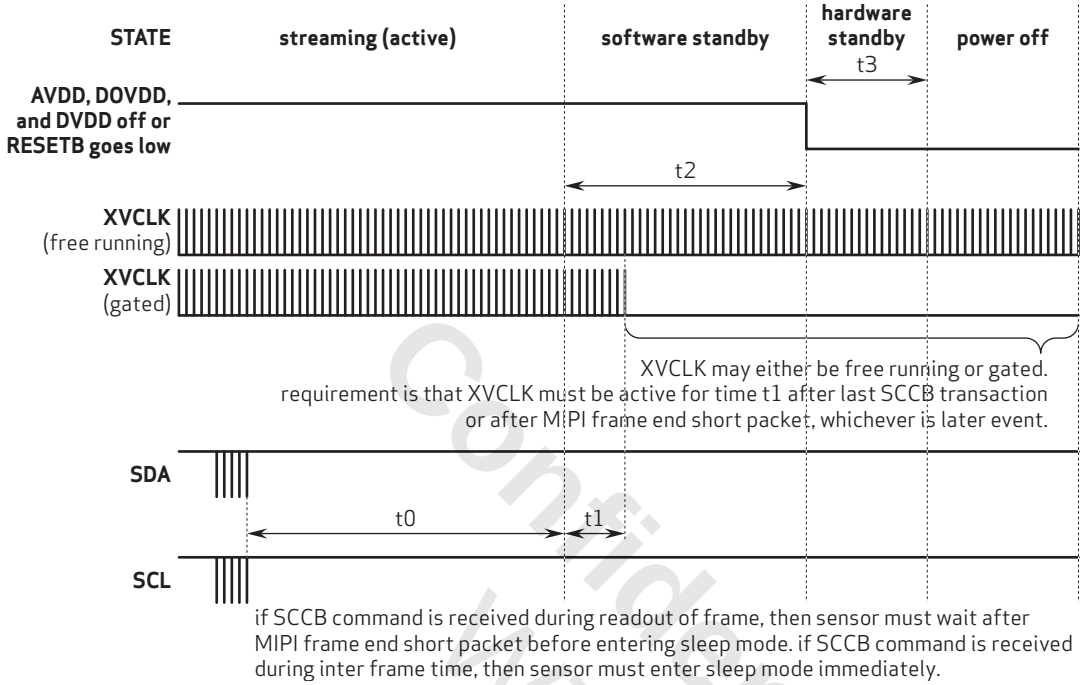


table 1-6 power down sequence timing constraints

constraint	label	min	max	unit
enter software standby SCCB command device in software standby mode	t0	when a frame of MIPI data is output, wait for MIPI end code before entering software for standby; otherwise, enter software standby mode immediately		
minimum of XVCLK cycles after last SCCB transaction or MIPI frame end	t1	512		XVCLK cycles
last SCCB transaction or MIPI frame end, RESETB falling	t2	512		XVCLK cycles
RESETB falling – AVDD falling or DOVDD falling whichever is first	t3	0.0		ns

1.6 hardware and software standby

Two suspend modes are available for the OX03C10:

- hardware standby
- software standby

1.6.1 hardware standby

If RESETB is tied low, hardware standby mode will be initiated.

1.6.2 software standby

Executing a software standby (0x0100[0]) through the SCCB interface suspends internal circuit activity, but does not halt the device clock. All register content is maintained in standby mode. During the resume state, all the registers are restored to their original values.

table 1-7 hardware and standby description

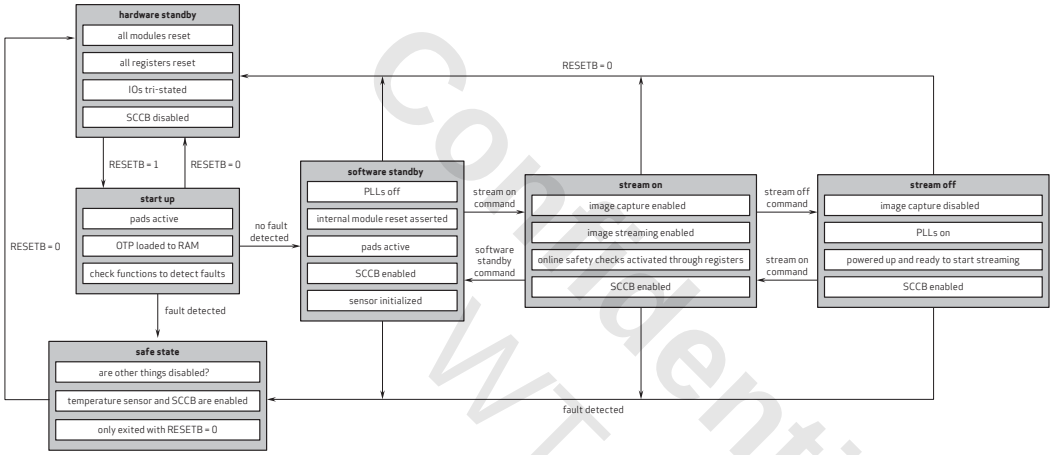
mode	description
hardware standby with RESETB	1. Enabled by pulling RESTB low or through software reset 2. Register values are reset to default values 3. No SCCB communication 4. Low power consumption
software standby	1. Default mode after power on reset 2. Power down all blocks except SCCB 3. Register values are maintained 4. SCCB communication is available 5. Low power consumption

1.7 operating modes

A software reset is required to reset all registers back to their default values. Set register 0x0103[0] and the sensor will be in standby mode after the software reset. It is highly recommended to wait 10 ms before programming other registers after a software reset. To perform a software reset and automatically reload OTP configuration, set register 0x0107[0]. The sensor will enter hardware standby and go through the start-up state before entering software standby.

The OX03C10 supports the following operating modes as depicted in **figure 1-8**.

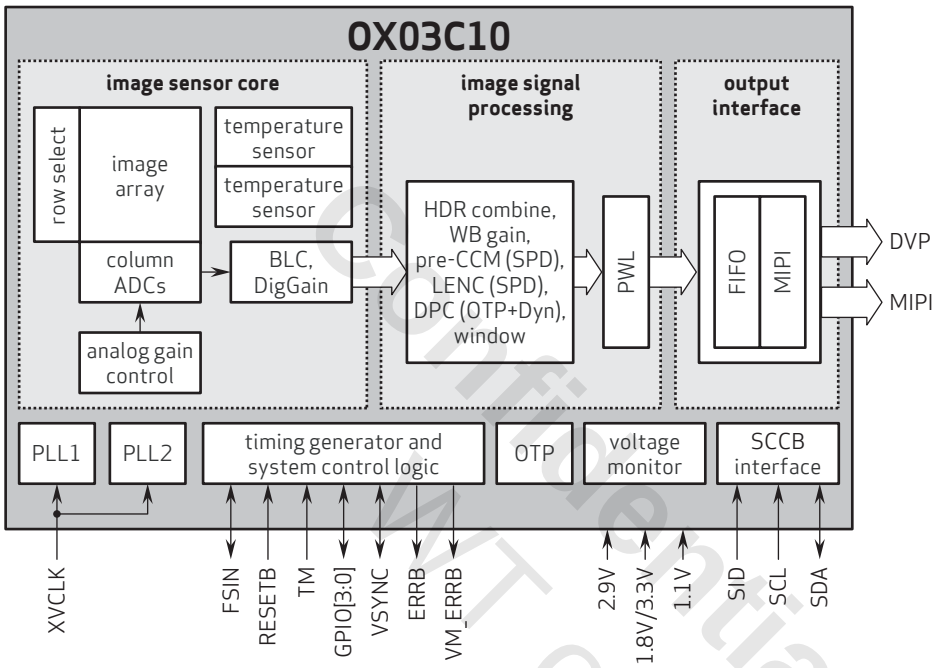
figure 1-8 operating mode state diagram



2 sensor architecture

figure 2-1 shows the top level block diagram of the OX03C10 sensor.

figure 2-1 OX03C10 block diagram



The sensor consists of three major functional blocks: image sensor core, image signal processor (ISP), and output interface.

The image sensor core receives the photo signal, which generates electrical charge collected by the pixel photo diodes (PDs). During readout, the accumulated charge is converted to a voltage signal in the pixel. This signal is then amplified and converted to a digital signal by the analog-to-digital converter (ADC). Dark current and circuit offsets are compensated by the black level correction circuit (BLC). The correction is implemented purely in the digital domain. Dark current increases exponentially with temperature and the BLC can be configured to automatically re-trigger with changes in exposure, output format, applied gain, and out of range offsets, in addition to manually triggering it. A temperature sensor is integrated in the image sensor core.

The OX03C10 supports dual conversion gain (DCG) HDR, which means switchable two conversion gain (CG) in one exposure (integration time) – low conversion gain (LCG) for large charge handling capacity in bright scenes and a high conversion gain (HCG) mode with increased sensitivity and low read noise for low-light scenes. Higher CG means higher sensitivity, as one signal electron can be more easily detected. Higher CG also means that the sensor will realize a reduction in read noise. Each pixel consists of a large and small PD. The large PD (LPD) is used for longer exposure with DCG and very short exposure (VS) using LCG, whereas the small PD (SPD) enables capture with lower light sensitivity.

The sensor core supports two main output modes of captures (CAPT1, CAPT2, CAPT3, CAPT4) that can be used to process a high dynamic range (HDR) image. The first mode consists of triple exposure staggered HDR with LPD and split pixel readout (i.e., HCG (LPD), LCG (LPD), VS (LPD) and SPD with on-chip HDR combination and LFM support for 140 dB (24-bit) through the ISP). The alternative mode consists of dual exposure with a staggered exposure of HCG, LCG, and VS, and can output on-chip HDR combination with LFM support for 120 dB (20-bit) image.

table 2-1 capture channels for both HDR operating modes[a]

capture name	triple exposure staggered HDR (HDR4)	dual exposure staggered HDR (HDR3)
capture 1 (CAPT1)	HCG (LPD)	HCG (LPD)
capture 2 (CAPT2)	LCG (LPD)	LCG (LPD)
capture 3 (CAPT3)	SPD	VS (LPD)
capture 4 (CAPT4)	VS (LPD)	–

a. HDR operating mode can only be changed while in software standby mode

The ISP also supports lens correction of SPD (LENC) and defect pixel correction (DPC). The processed linear and combined HDR image is formatted and output either through the MIPI interface or digital video port (DVP) interface. Two on-chip phase lock loops (PLLs) generate the required clock signals for all blocks from the XVCLK input clock. The timing generator generates the control signals for the pixel array to reset the PD at the beginning of the exposure, to stop the exposure by reading out the accumulated charge, and also to generate the required control timing for the readout amplifier and ADC. The sensor provides reference signals as vertical synchronization (VSYNC) and pixel clock (PCLK) that are internally generated and propagated outwards, so the backend processor could infer the general state of the sensor and the received image data stream. Complemented with the help of frame synchronization input (FSIN), the sensor can be synced and utilized in multi-camera application. In DVP mode, the horizontal synchronization reference (HREF), vertical synchronization (VSYNC), and pixel clock (PCLK) signals are also generated so the backend processor can receive the image data.

As a safety feature, the OX03C10 is also equipped with an error signal (ERRB) for indicating to the application processor or any other external device, the transition of the sensor into safe state mode, if a fault is detected.

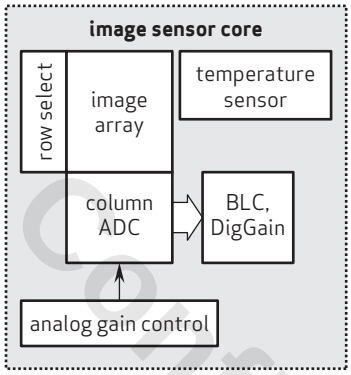
The one-time programmable (OTP) memory contains the DPC value and temperature offset value, etc.

All functional blocks are controlled by registers. The host controller can program and read back through the SCCB interface.

3 image sensor core

figure 3-1 shows the top level block diagram of the OX03C10 image sensor core.

figure 3-1 sensor core block diagram



The image sensor core consists of the active pixel array, row access control circuit, column parallel analog-to-digital converter (ADC) with gain control, and analog readout channel. A single analog readout channel is used for processing of the four capture channels (HCG, LCG, SPD, and VS). This provides optimal matching between the capture channels. Digital gain and BLC are implemented in the digital domain.

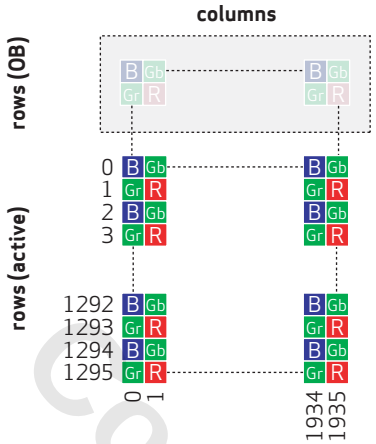
3.1 pixel array structure

The OX03C10 sensor, in total, has an image array of 1936 columns by 1296 rows (with an active image array of 1920x1280 contained within) covered with color filters arranged in a CFA (B-Gb-Gr-R) pattern. **figure 3-2** shows the pixel array color filter layout. In addition to the active pixel rows, optical black (OB) pixel rows are embedded to serve as reference pixels for the black level correction (BLC). The OB rows are covered with a light shield (solid metal layer). In order to minimize non-ideal edge effects in the output image, it is not recommended to use the pixels at the lowest and highest row and column addresses.

The entire readable column is 1920 active columns + 8 active border columns (image quality guarantee) + 8 dummy active border columns (no image quality guarantee) = 1936 columns.

The entire readable row is 1280 active rows + 8 active border rows (image quality guarantee) + 8 dummy active border rows (no image quality guarantee) = 1296 rows.

figure 3-2 pixel array region color filter layout



Each pixel has two photo diodes (PDs) with independent exposure and gain controls to extend the dynamic range. The two PDs also have different sizes to provide different sensitivity. The large PD (LPD) provides high sensitivity and the small PD (SPD) provides low sensitivity. Additionally, the LPD has two switchable conversion gains (CG) to extend the dynamic range. Higher CG (HCG) gives higher sensitivity, as one signal electron can be more easily detected, while low CG (LCG) results in lower sensitivity. The OX03C10 supports dual and triple exposure with up to four capture readouts (depending on the internal HDR operation mode):

Triple exposure staggered HDR (24-bit HDR4):

- T_{DCG}: exposure of the large photodiode (LPD) with HCG for first capture (CAPT1) and LCG for second capture (CAPT2)
- T_{SPD}: exposure of small photodiode (SPD) for third capture (CAPT3) with an exposure time larger, equal, or less than LPD exposure
- T_{VS}: very short exposure of LPD with LCG for fourth capture (CAPT4)

Dual exposure staggered HDR (20-bit HDR3):

- T_{DCG}: exposure of LPD with HCG for first capture (CAPT1) and LCG for second capture (CAPT2)
- T_{VS}: very short exposure of LPD with LCG for third capture (CAPT3)

The integration time for VS (T_{VS}) will always start after (T_{DCG}) finish. The sampling point of VS capture can either be fixed relative to DCG sampling (i.e., exposure time of VS capture will vary in relation to VS sampling) or the start of VS exposure can be fixed to be one row after the DCG sampling point (i.e., VS sampling point is [VS exposure time in rows + 1] rows after sampling of DCG).

figure 3-3 integration time diagram for triple exposure staggered HDR mode

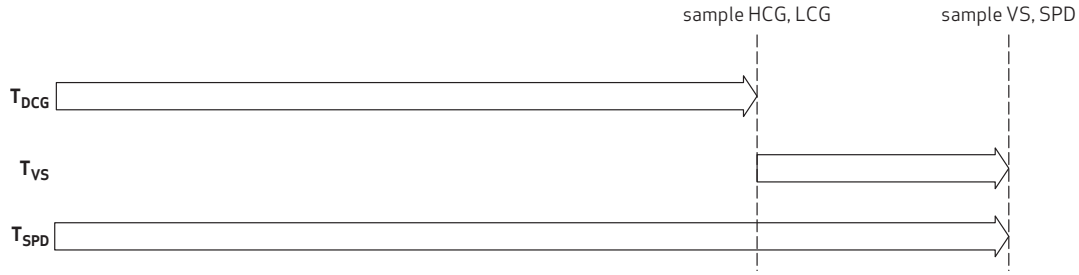
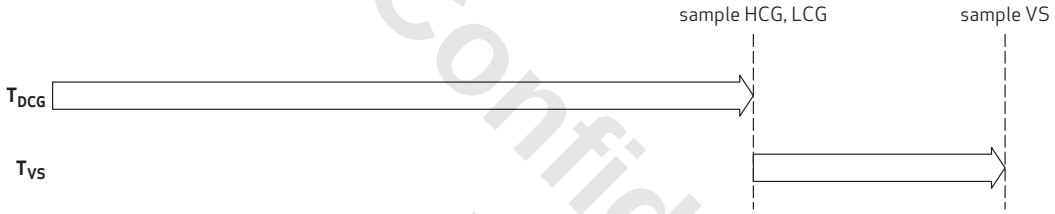


figure 3-4 integration time diagram for dual exposure staggered HDR mode



3.2 pixel array access

The readout image array size is fully programmable from 640 to 1936 in steps of 16 in the horizontal direction and from 20 to 1296 in steps of two in the vertical direction. Start address must be at an even row and column. End address must be at an odd row and column address in order to preserve the CFA pattern order. It represents the image array area that will be sampled and is defined by four 'crop' parameters - horizontal start (X_ADDR_START) {0x3800, 0x3801}, horizontal end (X_ADDR_END) {0x3804, 0x3805}, vertical start (Y_ADDR_START) {0x3802, 0x3803}, and vertical end (Y_ADDR_END) {0x3806, 0x3807}.

By properly setting the previously mentioned parameters, any portion within the sensor array size can be output as a visible area. This kind of windowing is achieved by masking off the pixels outside of the output window; thus, the original timing is not affected. The 'output window' is defined by an initial 'offset' from the 'crop' window, set in both horizontal (ISP_X_WIN_TRUNC) {0x3810, 0x3811} and vertical (ISP_Y_WIN_TRUNC) {0x3812, 0x3813} directions. Also, the actual image 'window size', that will be sent out, is specified in width (X_OUTPUT_SIZE) {0x3808, 0x3809} and height (Y_OUTPUT_SIZE) {0x380A, 0x380B}. The offset address should always be an even number, while the output end address should always be an odd number.

The 'crop' window is programmed larger than the processed output image resolution because the ISP uses extra rows and columns for the image processing algorithms (e.g., defect pixel correction). Also, if the embedded rows are enabled, the 'crop' window vertical size needs to be increased manually, depending on the number of these rows that have been enabled. These non-image array rows will increase the 'output window' vertical size automatically when enabled, so the user does not need to adjust that parameter in the sensor. Only the receiver needs to accommodate the extra window height produced as a result.

figure 3-5 pixel array access diagram

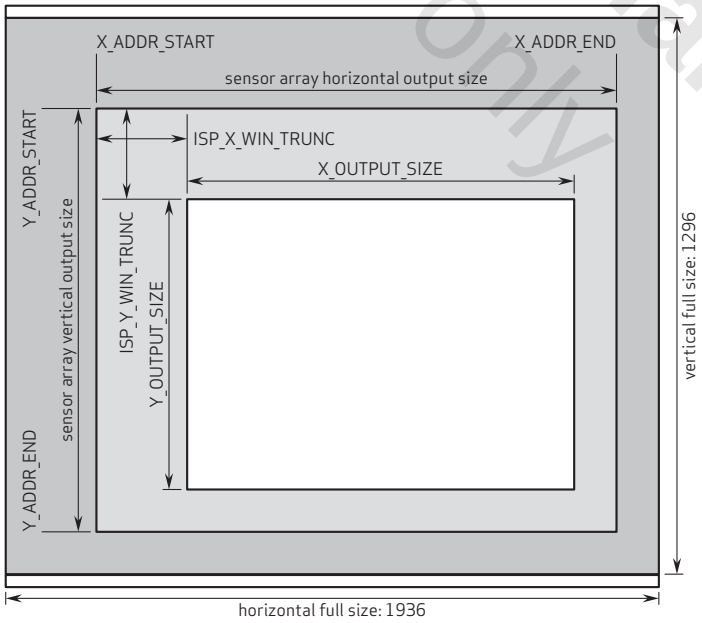


table 3-1 timing control registers

address	register name	default value	RW	description
0x3800	X_ADDR_START_H	0x00	RW	Bit[7:0]: Horizontal start address[15:8]
0x3801	X_ADDR_START_L	0x00	RW	Bit[7:0]: Horizontal start address[7:0]
0x3802	Y_ADDR_START_H	0x00	RW	Bit[7:0]: Vertical start address[15:8]
0x3803	Y_ADDR_START_L	0x04	RW	Bit[7:0]: Vertical start address[7:0]
0x3804	X_ADDR_END_H	0x07	RW	Bit[7:0]: Horizontal end address[15:8]
0x3805	X_ADDR_END_L	0x9F	RW	Bit[7:0]: Horizontal end address[7:0]
0x3806	Y_ADDR_END_H	0x05	RW	Bit[7:0]: Vertical end address[15:8]
0x3807	Y_ADDR_END_L	0x0B	RW	Bit[7:0]: Vertical end address[7:0]
0x3808	X_OUTPUT_SIZE_H	0x07	RW	Bit[7:0]: Horizontal output size for final image[15:8]
0x3809	X_OUTPUT_SIZE_L	0x80	RW	Bit[7:0]: Horizontal output size for final image[7:0]
0x380A	Y_OUTPUT_SIZE_H	0x05	RW	Bit[7:0]: Vertical output size for final image[15:8]
0x380B	Y_OUTPUT_SIZE_L	0x00	RW	Bit[7:0]: Vertical output size for final image[7:0]
0x3810	ISP_X_WIN_TRUNC_H	0x00	RW	Bit[7:0]: Number of pixels to be cut off at horizontal beginning of image[15:8]
0x3811	ISP_X_WIN_TRUNC_L	0x08	RW	Bit[7:0]: Number of pixels to be cut off at horizontal beginning of image[7:0]
0x3812	ISP_Y_WIN_TRUNC_H	0x00	RW	Bit[7:0]: Number of rows to be cut off at vertical beginning of image[15:8]
0x3813	ISP_Y_WIN_TRUNC_L	0x04	RW	Bit[7:0]: Number of rows to be cut off at vertical beginning of image[7:0]

3.3 mirror and flip

The pixel array can be accessed in reverse order in column and row directions (i.e., image can be horizontally mirrored and vertically flipped) (see **figure 3-6**). Image flip is controlled by setting or clearing register bit 0x3820[2]. Mirror is controlled by register 0x3820[5]. The image mirror and flip setting is shown in **table 3-2**. The sensor needs to be in standby mode when configuring mirror or flip.

The sensor provides an option (register bit 0x6A09[0] = 1) to maintain CFA pattern when implementing mirror.

figure 3-6 horizontal mirror and vertical flip samples

original image | mirrored image | flipped image | mirrored and flipped image

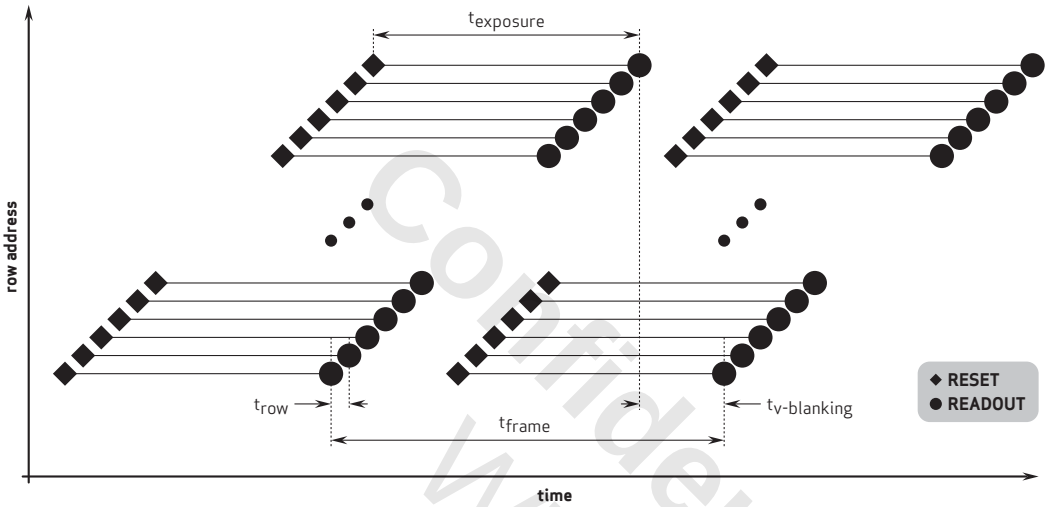
table 3-2 mirror and flip control registers

address	register name	default value	R/W	description
0x3820	TIMING_CTRL_REG_20	0x00	RW	Bit[5]: Horizontal mirror enable Bit[2]: Image lines flip enable

3.4 frame timing and maximum frame rate

The OX03C10 employs an electronic rolling shutter (ERS) for exposure control (see **figure 3-7**). The pixel array is first reset row by row and when the exposure time has elapsed, the readout of the pixel array is done row by row.

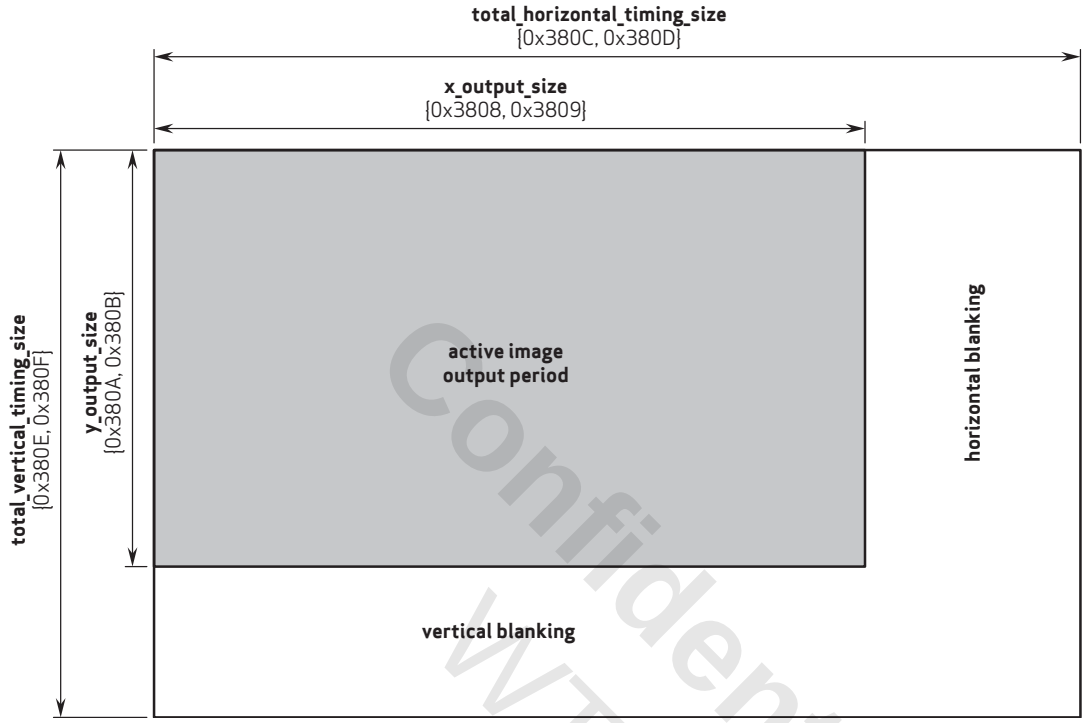
figure 3-7 row address versus time graph



The timing generator generates all the control signals based on a row counter and column counter. Refer to **figure 3-8** for frame timing. The row period consists of an active output period and a horizontal blanking period. A vertical blanking period is also required to perform frame-based operation. The vertical blanking period seen by the backend processor is usually longer than the internal vertical blanking because the BLC is reading the optical black rows required to perform the correction.

A minimum number of clock periods are required to complete all the required operations per row (blanking time).

figure 3-8 frame output timing diagram



The maximum frame rate is determined by the maximum pixel clock, total number of pixels read out of the entire frame, and minimum horizontal/vertical blanking time. The system clock and the minimum blanking time are usually fixed for a given design and the frame rate is dependent on the number of pixels read out. If the requested output image size (ISP window size) is smaller than the maximum supported pixel array size, the frame rate can be increased by cropping the pixel array (see **figure 3-5**). **table 3-3** and **table 3-4** list the most common image sizes and maximum frame rates that the sensor can achieve. Other image sizes are also possible by cropping. Please refer to **section 6** for details. The maximum MIPI bitrate for the combined MIPI/DVP interface is limited to 1200 Mbps/lane, which will limit the frame rate for some of the output formats.

table 3-3 supported output formats and frame rates for MIPI

maximum frame rate supported via MIPI interface				
format		resolution (HxV)	maximum frame rate	min/typ/max MIPI bitrate (Mbps/lane)
4x10b	non-combined HDR	1920x1280	30 fps	970/–/1200
HDR4 COMB/COMB-PWL	uncompressed 24-bit	1920x1280	60 fps	1100/–/1200
	20/16/14/12-bit (PWL) combined HDR	1920x1280	60 fps	920/730/640/ 550/–/1200
HDR4_LFM COMB/COMB-PWL	uncompressed 24-bit	1920x1280	55 fps	1160/–/1200
	20/16/14/12-bit (PWL) combined HDR+LFM bit[a]	1920x1280	60 fps	1070/880/780/ 680/–/1200
HDR4_SPD COMB/COMB-PWL	uncompressed 24-bit	1920x1280	40 fps	1100/–/1200
	20/16/14/12-bit (PWL) combined HDR+10-bit SPD[b]	1920x1280	47/55/60/ 60 fps	1140/1160/1170/ 1070/–/1200
HDR3 COMB/COMB-PWL	uncompressed 20-bit	1920x1280	60 fps	920/–/1200
	16/14/12-bit (PWL) combined HDR	1920x1280	60 fps	730/640/ 550/–/1200
HDR3_LFM COMB/COMB-PWL	uncompressed 20-bit	1920x1280	60 fps	1070/–/1200
	16/14/12-bit (PWL) combined HDR+LFM bit[a]	1920x1280	60 fps	880/780/ 680/–/1200
HDR3_SPD COMB/COMB-PWL	uncompressed 20-bit	1920x1280	47 fps	1140/–/1200
	16/14/12-bit (PWL) combined HDR+10-bit SPD[b]	1920x1280	55/60/60 fps	1160/1170/ 1070/–/1200

a. LFM bits packed in MIPI RAW 8b format on separate VC

b. 10-bit SPD output on separate VC can optionally include LFM bit packed as {LFM[9:2], LFM_bit, 0}

table 3-4 supported output formats and frame rates for DVP

maximum frame rate supported via DVP (12-bit) interface				
format		resolution (HxV)	maximum frame rate	min/typ/max PCLK (MHz)
HDR4 COMB-PWL	12-bit (PWL) combined HDR	1920x1280	30 fps	80/–/100
HDR3 COMB-PWL	12-bit (PWL) combined HDR	1920x1280	30 fps	68/–/100

3.5 exposure and gain control

The OX03C10 supports up to three exposures: DCG (HCG, LCG), SPD, and VS. Their exposure time can be set manually by registers (see **table 3-6**):

- minimum value for DCG, SPD = 2, VS expo = 0.5 (in double row time, which means 1 double row time = 2 rows)
- maximum exposure value depends on HDR operating mode:
  - HDR4 mode:
    Max (DCG_exp + VS_exp, SPD_exp) < VTS - 12
    VS_exp_max < 35
  - HDR3 mode:
    DCG_exp + VS_exp_max < VTS - 12
    VS_exp_max < 35

Minimum exposure change step for all exposures: 1 (in double row time)

- {0x3501, 0x3502} for DCG exposure time
- {0x3541, 0x3542} for SPD exposure time
- {0x35C1, 0x35C2} for VS exposure time

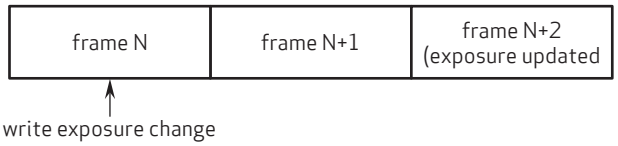
All exposure time values are represented in units of double row time:

$$\text{row time} = \frac{\text{HTS}}{\text{SCLK}}$$

where SCLK is the system (core) clock frequency (Hz) and HTS is the horizontal timing size (number of SCLK cycles), which is separated for DCG {0x380C, 0x380D}, SPD {0x384C, 0x384D}, and VS {0x388C, 0x388D} exposures. The total HTS value {0x386E, 0x386F} depends on the operating mode. The value will contain the sum of the HTS parts for the exposures that are currently active, e.g., in HDR3 mode, only the HTS value of DCG and VS will be included (i.e., HTS = HTS_DCG + HTS_VS).

The exposure control is double frame-synced, which means that a change in the setting of the current frame (N) will take place. The actual exposure will change on the second frame after (at N+2). This period is fixed and cannot be adjusted.

figure 3-9 exposure control timing



The analog gain for the OX03C10, referred to as real gain, can be set individually for each exposure channel and consists of two bytes. It follows 4.4 bits format, where the lower 4b of the first byte represent an integer value. While the upper 4b of the second (consecutive) byte represent the fractional part (units of 1/16). The value range of the analog gain is 1.0x ~ 15.5x. The resolution of the fractional part decreases as the gain value increases (see **table 3-5** for details).

The digital gain for the OX03C10 can also be set individually for each capture and it consists of three bytes. It follows 4.10 bits format, where the first 4b are held in the lower nibble of the first byte and represent an integer value. While the

10b represent the fractional part (units of 1/1024) and are distributed across the next two bytes in consecutive order with the MSB held in the second byte and the remaining two bits contained in the higher bits of the last byte. The value range of the digital gain is 1.000x~15.999x, where the maximum value needs to be set to 1 across all the valid bits.

table 3-5 analog gain resolution

real gain range	fractional resolution	min gain step	real gain bits
1.0000 ~1.9375	1/16	0.0625	0001.xxxx
2.000 ~ 3.875	1/8	0.125	001x.xxx0
4.00 ~ 7.75	1/4	0.25	01xx.xx00
8.0 ~ 15.5	1/2	0.5	1xxx.x000

table 3-6 exposure and gain control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3501	AEC_HCG_CTRL_01	0x00	RW	Bit[7:0]: Exposure[15:8] Exposure in unit of rows
0x3502	AEC_HCG_CTRL_02	0x08	RW	Bit[7:0]: Exposure[7:0] Exposure in unit of rows
0x3508	AEC_HCG_CTRL_08	0x01	RW	Bit[3:0]: Real gain[7:4]
0x3509	AEC_HCG_CTRL_09	0x00	RW	Bit[7:4]: Real gain[3:0]
0x350A	AEC_HCG_CTRL_0A	0x01	RW	Bit[3:0]: Digital gain[13:10]
0x350B	AEC_HCG_CTRL_0B	0x00	RW	Bit[7:0]: Digital gain[9:2]
0x350C	AEC_HCG_CTRL_OC	0x00	RW	Bit[7:6]: Digital gain[1:0]
0x3541	AEC_SPD_CTRL_01	0x00	RW	Bit[7:0]: Exposure[15:8] Exposure in unit of rows
0x3542	AEC_SPD_CTRL_02	0x04	RW	Bit[7:0]: Exposure[7:0] Exposure in unit of rows
0x3548	AEC_SPD_CTRL_08	0x01	RW	Bit[3:0]: Real gain[7:4]
0x3549	AEC_SPD_CTRL_09	0x00	RW	Bit[7:4]: Real gain[3:0]
0x354A	AEC_SPD_CTRL_0A	0x01	RW	Bit[3:0]: Digital gain[13:10]
0x354B	AEC_SPD_CTRL_0B	0x00	RW	Bit[7:0]: Digital gain[9:2]
0x354C	AEC_SPD_CTRL_OC	0x00	RW	Bit[7:6]: Digital gain[1:0]
0x3588	AEC_LCG_CTRL_08	0x01	RW	Bit[3:0]: Real gain[7:4]
0x3589	AEC_LCG_CTRL_09	0x00	RW	Bit[7:4]: Real gain[3:0]

table 3-6 exposure and gain control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x358A	AEC_LCG_CTRL_0A	0x01	RW	Bit[3:0]: Digital gain[13:10]
0x358B	AEC_LCG_CTRL_0B	0x00	RW	Bit[7:0]: Digital gain[9:2]
0x358C	AEC_LCG_CTRL_OC	0x00	RW	Bit[7:6]: Digital gain[1:0]
0x35C1	AEC_VS_CTRL_01	0x00	RW	Bit[7:0]: Exposure[15:8] Exposure in unit of rows
0x35C2	AEC_VS_CTRL_02	0x02	RW	Bit[7:0]: Exposure[7:0] Exposure in unit of rows
0x35C8	AEC_VS_CTRL_08	0x01	RW	Bit[3:0]: Real gain[7:4]
0x35C9	AEC_VS_CTRL_09	0x00	RW	Bit[7:4]: Real gain[3:0]
0x35CA	AEC_VS_CTRL_0A	0x01	RW	Bit[3:0]: Digital gain[13:10]
0x35CB	AEC_VS_CTRL_0B	0x00	RW	Bit[7:0]: Digital gain[9:2]
0x35CC	AEC_VS_CTRL_0C	0x00	RW	Bit[7:6]: Digital gain[1:0]
0x380C	HTS_DCG_H	0x04	RW	Bit[7:0]: Portion of row time used for long exposure control and readout, in units of SCLK cycles[15:8]
0x380D	HTS_DCG_L	0x24	RW	Bit[7:0]: Portion of row time used for long exposure control and readout, in units of SCLK cycles[7:0]
0x380E	VTS_H	0x02	RW	Bit[7:0]: Total number of rows per frame[15:8]
0x380F	VTS_L	0xAE	RW	Bit[7:0]: Total number of rows per frame[7:0]
0x384C	HTS_SPD_H	0x02	RW	Bit[7:0]: Portion of row time used for short exposure control and readout, in units of SCLK cycles[15:8]
0x384D	HTS_SPD_L	0x12	RW	Bit[7:0]: Portion of row time used for short exposure control and readout, in units of SCLK cycles[7:0]
0x388C	HTS_VS_H	0x02	RW	Bit[7:0]: Portion of row time used for very short exposure control and readout, in units of SCLK cycles[15:8]
0x388D	HTS_VS_L	0x12	RW	Bit[7:0]: Portion of row time used for very short exposure control and readout, in units of SCLK cycles[7:0]

3.6 black level calibration (BLC)

The pixel array contains several optically shielded (black) rows positioned at the lower side of the array. That section of the image matrix is used as reference for black level calibration. The main function of the BLC is to adjust all normal pixel values based on the values of the black levels.

table 3-7 BLC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4000	BLC_CTRL_0	0xF8	RW	Bit[7]: off_trig_en Enable triggering of BLC update after offset out of range Bit[6]: exp_chg_trig_en Enable triggering of BLC update after exposure changes Bit[5]: gain_chg_trig_en Enable triggering of BLC update after gain changes Bit[4]: fmt_chg_trig_en Enable triggering of BLC update after format changes Bit[3]: rst_trig_en Enable triggering of BLC update after reset release Bit[2]: Manual trigger BLC update Bit[1]: off_frz_en BLC update freeze Bit[0]: off_always_up BLC updates every frame
0x4001	BLC_CTRL_1	0x2B	RW	Bit[7]: zero_ln_out_en Enable of zero row output Bit[6]: blk_ln_out_en Enable of black row output Bit[5]: Dither function enable Bit[4]: off_man_en Use manual offset value for BL correction Bit[3]: Median filter enable Bit[2]: Zero banding correction (ZBC) enable Bit[1]: Dark current BLC function enable Bit[0]: BLC enable (MSB pass-through if disabled)
0x4026	BLK_LVL_TARGET_HCG_H	0x00	RW	Bit[1:0]: Black level target for HCG expo[9:8]
0x4027	BLK_LVL_TARGET_HCG_L	0x40	RW	Bit[7:0]: Black level target for HCG expo[7:0]

table 3-7 BLC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4028	BLK_LVL_TARGET_LCG_H	0x00	RW	Bit[1:0]: Black level target for LCG expo[9:8]
0x4029	BLK_LVL_TARGET_LCG_L	0x40	RW	Bit[7:0]: Black level target for LCG expo[7:0]
0x402A	BLK_LVL_TARGET_SPD_H	0x00	RW	Bit[1:0]: Black level target for SPD expo[9:8]
0x402B	BLK_LVL_TARGET_SPD_L	0x40	RW	Bit[7:0]: Black level target for SPD expo[7:0]
0x402C	BLK_LVL_TARGET_VS_H	0x00	RW	Bit[1:0]: Black level target for VS expo[9:8]
0x402D	BLK_LVL_TARGET_VS_L	0x40	RW	Bit[7:0]: Black level target for VS expo[7:0]

3.7 PLL

PLL settings can only be changed during sensor standby mode (0x0100 = 0).

The OX03C10 implements two PLLs with both inputs connected to the XVCLK pin. One can support the MIPI bit clock and output clock PCLK, while the other one can support internal SCLK. Having two PLLs enables the internal clock (SCLK) to be separate from the output clock (PCLK). Additionally, in MIPI mode, the two PLLs can be used to optimize for EMC and/or minimize the required MIPI frequency.

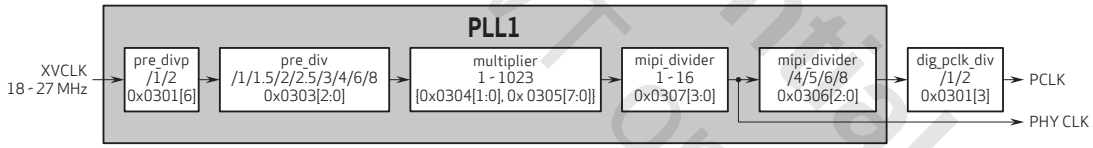
In order to reduce EMI's impact, this PLL also supports spread spectrum mode (SSM). Spread profile is a triangular waveform spread. The spectrum can be up spread, both side spread, or down spread depending on the input setting dsm[19:0]. Tssc is the modulation period. Fssc(1/Tssc) is the modulation frequency, which is about 30 kHz~33 kHz in many interface designs. DeltaF is modulation amplitude, which is normally smaller than 5000 ppm. For example, if normal clock frequency Fo = 1 GHz, then 5000 ppm = 5000 x Fo/1e6 = 5 MHz.

Maximum operating clock frequencies: SCLK = 90 MHz, PCLK = 75 MHz for MIPI mode and 100 MHz for DVP mode.

3.7.1 PLL1

The PLL1 generates a default (maximum) 75 MHz pixel clock (PCLK) and 1200 MHz MIPI serial clock from an 18~27 MHz input clock. The VCO range is from 1250 MHz to 2500 MHz. A programmable clock is provided to generate different frequencies.

figure 3-10 PLL1 control diagram



3.7.2 PLL2

The PLL2 generates a default 90 MHz system clock (SCLK) from an 18~27 MHz input clock. The VCO range is from 1250 MHz to 2500 MHz. A programmable clock divider is provided to generate different frequencies.

figure 3-11 PLL2 control diagram

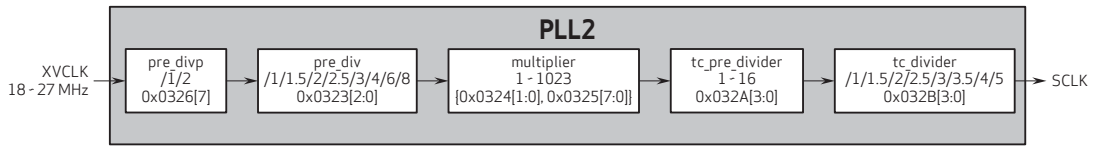


table 3-8 PLL control registers

address	register name	default value	R/W	description
0x0301	PLL1_CTRL1	0xC8	RW	Bit[7]: pll1_divs Bit[6]: pll1_predivp Bit[3]: pll1_divpix
0x0303	PLL1_CTRL3	0x01	RW	Bit[2:0]: pll1_prediv
0x0304	PLL1_CTRL4	0x01	RW	Bit[1:0]: pll1_loopdiv[9:8]
0x0305	PLL1_CTRL5	0x2C	RW	Bit[7:0]: pll1_loopdiv[7:0]
0x0306	PLL1_CTRL6	0x04	RW	Bit[2:0]: pll1_divmipi
0x0307	PLL1_CTRL7	0x01	RW	Bit[3:0]: pll1_divm
0x0308	PLL1_CTRL8	0x13	RW	Bit[4]: pll1_divs_div2 Bit[1:0]: pll1_divsp
0x0323	PLL2_CTRL3	0x04	RW	Bit[2:0]: pll2_prediv
0x0324	PLL2_CTRL4	0x00	RW	Bit[1:0]: pll2_divp[9:8]
0x0325	PLL2_CTRL5	0xC8	RW	Bit[7:0]: pll2_divp[7:0]
0x0326	PLL2_CTRL6	0x09	RW	Bit[7]: pll2_predivp Bit[6]: pll2_bias_ext Bit[5]: pll2_sa1_clk_sel Bit[4:0]: pll2_divsa1
0x0327	PLL2_CTRL7	0x04	RW	Bit[3:0]: pll2_divsram 1+r_divsam
0x0329	PLL2_CTRL9	0x01	RW	Bit[3:0]: pll2_divdac 1+r_divdac
0x032A	PLL2_CTRLA	0x04	RW	Bit[3:0]: pll2_divsys_pre 1+r_div_sys_pre
0x032B	PLL2_CTRLB	0x06	RW	Bit[3:0]: pll2_divsys 0000: /1 0001: /1.5 0010: /2 0011: /2.5 0100: /3 0101: /3.5 0110: /4 0111: /4.5 1000: /5 1001: /6 1010: /7 1011: /8 1100: /9 1101: /10 111x: /1

3.8 temperature sensor

The OX03C10 has an embedded temperature sensors in the image sensor core to measure its junction temperature. These two temperature sensors require a 1~3 MHz input clock, which is divided from XVCLK by the divisor specified in register bits 0x4D06[7:4]. The value of each temperature sensor or their average value can be read directly from two registers in a direct 8.8b format, where the first byte holds the integer part of the value and the second one holds the decimal, number of units of 1/256, all in degrees Celsius.

Following are the register sets:

- temperature sensor 0 {0x4D56, 0x4D57}
- temperature sensor 1 {0x4D58, 0x4D59}
- average value of the two sensors {0x4D2A, 0x4D2B}

All the registers can take values from 0x0000 to 0xFFFF, which correlate to the valid readout temperature range from -63.996 (-3F.FF) to 192 (C0.00) °C. The accuracy is:

- ±2°C at the calibration points (-40°C and 125°C) and in the range of -40°C to -30°C and 115°C to 135°C
- ±5°C for the rest of the range from -30°C to 115°C and above 135°C

To distinguish between positive or negative temperatures and to translate the register read values into actual temperatures, the procedure below must be followed:

If the readout of the two register sets of each temperature value ≤ 0xC000, the temperature is positive. It can be interpreted directly with the 8.8b format.

If the readout of the two register sets of each temperature value > 0xC000, the temperature is negative. The readout value needs to be converted by subtracting it by 0xC000. For the remainder, apply 8.8b format again as normal. Keep in mind, the resulting value is absolute and the minus needs to be appended for further calculations. For example, if the readout of the two register sets of each temperature value is 0xD000, the measured temperature is 0xD0 - 0xC0 =16 or -16°C.

The temperature readout function is enabled by default. The temperature data in the module is being updated:

- at every start of frame, when register bit 0x4D07[5] is set. This applies only in stream mode.
- when a new value is available when register bit 0x4D07[4] is set. This applies to both sleep and stream modes.

Note that an update will be postponed when the module registers are being read.

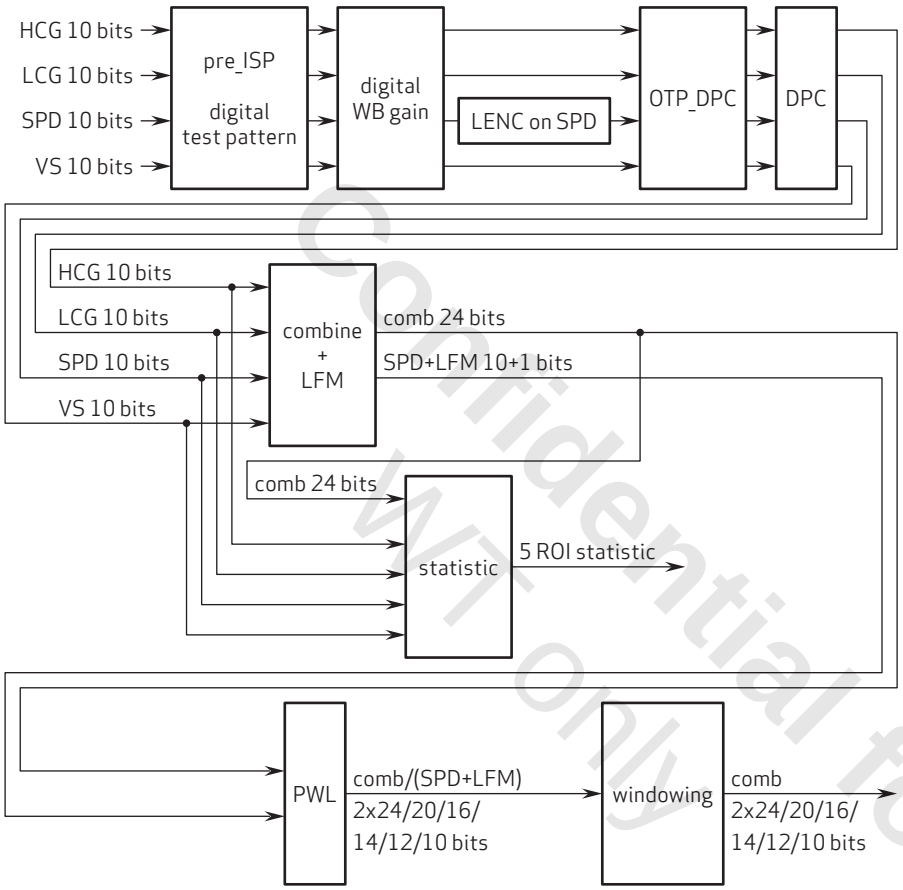
table 3-9 temperature sensor registers

address	register name	default value	R/W	description
0x4D06	TPM_REG_6	0x88	RW	Bit[7:4]: tpm_clk_divisor Bit[3:1]: cnt_bit
0x4D07	TPM_REG_7	0x31	RW	Bit[5]: sof_update_en Update on SOF Bit[4]: tpm_cont Continuous updating Bit[3]: pd_tpm_snr Power down temperature sensors Bit[2]: format_slope Bit[1]: mul_div_sel Bit[0]: shift_ave
0x4D2A	TPM_REG_26	–	R	Bit[7:0]: tpm_int_rdout Averaged temperature (integer part)
0x4D2B	TPM_REG_27	–	R	Bit[7:0]: tpm_dec_rdout Averaged temperature (decimal part)
0x4D56	TPM_REG_56	–	R	Bit[7:0]: tpm0_int_rdout Sensor 0 temperature (integer part)
0x4D57	TPM_REG_57	–	R	Bit[7:0]: tpm0_dec_rdout Sensor 0 temperature (decimal part)
0x4D58	TPM_REG_58	–	R	Bit[7:0]: tpm1_int_rdout Sensor 1 temperature (integer part)
0x4D59	TPM_REG_59	–	R	Bit[7:0]: tpm1_dec_rdout Sensor 1 temperature (decimal part)
0x4D5B	TPM_REG_5B	–	R	Bit[4]: wd_injected_fault_latch Bit[2]: fault_alarm_cel_latch Bit[1]: fault_alarm_latch Bit[0]: fault_failed_latch

4 image processor

figure 4-1 shows the top level block diagram of the OX03C10 image processor.

figure 4-1 image processor block diagram



The ISP receives image data from the sensor core and includes modules for RAW image processing. The video stream arrives as 10-bit parallel data separated in four different captures: HCG, LCG, SPD, and VS. Unused rows and columns are cut before further processing. After processing the data from the ISP, it is configured to the correct output format in the output interface.

Digital gain is the first process in the ISP, which is applied to make the image white balanced (WB gain), if enabled. The LENC block corrects the shading caused by lens fall off (LENC) for SPD. Defect pixel and clusters (DPC) are corrected on-the-fly for each capture. After that, image statistics are being gathered and the DCG captures (HCG and LCG) together with the SPD are combined into a 20-bit or 24-bit HDR linear image with a staggered exposure of LPD (VS). In addition to the combined image, depending on the output mode, either LFM-bit will be output with MIPI RAW8 (8 LFM-bit is transmitted per clock) or 10-bit SPD {SPD[9:2], LFM-bit, 0} will be output with MIPI RAW10 in a separated virtual

channel. In the transition area, the data is linearly combined. The HDR combined image can be then PWL-mapped to 20/16/14/12-bit image. At the end, image windowing is performed if enabled. **table 4-1** shows registers for ISP control.

table 4-1 ISP top registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP_CTRL_00	0x8F	RW	Bit[7]: Output size latch (by get_ready) operation enable Bit[6]: Output stream 1 post RAW binning mono mode enable Bit[5]: pre_bin_h_en Output stream 1 post RAW H binning enable Bit[4]: pre_bin_v_en Output stream 1 post RAW V binning enable Bit[3]: Insert dummy line for pre-bin, DPC, SCIP, LFM, post-bin Bit[2]: para_latch_en Latch (by get_ready) operation enable Bit[1]: ctrl_latch_en Latch (by VSYNC) operation enable Bit[0]: ISP enable
0x5001	ISP_CTRL_01	0x74	RW	Bit[7]: gain_iterate_en Bit[6]: rst_protect_en HREF before first VSYNC mask enable Bit[5]: Digital gain work enable Bit[4]: spd_used_in_combine Bit[2]: Split mode Bit[1]: bypass_combine Bit[0]: LFM's timing go with main combine
0x5002	ISP_CTRL_02	0x3F	RW	Bit[5]: Retiming enable Bit[4]: Statistic block 4 enable Bit[3]: Statistic block 3 enable Bit[2]: Statistic block 2 enable Bit[1]: Statistic block 1 enable Bit[0]: Statistic block 0 enable
0x5003	ISP_CTRL_03	0xEE	RW	Bit[7]: awb_revs_en Reverse AWB gain enable Bit[6]: LFM enable Bit[5]: Combine enable Bit[4]: Pre-matrix enable Bit[3]: Combine sync buffer enable Bit[2]: LENC enable Bit[1]: HDR sync buffer enable Bit[0]: Pre-RAW binning enable

table 4-1 ISP top registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5004	ISP_CTRL_04	0x1E	RW	Bit[4]: scip_hcg_en HCG channel SCIP enable Bit[3]: dpc_hcg_en HCG channel DPC enable Bit[2]: otp_hcg_en HCG channel OTP_DPC enable Bit[1]: awb_gain_hcg_en HCG channel AWB gain enable Bit[0]: pre_isp_hcg_en HCG channel pre ISP enable
0x5005	ISP_CTRL_05	0x1E	RW	Bit[4]: scip_lcg_en LCG channel SCIP enable Bit[3]: dpc_lcg_en LCG channel DPC enable Bit[2]: otp_lcg_en LCG channel OTP_DPC enable Bit[1]: awb_gain_lcg_en LCG channel AWB gain enable Bit[0]: pre_isp_lcg_en LCG channel pre ISP enable
0x5006	ISP_CTRL_06	0x1E	RW	Bit[4]: scip_spd_en SPD channel SCIP enable Bit[3]: dpc_spd_en SPD channel DPC enable Bit[2]: otp_spd_en SPD channel OTP_DPC enable Bit[1]: awb_gain_spd_en SPD channel AWB gain enable Bit[0]: pre_isp_spd_en SPD channel pre ISP enable
0x5007	ISP_CTRL_07	0x1E	RW	Bit[4]: scip_vs_en VS channel SCIP enable Bit[3]: dpc_vs_en VS channel DPC enable Bit[2]: otp_vs_en VS channel OTP_DPC enable Bit[1]: awb_gain_vs_en VS channel AWB gain enable Bit[0]: pre_isp_vs_en VS channel pre ISP enable

table 4-1 ISP top registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5008	POST_RAW_ BIN_CTRL	0x00	RW	Bit[7]: lfm_bin_mode 0: All bits or with each other 1: All bits and with each other Bit[6]: post_bin1_mono_en Output stream 1 post RAW binning mono mode enable Bit[5]: post_bin1_h_en Output stream 1 post RAW H binning enable Bit[4]: post_bin1_v_en Output stream 1 post RAW V binning enable Bit[2]: post_bin0_mono_en Output stream 0 post RAW binning mono mode enable Bit[1]: post_bin0_h_en Output stream 0 post RAW H binning enable Bit[0]: post_bin0_v_en Output stream 0 post RAW V binning enable

4.1 test pattern

For testing purposes, the OX03C10 supports a color bar digital test pattern with two digital effects: transparent and rolling effect. The digital test pattern is controlled by a set of four registers named PRE_ISP_0, each assigned for each channel at addresses: for HCG (0x5240), for LCG (0x5440), for SPD (0x5640), and for VS (0x5840).

The color bar style of the digital test pattern is controlled by the PRE_ISP_0[5:4] register. The digital test pattern function is either enabled/disabled by register PRE_ISP_0[0] for each channel. It is noted that the PRE_ISP enable for HCG and SPD channels are tied together, so if either register bit 0x5004[0] or register bit 0x5006[0] is set, the test pattern is visible on both the channels. The data path test patterns for each channel are only available if the ISP (0x5000[0]) and the PRE_ISP for each channel (registers from 0x5004[0] to 0x5007[0]) are enabled. The test patterns are processed by the ISP and outputted as regular images. However, they are unaffected by sensor exposure time and digital gain. **table 4-2** lists registers for the test pattern control.

table 4-2 test pattern control registers

address	register name	default value	R/W	description
0x5240	PRE_ISP_0_HCG	0x0F	RW	Bit[5:4]: bar_style Bit[2]: Transparent mode enable Combine test data and image data Bit[1]: Rolling bar mode enable Bit[0]: Test pattern enable
0x5440	PRE_ISP_0_LCG	0x0F	RW	Bit[5:4]: bar_style Bit[2]: Transparent mode enable Combine test data and image data Bit[1]: Rolling bar mode enable Bit[0]: Test pattern enable
0x5640	PRE_ISP_0_SPD	0x0F	RW	Bit[5:4]: bar_style Bit[2]: Transparent mode enable Combine test data and image data Bit[1]: Rolling bar mode enable Bit[0]: Test pattern enable
0x5840	PRE_ISP_0_VS	0x0F	RW	Bit[5:4]: bar_style Bit[2]: Transparent mode enable Combine test data and image data Bit[1]: Rolling bar mode enable Bit[0]: Test pattern enable

4.1.1 color bar

There are four types of color bars, which are switched by bar-style in register PRE_ISP_0[5:4] (see **figure 4-2**).

figure 4-2 color bar types

4.1.2 transparent effect

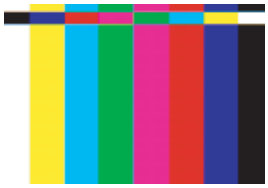
The transparent effect is enabled by PRE_ISP_0[2]. If this register is set, the transparent test pattern will be displayed. **figure 4-3** is an example showing a transparent color bar image.

figure 4-3 transparent effect

4.1.3 rolling bar effect

The rolling bar is enabled by setting the registers PRE_ISP_0[1] for each of the different captures, HCG, LCG, SPD, and VS, at the same time. If it is enabled, an inverted-color rolling bar will roll from top to bottom. **figure 4-4** is an example showing a rolling bar on color bar image.

figure 4-4 rolling bar effect



4.2 white balance gain (WB gain)

The next process in the pipeline is white balance. The RAW red, green and blue values of a gray object vary with the light source spectrum and the pixel QE spectrum response. Light source spectrum is usually described by "color temperature", which is the surface temperature of a black body radiating equivalent spectrum. In the real world, the light color temperature ranges from very low (reddish) to very high (bluish) value. For example, the color temperature of an incandescent lamp is about 2850k, while the color temperature of an overcast day is about 6500k.

To make sure that a gray image is truly gray regardless of the light spectrum, the sensor needs to adjust the gain for each RGB channel according to color temperature. This process is called white balance (WB) and it can be adjusted manually. The registers to control white balance are programmed over SCCB. An image signal process (external ASIC from this sensor) can set the white balance to a fixed value, or run an auto white balance (AWB) function that will evaluate the white balance of each frame and update the sensor WB gains over SCCB.

White balance gain is enabled by default and can be disabled by register bits 0x5004[1] ~ 0x5007[1] (see **table 4-3**). It is controlled by registers (allotted for each capture channel and color channel individually). The following ranges are comprised of 4 byte-pairs (2 bytes) ordered for each color channel, B[0], Gb[1], Gr[2] and R[3], respectively, for each capture channel:

- HCG WB gain registers: 0x5280~0x5287
- LCG WB gain registers: 0x5480~0x5487
- SPD WB gain registers: 0x5680~0x5687
- VS WB gain registers: 0x5880~0x5887

Each WB gain is set as a 15-bit value occupying the LSB's portion of each byte pair. The format is 5.10b, where the integer part is contained in the higher bits [6:2] of the first register, while the fractional part is stored in the lower bits [1:0] of the first register and continues through all the bits [7:0] in the second register. For example, a WB gain of 1x for HCG, blue color is {0x5280, 0x5281} = 0x0400.

Adjustable white balance gain has an internal latch function. Once it is set, it will take effect during the next frame.

table 4-3 WB control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5280	AWB_GAIN_HCG_0	0x04	RW	Bit[7:0]: Manual AWB gain B[15:8]
0x5281	AWB_GAIN_HCG_1	0x00	RW	Bit[7:0]: Manual AWB gain B[7:0]
0x5282	AWB_GAIN_HCG_2	0x04	RW	Bit[7:0]: Manual AWB gain Gb[15:8]
0x5283	AWB_GAIN_HCG_3	0x00	RW	Bit[7:0]: Manual AWB gain Gb[7:0]
0x5284	AWB_GAIN_HCG_4	0x04	RW	Bit[7:0]: Manual AWB gain Gr[15:8]
0x5285	AWB_GAIN_HCG_5	0x00	RW	Bit[7:0]: Manual AWB gain Gr[7:0]
0x5286	AWB_GAIN_HCG_6	0x04	RW	Bit[7:0]: Manual AWB gain R[15:8]
0x5287	AWB_GAIN_HCG_7	0x00	RW	Bit[7:0]: Manual AWB gain R[7:0]

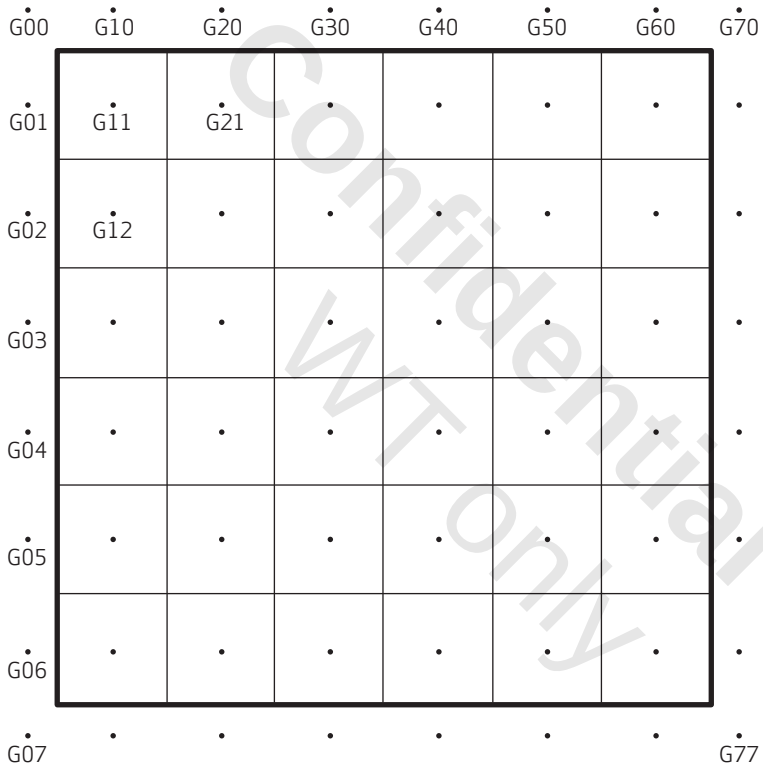
table 4-3 WB control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5480	AWB_GAIN_LCG_0	0x04	RW	Bit[7:0]: Manual AWB gain B[15:8]
0x5481	AWB_GAIN_LCG_1	0x00	RW	Bit[7:0]: Manual AWB gain B[7:0]
0x5482	AWB_GAIN_LCG_2	0x04	RW	Bit[7:0]: Manual AWB gain Gb[15:8]
0x5483	AWB_GAIN_LCG_3	0x00	RW	Bit[7:0]: Manual AWB gain Gb[7:0]
0x5484	AWB_GAIN_LCG_4	0x04	RW	Bit[7:0]: Manual AWB gain Gr[15:8]
0x5485	AWB_GAIN_LCG_5	0x00	RW	Bit[7:0]: Manual AWB gain Gr[7:0]
0x5486	AWB_GAIN_LCG_6	0x04	RW	Bit[7:0]: Manual AWB gain R[15:8]
0x5487	AWB_GAIN_LCG_7	0x00	RW	Bit[7:0]: Manual AWB gain R[7:0]
0x5680	AWB_GAIN_SPD_0	0x04	RW	Bit[7:0]: Manual AWB gain B[15:8]
0x5681	AWB_GAIN_SPD_1	0x00	RW	Bit[7:0]: Manual AWB gain B[7:0]
0x5682	AWB_GAIN_SPD_2	0x04	RW	Bit[7:0]: Manual AWB gain Gb[15:8]
0x5683	AWB_GAIN_SPD_3	0x00	RW	Bit[7:0]: Manual AWB gain Gb[7:0]
0x5684	AWB_GAIN_SPD_4	0x04	RW	Bit[7:0]: Manual AWB gain Gr[15:8]
0x5685	AWB_GAIN_SPD_5	0x00	RW	Bit[7:0]: Manual AWB gain Gr[7:0]
0x5686	AWB_GAIN_SPD_6	0x04	RW	Bit[7:0]: Manual AWB gain R[15:8]
0x5687	AWB_GAIN_SPD_7	0x00	RW	Bit[7:0]: Manual AWB gain R[7:0]
0x5880	AWB_GAIN_VS_0	0x04	RW	Bit[7:0]: Manual AWB gain B[15:8]
0x5881	AWB_GAIN_VS_1	0x00	RW	Bit[7:0]: Manual AWB gain B[7:0]
0x5882	AWB_GAIN_VS_2	0x04	RW	Bit[7:0]: Manual AWB gain Gb[15:8]
0x5883	AWB_GAIN_VS_3	0x00	RW	Bit[7:0]: Manual AWB gain Gb[7:0]
0x5884	AWB_GAIN_VS_4	0x04	RW	Bit[7:0]: Manual AWB gain Gr[15:8]
0x5885	AWB_GAIN_VS_5	0x00	RW	Bit[7:0]: Manual AWB gain Gr[7:0]
0x5886	AWB_GAIN_VS_6	0x04	RW	Bit[7:0]: Manual AWB gain R[15:8]
0x5887	AWB_GAIN_VS_7	0x00	RW	Bit[7:0]: Manual AWB gain R[7:0]

4.3 lens correction (LENC) for SPD

The LENC block is used to correct the shading due to light fall off in the edges and corner areas for the SPD. This lens correction feature can be used to align the lens shading of the SPD with the LPD, so further lens correction can be applied on the combined data in an external processor. The correction is done by multiplying each pixel with a gain based on the area where each pixel is located, based on a control point matrix for each color, red, green, and blue. LENC is disabled by default and can be enabled by register bit 0x5003[2]. The control point matrix for the green color channels is 8x8.

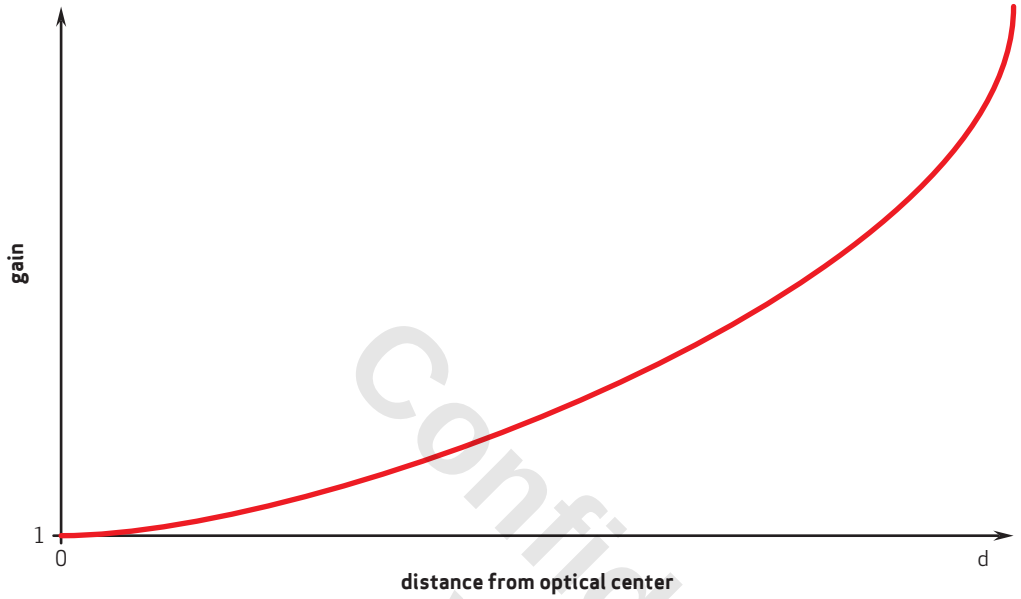
figure 4-5 8x8 control point matrix for color channel (0x5A20-0x5ADF)



The control points are shown in **figure 4-5** and the lens correction gain values can be set by registers 0x5A20~0x5A5F for the green color channel, registers 0x5A60~0x5A9F for the blue color channel, and registers 0x5AA0~0x5ADF for the red color channel. The control point matrix can be scaled both vertically and horizontally with registers 0x5A07~0x5A0E, and an offset can be applied for the gain matrix through registers 0x5A16~0x5A19.

Under dark conditions, the signal-to-noise ratio (SNR) drops in the corner areas. The noise can be significantly amplified by the lens correction gain and results in a brighter corner. A parameter m_nq (0x5A1A[6:0]) is used to adjust gain for the pixel. It can be auto calculated from the real gain or manually set it.

figure 4-6 LENC shading gain



LENC control point parameters must be calibrated with a specific tool. Please contact your regional OmniVision FAE for assistance.

All LENC control registers are not frame-synced, thus any setting change will take effect immediately (during the current frame [N]).

table 4-4 LENC control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5003	ISP_CTRL_03	0xEE	RW	Bit[7]: awb_revs_en Reverse AWB gain enable Bit[6]: LFM enable Bit[5]: Combine enable Bit[4]: Pre-matrix enable Bit[3]: Combine sync buffer enable Bit[2]: LENC enable Bit[1]: HDR sync buffer enable Bit[0]: Pre-RAW binning enable
0x5A00	LENC_0	0x05	RW	Bit[2]: less_1x_en Bit[1]: rand_bit_en Less than 1x gain process Bit[0]: auto_q_en Enable dithering function to avoid lost bit

table 4-4 LENC control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5A01	LENC_1	0x18	RW	Bit[6:0]: minq_s Minqfros
0x5A02	LENC_2	0x40	RW	Bit[6:0]: maxq_s Maxqfros
0x5A03	LENC_3	0x00	RW	Bit[3:0]: min_gain[11:8]
0x5A04	LENC_4	0x20	RW	Bit[7:0]: min_gain[7:0]
0x5A05	LENC_5	0x00	RW	Bit[3:0]: max_gain[11:8]
0x5A06	LENC_6	0x60	RW	Bit[7:0]: max_gain[7:0]
0x5A07	LENC_7	0x00	RW	Bit[7:0]: br_hscale_man[15:8]
0x5A08	LENC_8	0x00	RW	Bit[7:0]: br_hscale_man[7:0] Scale H for Br channel
0x5A09	LENC_9	0x00	RW	Bit[7:0]: br_vscale_man[15:8] Scale V for BR channel
0x5A0A	LENC_A	0x00	RW	Bit[7:0]: br_vscale_man[7:0] Scale V for BR channel
0x5A0B	LENC_B	0x00	RW	Bit[7:0]: g_hscale_man[15:8] Scale H for G channel
0x5A0C	LENC_C	0x00	RW	Bit[7:0]: g_hscale_man[7:0] Scale H for G channel
0x5A0D	LENC_D	0x00	RW	Bit[7:0]: g_vscale_man[15:8] Scale V for G channel
0x5A0E	LENC_E	0x00	RW	Bit[7:0]: g_vscale_man[7:0] Scale V for G channel
0x5A0F	LENC_F	0x00	RW	Bit[3:0]: real_gain_s_man[11:8] Real gain for manual
0x5A10	LENC_10	0x00	RW	Bit[7:0]: real_gain_s_man[7:0] Real gain for manual
0x5A11	LENC_11	0x00	RW	Bit[3]: real_gain_for_man_en Bit[2]: scale_man_en Bit[1]: Mnq_man_en Bit[0]: blc_man_en
0x5A12	LENC_12	0x00	RW	Bit[1:0]: blc_s_man[9:8] Manual BLC
0x5A13	LENC_13	0x00	RW	Bit[7:0]: blc_s_man[7:0] Manual BLC

table 4-4 LENC control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5A14	LENC_14	0x00	RW	Bit[6]: cfa_pattern_man_en Bit[5]: mirror_man_en Bit[4]: flip_man_en Bit[3]: skip_man_en Bit[2]: offset_man_en Bit[1]: mirror_man Manual mirror Bit[0]: flip_man Manual flip
0x5A15	LENC_15	0x00	RW	Bit[5:4]: cfa_pn_man Manual CFA pattern Bit[3:2]: x_skip_man Manual X skip Bit[1:0]: y_skip_man Manual Y skip
0x5A16	LENC_16	0x00	RW	Bit[3:0]: x_offset_man[11:8] Manual X offset
0x5A17	LENC_17	0x00	RW	Bit[7:0]: x_offset_man[7:0] Manual X offset
0x5A18	LENC_18	0x00	RW	Bit[3:0]: y_offset_man[11:8] Manual Y offset
0x5A19	LENC_19	0x00	RW	Bit[7:0]: y_offset_man[7:0] Manual Y offset

4.4 static defect pixel cancellation

The OTP_DPC is a function using an absolute address to detect defect pixels and make corrections. It supports mirror and flip options. It is enabled by setting register bits (0x5004[2]~0x5007[2]) for the four captures (see **table 4-1**). The toggling of which must only occur while the sensor is in software standby. It must load the OTP cluster information from OTP eFUSE.

- X-coordinate is cluster's horizontal direction start point in sensor array
- Y-coordinate is cluster's vertical direction start point in sensor array

Cluster coordinate information is stored in the OTP memory. When the system boots up, the defect information is read out of OTP and programmed in to the OTP_DPC function. As every pixel flows through the OTP_DPC function, it identifies the locations marked in the OTP data and corrects the defects in line based on the adjacent pixels.

To read the cluster information in eFUSE, the register, OTP eFUSE start address ({0x5314, 0x5315} must be set. **table 4-5** shows registers for OTP_DPC setting.

table 4-5 OTP_DPC control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5300	OTP_DPC_HCG_0	0xC2	RW	Bit[7]: Mirror option Bit[6]: Flip option Bit[5]: Disable mirror and flip Bit[4]: Auto mode using gain enable Bit[3]: Auto mode using exposure enable Bit[2]: ThresEn Detection enable Bit[1]: Fixed pattern selection Bit[0]: Fixed pattern enable
0x5301	OTP_DPC_HCG_1	0x10	RW	Bit[4]: GainSelect Gain-dependent OTP_DPC cluster enable Bit[3]: EnableBWBin2 BW binning mode Bit[2]: Disable binning Bit[1]: Manual increase step enable Bit[0]: Manual offset enable
0x5302	OTP_DPC_HCG_2	0x30	RW	Bit[6:4]: Recovery method selection Bit[3:2]: Horizontal binning mode Bit[1:0]: Vertical binning mode
0x5303	OTP_DPC_HCG_3	0x18	RW	Bit[7:4]: GainSelectThres Gain-dependent threshold Bit[3:0]: OTPThres Detection threshold
0x5309	OTP_DPC_HCG_8	0x07	RW	Bit[5:0]: GainLimit Gain threshold
0x530A	OTP_DPC_HCG_A	0x00	RW	Bit[6:0]: ExposureLimit[14:8] Exposure threshold

table 4-5 OTP_DPC control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x530B	OTP_DPC_HCG_B	0x00	RW	Bit[7:0]: ExposureLimit[7:0] Exposure threshold
0x530C	OTP_DPC_HCG_C	0x00	RW	Bit[7:0]: Manual X offset[15:8]
0x530D	OTP_DPC_HCG_D	0x00	RW	Bit[7:0]: Manual X offset[7:0]
0x530E	OTP_DPC_HCG_E	0x00	RW	Bit[7:0]: Manual Y offset[15:8]
0x530F	OTP_DPC_HCG_F	0x00	RW	Bit[7:0]: Manual Y offset[7:0]
0x5314	OTP_DPC_HCG_14	0x70	RW	Bit[7:0]: OTP eFUSE start address[15:8]
0x5315	OTP_DPC_HCG_15	0x70	RW	Bit[7:0]: OTP eFUSE start address[7:0]
0x5316	OTP_DPC_HCG_16	0x73	RW	Bit[7:0]: OTP eFUSE end address[15:8]
0x5317	OTP_DPC_HCG_17	0xFF	RW	Bit[7:0]: OTP eFUSE end address[7:0]
0x5500	OTP_DPC_LCG_0	0xC2	RW	Bit[7]: Mirror option Bit[6]: Flip option Bit[5]: Disable mirror and flip Bit[4]: Auto mode using gain enable Bit[3]: Auto mode using exposure enable Bit[2]: ThresEn Detection enable Bit[1]: Fixed pattern selection Bit[0]: Fixed pattern enable
0x5501	OTP_DPC_LCG_1	0x10	RW	Bit[4]: GainSelect Gain-dependent OTP_DPC cluster enable Bit[3]: EnableBWBin2 BW binning mode Bit[2]: Disable binning Bit[1]: Manual increase step enable Bit[0]: Manual offset enable
0x5502	OTP_DPC_LCG_2	0x30	RW	Bit[6:4]: Recovery method selection Bit[3:2]: Horizontal binning mode Bit[1:0]: Vertical binning mode
0x5503	OTP_DPC_LCG_3	0x18	RW	Bit[7:4]: GainSelectThres Gain-dependent threshold Bit[3:0]: OTPThres Detection threshold
0x5509	OTP_DPC_LCG_8	0x07	RW	Bit[5:0]: GainLimit Gain threshold
0x550A	OTP_DPC_LCG_A	0x00	RW	Bit[6:0]: ExposureLimit[14:8] Exposure threshold
0x550B	OTP_DPC_LCG_B	0x00	RW	Bit[7:0]: ExposureLimit[7:0] Exposure threshold

table 4-5 OTP_DPC control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x550C	OTP_DPC_LCG_C	0x00	RW	Bit[7:0]: Manual X offset[15:8]
0x550D	OTP_DPC_LCG_D	0x00	RW	Bit[7:0]: Manual X offset[7:0]
0x550E	OTP_DPC_LCG_E	0x00	RW	Bit[7:0]: Manual Y offset[15:8]
0x550F	OTP_DPC_LCG_F	0x00	RW	Bit[7:0]: Manual Y offset[7:0]
0x5700	OTP_DPC_SPD_0	0xC2	RW	Bit[7]: Mirror option Bit[6]: Flip option Bit[5]: Disable mirror and flip Bit[4]: Auto mode using gain enable Bit[3]: Auto mode using exposure enable Bit[2]: ThresEn Detection enable Bit[1]: Fixed pattern selection Bit[0]: Fixed pattern enable
0x5701	OTP_DPC_SPD_1	0x10	RW	Bit[4]: GainSelect Gain-dependent OTP_DPC cluster enable Bit[3]: EnableBWBin2 BW binning mode Bit[2]: Disable binning Bit[1]: Manual increase step enable Bit[0]: Manual offset enable
0x5702	OTP_DPC_SPD_2	0x30	RW	Bit[6:4]: Recovery method selection Bit[3:2]: Horizontal binning mode Bit[1:0]: Vertical binning mode
0x5703	OTP_DPC_SPD_3	0x18	RW	Bit[7:4]: GainSelectThres Gain-dependent threshold Bit[3:0]: OTPThres Detection threshold
0x5709	OTP_DPC_SPD_8	0x07	RW	Bit[5:0]: GainLimit Gain threshold
0x570A	OTP_DPC_SPD_A	0x00	RW	Bit[6:0]: ExposureLimit[14:8] Exposure threshold
0x570B	OTP_DPC_SPD_B	0x00	RW	Bit[7:0]: ExposureLimit[7:0] Exposure threshold
0x570C	OTP_DPC_SPD_C	0x00	RW	Bit[7:0]: Manual X offset[15:8]
0x570D	OTP_DPC_SPD_D	0x00	RW	Bit[7:0]: Manual X offset[7:0]
0x570E	OTP_DPC_SPD_E	0x00	RW	Bit[7:0]: Manual Y offset[15:8]
0x570F	OTP_DPC_SPD_F	0x00	RW	Bit[7:0]: Manual Y offset[7:0]

table 4-5 OTP_DPC control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x5900	OTP_DPC_VS_0	0xC2	RW	Bit[7]: Mirror option Bit[6]: Flip option Bit[5]: Disable mirror and flip Bit[4]: Auto mode using gain enable Bit[3]: Auto mode using exposure enable Bit[2]: ThresEn Detection enable Bit[1]: Fixed pattern selection Bit[0]: Fixed pattern enable
0x5901	OTP_DPC_VS_1	0x10	RW	Bit[4]: GainSelect Gain-dependent OTP_DPC cluster enable Bit[3]: EnableBWBin2 BW binning mode Bit[2]: Disable binning Bit[1]: Manual increase step enable Bit[0]: Manual offset enable
0x5902	OTP_DPC_VS_2	0x30	RW	Bit[6:4]: Recovery method selection Bit[3:2]: Horizontal binning mode Bit[1:0]: Vertical binning mode
0x5903	OTP_DPC_VS_3	0x18	RW	Bit[7:4]: GainSelectThres Gain-dependent threshold Bit[3:0]: OTPThres Detection threshold
0x5909	OTP_DPC_VS_8	0x07	RW	Bit[5:0]: GainLimit Gain threshold
0x590A	OTP_DPC_VS_A	0x00	RW	Bit[6:0]: ExposureLimit[14:8] Exposure threshold
0x590B	OTP_DPC_VS_B	0x00	RW	Bit[7:0]: ExposureLimit[7:0] Exposure threshold
0x590C	OTP_DPC_VS_C	0x00	RW	Bit[7:0]: Manual X offset[15:8]
0x590D	OTP_DPC_VS_D	0x00	RW	Bit[7:0]: Manual X offset[7:0]
0x590E	OTP_DPC_VS_E	0x00	RW	Bit[7:0]: Manual Y offset[15:8]
0x590F	OTP_DPC_VS_F	0x00	RW	Bit[7:0]: Manual Y offset[7:0]

4.5 dynamic defect pixel cancellation

Defect pixels are defined as the pixels with a high possibility to be brighter or darker than their neighboring pixels, which includes both dead pixels and damaged pixels. When sensor gain exposure time, gain or temperature increases, there are more defect pixels.

Defect pixel cancellation (DPC) is an online defect pixel detection and correction algorithm, which can be enabled by setting register bits 0x5004[3]~0x5007[3] = 1 (see **table 4-1**). The bit must only be toggled while the sensor is in software standby.

The main purpose of the DPC function is to remove these white/black pixels. If the pixel is defective, DPC will use a value calculated from the neighboring normal pixels to replace it. Each capture channel has their own set of parameters. The register addresses start from 0x52C0, 0x54C0, 0x56C0, and 0x58C0 for HCG, LCG, SPD, and VS, respectively. Thus, DPC can process four frames separately.

The case reviewed below focuses on the first capture channel registers HCG.

The defect black pixel cancellation and defect white pixel cancellation are controlled by register bit 0x52C0[1] and register bit 0x52C0[0], respectively. DPC determines whether a pixel is defective or not based on the detection threshold. With a smaller detection threshold, more pixels are detected as white or black pixels are corrected, resulting in more blurry images.

In manual mode (register bit 0x52C0[3] = 1), the white pixel threshold is in registers 0x52C8~0x52CB for different light levels. The black threshold is defined in registers 0x52CC~0x52CF, and the maximum number of allowed defect pixels is stored in 0x52C6~0x52C7. In auto mode (register bit 0x52C0[3] = 0), the thresholds and maximum number of allowed defect pixels are controlled by sensor gain.

Users can specify a ROI window, where a number of defect pixels are statistically counted. The defect count is then compared with a setting value, If the count is greater or equal to the setting value, a DPC error flag will be set (register bit 0x4225[7] = 1). **table 4-6**, **table 4-7**, **table 4-8**, and **table 4-9** show DPC control registers for the four capture channels HCG, LCG, SPD and VS, respectively.

table 4-6 DPC HCG control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x52C0	DPC_HCG_NUM_0	0x33	RW	Bit[7:6]: correct_opt Option to correct G/BR pixel 00: RGB 01: G 10: BR Bit[5:4]: Edge filling option Bit[3]: manual_mode_en Enable manual mode Bit[2]: Enable cross cluster correction Bit[1]: Enable black pixel correction Bit[0]: Enable white pixel correction

table 4-6 DPC HCG control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x52C1	DPC_HCG_NUM_1	0x88	RW	Bit[7:4]: couplet_bgain_margin Black couplet defect pixel correction gain margin Bit[3:0]: couplet_wgain_margin White couplet defect pixel correction gain margin
0x52C2	DPC_HCG_NUM_2	0x88	RW	Bit[7:4]: cluster_b_th Black couplet threshold ratio Bit[3:0]: cluster_w_th White couplet threshold ratio
0x52C3	DPC_HCG_NUM_3	0x08	RW	Bit[7:0]: couplet_wgain_th White couplet defect pixel correction gain threshold
0x52C4	DPC_HCG_NUM_4	0x08	RW	Bit[7:0]: couplet_bgain_th Black couplet defect pixel correction gain threshold
0x52C5	DPC_HCG_NUM_5	0xFF	RW	Bit[7:0]: Saturation threshold
0x52C6	DPC_HCG_0	0x00	RW	Bit[7:4]: dp_num_list0 Max allowed defect pixel list0 Bit[3:0]: dp_num_list1 Max allowed defect pixel list1
0x52C7	DPC_HCG_1	0x12	RW	Bit[7:4]: dp_num_list2 Max allowed defect pixel list2 Bit[3:0]: dp_num_list3 Max allowed defect pixel list3
0x52C8	DPC_HCG_2	0x04	RW	Bit[7:0]: w_th_list0 White pixel threshold list
0x52C9	DPC_HCG_3	0x04	RW	Bit[7:0]: w_th_list1 White pixel threshold list
0x52CA	DPC_HCG_4	0x04	RW	Bit[7:0]: w_th_list2 White pixel threshold list
0x52CB	DPC_HCG_5	0x04	RW	Bit[7:0]: w_th_list3 White pixel threshold list
0x52CC	DPC_HCG_6	0x04	RW	Bit[7:0]: b_th_list0 Black pixel threshold list
0x52CD	DPC_HCG_7	0x04	RW	Bit[7:0]: b_th_list1 Black pixel threshold list
0x52CE	DPC_HCG_8	0x04	RW	Bit[7:0]: b_th_list2 Black pixel threshold list

table 4-6 DPC HCG control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x52CF	DPC_HCG_9	0x04	RW	Bit[7:0]: b_th_list3 Black pixel threshold list
0x52D0	DPC_HCG_A	0x03	RW	Bit[7:0]: gain_list0 Gain control point
0x52D1	DPC_HCG_B	0x08	RW	Bit[7:0]: gain_list1 Gain control point
0x52D2	DPC_HCG_C	0x0C	RW	Bit[7:0]: gain_list2 Gain control point
0x52D4	DPC_HCG_14	0x00	RW	Bit[3:0]: roi_start_x[11:8] ROI top left X location high byte
0x52D5	DPC_HCG_15	0x00	RW	Bit[7:0]: roi_start_x[7:0] ROI top left X location low byte
0x52D6	DPC_HCG_16	0x00	RW	Bit[3:0]: roi_start_y[11:8] ROI top left Y location high byte
0x52D7	DPC_HCG_17	0x00	RW	Bit[7:0]: roi_start_y[7:0] ROI top left Y location low byte
0x52D8	DPC_HCG_18	0x00	RW	Bit[3:0]: roi_width[11:8] ROI width high byte
0x52D9	DPC_HCG_19	0x0F	RW	Bit[7:0]: roi_width[7:0] ROI width low byte
0x52DA	DPC_HCG_1A	0x00	RW	Bit[3:0]: roi_height[11:8] ROI height high byte
0x52DB	DPC_HCG_1B	0x0F	RW	Bit[7:0]: roi_height[7:0] ROI height low byte
0x52DC	DPC_HCG_1C	0xFF	RW	Bit[7:0]: roi_dp_num Number of DP locations can be saved
0x52DD	DPC_HCG_1D	0xFF	RW	Bit[7:0]: roi_dp_num Number of DP locations can be saved
0x52DE	DPC_HCG_1E	0xFF	RW	Bit[7:0]: roi_dp_num Number of DP locations can be saved
0x52E6	DPC_HCG_26	–	R	Bit[7:0]: w_th
0x52E7	DPC_HCG_27	–	R	Bit[7:0]: b_th
0x52E8	DPC_HCG_28	–	R	Bit[3:0]: max_dp_num
0x52E9	DPC_HCG_29	–	R	Bit[1]: couplet_w_en Bit[0]: couplet_b_en
0x52EA	DPC_HCG_2A	–	R	Bit[7:0]: DPCount

table 4-6 DPC HCG control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x52EB	DPC_HCG_2B	–	R	Bit[7:0]: DPCount
0x52EC	DPC_HCG_2C	–	R	Bit[7:0]: DPCount
0x52ED	DPC_HCG_2D	–	R	Bit[7:0]: DPROICount
0x52EE	DPC_HCG_2E	–	R	Bit[7:0]: DPROICount
0x52EF	DPC_HCG_2F	–	R	Bit[7:0]: DPROICount

table 4-7 DPC LCG control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x54C0	DPC_LCG_NUM_0	0x33	RW	Bit[7:6]: correct_opt Option to correct G/BR pixel 00: RGB 01: G 10: BR Bit[5:4]: Edge filling option Bit[3]: manual_mode_en Enable manual mode Bit[2]: Enable cross cluster correction Bit[1]: Enable black pixel correction Bit[0]: Enable white pixel correction
0x54C1	DPC_LCG_NUM_1	0x88	RW	Bit[7:4]: couplet_bgain_margin Black couplet defect pixel correction gain margin Bit[3:0]: couplet_wgain_margin White couplet defect pixel correction gain margin
0x54C2	DPC_LCG_NUM_2	0x88	RW	Bit[7:4]: cluster_b_th Black couplet threshold ratio Bit[3:0]: cluster_w_th White couplet threshold ratio
0x54C3	DPC_LCG_NUM_3	0x08	RW	Bit[7:0]: couplet_wgain_th White couplet defect pixel correction gain threshold
0x54C4	DPC_LCG_NUM_4	0x08	RW	Bit[7:0]: couplet_bgain_th Black couplet defect pixel correction gain threshold
0x54C5	DPC_LCG_NUM_5	0xFF	RW	Bit[7:0]: Saturation threshold

table 4-7 DPC LCG control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x54C6	DPC_LCG_0	0x00	RW	Bit[7:4]: dp_num_list0 Max allowed defect pixel list0 Bit[3:0]: dp_num_list1 Max allowed defect pixel list1
0x54C7	DPC_LCG_1	0x12	RW	Bit[7:4]: dp_num_list2 Max allowed defect pixel list2 Bit[3:0]: dp_num_list3 Max allowed defect pixel list3
0x54C8	DPC_LCG_2	0x04	RW	Bit[7:0]: w_th_list0 White pixel threshold list
0x54C9	DPC_LCG_3	0x04	RW	Bit[7:0]: w_th_list1 White pixel threshold list
0x54CA	DPC_LCG_4	0x04	RW	Bit[7:0]: w_th_list2 White pixel threshold list
0x54CB	DPC_LCG_5	0x04	RW	Bit[7:0]: w_th_list3 White pixel threshold list
0x54CC	DPC_LCG_6	0x04	RW	Bit[7:0]: b_th_list0 Black pixel threshold list
0x54CD	DPC_LCG_7	0x04	RW	Bit[7:0]: b_th_list1 Black pixel threshold list
0x54CE	DPC_LCG_8	0x04	RW	Bit[7:0]: b_th_list2 Black pixel threshold list
0x54CF	DPC_LCG_9	0x04	RW	Bit[7:0]: b_th_list3 Black pixel threshold list
0x54D0	DPC_LCG_A	0x03	RW	Bit[7:0]: gain_list0 Gain control point
0x54D1	DPC_LCG_B	0x08	RW	Bit[7:0]: gain_list1 Gain control point
0x54D2	DPC_LCG_C	0x0C	RW	Bit[7:0]: gain_list2 Gain control point
0x54D4	DPC_LCG_14	0x00	RW	Bit[3:0]: roi_start_x[11:8] ROI top left X location high byte
0x54D5	DPC_LCG_15	0x00	RW	Bit[7:0]: roi_start_x[7:0] ROI top left X location low byte
0x54D6	DPC_LCG_16	0x00	RW	Bit[3:0]: roi_start_y[11:8] ROI top left Y location high byte
0x54D7	DPC_LCG_17	0x00	RW	Bit[7:0]: roi_start_y[7:0] ROI top left Y location low byte

table 4-7 DPC LCG control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x54D8	DPC_LCG_18	0x00	RW	Bit[3:0]: rob_width[11:8] ROI width high byte
0x54D9	DPC_LCG_19	0x0F	RW	Bit[7:0]: roi_width[7:0] ROI width low byte
0x54DA	DPC_LCG_1A	0x00	RW	Bit[3:0]: roi_height[11:8] ROI height high byte
0x54DB	DPC_LCG_1B	0x0F	RW	Bit[7:0]: roi_height[7:0] ROI height low byte
0x54DC	DPC_LCG_1C	0xFF	RW	Bit[7:0]: roi_dp_num Number of DP locations can be saved
0x54DD	DPC_LCG_1D	0xFF	RW	Bit[7:0]: roi_dp_num Number of DP locations can be saved
0x54DE	DPC_LCG_1E	0xFF	RW	Bit[7:0]: roi_dp_num Number of DP locations can be saved
0x54E6	DPC_LCG_26	–	R	Bit[7:0]: w_th
0x54E7	DPC_LCG_27	–	R	Bit[7:0]: b_th
0x54E8	DPC_LCG_28	–	R	Bit[3:0]: max_dp_num
0x54E9	DPC_LCG_29	–	R	Bit[1]: couplet_w_en Bit[0]: couplet_b_en
0x54EA	DPC_LCG_2A	–	R	Bit[7:0]: DPCount
0x54EB	DPC_LCG_2B	–	R	Bit[7:0]: DPCount
0x54EC	DPC_LCG_2C	–	R	Bit[7:0]: DPCount
0x54ED	DPC_LCG_2D	–	R	Bit[7:0]: DPROICount
0x54EE	DPC_LCG_2E	–	R	Bit[7:0]: DPROICount
0x54EF	DPC_LCG_2F	–	R	Bit[7:0]: DPROICount

table 4-8 DPC SPD control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x56C0	DPC_SPD_NUM_0	0x33	RW	Bit[7:6]: correct_opt Option to correct G/BR pixel 00: RGB 01: G 10: BR Bit[5:4]: Edge filling option Bit[3]: manual_mode_en Enable manual mode Bit[2]: Enable cross cluster correction Bit[1]: Enable black pixel correction Bit[0]: Enable white pixel correction
0x56C1	DPC_SPD_NUM_1	0x88	RW	Bit[7:4]: couplet_bgain_margin Black couplet defect pixel correction gain margin Bit[3:0]: couplet_wgain_margin White couplet defect pixel correction gain margin
0x56C2	DPC_SPD_NUM_2	0x88	RW	Bit[7:4]: cluster_b_th Black couplet threshold ratio Bit[3:0]: cluster_w_th White couplet threshold ratio
0x56C3	DPC_SPD_NUM_3	0x08	RW	Bit[7:0]: couplet_wgain_th White couplet defect pixel correction gain threshold
0x56C4	DPC_SPD_NUM_4	0x08	RW	Bit[7:0]: couplet_bgain_th Black couplet defect pixel correction gain threshold
0x56C5	DPC_SPD_NUM_5	0xFF	RW	Bit[7:0]: Saturation threshold
0x56C6	DPC_SPD_0	0x00	RW	Bit[7:4]: dp_num_list0 Max allowed defect pixel list0 Bit[3:0]: dp_num_list1 Max allowed defect pixel list1
0x56C7	DPC_SPD_1	0x12	RW	Bit[7:4]: dp_num_list2 Max allowed defect pixel list2 Bit[3:0]: dp_num_list3 Max allowed defect pixel list3
0x56C8	DPC_SPD_2	0x04	RW	Bit[7:0]: w_th_list0 White pixel threshold list
0x56C9	DPC_SPD_3	0x04	RW	Bit[7:0]: w_th_list1 White pixel threshold list
0x56CA	DPC_SPD_4	0x04	RW	Bit[7:0]: w_th_list2 White pixel threshold list

table 4-8 DPC SPD control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x56CB	DPC_SPD_5	0x04	RW	Bit[7:0]: w_th_list3 White pixel threshold list
0x56CC	DPC_SPD_6	0x04	RW	Bit[7:0]: b_th_list0 Black pixel threshold list
0x56CD	DPC_SPD_7	0x04	RW	Bit[7:0]: b_th_list1 Black pixel threshold list
0x56CE	DPC_SPD_8	0x04	RW	Bit[7:0]: b_th_list2 Black pixel threshold list
0x56CF	DPC_SPD_9	0x04	RW	Bit[7:0]: b_th_list3 Black pixel threshold list
0x56D0	DPC_SPD_A	0x03	RW	Bit[7:0]: gain_list0 Gain control point
0x56D1	DPC_SPD_B	0x08	RW	Bit[7:0]: gain_list1 Gain control point
0x56D2	DPC_SPD_C	0x0C	RW	Bit[7:0]: gain_list2 Gain control point
0x56D4	DPC_SPD_14	0x00	RW	Bit[3:0]: roi_start_x[11:8] ROI top left X location high byte
0x56D5	DPC_SPD_15	0x00	RW	Bit[7:0]: roi_start_x[7:0] ROI top left X location low byte
0x56D6	DPC_SPD_16	0x00	RW	Bit[3:0]: roi_start_y[11:8] ROI top left Y location high byte
0x56D7	DPC_SPD_17	0x00	RW	Bit[7:0]: roi_start_y[7:0] ROI top left Y location low byte
0x56D8	DPC_SPD_18	0x00	RW	Bit[3:0]: roi_width[11:8] ROI width high byte
0x56D9	DPC_SPD_19	0x0F	RW	Bit[7:0]: roi_width[7:0] ROI width low byte
0x56DA	DPC_SPD_1A	0x00	RW	Bit[3:0]: roi_height[11:8] ROI height high byte
0x56DB	DPC_SPD_1B	0x0F	RW	Bit[7:0]: roi_height[7:0] ROI height low byte
0x56DC	DPC_SPD_1C	0xFF	RW	Bit[7:0]: roi_dp_num Number of DP locations can be saved
0x56DD	DPC_SPD_1D	0xFF	RW	Bit[7:0]: roi_dp_num Number of DP locations can be saved
0x56DE	DPC_SPD_1E	0xFF	RW	Bit[7:0]: roi_dp_num Number of DP locations can be saved

table 4-8 DPC SPD control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x56E6	DPC_SPD_26	–	R	Bit[7:0]: w_th
0x56E7	DPC_SPD_27	–	R	Bit[7:0]: b_th
0x56E8	DPC_SPD_28	–	R	Bit[3:0]: max_dp_num
0x56E9	DPC_SPD_29	–	R	Bit[1]: couplet_w_en Bit[0]: couplet_b_en
0x56EA	DPC_SPD_2A	–	R	Bit[7:0]: DPCount
0x56EB	DPC_SPD_2B	–	R	Bit[7:0]: DPCount
0x56EC	DPC_SPD_2C	–	R	Bit[7:0]: DPCount
0x56ED	DPC_SPD_2D	–	R	Bit[7:0]: DPROICount
0x56EE	DPC_SPD_2E	–	R	Bit[7:0]: DPROICount
0x56EF	DPC_SPD_2F	–	R	Bit[7:0]: DPROICount

table 4-9 DPC VS control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x58C0	DPC_VS_NUM_0	0x33	RW	Bit[7:6]: correct_opt Option to correct G/BR pixel 00: RGB 01: G 10: BR Bit[5:4]: Edge filling option Bit[3]: manual_mode_en Enable manual mode Bit[2]: Enable cross cluster correction Bit[1]: Enable black pixel correction Bit[0]: Enable white pixel correction
0x58C1	DPC_VS_NUM_1	0x88	RW	Bit[7:4]: couplet_bgain_margin Black couplet defect pixel correction gain margin Bit[3:0]: couplet_wgain_margin White couplet defect pixel correction gain margin
0x58C2	DPC_VS_NUM_2	0x88	RW	Bit[7:4]: cluster_b_th Black couplet threshold ratio Bit[3:0]: cluster_w_th White couplet threshold ratio

table 4-9 DPC VS control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x58C3	DPC_VS_NUM_3	0x08	RW	Bit[7:0]: couplet_wgain_th White couplet defect pixel correction gain threshold
0x58C4	DPC_VS_NUM_4	0x08	RW	Bit[7:0]: couplet_bgain_th Black couplet defect pixel correction gain threshold
0x58C5	DPC_VS_NUM_5	0xFF	RW	Bit[7:0]: Saturation threshold
0x58C6	DPC_VS_0	0x00	RW	Bit[7:4]: dp_num_list0 Max allowed defect pixel list0 Bit[3:0]: dp_num_list1 Max allowed defect pixel list1
0x58C7	DPC_VS_1	0x12	RW	Bit[7:4]: dp_num_list2 Max allowed defect pixel list2 Bit[3:0]: dp_num_list3 Max allowed defect pixel list3
0x58C8	DPC_VS_2	0x04	RW	Bit[7:0]: w_th_list0 White pixel threshold list
0x58C9	DPC_VS_3	0x04	RW	Bit[7:0]: w_th_list1 White pixel threshold list
0x58CA	DPC_VS_4	0x04	RW	Bit[7:0]: w_th_list2 White pixel threshold list
0x58CB	DPC_VS_5	0x04	RW	Bit[7:0]: w_th_list3 White pixel threshold list
0x58CC	DPC_VS_6	0x04	RW	Bit[7:0]: b_th_list0 Black pixel threshold list
0x58CD	DPC_VS_7	0x04	RW	Bit[7:0]: b_th_list1 Black pixel threshold list
0x58CE	DPC_VS_8	0x04	RW	Bit[7:0]: b_th_list2 Black pixel threshold list
0x58CF	DPC_VS_9	0x04	RW	Bit[7:0]: b_th_list3 Black pixel threshold list
0x58D0	DPC_VS_A	0x03	RW	Bit[7:0]: gain_list0 Gain control point
0x58D1	DPC_VS_B	0x08	RW	Bit[7:0]: gain_list1 Gain control point
0x58D2	DPC_VS_C	0x0C	RW	Bit[7:0]: gain_list2 Gain control point
0x58D4	DPC_VS_14	0x00	RW	Bit[3:0]: roi_start_x[11:8] ROI top left X location high byte

table 4-9 DPC VS control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x58D5	DPC_VS_15	0x00	RW	Bit[7:0]: roi_start_x[7:0] ROI top left X location low byte
0x58D6	DPC_VS_16	0x00	RW	Bit[3:0]: roi_start_y[11:8] ROI top left Y location high byte
0x58D7	DPC_VS_17	0x00	RW	Bit[7:0]: roi_start_y[7:0] ROI top left Y location low byte
0x58D8	DPC_VS_18	0x00	RW	Bit[3:0]: roi_width[11:8] ROI width high byte
0x58D9	DPC_VS_19	0x0F	RW	Bit[7:0]: roi_width[7:0] ROI width low byte
0x58DA	DPC_VS_1A	0x00	RW	Bit[3:0]: roi_height[11:8] ROI height high byte
0x58DB	DPC_VS_1B	0x0F	RW	Bit[7:0]: roi_height[7:0] ROI height low byte
0x58DC	DPC_VS_1C	0xFF	RW	Bit[7:0]: roi_dp_num Number of DP locations can be saved
0x58DD	DPC_VS_1D	0xFF	RW	Bit[7:0]: roi_dp_num Number of DP locations can be saved
0x58DE	DPC_VS_1E	0xFF	RW	Bit[7:0]: roi_dp_num Number of DP locations can be saved
0x58E6	DPC_VS_26	–	R	Bit[7:0]: w_th
0x58E7	DPC_VS_27	–	R	Bit[7:0]: b_th
0x58E8	DPC_VS_28	–	R	Bit[3:0]: max_dp_num
0x58E9	DPC_VS_29	–	R	Bit[1]: couplet_w_en Bit[0]: couplet_b_en
0x58EA	DPC_VS_2A	–	R	Bit[7:0]: DPCount
0x58EB	DPC_VS_2B	–	R	Bit[7:0]: DPCount
0x58EC	DPC_VS_2C	–	R	Bit[7:0]: DPCount
0x58ED	DPC_VS_2D	–	R	Bit[7:0]: DPROICount
0x58EE	DPC_VS_2E	–	R	Bit[7:0]: DPROICount
0x58EF	DPC_VS_2F	–	R	Bit[7:0]: DPROICount

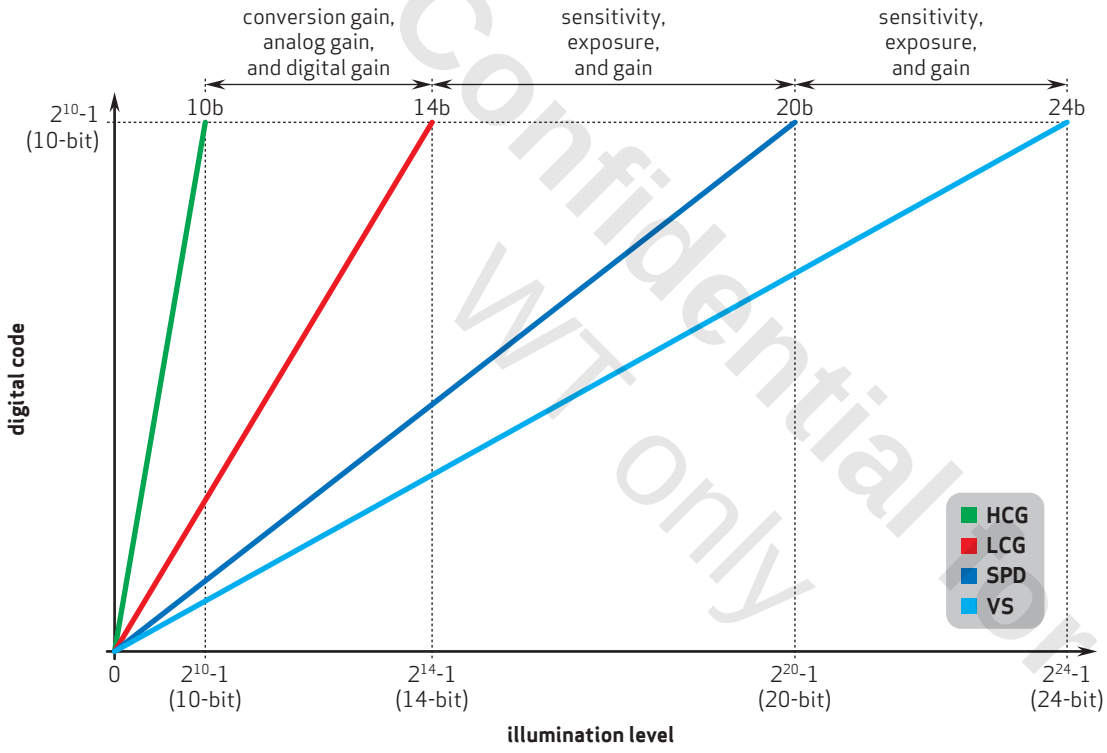
4.6 HDR combine

figure 4-7 shows the principle of HDR combination which takes place in the HDR combine block of the ISP.

- HCG and LCG output are 10-bit linear data.
- In HDR3 mode, long HCG, long LCG, and very short LCG are combined into linear uncompanded 20-bit data. PWL can be used to compand the linear 20-bit data to 16, 14, or 12-bit companded data. In this example, the ratio between HCG and LCG is determined by conversion gain, analog gain, and digital gain. The ratio between long LCG and very short LCG is determined by exposure and gain. The conversion ratio of HCG/LCG is 7.32.
- HDR4 uses long HCG, long LCG, very short LCG, and SPD to achieve 24-bit linear image data. The ratio between VS and SPD is determined by LPD/SPD sensitivity, exposure time, and gain configurations.

note CG ratio value is approximate.

figure 4-7 HDR combine principle diagram



5 image output interface

5.1 image output format

table 5-1 summarizes the output formats which the OX03C10 supports.

table 5-1 image output format summary (sheet 1 of 2)

format		description
4 x 10b RAW data		10-bit HCG+LCG+SPD+VS
HDR3 COMB/ COMB-PWL	uncompanded 20-bit	20-bit combined HDR data
	16/14/12-bit (PWL) combined HDR	16/14/12-bit data companded from 20-bit HDR combined data
HDR3_LFM COMB/COMB-PWL	uncompanded 20-bit + LFM bit	20-bit combined HDR data (by default on MIPI VC0) + LFM-bit (by default on MIPI VC1)
	16/14/12-bit (PWL) combined HDR + LFM bit	16/14/12-bit data companded from 20-bit HDR combined data (by default on MIPI VC0) + LFM-bit (by default on MIPI VC1) LFM replacement enabled
HDR3_SPD COMB/COMB-PWL	uncompanded 20-bit + 10-bit SPD	20-bit combined HDR data (by default on MIPI VC0) + 10-bit SPD {SPD[9:2], LFM_bit, 0} (by default on MIPI VC1)
	16/14/12-bit (PWL) combined HDR + 10-bit SPD	16/14/12-bit data companded from 20-bit HDR combined data (by default on MIPI VC0) + 10-bit SPD {SPD[9:2], LFM_bit, 0} (by default on MIPI VC1) LFM replacement disabled
HDR4 COMB/ COMB-PWL	uncompanded 24-bit	24-bit combined HDR data
	20/16/14/12-bit (PWL) combined HDR	20/16/14/12-bit data compressed from 24-bit HDR combined data
HDR4_LFM COMB/COMB-PWL	uncompanded 24-bit + LFM-bit	24-bit combined HDR data (by default on MIPI VC0) + LFM-bit (by default on MIPI VC1)
	20/16/14/12-bit (PWL) combined HDR+LFM-bit	20/16/14/12-bit data companded from 24-bit HDR combined data (by default on MIPI VC0) + LFM-bit (by default on MIPI VC1) LFM replacement enabled

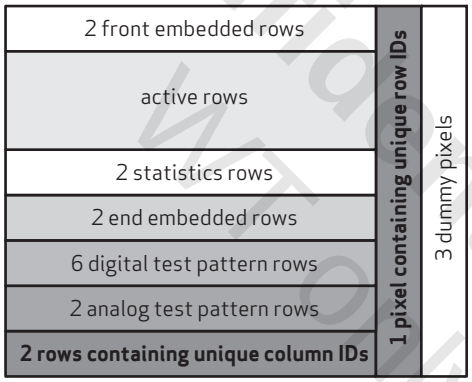
table 5-1 image output format summary (sheet 2 of 2)

format		description
	uncompanded 24-bit + 10-bit SPD	24-bit combined HDR data (by default on MIPI VC0) + 10-bit SPD {SPD[9:2], LFM_bit, 0} (by default on MIPI VC1)
HDR4_SPD COMB/COMB-PWL	20/16/14/12-bit (PWL) combined HDR + 10-bit SPD	20/16/14/12-bit data companded from 24-bit HDR combined data (by default on MIPI VC0) + 10-bit SPD {SPD[9:2], LFM_bit, 0} (by default on MIPI VC1) LFM replacement disabled

The enabling of each one of the modes holds a large sequence of register writes that has to be performed, which in itself configures multiple logic blocks in the sensor. Thus, individual settings will cover those.

The OX03C10 supports the formats shown in **table 5-1** with full output size: horizontal (1920 + 4) x vertical (1280 + 16).

figure 5-1 output image structure



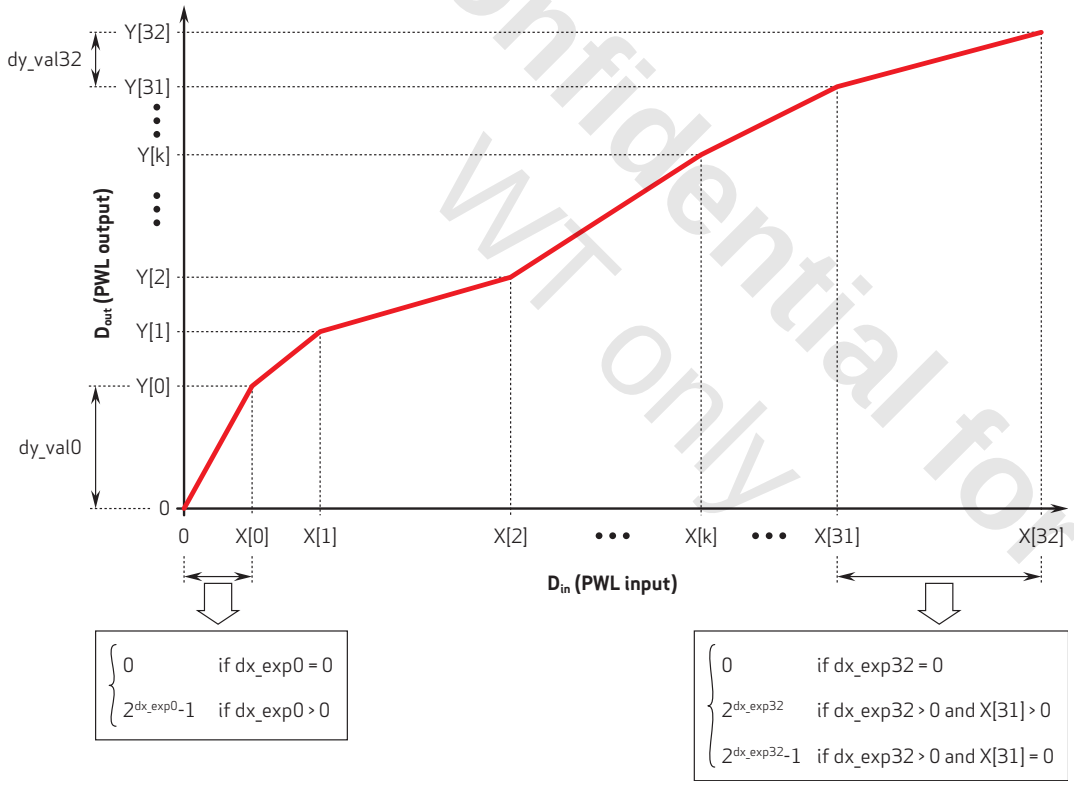
5.2 data compression algorithm

The OX03C10 offers data compression from 24-bit (20-bit) to 20/16/14/12-bit (16/14/12-bit), depending on the operating mode, by providing piecewise linear (PWL) method, utilizing up to 33 configurable knee points. The PWL module is enabled by setting register bit 0x431F[5] = 1 and is used for all output modes. These are defined by the formulas and curves shown in **figure 5-2** and **table 5-2** lists the PWL control registers.

$$D_{out} = Y[k-1] + \frac{D_{in} - X[k-1] \times (Y[k] - Y[k-1])}{X[k] - X[k-1]}$$

$$k \in \{1, 2, ..., 32\}$$

figure 5-2 PWL compression



In **figure 5-2**, the distance between two adjacent knee points of the X-coordinate is in a power of 2, while the output values in the Y-coordinate can be programmable, and the max value is selected based on compression modes pwl_mode (0x431F[4:3]):

- pwl_mode = 0 (12-bit) -> Y[32] = 4095
- pwl_mode = 1 (14-bit) -> Y[32] = 16383
- pwl_mode = 2 (16-bit) -> Y[32] = 65535
- pwl_mode = 3 (20-bit) -> Y[32] = 1048575

The register ranges to set the PWL parameters are 0x5E01~0x5E84.

table 5-2 PWL control registers

address	register name	default value	R/W	description
0x431F	FORMAT_REG_1F	0x00	RW	Bit[7:6]: pack24bit_sel Select one of four packing options for 24-bit format Bit[5]: pwl_en Enable PWL Bit[4:3]: pwl_bits PWL mode (12/14/16/20)
0x5002	ISP_CTRL_02	0x3F	RW	Bit[6]: PWL enable Bit[5]: Retiming enable Bit[4]: Statistic block 4 enable Bit[3]: Statistic block 3 enable Bit[2]: Statistic block 2 enable Bit[1]: Statistic block 1 enable Bit[0]: Statistic block 0 enable

5.3 MIPI HDR output

The OX03C10 supports on-chip HDR combination for both MIPI and DVP output interface, which is described in **section 5.3.1** and **section 5.3.2**.

5.3.1 MIPI

The MIPI interface supports 1, 2, or 4 lanes. The data output format is the same regardless of how many lanes are used with MIPI. The data packet illustrations in this section are to be interpreted line-wise as one consecutive data stream and show the layout of the data packet. The data packet is divided up between the lanes per byte (8 bits) according to MIPI CSI-2.

The OX03C10 can output HDR combined images over single virtual channel and also can output SPD or LFM bits on the separate virtual channel through the MIPI interface. Examples of the various supported output formats with MIPI interface are illustrated in **figure 5-3** through **figure 5-8**. Short-packets denote FS and FE in the virtual channel. The combined HDR image is outputted on virtual channel 0 by default. While in HDR4/3_LFM mode, the LFM-bit frame by default is outputted on virtual channel 1 using MIPI RAW-8 protocol and in HDR4/3_SPD mode, the SPD frame by default is outputted on virtual channel 1 using MIPI RAW-10 protocol.

figure 5-3 HDR combined image with MIPI virtual channel (VC)

figure 5-4 HDR with MIPI VC detail

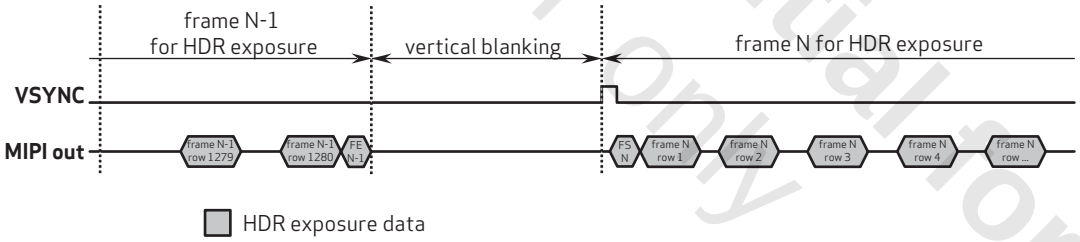


figure 5-5 HDR combined image + LFM-bit with MIPI VC

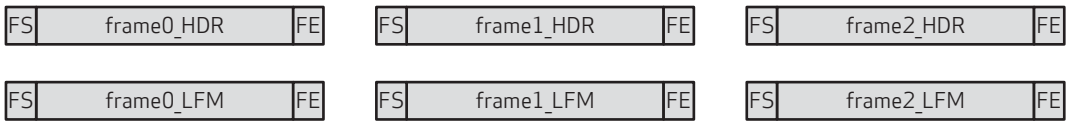


figure 5-6 HDR combined image + LFM-bit with MIPI VC detail

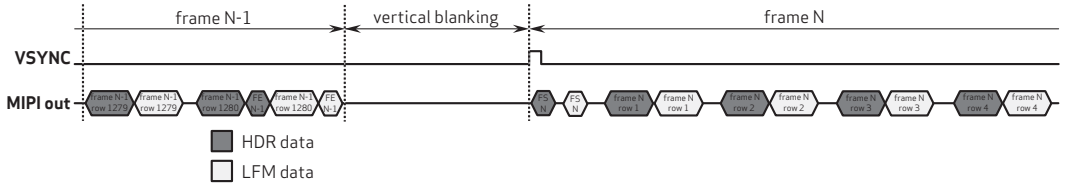


figure 5-7 HDR combined image + 10-bit SPD with MIPI VC

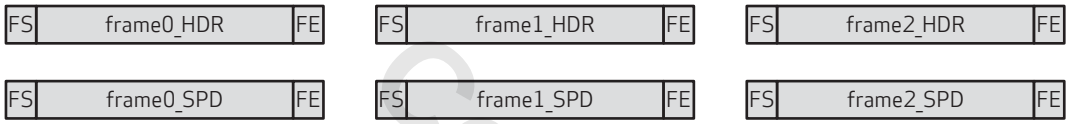
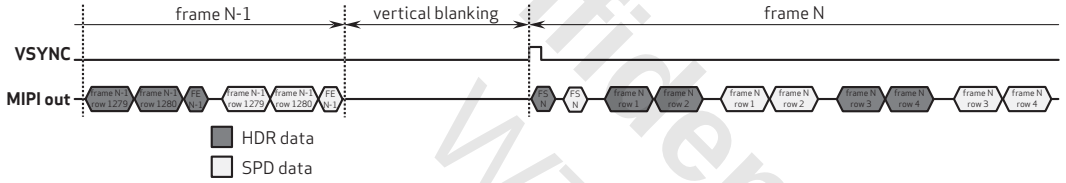


figure 5-8 HDR combined image + 10-bit SPD with MIPI VC detail



As a part of the MIPI protocol, when each row of the image (sensor) data is transmitted to the receiver at the beginning of each package, there is header information appending the rest of the row data being sent out. This header consists of 6 bits (wide), and its value can be specified. The application side of this feature implies that, if the MIPI receiver has the capability to recognize this header individually for each row, it can distinguish which type of output image data each row of incoming MIPI data belongs to (see **figure 5-1**).

table 5-3 defines the default MIPI RAW image data type codes (the header value), which belong to the active image, when being sent out (see **figure 5-1**). The data type codes can change and/or be fixed values, depending on the MIPI RAW image data (packetizing) format.

table 5-3 MIPI RAW image data types (sheet 1 of 2)

default data type	register address	description
2D	–	RAW 14 (active pixel array)
2C	–	RAW 12 (active pixel array)
2B	–	RAW 10 (active pixel array)
2A	–	RAW 8 (active pixel array)
13	0x430D[5:0]	top embedded data rows - data type

table 5-3 MIPI RAW image data types (sheet 2 of 2)

default data type	register address	description
14	0x430E[5:0]	bottom embedded data rows - data type
17	0x430F[5:0]	statistics data rows - data type
12	0x4318[5:0]	digital test pattern rows - data type
15	0x4310[5:0]	analog test pattern rows - data type
16	0x4311[5:0]	unique column ID rows - data type

If the MIPI speed is changed outside the values provided in the original setting files, the MIPI PCLK period must be manually (externally) recalculated and set in register 0x4837 for the sensor, according to the formula:

pclk_period_MIPI = 1000/pclk_freq_MHZ

For example:
If the MIPI PCLK frequency is set to 108 MHz, pclk_period_MIPI = 1000/108 approximately 9 = 0x09 to 0x4837.

table 5-4 MIPI control registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x4800	MIPI_CTRL00	0x04	RW	Bit[7]: sc_valid_opt Select sc_valid Bit[6]: vertical_en Enable vertical clock gating Bit[5]: gate_sc_en Enable clock gating Bit[4]: line_sync_en Enable line sync Bit[2]: pclk_inv Invert output PCLK Bit[1]: first_bit First bit is 1 Bit[0]: lpx_p_sel Select manual parameter or auto parameter

table 5-4 MIPI control registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x4802	MIPI_CTRL02	0x00	RW	Bit[7]: hs_prepare_sel Select manual parameter or auto parameter Bit[6]: clk_prepare_sel Select manual parameter or auto parameter Bit[5]: clk_post_sel Select manual parameter or auto parameter Bit[4]: clk_trail_sel Select manual parameter or auto parameter Bit[3]: hs_exit_sel Select manual parameter or auto parameter Bit[2]: hs_zero_sel Select manual parameter or auto parameter Bit[1]: hs_trail_sel Select manual parameter or auto parameter Bit[0]: clk_zero_sel Select manual parameter or auto parameter
0x4803	MIPI_CTRL03	0x00	RW	Bit[7]: test_en Bit[0]: dphy_test_escape_en
0x4804	MIPI_CTRL04	0xB6	RW	Bit[7:0]: mipi_phy_test_pattern
0x4805	MIPI_CTRL05	0x00	RW	Bit[5]: mipi_pkt_slp_en Option for pre-sleep Bit[4]: slp_change_en Option for pre-sleep Bit[3]: lpda_retim_manu Retiming Bit[2]: lpda_retim_sel Retiming Bit[1]: lpck_retim_manu Retiming Bit[0]: lpck_retim_sel Retiming
0x4806	MIPI_CTRL06	0x40	RW	Bit[7:6]: clk_data_pattern Bit[5]: clk_trail_data Bit[4]: pu_mark_en Enable power up mark Bit[3]: mipi_remot_rst Remote reset Bit[2]: mipi_susp Suspend Bit[1]: smia_lane_ch_en Enable SMIA lane Bit[0]: Output TXLSB first
0x4807	MIPI_CTRL07	0x03	RW	Bit[3:0]: sw_t_lpx Ultra low power mode state delay
0x4808	MIPI_CTRL08	0x18	RW	Bit[7:0]: Wake up delay

table 5-4 MIPI control registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x4809	MIPI_CTRL09	0x4C	RW	Bit[7]: lptx_pd_mode_man_en Manual control enable for lptx_pd_mode_sl Bit[6]: lptx_pd_mode_man Bit[5:0]: lptx_pd_ovlap
0x480A	MIPI_TMG_CTRL	0x2A	RW	Bit[7]: pkt_bit14_opt Bit[6]: frame_blk_out_opt Bit[5]: pre_sleep_opt Bit[1]: line_act_enable Bit[0]: wc_sel_opt
0x480B	MIPI_LANE_CTRL	0x10	RW	Bit[7]: lane1_pn_swap Bit[6:4]: lane1_swap Bit[3]: lane0_pn_swap Bit[2:0]: lane0_swap
0x480C	MIPI_LANE_CTRLC	0x80	RW	Bit[7:5]: clk_lane_swap Bit[4]: lane_num_man_en Bit[3:0]: lane_num_man
0x480E	MIPI_CTRL0E	0x04	RW	Bit[7]: ring_cnt_err_opt Bit[6]: clk_lane_pn_swap Bit[5:4]: frm_end_time_opt Bit[3]: Enable data type2 Bit[2]: Enable img2
0x480F	MIPI_TMG_CTRL_F	0x32	RW	Bit[7]: lane3_pn_swap Bit[6:4]: lane3_swap Bit[3]: lane2_pn_swap Bit[2:0]: lane2_swap
0x4810	MIPI_CTRL10	0xFF	RW	Bit[7:0]: fcnt_max[15:8] Max frame count value
0x4811	MIPI_CTRL11	0xFF	RW	Bit[7:0]: fcnt_max[7:0] Max frame count value
0x4812	MIPI_CTRL04_12	0x12	RW	Bit[5:0]: emb_dt
0x4813	MIPI_CTRL13	0xE4	RW	Bit[7:6]: VC3 Virtual channel ID Bit[5:4]: VC2 Virtual channel ID Bit[3:2]: VC1 Virtual channel ID Bit[1:0]: VC0 Virtual channel ID
0x4814	MIPI_CTRL14	0x2A	RW	Bit[6]: lpkt_dt_sel Data type select Bit[5:0]: dt_man0 Data type

table 5-4 MIPI control registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x4815	MIPI_CTRL15	0x2B	RW	Bit[5:0]: dt_man1 Data type
0x4816	MIPI_CTRL16	0x2B	RW	Bit[5:0]: dt_man2 Data type
0x4817	MIPI_CTRL17	0x00	RW	Bit[7:6]: fcnt_sel Bit[5:4]: lcnt_sel Bit[3:2]: frame_act_sel Bit[1:0]: last_sel
0x4818	MIPI_CTRL18	0x00	RW	Bit[1:0]: hs_zero_min[9:8]
0x4819	MIPI_CTRL19	0x70	RW	Bit[7:0]: hs_zero_min[7:0]
0x481A	MIPI_CTRL1A	0x00	RW	Bit[1:0]: hs_trail_min[9:8]
0x481B	MIPI_CTRL1B	0x3C	RW	Bit[7:0]: hs_trail_min[7:0]
0x481C	MIPI_CTRL1C	0x01	RW	Bit[1:0]: clk_zero_min[9:8]
0x481D	MIPI_CTRL1D	0x2C	RW	Bit[7:0]: clk_zero_min[7:0]
0x481E	MIPI_CTRL1E	0x5F	RW	Bit[7:0]: clk_prepare_max
0x481F	MIPI_CTRL1F	0x30	RW	Bit[7:0]: clk_prepare_min
0x4820	MIPI_CTRL20	0x00	RW	Bit[1:0]: clk_post_min[9:8]
0x4821	MIPI_CTRL21	0x3C	RW	Bit[7:0]: clk_post_min[7:0]
0x4822	MIPI_CTRL22	0x00	RW	Bit[1:0]: clk_trail_min[9:8]
0x4823	MIPI_CTRL23	0x3C	RW	Bit[7:0]: clk_trail_min[7:0]
0x4824	SOF_PCLK_I	0x00	RW	Bit[1:0]: lpx_p_min[9:8]
0x4825	MIPI_CTRL25	0x32	RW	Bit[7:0]: lpx_p_min[7:0]
0x4826	MIPI_CTRL26	0x32	RW	Bit[7:0]: hs_prepare_min
0x4827	MIPI_CTRL27	0x55	RW	Bit[7:0]: hs_prepare_max
0x4828	MIPI_CTRL28	0x00	RW	Bit[1:0]: hs_exit_min[9:8]
0x4829	MIPI_CTRL29	0x64	RW	Bit[7:0]: hs_exit_min[7:0]
0x482A	MIPI_CTRL2A	0x06	RW	Bit[5:0]: ui_hs_zero_min
0x482B	MIPI_CTRL2B	0x04	RW	Bit[5:0]: ui_hs_trail_min
0x482C	MIPI_CTRL2C	0x00	RW	Bit[5:0]: ui_clk_zero_min
0x482D	MIPI_CTRL2D	0x00	RW	Bit[7:4]: ui_clk_prepare_max Bit[3:0]: ui_clk_prepare_min
0x482E	MIPI_CTRL2E	0x34	RW	Bit[5:0]: ui_clk_post_min
0x482F	MIPI_CTRL2F	0x00	RW	Bit[5:0]: ui_clk_trail_min

table 5-4 MIPI control registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x4830	MIPI_CTRL30	0x00	RW	Bit[5:0]: ui_lpx_p_min
0x4831	MIPI_CTRL31	0x64	RW	Bit[7:4]: ui_hs_prepare_max Bit[3:0]: ui_hs_prepare_min
0x4832	MIPI_CTRL32	0x00	RW	Bit[5:0]: ui_hs_exit_min
0x4833	MIPI_CTRL33	0x15	RW	Bit[5:0]: Packet FIFO ready mark
0x4834	MIPI_CTRL34	0x02	RW	Bit[6]: dphy_preamble_en Bit[5:0]: t_dphy_preamble
0x4835	MIPI_CTRL34_35	0x55	RW	Bit[7:0]: dphy_preamble_data
0x4837	MIPI_CTRL37	0x07	RW	Bit[7:0]: MIPI PCLK period Should be changed when PCLK frequency changes
0x4838	MIPI_CTRL38	0x00	RW	Bit[7]: Low power select for lane0 Bit[6]: lp_dir_man0 Low power direction for lane0 Bit[5]: lp_p0_out Lp p0 for lane0 Bit[4]: lp_n0_out Lp n0 for lane0 Bit[3]: Low power select for lane1 Bit[2]: lp_dir_man1 Low power direction for lane1 Bit[1]: lp_p1_out Lp p0 for lane1 Bit[0]: lp_n1_out Lp n0 for lane1
0x4839	MIPI_CTRL39	0x00	RW	Bit[7]: Low power select for lane2 Bit[6]: lp_dir_man2 Low power direction for lane2 Bit[5]: lp_p2_out Lp p0 for lane2 Bit[4]: lp_n2_out Lp n0 for lane2 Bit[3]: Low power select for lane3 Bit[2]: lp_dir_man3 Low power direction for lane3 Bit[1]: lp_p3_out Lp p0 for lane3 Bit[0]: lp_n3_out Lp n0 for lane0
0x483C	MIPI_CTRL3C	0x10	RW	Bit[7:0]: t_clk_pre

table 5-4 MIPI control registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x483D	MIPI_CTRL3D	0x00	RW	Bit[3]: lp_ck_sel0 Low power select for clock lane Bit[1]: lp_ck_p_out0 Lp clock lane p Bit[0]: lp_ck_n_out0 Lp clock lane n
0x483E	MIPI_CTRL3E	–	R	Bit[7:0]: fcnt_rd[15:8] Frame count value
0x483F	MIPI_CTRL3F	–	R	Bit[7:0]: fcnt_rd[7:0] Frame count value
0x484A	MIPI_CTRL4A	0x3F	RW	Bit[5]: slp_lp_pon_man Sleep power down select Bit[4]: slp_lp_pon_da lp_pon data Bit[3]: slp_lp_pon_ck_da lp_pon clock lane data Bit[2]: mipi_slpst_man Manual sleep state Bit[1]: slpst_clk_lane Clock lane sleep state Bit[0]: slpst_data_lane Data lane sleep state
0x484B	MIPI_CTRL4B	0x47	RW	Bit[6]: line_start_sel 0: Line start short packet from VFIFO non-empty 1: Line start short packet from VFIFO ready Bit[5]: r_eof_man EOF select Bit[4]: Virtual channel select Bit[3]: Data scramble enable Bit[2]: eof_busy_en EOF busy select Bit[1]: Clock start select Bit[0]: SOF select
0x484C	MIPI_CTRL4C	0x00	RW	Bit[0]: fcnt_inact Disable frame count
0x484E	MIPI_CTRL4E	0x10	RW	Bit[7:0]: Frame end delay
0x484F	MIPI_CTRL4F	0x00	RW	Bit[7:4]: vc_height_sel Bit[0]: line_sleep_en

table 5-4 MIPI control registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x4850	MIPI_CTRL50	0x42	RW	Bit[6]: dphy12_frm_blk_opt Bit[5]: Deskew output enable Bit[4]: Deskew manual trigger Bit[3]: Initial deskew disable Bit[2]: Frame deskew disable Bit[1]: alt_cal_dis Bit[0]: DPHY1, 2 enable
0x4851	MIPI_CTRL51	0xAA	RW	Bit[7:0]: dskew_hsdat Deskew data
0x4852	MIPI_CTRL52	0xFF	RW	Bit[7:0]: Deskew sync data
0x4853	MIPI_CTRL53	0x8A	RW	Bit[7:0]: Deskew start delay
0x4854	MIPI_CTRL54	0x05	RW	Bit[7:0]: Frame deskew width
0x4855	MIPI_CTRL55	0x1C	RW	Bit[7:0]: Initial deskew width
0x4856	MIPI_CTRL56	0x01	RW	Bit[7:0]: Frame deskew interval
0x4857	MIPI_CTRL57	0x08	RW	Bit[3]: hs_same_time Bit[0]: deskew_en_man
0x4858	MIPI_CTRL58	0x1C	RW	Bit[7:0]: alt_deskew_width
0x4870	MIPI_CTRL70	0x00	RW	Bit[7]: giic_ctrl_en
0x4871	MIPI_CTRL71	0x10	RW	Bit[6:4]: prbs_deg_opt 000: prbs_disable 001: Deg92 010: Deg113 011: Deg16 100: Deg18 101: 4444pattern Bit[2]: dphy_prbs9_opt
0x4872	MIPI_CTRL72	0x00	RW	Bit[1:0]: prbs_seed_lane0
0x4873	MIPI_CTRL73	0x00	RW	Bit[7:0]: prbs_seed_lane0
0x4874	MIPI_CTRL74	0xFF	RW	Bit[7:0]: prbs_seed_lane0
0x4875	MIPI_CTRL75	0x00	RW	Bit[7:0]: prbs_seed_lane1
0x4876	MIPI_CTRL76	0xFE	RW	Bit[7:0]: prbs_seed_lane1
0x4877	MIPI_CTRL77	0x00	RW	Bit[7:0]: prbs_seed_lane2
0x4878	MIPI_CTRL78	0xFD	RW	Bit[7:0]: prbs_seed_lane2
0x4879	MIPI_CTRL79	0x00	RW	Bit[7:0]: prbs_seed_lane3
0x487A	MIPI_CTRL7A	0xFC	RW	Bit[7:0]: prbs_seed_lane3

5.3.2 DVP

The OX03C10 can output pixel data on a 12-bit DVP bus. In DVP mode, the sensor can output 12b compressed data from either HDR3 or HDR4 combined, and VSYNC indicates the start of the output. The HREF signal will be asserted when the pixel data output on DVP (either HDR3 or HDR4) is valid.

HREF, VSYNC, and PCLK are configured as video output ports as shown in **figure 5-9**. The leading edge of VSYNC is triggered by an internal SOF signal and the interval between the internal SOF signal and VSYNC is controlled by v_sync_delay (0x4704~0x4706 in unit of PCLK periods). VSYNC pulse width is set by registers 0x4700~0x4703 as in the following formula:

VSYNC width = [VSYNC width line × t_{ROW}] + [VSYNC width pixel × t_{PCLK}]

where:

t_{ROW} is row period

t_{PCLK} is PCLK period

VSYNC width line: {0x4700, 0x4701}

VSYNC width pixel: {0x4702, 0x4703}

figure 5-9 DVP setup/hold time diagram

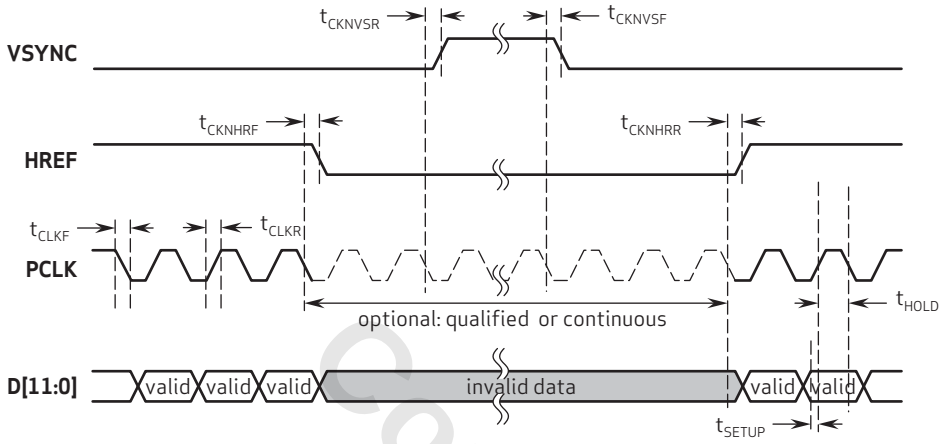
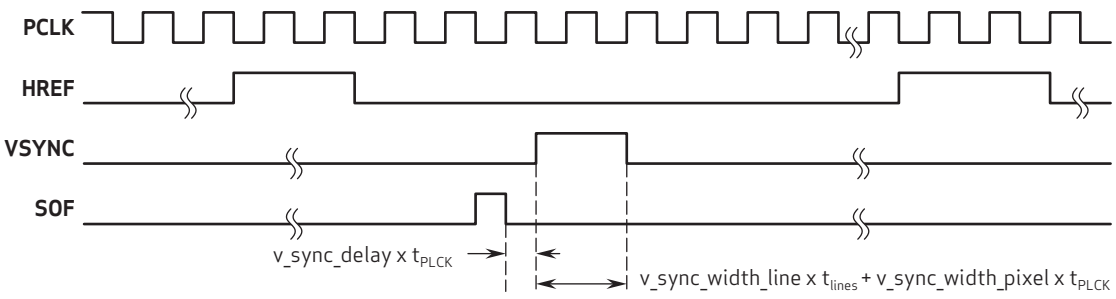


table 5-5 DVP setup/hold time

symbol	parameter	min	typ	max	unit
t_{CKNVSR}	PCLK falling edge to VSYNC rising edge delay	–	TBD	–	ns
t_{CKNVSF}	PCLK falling edge to VSYNC falling edge delay	–	TBD	–	ns
t_{CKNHRF}	PCLK falling edge to HREF falling edge delay	–	TBD	–	ns
t_{CKNHRR}	PCLK falling edge to HREF rising edge delay	–	TBD	–	ns
t_{CLKF}	PCLK fall time	–	TBD	–	ns
t_{CLKR}	PCLK rise time	–	TBD	–	ns
t_{SETUP}	data setup time	TBD	TBD	TBD	ns
t_{HOLD}	data hold time	TBD	TBD	TBD	ns

figure 5-10 DVP diagram

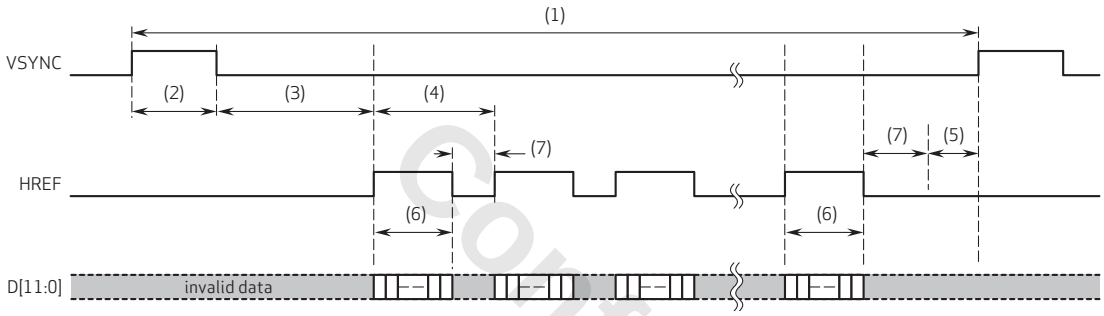


The OX03C10 supports walking one test pattern to test the connection between the sensor and the backend processor. The test pattern is enabled by register bit 0x4708[0]. By default, the image data bits are aligned with pins D[11:0].

The driver strength of the DVP pins can be configured by register bits 0x3009[6:5].

The DVP output is qualified by VSYNC and HREF and the timing is shown in **figure 5-11**.

figure 5-11 DVP timing diagram



(1) frame period

(2) VSYNC width

(3) VSYNC to HREF

(4) line period

(5) HREF to VSYNC

(6) active pixel

(7) horizontal blanking

(8) last horizontal blanking to VSYNC high

VSYNC pulse width is programmable from 1 CLK to 1 frame (high period = #lines + #pixels): registers 0x4700~0x4701: #lines, registers 0x4702~0x4703: #pixels

N = VS-delay in whole rows × image width

Height = rows × image width

table 5-6 DVP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4700	VSYNC_WIDTH_LINE_H	0x00	RW	Bit[7:0]: vsync_width_line[15:8]
0x4701	VSYNC_WIDTH_LINE_L	0x00	RW	Bit[7:0]: vsync_width_line[7:0]
0x4702	VSYNC_WIDTH_PIXEL_H	0x02	RW	Bit[7:0]: vsync_width_pixel[15:8]
0x4703	VSYNC_WIDTH_PIXEL_L	0x00	RW	Bit[7:0]: vsync_width_pixel[7:0]

table 5-6 DVP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4704	VSYNC_DELAY_H	0x00	RW	Bit[7:0]: vsync_delay[23:16]
0x4705	VSYNC_DELAY_M	0x01	RW	Bit[7:0]: vsync_delay[15:8]
0x4706	VSYNC_DELAY_L	0x00	RW	Bit[7:0]: vsync_delay[7:0]
0x4707	POLARITY_CTRL	0x00	RW	Bit[6]: Invert output bits Bit[2]: href_polarity 0: Active high 1: Active low Bit[1]: vsync_polarity 0: Active high 1: Active low
0x4708	MOTO_ORDER	0x00	RW	Bit[3]: moto_test_mode When set, only change moto data every other clock Bit[2]: moto_test_bit10 Enable 10-bit test Bit[1]: moto_test_bit8 Enable 8-bit test Bit[0]: moto_test_enable Enable moto test
0x4709	BYP_SELECT	0x00	RW	Bit[5]: data_bit_shift Used in moto mode to select between bit swap methods when using 16 bits
0x470A	R_FIFO	0x00	RW	Bit[1]: dvp_sync_pclk_pol Invert output PCLK within DVP_SYNC module Bit[0]: dvp_sync_pll_pclk_inv Invert input PLL PCLK within DVP_SYNC module
0x470B	CHANNEL_SELECT	0x0F	RW	Bit[3]: channel3_sel Bit[2]: channel2_sel Bit[1]: channel1_sel Bit[0]: channel0_sel
0x470C	DVP_SYNC_CONTROL	0x01	RW	Bit[1]: dvp_bypass Bit[0]: dvp_vsync_en

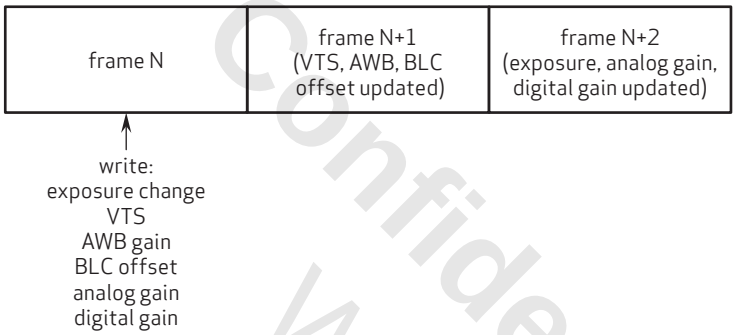
5.4 register writing

5.4.1 suggestion for writing register value just after VSYNC or FS

In order to avoid register settings for one frame being split into two frames by mistake, the register value should be written as early as possible after VSYNC or FS. If the register values are written during frame N, new parameters can be seen in frame:

- n+1: AWB gain, BLC offset, VTS
- n+2: exposure, analog gain, digital gain, and conversion gain

figure 5-12 parameter update schedule



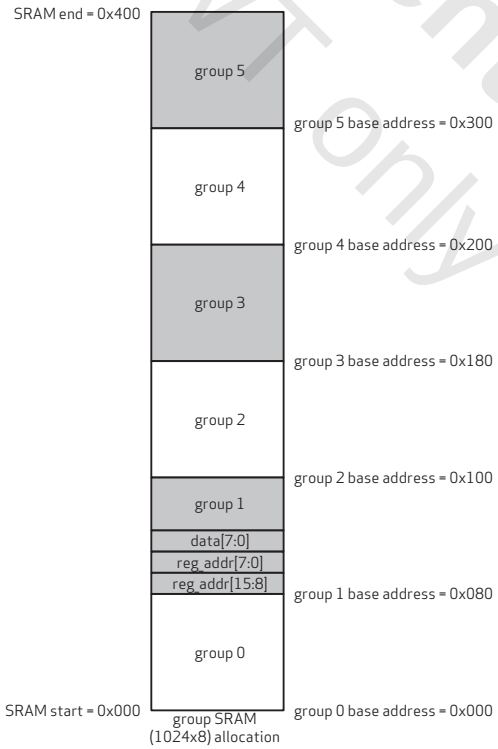
5.5 group hold

The OX03C10 supports a group hold function, which is used to manipulate registers programmed into the sensor. Multiple sets of register settings, which are called groups, can be stored into different virtual memory spaces (hold operation) during sensor initiation and programmed into individual registers later on when desired (launch operation).

The idea is to allow for better synchronization and frame alignment of setting changes between frames to ensure that a certain set of register changes occur in a single time window, in a single frame, or over a number of frames, depending on the way the group hold has been set. Overall, the set of registers are guaranteed to be written prior to the internal latch at the frame boundary. In summation, the group hold functionality allows configuration of many of the sensor's parameters in a single instance, something that cannot be applied or guaranteed when using direct SCCB register writes.

The OX03C10 supports up to six groups (0 to 5) and they all share 1024 bytes of memory (SRAM) used to store register settings. The maximum size of each group is programmable by adjusting the start address amongst the groups (see **figure 5-13**). By default, groups 0 to 3 are assigned 128 bytes each. Groups 4 and 5 are assigned 256 bytes each. Regarding groups 0 to 3, for each register in the setting, three bytes of SRAM space are required for storage of a setting, the register high byte address, the register low byte address, and the desired byte value to be written. Thus, utilizing the first four groups, a total of 170 (768 bytes/3) register values can be changed. Groups 4 and 5 have somewhat different behaviors and structures dedicated to embedded data (see **section 5.6**). They cannot be reconfigured to perform group hold operations as in the other groups (ordinary register settings write) case.

figure 5-13 groups default SRAM allocation



5.5.1 group configuration

The starting address of each group (group base address) is programmed by writing to registers addresses 0x3200~0x3205. The value writing into these registers is the physical SRAM address divided by 16. For example, for the SRAM configuration of groups 0 to 3, registers 0x3200~0x3203 can be set to 0x00, 0x10, 0x28, and 0x38, respectively.

By properly setting the group base address registers previously mentioned, the SRAM can be configured into 1~4 groups. For example, to use group 1 and group 3, set register 0x3201 to 0x00 and register 0x3203 to 0x38. The values to registers 0x3200 and 0x3202 do not matter as long as the hold operations are not performed on these two groups.

5.5.2 group hold

After the groups are configured properly, users can perform the hold operation to store register settings into the SRAM of each group. The hold of each group starts and ends with the group access control register 0x3208. The lower four bits of 0x3208 control which group to access. The upper 4 bits control the start (0x0: hold start) and end (0x1: hold end) of the hold operation.

The example setting below shows the sequence to hold group 0 and group 1:

```
6C 3208 00; group 0 hold start

6C 3800 11; first register into group 0

6C 3911 22; second register into group 0

6C 3208 10; group 0 hold end

6C 3208 01; group 1 hold start

6C 3810 11; first register into group 1

6C 3921 22; second register into group 1

6C 3931 33; third register into group 1

6C 3208 11; group 1 hold end
```

Group 0 holds two registers and group 1 holds three registers in the example shown above. Keep in mind not to hold more than the maximum register numbers for each group as defined in the group configuration step.

5.5.3 group launch

After the contents of each group are defined in the hold operation, all registers belonging to each group are stored in the SRAM and ready to be written into the target registers (i.e., launch of that group). There are five launch modes as described in the sections below, using the group hold setup from the previous section.

5.5.3.1 launch mode 1 – quick manual launch

Manual launch is enabled by setting the group switch control register 0x3211 to 0.

Quick manual launch is achieved by writing to control register 0x3208. The value written into this register is 0xEX, the upper 4 bits (0xE) are the quick launch command and the lower four bits (0xX) are the group number. For example, if the user wants to launch group 0, they would write the value 0xE0 to 0x3208. Then, the contents of group

0 will be written to the target registers immediately after the sensor receives this command through the SCCB. The following is a setting example:

```
6C 3211 00; manual launch on
6C 3208 E0; quick launch group 0
6C 3208 E1; quick launch group 1
```

5.5.3.2 launch mode 2 – delay manual launch

Delay manual launch is achieved by writing to register 0x3208. The value written into this register is 0xAX, where the upper four bits (0xA) are the delay launch command and the lower four bits (0xX) are the group number. For example, if the user wants to launch group 1, they write the value 0xA1 to 0x3208. Then, the contents of group 1 will be written to the target registers. The difference with mode 1 is that the writing will wait for an internally defined time spot in vertical blanking, thus delaying until the current frame sampling ends. The following is a setting example:

```
6C 3211 00; manual launch on
6C 3208 A0; delay launch group 0
6C 3208 A1; delay launch group 1
```

5.5.3.3 launch mode 3 – quick auto launch

Quick auto launch works like the mode 1, but it is different in that it will return to a specified group automatically. This is controlled by the register 0x3211, where register bit 0x320D[4] enables mode and register bits 0x320D[1:0] control which group to return. The auto launch will automatically switch from group 0 to 1 to 2 to 3. If group auto launch starts from the low number group, returns to high number group, and the user would like to skip the middle group, set that group number to 0. If it is not set to 0, the sensor will switch to the middle group first. Also, the user will need to set a target return group number to be non-zero. Frame numbers 0x320A, 0x320B, 0x320C, and 0x320D for groups 0,1, 2, and 3, respectively, control how many frames to stay before returning. The operation can be better understood with a setting example:

```
6C 3211 11;
6C 320A 04; stay in group 0 for 4 frames
6C 3208 01; number of frames to stay in group 1
6C 3208 E0; quick launch group 0
```

5.5.3.4 launch mode 4 – delay auto launch

Delay auto launch works like mode 2 in the delay launch part and like mode 3 in the return part.

The operation can be better understood with a setting example:

```
6C 3211 11; Bit[1:0]: 1, return to group 1, Bit[4]: enable auto switch
6C 320A 04; stay in group 0 for 4 frames
6C 3208 01; number of frames to stay in group 1
6C 3208 A0; delay launch group 0
```

In this example, the sensor will delay launch group 0, stay at group 0 for four frames, and then return to group 1.

5.5.3.5 launch mode 5 – repeat launch

Repeat launch is enabled by register bit 0x3211[5]. It can support up to four groups repeatedly. Frame numbers 0x320A, 0x320B, 0x320C, and 0x320D for groups 0, 1, 2, and 3, respectively, control how many frames to stay before jumping to the next one. In this mode, the launch is repeated automatically between the first group (must be group 0) and the second group (can be either one of groups 1~3). Any group number set at 0 will be skipped.

The operation can be better understood with a setting example:

```
6C 320A 02; Bit[7:0]: 2, stay 2 frames in group 0

6C 320B 03; Bit[7:0]: 3, stay 3 frames in group 1

6C 320C 00; Bit[7:0]: 0, don't stay in group 2

6C 320D 08; Bit[7:0]: 8, stay 8 frames in group 3

6C 3211 30; Bit[5]: repeat switch enable, [4] context switch enable

6C 3208 A0; always use a0 for repeat launch
```

In this example, the sensor will delay launch group 0, stay at group 0 for 2 frames, switch to group 1 for 3 frames, and group 3 for 8 frames. Then it will switch back to group 0 for 2 frames, group 1 for 3 frames, group 3 for 8 frames, and so on.

In manual mode, a register write burst can be triggered with a SCCB write and the specified group's register settings will be written to the register interface. In automatic mode, two groups are selected and the number of frames each group should be active. The sensor will continuously update the register settings accordingly.

It can be noted that if a certain group hold number is desired to be disabled, the adjacent register for 'stay for a number of frames' for that group number (0x320A~ 0x320D), can be set to 0, thus eliminating the possibility for that group to execute.

Additionally, the OX03C10 supports group record and group launch, not only while in stream mode, but also while in sleep mode, in order to make the first frame with the updated configuration when the sensor is put into streaming. This is especially emphasized for exposure and gain (analog and digital) changes. **table 5-7** shows group hold control registers.

table 5-7 group hold control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x3200	GRP_HOLD_CTRL_0	0x00	RW	Bit[7:0]: Ba0 Group 0 base address
0x3201	GRP_HOLD_CTRL_1	0x08	RW	Bit[7:0]: Ba1 Group 1 base address
0x3202	GRP_HOLD_CTRL_2	0x10	RW	Bit[7:0]: Ba2 Group 2 base address
0x3203	GRP_HOLD_CTRL_3	0x18	RW	Bit[7:0]: Ba3 Group 3 base address

table 5-7 group hold control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x3204	GRP_HOLD_CTRL_4	0x20	RW	Bit[7:0]: Ba4 Group 4 base address
0x3205	GRP_HOLD_CTRL_5	0x30	RW	Bit[7:0]: Ba5 Group 5 base address
0x3208	GRP_HOLD_8	–	W	Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: V-blank group launch 0110: H-blank group launch 1110: Immediate group launch Bit[3:0]: group_id 0000: Group bank 0 0001: Group bank 1 0010: Group bank 2 0011: Group bank 3
0x320A	GRP_HOLD_CTRL_A	0x00	RW	Bit[7:0]: grp0_frms Number of frames staying in group0
0x320B	GRP_HOLD_CTRL_B	0x00	RW	Bit[7:0]: grp1_frms Number of frames staying in group1
0x320C	GRP_HOLD_CTRL_C	0x00	RW	Bit[7:0]: grp2_frms Number of frames staying in group2
0x320D	GRP_HOLD_CTRL_D	0x00	RW	Bit[7:0]: grp3_frms Number of frames staying in group3
0x320E~ 0x320F	RSVD	–	–	Reserved
0x3210	GRP_HOLD_CTRL_10	0x00	RW	Bit[5]: first_frame_context_en Bit[4]: FSIN enable in context switch Bit[1:0]: FSIN group number
0x3211	GRP_HOLD_CTRL_11	0x61	RW	Bit[6]: grf_vrf_en Enable read-back checking Bit[5]: Repeat context switch enable Bit[4]: Context switch enable Bit[1:0]: sw_back_grp_reg When in context switch mode, but not repeat switch, switch back group number
0x3213	GRP_HOLD_CTRL_13	0x02	RW	Bit[3:0]: emb_line_num Number of embedded lines
0x3214	GRP_HOLD_CTRL_14	0x00	RW	Bit[7:0]: Padding data

table 5-7 group hold control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x3215	GRP_HOLD_CTRL_15	0xCD	RW	Bit[7:6]: hblk_ctrl Next embedded line start options Bit[5]: padding_md2 Bit[4]: frame_cnt_trig Bit[3]: emline_eof_en Bit[2]: emline_sof_en Bit[1]: Send address in embedded rows Bit[0]: tag_en Send tag in embedded rows
0x3216	GRP_HOLD_CTRL_16	0xDA	RW	Bit[7:0]: Tag data
0x3217	GRP_HOLD_CTRL_17	0x09	RW	Bit[7:0]: emb_width_offset
0x3218	GRP_HOLD_CTRL_18	0x06	RW	Bit[5]: front_emb_size_man Manual front embedded row size Bit[4]: end_emb_size_man Manual end embedded row size Bit[2]: mem_crc_en Output CRC of configuration for each embedded Bit[1]: emb_crc_en Bit[0]: emb_crc_dat_inv
0x3219	MEM_CRC_FAULT_ MASKED	0x0E	RW	Bit[3]: wd_fault_inject_mask Mask manual fault injection to watchdog Bit[2]: grp_verif_fault_mask Mask read-back check fault for group 0~3 Bit[1]: grp_mem_crc_fault_mask Mask memory CRC fault for group 0~3 Bit[0]: emb_mem_crc_fault_mask Mask memory CRC fault for embedded rows
0x321A	GRP_HOLD_SRAM_T0	0x06	RW	Bit[5:0]: SRAM test control signals
0x321B	GRP_HOLD_SRAM_T1	0x06	RW	Bit[7:0]: SRAM test control signals
0x321C	EMB_SRAM_T0	0x06	RW	Bit[5:0]: emb_sram_tstctrl SRAM test control signals for embedded FIFO
0x321D	EMB_SRAM_T1	0x06	RW	Bit[7:0]: emb_sram_tstctrl SRAM test control signals for embedded FIFO
0x321E	GRP_HOLD_STATUS	–	R	Bit[5:0]: crc_status Result of CRC check for SRAM

table 5-7 group hold control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x321F	MEM_CRC_FAULT_ STATUS	–	R	Bit[7]: Memory fault state Bit[3]: wd_fault_inject_status Manually injected fault to watchdog Bit[2]: grp_verif_fault Read-back check fault of group 0~3 Bit[1]: grp_mem_crc_fault Memory check fault of group 0~3 Bit[0]: emb_mem_crc_fault Memory check fault of embedded rows
0x3220	GRP_HOLD_LEN_0	–	R	Bit[7:0]: len0_rd Group 0 length
0x3221	GRP_HOLD_LEN_1	–	R	Bit[7:0]: len1_rd Group 1 length
0x3222	GRP_HOLD_LEN_2	–	R	Bit[7:0]: len2_rd Group 2 length
0x3223	GRP_HOLD_LEN_3	–	R	Bit[7:0]: len3_rd Group 3 length
0x3224	GRP_HOLD_LEN_4	–	R	Bit[7:0]: len4_rd Group 4 length
0x3225	GRP_HOLD_LEN_5	–	R	Bit[7:0]: len5_rd Group 5 length
0x3226	GRP_HOLD_CTRL_26	–	R	Bit[7:0]: Frame counter group 0
0x3227	GRP_HOLD_CTRL_27	–	R	Bit[7:0]: Frame counter group 1
0x3228	GRP_HOLD_CTRL_28	–	R	Bit[7:0]: Frame counter group 2
0x3229	GRP_HOLD_CTRL_29	–	R	Bit[7:0]: Frame counter group 3
0x322A~ 0x322C	RSVD	–	–	Reserved
0x322D	GRP_HOLD_CTRL_2D	–	R	Bit[7:0]: grp_sel_real Selected group
0x322E	GRP_HOLD_ERR_ STATUS	–	R	Bit[2]: grp_verif_err Read-back check result of group 0-3 Bit[1]: grp_mem_crc_err Memory check result of group 0-3 Bit[0]: emb_mem_crc_err Memory check result of embedded rows
0x322F	WD_INJECT_FAULT	0x00	RW	Bit[0]: Inject fault to watchdog manually
0x3230	FRONT_EMB_SIZE_H	–	R	Bit[7:0]: Size of front embedded rows[15:8]

table 5-7 group hold control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x3231	FRONT_EMB_SIZE_L	–	R	Bit[7:0]: Size of front embedded rows[7:0]
0x3232	END_EMB_SIZE_H	–	R	Bit[7:0]: Size of end embedded rows[15:8]
0x3233	END_EMB_SIZE_L	–	R	Bit[7:0]: Size of end embedded rows[7:0]

5.5.4 group hold CRC

The CRC over group hold (groups 0 to 3) is calculated using CRC-32C (Castagnoli). The polynomials are 0x1EDC6F41 (normal). **table 5-8** shows group hold CRC registers. The group hold memory CRC register values (0x3234~0x324B) are inverted. The 32-bit checksum can be found using the following formula:

CRC value = ~CRC_byte0 + (~CRC_byte1 << 8) + (~CRC_byte2 << 16) + (~CRC_byte3 << 24)

table 5-8 group hold CRC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3234	GRP_CRC_0_3	–	R	Bit[7:0]: Group 0 mem CRC, byte 3
0x3235	GRP_CRC_0_2	–	R	Bit[7:0]: Group 0 mem CRC, byte 2
0x3236	GRP_CRC_0_1	–	R	Bit[7:0]: Group 0 mem CRC, byte 1
0x3237	GRP_CRC_0_0	–	R	Bit[7:0]: Group 0 mem CRC, byte 0
0x3238	GRP_CRC_1_3	–	R	Bit[7:0]: Group 1 mem CRC, byte 3
0x3239	GRP_CRC_1_2	–	R	Bit[7:0]: Group 1 mem CRC, byte 2
0x323A	GRP_CRC_1_1	–	R	Bit[7:0]: Group 1 mem CRC, byte 1
0x323B	GRP_CRC_1_0	–	R	Bit[7:0]: Group 1 mem CRC, byte 0
0x323C	GRP_CRC_2_3	–	R	Bit[7:0]: Group 2 mem CRC, byte 3
0x323D	GRP_CRC_2_2	–	R	Bit[7:0]: Group 2 mem CRC, byte 2
0x323E	GRP_CRC_2_1	–	R	Bit[7:0]: Group 2 mem CRC, byte 1
0x323F	GRP_CRC_2_0	–	R	Bit[7:0]: Group 2 mem CRC, byte 0
0x3240	GRP_CRC_3_3	–	R	Bit[7:0]: Group 3 mem CRC, byte 3
0x3241	GRP_CRC_3_2	–	R	Bit[7:0]: Group 3 mem CRC, byte 2
0x3242	GRP_CRC_3_1	–	R	Bit[7:0]: Group 3 mem CRC, byte 1
0x3243	GRP_CRC_3_0	–	R	Bit[7:0]: Group 3 mem CRC, byte 0
0x3244	GRP_CRC_4_3	–	R	Bit[7:0]: Group 4 mem CRC, byte 3

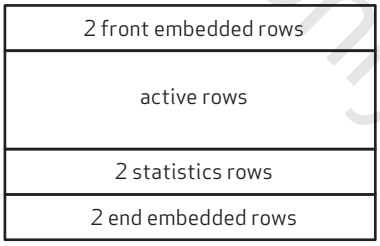
table 5-8 group hold CRC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3245	GRP_CRC_4_2	–	R	Bit[7:0]: Group 4 mem CRC, byte 2
0x3246	GRP_CRC_4_1	–	R	Bit[7:0]: Group 4 mem CRC, byte 1
0x3247	GRP_CRC_4_0	–	R	Bit[7:0]: Group 4 mem CRC, byte 0
0x3248	GRP_CRC_5_3	–	R	Bit[7:0]: Group 5 mem CRC, byte 3
0x3249	GRP_CRC_5_2	–	R	Bit[7:0]: Group 5 mem CRC, byte 2
0x324A	GRP_CRC_5_1	–	R	Bit[7:0]: Group 5 mem CRC, byte 1
0x324B	GRP_CRC_5_0	–	R	Bit[7:0]: Group 5 mem CRC, byte 0

5.6 embedded data

Additional information about sensor configuration, such as frame counter and exposure time and gain, can be added as embedded rows in the video stream. The embedded data contains values of registers from a programmable range. It is added before the active image area (2 front/top embedded rows), and/or after statistics data (2 end/bottom embedded rows) of the video stream. The statistics data consists of two rows and are appended after the active image area. Depending on the output format used and the type of embedded and/or statistic data, the output (crop and windows) size must be increased by the corresponding amount of rows to accommodate for the extra lines of the data. **figure 5-14** shows the structure of the outputted image when embedded and statistics data are enabled.

figure 5-14 image output



The front and end embedded information can be displayed in the image by setting register bits 0x4317[5], 0x4317[4], respectively. It is read using a specific read bus from the registers. The normal register bus will not be used since it will be occupied.

5.6.1 embedded data format at output

Different address ranges can be set for the front embedded rows (through group 4) and the end embedded rows (through group 5) in group hold. Each register value is preceded by the tag specified by register 0x3216. As the output data width is more than 8 bits, the tag and register values will be MSB aligned.

The number of registers transmitted is dependent on the register start and end address. A number of output registers is required to be multiple of 4. The last 8 bytes in the embedded data rows are two CRC values (4 bytes each), group hold memory CRC (MCRC), and embedded data CRC (CRC), preceded with the tag value before each byte and are laid out in MSB to LSB (left to right) order along the row (see **figure 5-15**). The group hold memory CRC data is calculated on addresses and data specified in group hold configuration for the embedded rows. The embedded data CRC is calculated only on the data and MCRC, all other info like tag will be ignored. The CRCs over embedded data are calculated using CRC-32C (Castagnoli). The polynomials are 0x1EDC6F41 (normal) and if users pass through all the data bytes with the 8 CRC bytes transmitted through their CRC calculation, the result will always equal a fixed number 0x48674BC7. The embedded data row will automatically continue on the next row. When the whole range has been output, the two CRC data will be appended. If the requested range does not fit within two embedded data rows, the range will be truncated with an appended CRC value. If there is any remaining space on the embedded rows, they will be terminated by 0x00 after the last CRC byte (CRC0). **figure 5-15** shows the data format of the embedded data.

figure 5-15 embedded data format diagram

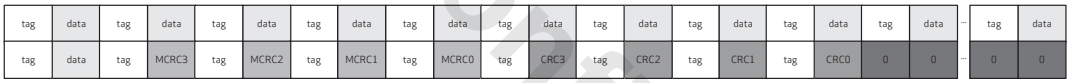


table 5-9 embedded data registers and initialization (sheet 1 of 2)

step	registers	comment
1		Embedded lines are configured through group hold functional block. Group 4 is for front embedded row. Set address ranges that are going to be outputted on front embedded rows.
	0x3208 = 0x04	1. Set group 4 to start recording register ranges.
	0x3800 = 0x02	2. Execute a SCCB write - configuring two consecutive registers values starting from 0x3800 address to be outputted over embedded rows.
	0x4800 = 0x02	3. Execute a SCCB write - configuring two consecutive registers values starting from 0x4800 address to be outputted over embedded rows.
	0x3208 = 0x14	4. Set group 4 to stop recording register ranges.
		Set address ranges that are going to be outputted on end embedded rows.
	0x3208 = 0x05	5. Set group 5 to start recording register ranges.
	0x3500 = 0x10	6. Execute a SCCB write - configuring 16 consecutive registers values starting from 0x3500 address, to be outputted over embedded rows.
	0x3600 = 0x19	7. Execute a SCCB write - configuring 16 consecutive registers values starting from 0x4800 address, to be outputted over embedded rows.
	0x3208 = 0x15	8. Set group 5 to stop recording register ranges.

table 5-9 embedded data registers and initialization (sheet 2 of 2)

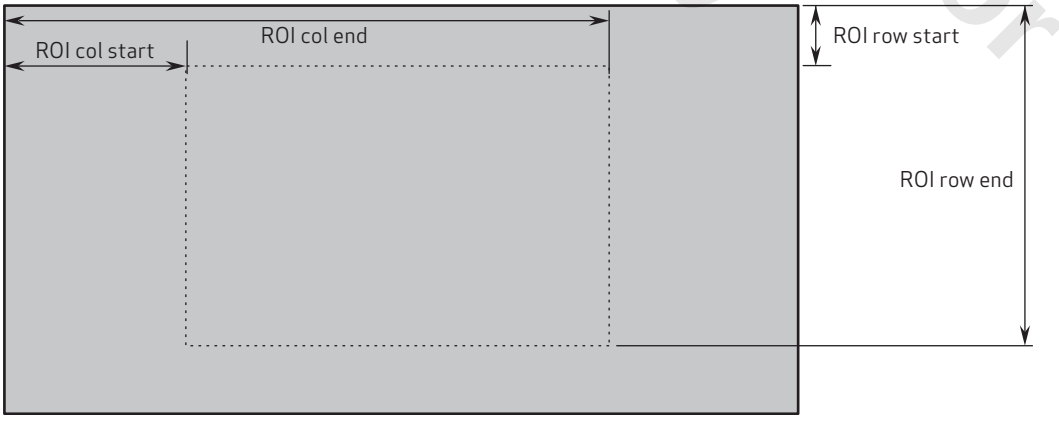
step	registers	comment
2	0x3216 = 0xDA (default) 0x3218[1] = 1 (default) 0x3218[2] = 1 (default)	9. Select a value to be used for TAGs. 10. Enable embedded data CRC. 11. Enable group hold memory CRC.
3	0x4317[5] = 1 0x4317[4] = 1	After finishing configuration, enable all embedded data lines: 12. Enable 2 rows of front embedded data. 13. Enable 2 rows of end embedded data. Streamed image at this point should contain embedded data.

5.6.2 statistics data

As mentioned in the previous section, it is possible to include statistics data as an embeddable (rows) option in the image output. The feature is handled by five statistic engines (blocks), from STAT_0 to STAT_4, in the sensor and relies on their configurable region of interest (ROI) to calculate histogram data as a result. The STAT_0, STAT_1, and STAT_2 engines support both 10-bit and 24-bit input data, meaning that they can either provide statistics of combined data or each capture of HCG, LCG, SPD, and VS. STAT_3 and STAT_4 engines only support 10-bit input data, and thus can only provide statistics of HCG, LCG, SPD, and VS captures, individually. **table 5-10** lists control registers of each statistics engine. The ROI defines the valid area of the pixel array. The statistics engine will calculate histogram by (row-1) × (column-1), which means that if users want to calculate the region of N × M, the ROI must be set to (N+1) × (M+1). A 4-bit CFA mask defines the valid pixels. One or more of the color channels (R, Gr, Gb, R) can be selected using this mask. The engines have an option to skip every odd row and column pixel pair (i.e., at most 4 (2x2) out of 16 (4x4) pixels can be selected). Each statistics engine can be enabled by setting register bits 0x5002[4:0] (see **table 5-10**). Each statistics block is assigned to one of the exposure channels, combined data, HCG, LCG, SPD, or VS.

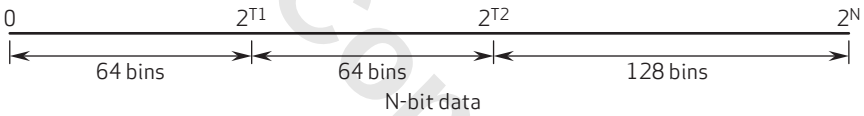
The ROI is defined in **figure 5-16**, where the parameters are presented as offsets from the set crop windows boundaries.

figure 5-16 ROI area setup



For the histogram data, the statistics engines encode incoming pixel data to 256 sub-ranges, also referred to as bins (256 bins). Each bin accounts for a certain pixel value range. The bins can be distributed to represent the values along N-bit (10 or 24 depending on input data) values axis either linearly (evenly/equally) or non-linearly with the help of two section threshold parameters, T1 and T2, which act as x power of 2 (2^) values as shown in **figure 5-17**. This allows some level of programmability. The first section (lower bit range) marker T1 will specify the value range, starting from 0 until 2^T1, the first 64 bins are going to take. That range will be equally distributed amongst all the bins in that range. The same scheme is applied for the (mid-range) marker T2, specifying a range of values from 2^T1 until 2^T2, that bins 65 to 128 are going to take. The last (third) range from 2^T2 until 2^N, will be encoded into bins 129 to 256. This way it is possible to make the bins narrower in the lower bit range and wider in the higher bit range. Setting T1 = N-2 and T2 = N-1, will give linear decoding with all 256 bins having the same (values) width.

figure 5-17 bin arrangements (distribution) for histogram across N-bit pixel values



Each of the 256 bins is 24-bit wide. They will count and store the number of times the values in its range have been encountered for each frame inside the ROI. It is important to note that the histogram data for the combined data and each capture channel is averaged over the pixel color group.

table 5-10 statistic engine control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5002	ISP_CTRL_02	0x3F	RW	Bit[6]: PWL enable Bit[5]: Retiming enable Bit[4]: Statistic block 4 enable Bit[3]: Statistic block 3 enable Bit[2]: Statistic block 2 enable Bit[1]: Statistic block 1 enable Bit[0]: Statistic block 0 enable
0x6000	STAT0_CTRL_00	0x0F	RW	Bit[3:0]: Histogram CFA mask
0x6001	STAT0_CTRL_01	0x07	RW	Bit[4:0]: Histogram bin control point0; 4~10
0x6002	STAT0_CTRL_02	0x08	RW	Bit[4:0]: Histogram bin control point1; 4~10
0x6003	STAT0_CTRL_03	0x07	RW	Bit[2]: stats_row Bit[1]: avg_en Enable average statistics Bit[0]: hist_en Enable histogram statistics
0x6004	STAT0_CTRL_04	0x00	RW	Bit[0]: skip_col
0x6005	STAT0_CTRL_05	0x00	RW	Bit[0]: skip_row

table 5-10 statistic engine control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x6006	STAT0_CTRL_06	0x00	RW	Bit[3:0]: ROI row start[11:8]
0x6007	STAT0_CTRL_07	0x3C	RW	Bit[7:0]: ROI row start[7:0]
0x6008	STAT0_CTRL_08	0x03	RW	Bit[3:0]: ROI row end[11:8]
0x6009	STAT0_CTRL_09	0x20	RW	Bit[7:0]: ROI row end[7:0]
0x600A	STAT0_CTRL_0A	0x00	RW	Bit[3:0]: ROI column start[11:8]
0x600B	STAT0_CTRL_0B	0x3C	RW	Bit[7:0]: ROI column start[7:0]
0x600C	STAT0_CTRL_0C	0x03	RW	Bit[3:0]: ROI column end1[11:8]
0x600D	STAT0_CTRL_0D	0x20	RW	Bit[7:0]: ROI column end1[7:0]
0x6016	STAT0_CTRL_16	0x00	RW	Bit[2:0]: Engine select
0x6020	STAT1_CTRL_00	0x0F	RW	Bit[3:0]: Histogram CFA mask
0x6021	STAT1_CTRL_01	0x07	RW	Bit[4:0]: Histogram bin control point0; 4~10
0x6022	STAT1_CTRL_02	0x08	RW	Bit[4:0]: Histogram bin control point1; 4~10
0x6023	STAT1_CTRL_03	0x07	RW	Bit[2]: statistics_row Bit[1]: avg_en Enable average statistics Bit[0]: hist_en Enable histogram statistics
0x6024	STAT1_CTRL_04	0x00	RW	Bit[0]: skip_col
0x6025	STAT1_CTRL_05	0x00	RW	Bit[0]: skip_row
0x6026	STAT1_CTRL_06	0x00	RW	Bit[3:0]: ROI row start[11:8]
0x6027	STAT1_CTRL_07	0x3C	RW	Bit[7:0]: ROI row start[7:0]
0x6028	STAT1_CTRL_08	0x03	RW	Bit[3:0]: ROI row end[11:8]
0x6029	STAT1_CTRL_09	0x20	RW	Bit[7:0]: ROI row end[7:0]
0x602A	STAT1_CTRL_0A	0x00	RW	Bit[3:0]: ROI column start[11:8]
0x602B	STAT1_CTRL_0B	0x3C	RW	Bit[7:0]: ROI column start[7:0]
0x602C	STAT1_CTRL_0C	0x03	RW	Bit[3:0]: ROI column end1[11:8]
0x602D	STAT1_CTRL_0D	0x20	RW	Bit[7:0]: ROI column end1[7:0]
0x6036	STAT1_CTRL_16	0x00	RW	Bit[2:0]: Engine select
0x6040	STAT2_CTRL_00	0x0F	RW	Bit[3:0]: Histogram CFA mask
0x6041	STAT2_CTRL_01	0x07	RW	Bit[4:0]: Histogram bin control point0
0x6042	STAT2_CTRL_02	0x08	RW	Bit[4:0]: Histogram bin control point1

table 5-10 statistic engine control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x6043	STAT2_CTRL_03	0x07	RW	Bit[2]: stats_row Bit[1]: avg_en Enable average statistics Bit[0]: hist_en Enable histogram statistics
0x6044	STAT2_CTRL_04	0x00	RW	Bit[0]: skip_col
0x6045	STAT2_CTRL_05	0x00	RW	Bit[0]: skip_row
0x6046	STAT2_CTRL_06	0x00	RW	Bit[3:0]: ROI row start[11:8]
0x6047	STAT2_CTRL_07	0x3C	RW	Bit[7:0]: ROI row start[7:0]
0x6048	STAT2_CTRL_08	0x03	RW	Bit[3:0]: ROI row end[11:8]
0x6049	STAT2_CTRL_09	0x20	RW	Bit[7:0]: ROI row end[7:0]
0x604A	STAT2_CTRL_0A	0x00	RW	Bit[3:0]: ROI column start[11:8]
0x604B	STAT2_CTRL_0B	0x3C	RW	Bit[7:0]: ROI column start[7:0]
0x604C	STAT2_CTRL_0C	0x03	RW	Bit[3:0]: ROI column end1[11:8]
0x604D	STAT2_CTRL_0D	0x20	RW	Bit[7:0]: ROI column end1[7:0]
0x6056	STAT2_CTRL_16	0x00	RW	Bit[2:0]: Engine select
0x6060	STAT3_CTRL_00	0x0F	RW	Bit[3:0]: Histogram CFA mask
0x6061	STAT3_CTRL_01	0x07	RW	Bit[4:0]: Histogram bin control point0; 4~10
0x6062	STAT3_CTRL_02	0x08	RW	Bit[4:0]: Histogram bin control point1; 4~10
0x6063	STAT3_CTRL_03	0x07	RW	Bit[2]: stats_row Bit[1]: avg_en Enable average statistics Bit[0]: hist_en Enable histogram statistics
0x6064	STAT3_CTRL_04	0x00	RW	Bit[0]: skip_col
0x6065	STAT3_CTRL_05	0x00	RW	Bit[0]: skip_row
0x6066	STAT3_CTRL_06	0x00	RW	Bit[3:0]: ROI row start[11:8]
0x6067	STAT3_CTRL_07	0x3C	RW	Bit[7:0]: ROI row start[7:0]
0x6068	STAT3_CTRL_08	0x03	RW	Bit[3:0]: ROI row end[11:8]
0x6069	STAT3_CTRL_09	0x20	RW	Bit[7:0]: ROI row end[7:0]
0x606A	STAT3_CTRL_0A	0x00	RW	Bit[3:0]: ROI column start[11:8]
0x606B	STAT3_CTRL_0B	0x3C	RW	Bit[7:0]: ROI column start[7:0]
0x606C	STAT3_CTRL_0C	0x03	RW	Bit[3:0]: ROI column end1[11:8]

table 5-10 statistic engine control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x606D	STAT3_CTRL_0D	0x20	RW	Bit[7:0]: ROI column end1[7:0]
0x6076	STAT3_CTRL_16	0x00	RW	Bit[2:0]: Engine select
0x6080	STAT4_CTRL_00	0x0F	RW	Bit[3:0]: Histogram CFA mask
0x6081	STAT4_CTRL_01	0x07	RW	Bit[4:0]: Histogram bin control point0; 4~10
0x6082	STAT4_CTRL_02	0x08	RW	Bit[4:0]: Histogram bin control point1; 4~10
0x6083	STAT4_CTRL_03	0x07	RW	Bit[2]: stats_row Bit[1]: avg_en Enable average statistics Bit[0]: hist_en Enable histogram statistics
0x6084	STAT4_CTRL_04	0x00	RW	Bit[0]: skip_col
0x6085	STAT4_CTRL_05	0x00	RW	Bit[0]: skip_row
0x6086	STAT4_CTRL_06	0x00	RW	Bit[3:0]: ROI row start[11:8]
0x6087	STAT4_CTRL_07	0x3C	RW	Bit[7:0]: ROI row start[7:0]
0x6088	STAT4_CTRL_08	0x03	RW	Bit[3:0]: ROI row end[11:8]
0x6089	STAT4_CTRL_09	0x20	RW	Bit[7:0]: ROI row end[7:0]
0x608A	STAT4_CTRL_0A	0x00	RW	Bit[3:0]: ROI column start[11:8]
0x608B	STAT4_CTRL_0B	0x3C	RW	Bit[7:0]: ROI column start[7:0]
0x608C	STAT4_CTRL_0C	0x03	RW	Bit[3:0]: ROI column end1[11:8]
0x608D	STAT4_CTRL_0D	0x20	RW	Bit[7:0]: ROI column end1[7:0]
0x6096	STAT4_CTRL_16	0x00	RW	Bit[2:0]: Engine select

5.6.3 statistics data format at output

In order to enable statistic row output, the user must set register bit 0x430F[6] = 1. The statistics data is added as two rows after the video stream (see **figure 5-14**). If five engines are enabled, the two rows of statistics data will have the format shown in **figure 5-18**, where A, B, C, D, and E represent the five statistics engines. The statistics results are placed in the following order: combined data, HCG, LCG, SPD, and VS. The statistics data are LSB aligned in pixel data. For example, the statistics data format in case of PWL16 is {4'h0, statistics_data[11:0]}, {4'h0, statistics_data[23:12]}.

figure 5-18 statistics data format

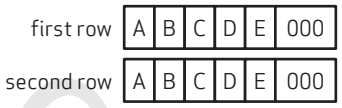
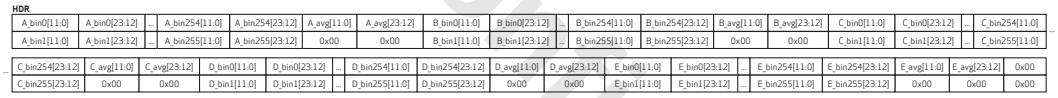


figure 5-19 statistics data format with details (HDR output mode)



6 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. SCCB is fully compatible with I2C standard mode, fast mode, and fast mode plus (when the sensor input clock is 12 MHz or higher).

The OX03C10 offers end-to-end protection of SCCB control data by using CRC (see **section 6.2**).

6.1 SCCB timing

figure 6-1 SCCB interface timing

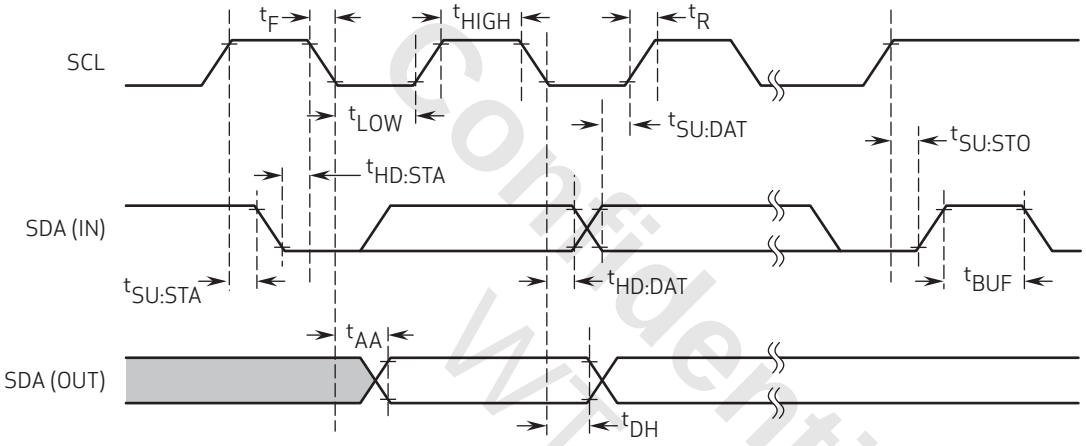


table 6-1 SCCB interface timing specifications based on 400 kHz[a] (sheet 1 of 2)

symbol	parameter	min	typ	max	unit
f_{SCL}	clock frequency		400		kHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SCL low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs

table 6-1 SCCB interface timing specifications based on 400 kHz[a] (sheet 2 of 2)

symbol	parameter	min	typ	max	unit
t_{DH}	data out hold time	0.05			µs

a. timing measurement shown at beginning of rising edge or end of falling edge signifies 30%,
timing measurement shown in middle of rising/falling edge signifies 50%,
timing measurement shown at end of rising edge or beginning of falling edge signifies 70%

table 6-2 SCCB interface timing specifications based on 1000 kHz[a]

symbol	parameter	min	typ	max	unit
f_{SCL}	clock frequency		1000[b]		kHz
t_{LOW}	clock low period	0.5			µs
t_{HIGH}	clock high period	0.26			µs
t_{AA}	SCL low to data out valid			0.45	µs
t_{BUF}	bus free time before new start	0.5			µs
$t_{HD:STA}$	start condition hold time	0.26			µs
$t_{SU:STA}$	start condition setup time	0.26			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.5			µs
$t_{SU:STO}$	stop condition setup time	0.26			µs
t_R, t_F	SCCB rise/fall times			0.12	µs
t_{DH}	data out hold time	0.05			µs

a. timing measurement shown at beginning of rising edge or end of falling edge signifies 30%,
timing measurement shown in middle of rising/falling edge signifies 50%,
timing measurement shown at end of rising edge or beginning of falling edge signifies 70%

b. for 1000 kHz mode, minimum input clock is 12 MHz; for 400 kHz or less, minimum input clock is 6

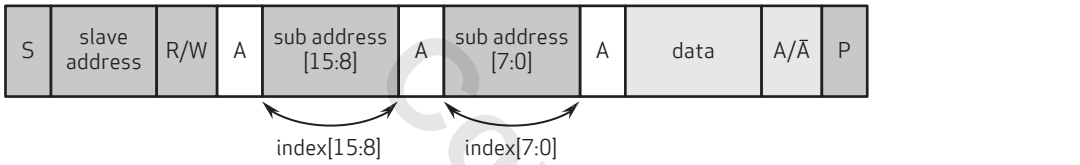
6.2 direct access mode

6.2.1 message format

The OX03C10 supports the message format shown in **figure 6-2**. The repeated START (Sr) condition is shown in **figure 6-3** and **figure 6-5**.

figure 6-2 message type

message type: 16-bit sub-address, 8-bit data, and 7-bit slave address



from slave to master
from master to slave
direction depends on operation

S START condition
P STOP condition
Sr repeated START condition

A acknowledge
Ā negative acknowledge

6.2.2 read / write operation

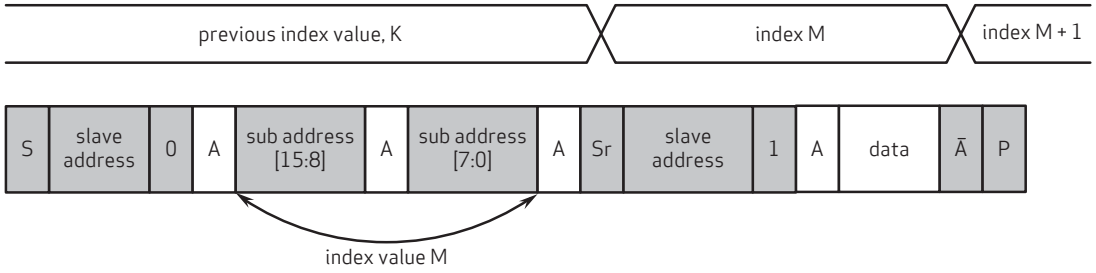
The OX03C10 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

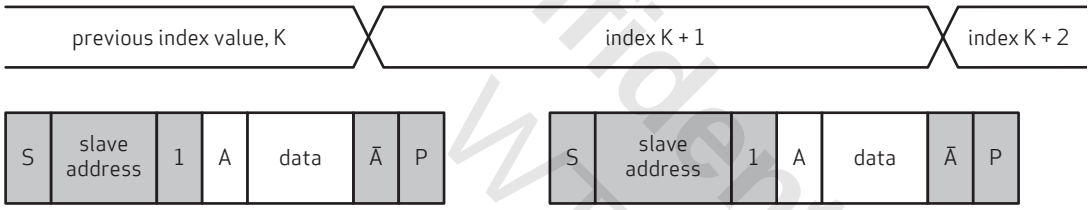
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SDA line as shown in **figure 6-3**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 6-3 SCCB single read from random location



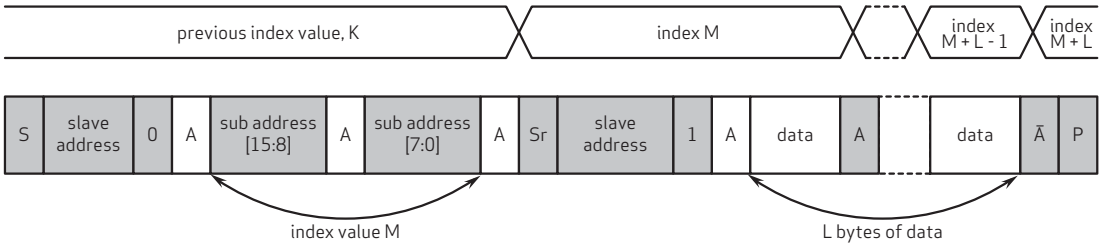
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SDA line as shown in **figure 6-4**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 6-4 SCCB single read from current location



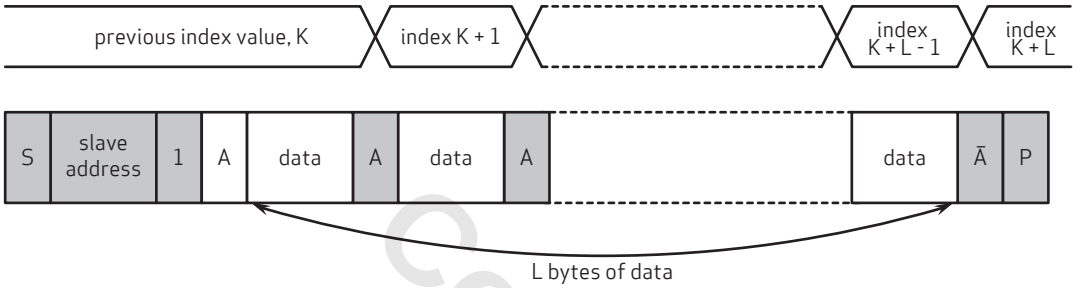
The sequential read from a random location is illustrated in **figure 6-5**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 6-5 SCCB sequential read from random location



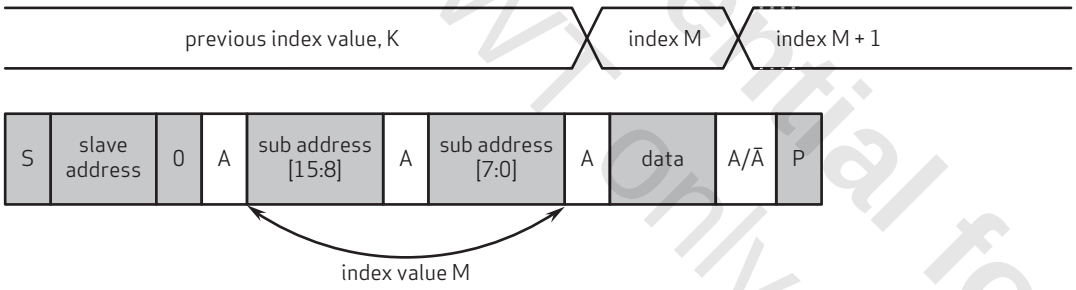
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation as shown in **figure 6-6**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 6-6 SCCB sequential read from current location



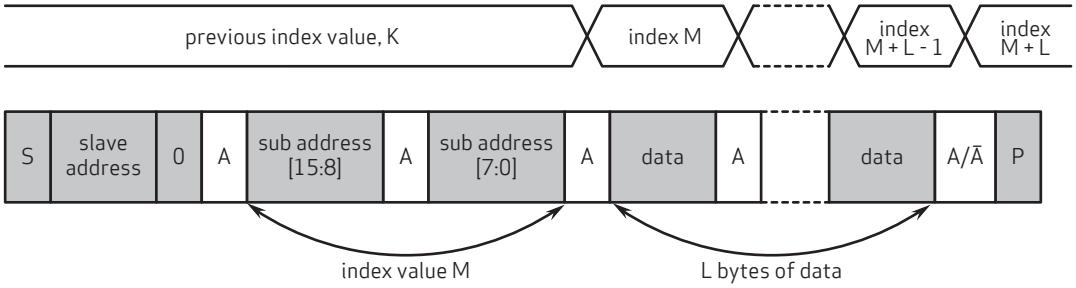
The write operation to a random location is illustrated in **figure 6-7**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 6-7 SCCB single write to random location



The sequential write is illustrated in **figure 6-8**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 6-8 SCCB sequential write to random location



6.3 SCCB CRC

When the OX03C10 is configured to normal SCCB mode, a CRC-16-IBM is continuously calculated when single messages (address and data) or sequential messages are being written to the sensor. The CRC is updated by a dedicated register. The host can calculate the CRC before sending and can read back this register for comparison, either by embedded line or SCCB read.

The CRC-16 is initialized to 0xFFFF at the start of the transmission, and is calculated on both the register address and data (high address byte, low address byte, and data). A SCCB read operation to any of the CRC registers will reset the CRC calculation. The CRC registers will be reset on the next SCCB write operation (i.e., they will hold the result of the previous CRC calculation until a new SCCB write occurs). CRC registers can appear as part of embedded data without being reset automatically.

6.3.1 single/sequential write with CRC

The OX03C10 is configured to normal SCCB mode (0x3182[0] = 0) (i.e., PEC mode is not enabled). A CRC is continuously calculated on single messages or sequential messages and updated in a dedicated register. The host can calculate an expected CRC after each write and compare that with the read value from the sensor's own CRC calculation, held in registers {0x3180, 0x3181}.

The CRC is calculated on both the register address and data (high address byte, low address byte, data byte) using CRC-16-IBM, polynomial 0x8005.

A SCCB read operation to any of the CRC registers {0x3180, 0x3181} will reset the CRC calculation. The CRC registers will be updated on the next SCCB write operation (i.e., they will hold the result of the previous CRC calculation until a new SCCB write occurs or until sequence end for sequential write).

Additionally, the CRC registers can be set to appear as part of embedded data.

6.3.2 block read/write with PEC

The OX03C10 implements a mechanism to check the CRC code which is sent with all data via the SCCB interface. The system attaches a CRC checksum over the SCCB data and the OX03C10 checks this CRC and counts an error if the checksums are different.

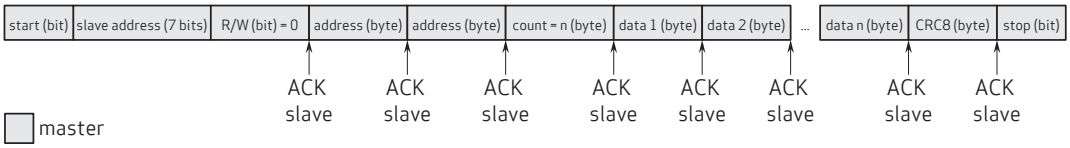
The block read/write with PEC is enabled with register bit 0x3182[0] = 1.

6.3.2.1 SCCB write with PEC

The system provides a CRC code for all data sent via the SCCB interface and the sensor will check the CRC. In case of a mismatch, a corresponding error reaction is triggered.

All write messages of 6 to 21 bytes (16 data bytes) are interpreted as one SCCB ID byte, two address bytes, one count byte, n data bytes, and one CRC-8 byte.

figure 6-9 SCCB with PEC - single write message



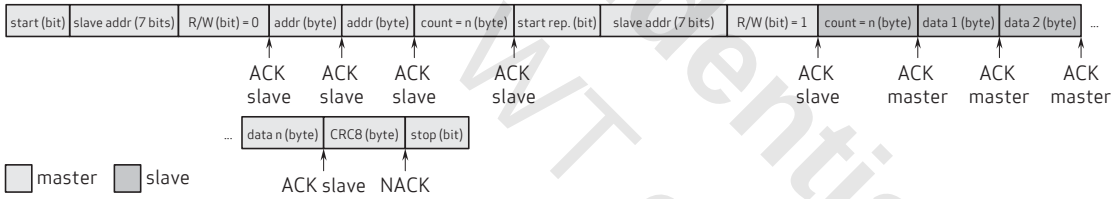
The CRC-8 will be initialized to zero at start of transmission and calculate on the transmitted data including everything from the slave address to the CRC data. At stop of transmission, the CRC-8 is checked. A status bit indicating successful reception can be read from SCCB.

6.3.2.2 SCCB read with PEC

The system must check the CRC code which is received with all data via the SCCB interface. In case of a mismatch, a corresponding error reaction must be triggered.

A block read messages is interpreted as one SCCB ID byte, two address bytes and one count byte. Count may be 1 to 255 bytes.

figure 6-10 SCCB with PEC - single read message



The CRC-8 will be initialized to zero at the start of the transmission and calculate on the transmitted data including everything from the slave address to the last data byte.

6.3.2.3 SCCB PEC error and error rate

The SCCB PEC can use an error rate to signal continuous SCCB errors during streaming. If an error counter (0x3185) exceeds a programmable threshold (0x3184), the OX03C10 will set the error flag (see **table 8-1**) and can transition to safe state.

The 8-bit counter (0x3185) increments each time a CRC error is detected on a block write message. A second 8-bit internal counter will count successful block write messages, and decrement the error counter (0x3185) after a certain number of successful PEC writes (set in 0x3183).

If critical registers are written in the PEC sequence (e.g., during configuration), the error counter (0x3185) must be checked at minimum every 0x3183 PEC write. If a CRC error is detected, the PEC packet(s) must be resent.

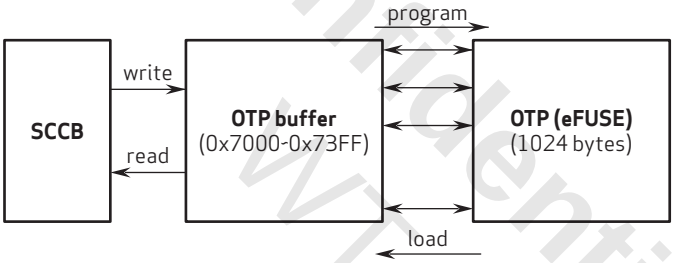
7 one-time programmable (OTP) memory

The OX03C10 supports a maximum of 1024 bytes of one-time programmable (OTP/eFUSE) memory to store chip identification and manufacturing information, which can be used to update the sensor's default setting and can be controlled through the SCCB. The auto load function enables writing OTP memory (temperature calibration, PLL configuration, etc.) to registers during start up phase (transition from hardware standby to software standby).

Out of 8k bits (1024 bytes), a large portion of the memory will be reserved for storage of OmniVision information, die unique ID, temperature sensor calibration, cluster DPC data, and register trimming, etc. A smaller portion is reserved for the user's own definition.

There is a dedicated 1024 byte SRAM buffer, which is used to temporarily store data to be programmed (written) into OTP (eFUSE) or loaded (read) from OTP (eFUSE). The SCCB can read/write to this OTP buffer (OTP_SRAM) by assigned addresses, which range from 0x7000 to 0x73FF.

figure 7-1 OTP buffer



OTP data load will be triggered automatically at start up. OTP data load can also be triggered manually by writing 0x01 to register 0x3D81 while streaming. Auto mode and manual mode can be chosen by setting register bit 0x3D84[6] to 0 and 1, respectively. By default, OTP data load is in auto mode. In auto mode, all data in the OTP will be loaded to the OTP buffer. While in manual mode, the part of the data which is defined by the start address {0x3D88, 0x3D89} and the end address {0x3D8A, 0x3D8B} of the OTP will be loaded to the OTP buffer. There is straight mapping among the addresses of the OTP (eFUSE) and OTP (SRAM) buffer.

OTP data can be loaded from 0x7000 to 0x73FF and also through SCCB interface, using a total of 1024 bytes. It is important to note that the OX03C10 must be in streaming mode while programming OTP.

7.1 OTP allocation

The exact size, mapping, overall assignment of the different types of information, and section data are supposed to be sent to this memory location. The OTP allocation is to be consolidated in the later stage of production.

7.2 OTP write

The following method shows partial OTP programming, where data is written from the OTP buffer to the actual OTP memory. This method is used to write specific bytes into the OTP and is the recommended way to carry this out:

1. Set register bit 0x3D84[6] = 1 to enable partial OTP program mode.
2. Set address range of OTP to be programmed.
   a. Start address: high byte register 0x3D88, low byte register 0x3D89
   b. End address: high byte register 0x3D8A, low byte register 0x3D8B
3. Write data into dedicated buffer corresponding to address specified in step 2.
4. Set register bit 0x3D80[0] = 1 to program data stored in buffer into specified OTP bytes.

Example of a partial OTP write:

table 7-1 partial OTP program

step	register	comment
1	0x3D84 = 0x40	Bit[6]: Partial mode enable Do not run any OTP load or BIST action
2	0x3D88 = 0x70 0x3D89 = 0x00 0x3D8A = 0x71 0x3D8B = 0xFF	Partial Mode OTP Read Start Address High Byte Partial Mode OTP Read Start Address Low Byte Start @ 0x7000 in this Example Partial Mode OTP Read End Address High Byte Partial Mode OTP Read End Address High Byte End @ 0x71FF in this Example
3	6C 7000 xx ;; data[0] 6C 7001 xx ;; data[1] 6C 7002 xx ;; data[2] 6C 7003 xx ;; data[3] 6C 7004 xx ;; data[4] … … 6C 71FC xx ;; data[508] 6C 71FD xx ;; data[509] 6C 71FE xx ;; data[510] 6C 71FF xx ;; data[511]	Specify data user wants stored in OTP (eFUSE) at end by issuing SCCB writes with data values towards corresponding addresses of the SRAM buffer.
4	0x3D80 = 0x01	Bit[0]: Program enable Start writing to OTP (eFUSE)
5	loop while (0x3D80[7] == 1)	Loop until OTP is busy being programmed, register bit 0x3D80[7] = 1. When OTP programming is finished, register bit 0x3D80[7] = 0.

7.3 OTP read

The following method shows partial OTP loading, where data is being transferred from the actual OTP memory to the OTP buffer. This approach is used to read specific bytes from the OTP (eFUSE). There is an optional step, which allows for this method to turn and transfer certain data from the OTP memory as values that will be loaded automatically into the sensor's registers, provided that the data adheres to a specific format.

1. Set register bit 0x3D84[6] = 1 to enable manual mode.
2. Set address range of OTP to be loaded.
   a. start address: high byte register 0x3D88, low byte register 0x3D89
   b. end address: high byte register 0x3D8A, low byte register 0x3D8B
3. Set header address if this partial load includes a setting with an auto load feature (see **section note**).
   a. high byte register 0x3D8C, low byte register 0x3D8D
4. Set register bit 0x3D81[0] = 1 to load data from specified OTP bytes to corresponding buffer.
5. User can read registers within range from start address to end address to check OTP data.
6. Setting with auto load feature will be written into corresponding registers automatically (see **section note**).

note It is possible to use the OTP memory load up to configure\set arbitrary registers of the sensor to some OTP stored value at this step.

Example of a partial OTP read (see **table 7-4** for an example on how to load register settings from OTP):

table 7-2 partial OTP load

step	register	comment
1	0x3D84 = 0x40	Bit[6]: Partial mode enable
2	0x3D88 = 0x73 0x3D89 = 0xBB 0x3D8A = 0x73 0x3D8B = 0xCF	Partial Mode OTP Read Start Address High Byte Partial Mode OTP Read Start Address Low Byte Start @ 0x73BB in this Example Partial Mode OTP Read End Address High Byte Partial Mode OTP Read End Address High Byte End @ 0x73CF in this Example
3	loop while (0x3D81[7] == 1)	Loop until OTP is busy being read, register bit 0x3D81[7] = 1. When OTP reading is finished, register bit 0x3D81[7] = 0.

In contrast to the partial approach, there is also an all byte approach that will load the entire contents (all 1024 bytes) of the OTP memory into the OTP buffer. The all byte method follows these steps:

1. Set register bit 0x3D84[6] = 0 to enable auto mode.
2. Set header address for setting with auto load feature (see **section note**).
   a. high byte register 0x3D8C, low byte register 0x3D8D
3. Set register bit 0x3D81[0] = 1 to load all 1024 byte data from OTP to buffer.
4. User can read registers from 0x7000 to 0x73FF to check OTP data.
5. Setting with auto load feature will be written into corresponding registers automatically (see **section note**).

Example of an all byte OTP read (with optional registers setting load):

table 7-3 all byte OTP load

step	register	comment
1	0x3D84 = 0x00	Bit[6]: All byte mode enable
2	0x3D81 = 0x01	Bit[0]: Load enable Start loading all the data from OTP (eFUSE) to OTP buffer Load all byte OTP data into addresses from 0x7000 to 0x73FF
3	loop while (0x3D81[7] == 1)	Loop until OTP is busy being read, register bit 0x3D81[7] = 1. When OTP reading is finished, register bit 0x3D81[7] = 0.

There are two modes for OTP load action in the OX03C10. The methods mentioned above are all under the manual trigger mode, due to a manual SCCB write that has to be written by the user to start the read process. For the other mode, the OTP load will trigger automatically (e.g., OTP load at start up on every power on). There are also settings to choose if and when to reload OTP automatically when entering streaming:

- Set register bit 0x3D85[2] = 0 to avoid any OTP load when entering streaming. OTP will be loaded only at start up (default).
- If register bit 0x3D85[2] = 1, set register bit 0x3D85[3] = 0 to load OTP data only on the first time entering streaming; set register bit 0x3D85[3] = 1 to load OTP data every time sensor wakes up from software standby/stream off.
- If register bit 0x3D85[1] is also set to 1, enable register auto-load in automatic trigger mode.
- If register bit 0x3D85[0] is also set to 1, enable register auto-load in manual trigger mode.

As mentioned earlier, it is possible to use the OTP memory load up to configure/set arbitrary registers of the sensor to some OTP stored value. The capability is named 'OTP auto load setting feature', which works in partial and all byte load operations. This feature is usually incorporated for storing calibration data for the BLC and temperature sensors during the mass production phase and loading it when the sensor is used. Effectively, what happens is the data from the OTP (eFUSE) is loaded into the OTP (SRAM) buffer, and then the sections which have been enabled for this feature will be loaded from the OTP buffer to the register settings. This takes place in two stages. To enable this feature, the user must follow the procedure and format of the OTP data below:

1. Specify the load setting start address registers of the OTP SRAM address holding the first data value, from where the register values interpretation is going to begin {0x3D8C, 0x3D8D}.
2. Data programmed into the first and consecutive OTP addresses, assigned for the settings load, should include:
    a. command code: number of bytes to be loaded (no more than 16), specified by prefix 'A' or '5', where:
    AN: read n+1 bytes with address specified in following two-byte setting
    5N: read n+1 bytes with address right after previous read/write operation
    b. two bytes of start address
    c. (n+1) data bytes, that are going to be written to the addresses in continuous order

It is important to note several specifics of this mode:

- First command code can only be AN type, not 5N.
- Address for initial command code is set by registers {0x3D8C, 0x3D8D}.
- All OTP information for OTP load setting should be grouped together.
- Reserved range for OTP load setting is at least one more byte than real use.

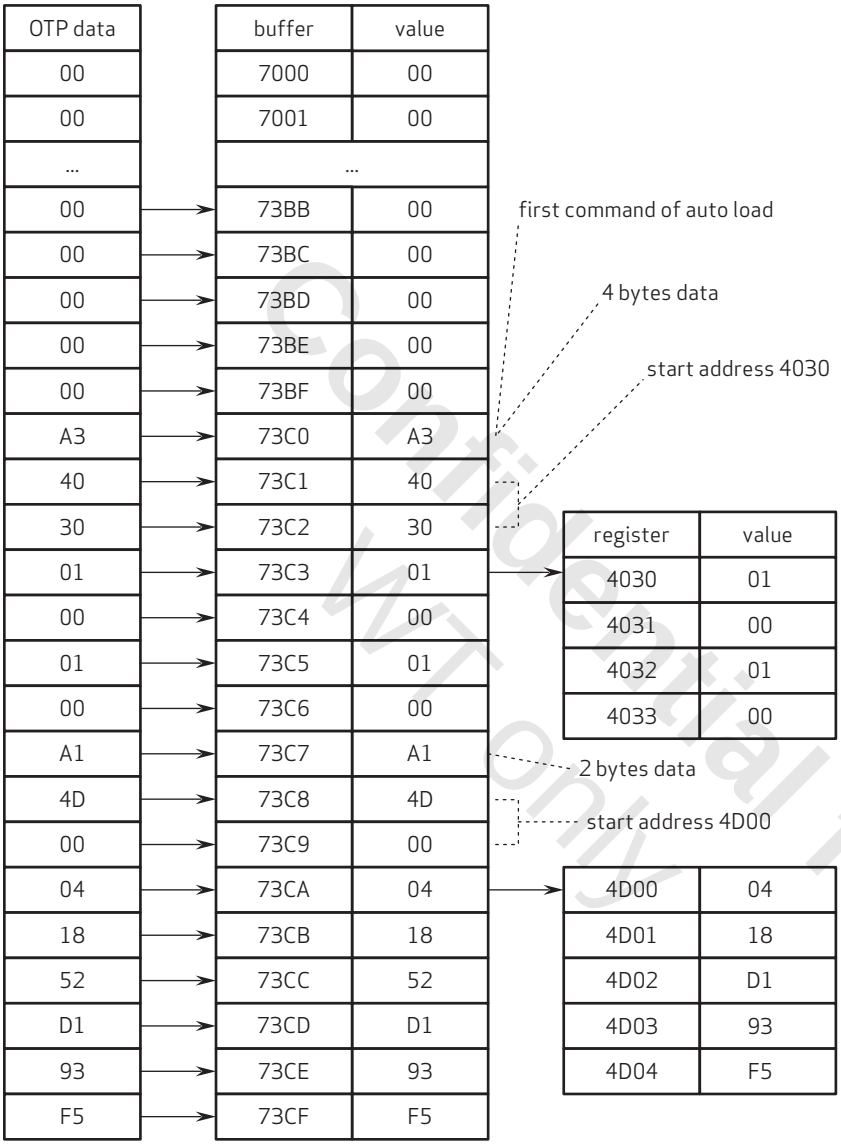
An example of an OTP load setting is shown below:

table 7-4 partial OTP load and load setting procedure

step	register	comment
1	0x3D84 = 0x40	Bit[6]: Partial mode enable
2	0x3D88 = 0x73 0x3D89 = 0xBB 0x3D8A = 0x73 0x3D8B = 0xCF	Partial Mode OTP Read Start Address High Byte Partial Mode OTP Read Start Address Low Byte Start @ 0x73BB in this example Partial Mode OTP Read End Address High Byte Partial Mode OTP Read End Address High Byte End @ 0x73CF in this Example
3	0x3D8C = 0x73 0x3D8D = 0xC0	First Load Setting Address High Byte First Load Setting Address Low Byte OTP SRAM Region Start, which holds the register settings data
4	0x3D85 = 0x0F	Allow for: Bit[1]: All byte automatic load setting feature Bit[0]: Manual trigger load setting to occur
5	0x3D81 = 0x01	Manual Trigger OTP Read Enable
6	loop while (0x3D81[7] == 1)	Loop until OTP is busy being read, register bit 0x3D81[7] = 1. When OTP reading is finished, register bit 0x3D81[7] = 0.

The result of the partial OTP load and load setting example procedure previously mentioned can be explained as:

figure 7-2 partial OTP load and load setting procedure result



The OTP memory access conditions are based on typical conditions: sensor wake up, 2.9V AVDD, 1.1V DVDD, and a 90 MHz system clock. To use OTP memory under different operating conditions, please contact your local OmniVision FAE.

7.4 OTP_DPC

The OTP content can contain data for defect pixel clusters that if enabled, will be used by the OTP_DPC block for image correction. The same is true for the product ID and customer reserved bytes. OTP_DPC requires and uses a traditional load process (address allocation has not been finalized for the OX03C10) to read the data from OTP memory to its buffer, so it can function. Further information about its functionality is described in **section 4.5**.

8 safety concepts

The OX03C10 is designed as a Safety Element out of Context (*ISO26262:2018-1, 3.138*) complying with ISO262626 ASIL D requirements for development process.

The OX03C10 internal safety mechanisms can detect random hardware errors from the sensor circuitry with ASIL C capability (*ISO26262:2018-1, 3.2*).

8.1 high level safety requirements

The OX03C10 safety analysis considers the following safety requirements for developing safety mechanisms.

The OX03C10 shall not:

- output frozen images, not updated image, or a part of it, more than once
- output more than one successive defect line or column
- output duplicate/tripled parts of the image
- output unintentional flipped/mirrored image
- output images with wrong crop size from array according to set ROI
- output images at wrong point in time or with wrong frame rate
- output shifted image (whole image or parts of the image) in X or Y direction
- output unintentional mirrored on flipped image
- output a test pattern unintentionally
- introduce unintentional image artifacts which could lead to hidden or occluded real world objects
- unintentionally degrade images in terms of contrast, dynamic range, and brightness which could lead to hidden or occluded real world objects
- send any data which is not protected by a CRC

The safety mechanisms should detect random hardware faults or soft errors and report them to the host through SCCB embedded line, or dedicated hardware pins.

8.2 error flags

To notify the host when an OX03C10 safety mechanism detects an error, the OX03C10 has a number of error flags in registers. The registers can be read out through SCCB interface protected with CRC or read via embedded line protected with CRC.

The error flags are divided into two modes:

- Permanent: one set of error flags will trigger when a safety mechanism detects an error. It will stay high until a RESET or an SCCB command sequence can reset it again. This requires host intervention.
- Transient: error flags will trigger when a safety mechanism detects an error, but it will clear automatically if subsequent results from the same safety mechanism show no error detected. The host can decide whether or not to continue streaming if the detected error is a transient fault, e.g., in a circular buffer.

8.3 safe state mode

The OX03C10 has implemented a safe state mode (*ISO26262:2018-1, section 3.131*) that can be entered automatically after one of the internal safety mechanisms has detected a failure. Error flags in registers indicate which safety mechanism detected the error and a hardware pin can be asserted, and optionally, safe state mode is entered. In safe state mode, the sensor is guaranteed to not violate any safety requirements.

8.4 error signal pin

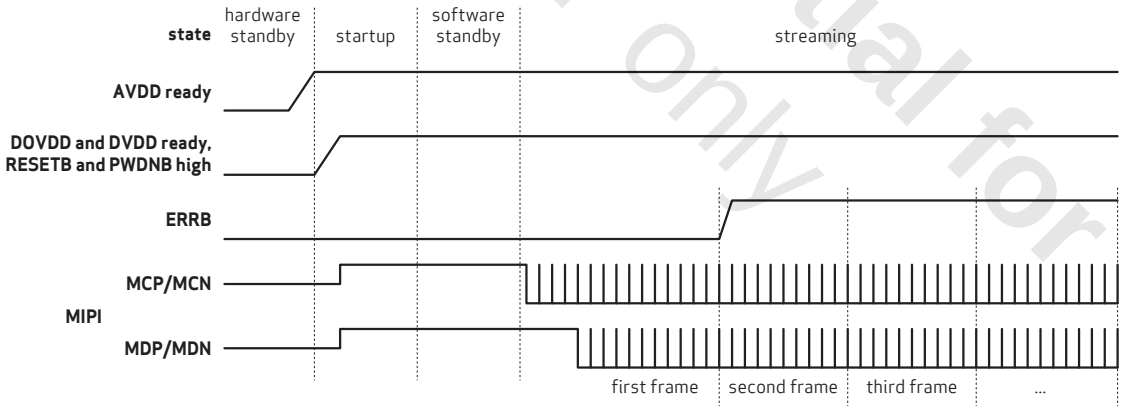
The OX03C10 has an error signal pin (ERRB), which signals the transition of the device into safe state mode. The ERRB pin is active low:

- low: error detected, system is in a safe state mode
- high: no error

The ERRB pin will be low in RESET state (RESETB = 0), and rise after the first frame in streaming mode when all startup and online safety checks have reported 'no error detected' status. If an error is detected during start-up mode or during first frame in streaming mode, ERRB will remain low. The ERRB pin can be tested manually (toggled) in standby mode.

The sensor checks the ERRB pin state by setting the signal to the correct state and then reading it to make sure it reflects the correct state. This protects against shorts on the board. If the read back of the ERRB pin output does not match the expected state, it will trigger an error signal (read from register/embedded line) and the OX03C10 can transition to safe state (if configured).

figure 8-1 EERB pin timing



8.5 safety mechanisms

A safety mechanism is defined (*ISO26262:2018-1, section 3.142*) as a 'technical solution implemented by E/E functions or elements, or by other technologies, to detect and mitigate or tolerate faults or control or avoid failures in order to achieve maintain intended functionality or achieve or maintain a safe state'.

The OX03C10 safety mechanisms cover all internal blocks with detection coverage according to ISO26262 ASIL-C rating. The safety mechanisms for the OX03C10 have been designed for this purpose and can alert the host processor so that the effect of the failure can be controlled. It can also transition itself into a safe state.

The safety mechanisms in OX03C10 are summarized in **table 8-1**. Available safety features may depend on the exact operating mode.

figure 8-2 OX03C10 safety mechanisms

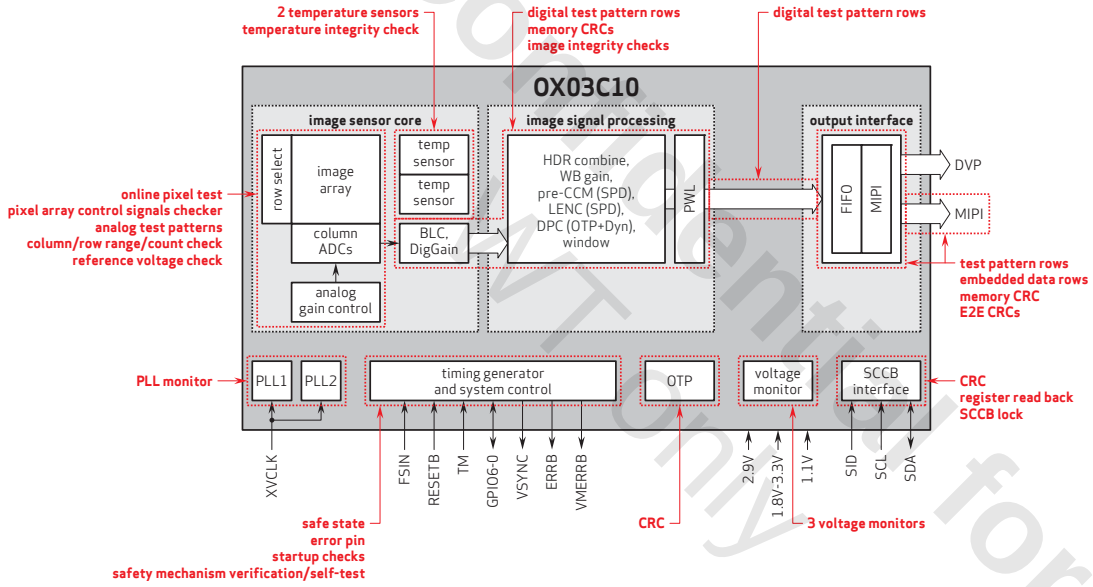


table 8-1 OX03C10 safety mechanisms (sheet 1 of 4)

test function	coverage	start up (start up mode)	online (streaming mode)	enable safe state
analog, ADC processing blocks and addressing of pixel area				
online pixel test	pixel level check, no added row time integrity check	no	yes	configurable
analog test pattern row	analog test pattern run true ADC/memory, can be output every image frame	no	yes	N/A

table 8-1 OX03C10 safety mechanisms (sheet 2 of 4)

test function	coverage	start up (start up mode)	online (streaming mode)	enable safe state
analog test pattern row checker	analog test pattern rows are checked internally every image frame	no	yes	configurable
column IDs	column IDs will indicate missing/frozen columns, and IDs can be output every image frame	no	yes	N/A
row IDs	row IDs will indicate missing/frozen rows, and IDs can be output every image frame	no	yes	N/A
ID checker	compare row and column identifiers against array crop ROI settings and flip/mirror settings to check correct addressing and correct number of rows/columns	no	yes	configurable
array row control check	signal integrity check for pixel array control signals	no	yes	configurable
internal reference voltage	monitor internal derived reference voltages	no	yes	configurable
analog to digital sync check	check readout and synchronization logic and buffers from analog datapath output (ADCs) to digital datapath input (BLC)	no	yes	configurable
digital processing blocks				
digital test pattern rows	digital test pattern rows will be processed by digital processing blocks (including BLC, ISP, output FIFO) and can be output every image frame	no	yes	N/A
digital test pattern rows checker	dual path processing modules by comparison, ISP modules and output FIFO with CRC check based on pre-known CRC and CRC comparison (pre-known processing settings)	no	yes	configurable
BLC checker	BLC calculation and correction integrity check	no	yes	configurable
clock generation				
PLL clock monitor	monitor internal clock generation (PLL), PLL clock monitor integrity check	no	yes	configurable
PLL lock	check PLL lock signal	no	yes	configurable
E2E protection of control data				
SCCB CRC	CRC on SCCB writes, host must check result	no	yes	no

table 8-1 OX03C10 safety mechanisms (sheet 3 of 4)

test function	coverage	start up (start up mode)	online (streaming mode)	enable safe state
PEC	group write with CRC, self-check, host must check status for CRC check	no	yes	configurable
SCCB register lock	lock SCCB register access to avoid registers from being unintentionally written to; registers commonly used during streaming not locked	no	yes	N/A
internal register read-back	all registers written to sensor are read back from register to check correct setting (SCCB, ROM, OTP)	yes	yes	configurable
embedded data	meta data attached to actual image for each frame	no	yes	N/A
embedded data CRC	32-bit CRC to check embedded data transmission; output embedded CRC checked internally against actual registers	yes	no	configurable
SI default register check	register default values stored on ROM; ROM CRC plus internal register read back to ensure correct configuration	yes	no	configurable
E2E protection of image data				
MIPI ECC/CRC	enable system checks of transmission link	no	yes	N/A
output interface				
output FIFO CRC	checks internal output data buffer	no	yes	configurable
non-volatile memory				
ROM CRC	ROM CRC is always run at power up	yes	no	configurable
OTP CRC	CRC codes added to OTP	yes	no	no
volatile memory				
SRAM built in self-test	pattern check of all memories (SRAM) at start up	yes	no	configurable
SRAM CRC	online CRC on processing buffers/memories	no	yes	configurable
system				
test of safety mechanisms	all safety mechanisms must pass initial internal test before considered safe to use	yes	some	configurable

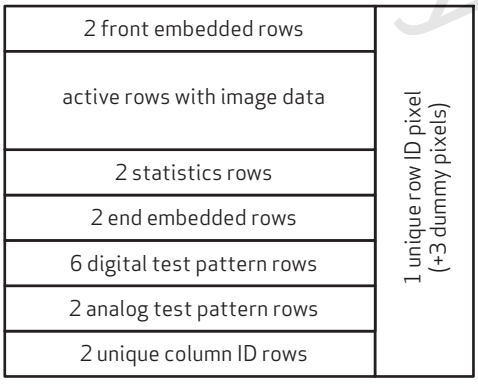
table 8-1 OX03C10 safety mechanisms (sheet 4 of 4)

test function	coverage	start up (start up mode)	online (streaming mode)	enable safe state
temperature sensor	read and report junction temperature; integrity check: use two temperature sensors, compare against each other; self-check of digital part	no	yes	configurable
voltage sensor external supply	measure supply voltages delivered to sensor; self-check of digital part	no	yes	configurable
frame counter	sensor/interface issues that leads to not updated frame; enable system check for frozen/locked frames	no	yes	no
ERRB pin monitor	continuously check ERRB pin status is as expected	no	yes	configurable
digital test pattern generator	digital test pattern overwrite image data	no	yes	no
ERRB pin functionality	ERRB state is continuously checked and compared against expected state	configurable	no	no

8.5.1 test pattern rows

The OX03C10 will provide a set of pre-known analog and digital test pattern rows which can be sent with every image frame as indicated in **figure 8-3**. Both ATPR and DTPR must be enabled and run simultaneously if they are to be sent over the MIPI interface. The test pattern rows will be used for internal safety checks on the sensor and it is not necessary to output the test pattern rows.

figure 8-3 example positions of column/row identifiers and analog/digital test rows



8.5.2 safety mechanisms during start up mode

After entering start up mode, all safety mechanisms for start up will run automatically as indicated in **table 8-1** if enabled. After all required self-tests have completed, passed/not passed information is available by SCCB registers. If an error is detected, the OX03C10 can transition into safe state mode after the first frame in streaming mode. The start up time including all self-tests is 8 ms (at nominal XVCLK = 24 MHz).

8.5.3 online safety mechanisms during streaming mode

After entering standard streaming mode, all online safety mechanisms run continuously as indicated in **table 8-1**. The result of safety checks is continuously reported through registers/embedded line. If an error is detected, safe state mode can be entered and signaled through the hardware ERRB pin after the fist frame in streaming mode. Latency between failure occurrence and transition to safe state mode is less than 60 ms (at nominal XVCLK = 24 MHz).

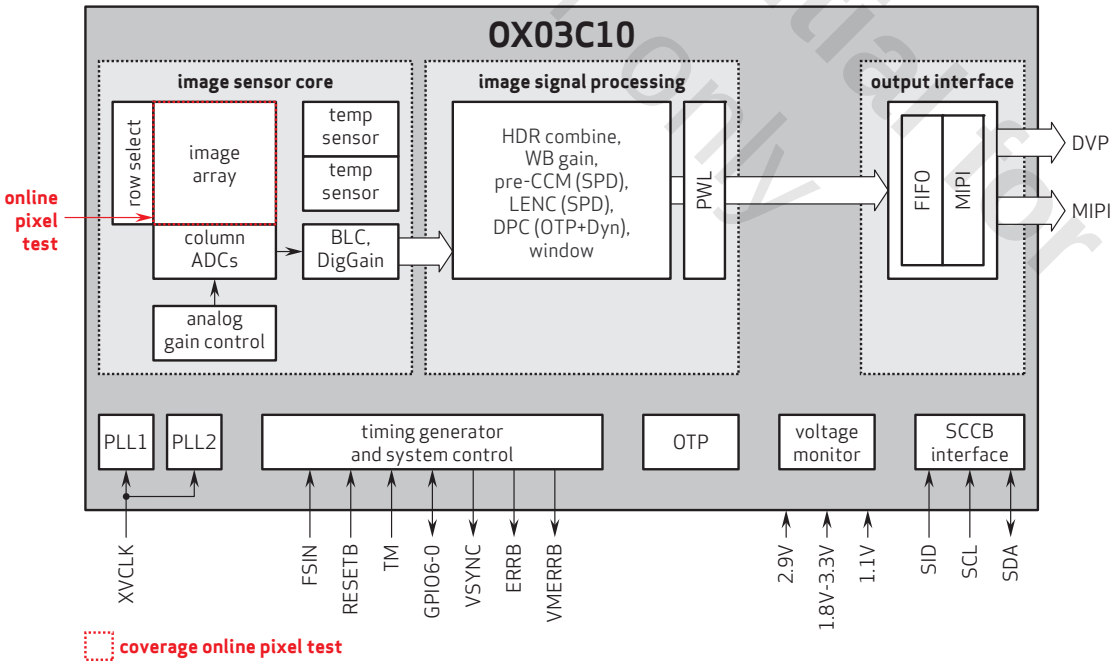
8.5.4 online pixel test

Online pixel test checks the output stage of the pixel for every row by sensing the bitline voltage to the pixel.

The online pixel test runs in parallel with normal exposure, and has no impact on normal readout W.R.T. IQ or row and frame time. The online pixel test can use a region of interest (ROI) to determine the total number of faulty pixels within that ROI. If the detected number of failing pixels in the ROI is higher than a configurable threshold, an error signal (read from register/embedded line and/or ERRB pin) will trigger and the OX03C10 can transition to safe state (if configured).

The online pixel test can also check it is functional every frame with an integrity test in parallel with the pixel test itself, and by fault injection in a test row.

figure 8-4 online pixel test



8.5.5 analog test pattern row (ATPR)

The OX03C10 sensor supports two analog test pattern rows embedded with every frame. The test patterns are inserted early in the analog datapath at the input of the analog readout channel (A/D converter), and can optionally be output as additional rows in the output image data. The test pattern rows will be used for internal safety checks on the sensor and it is not necessary to output the test pattern rows.

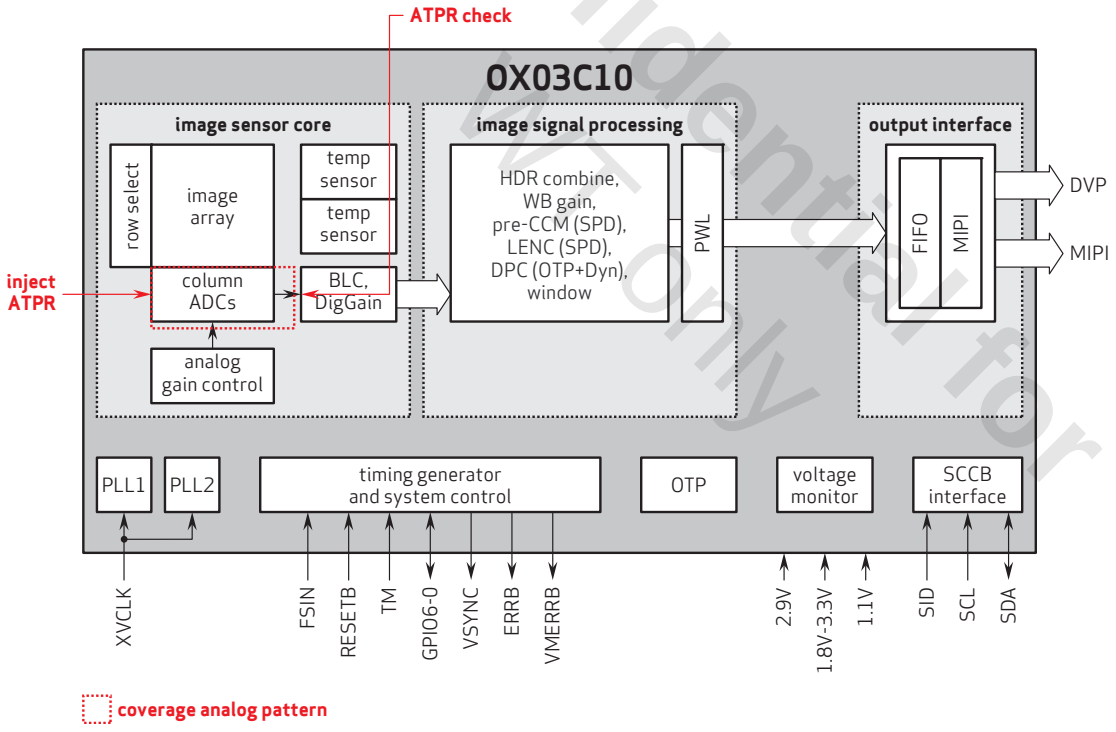
The test patterns are generated by applying pre-known and pre-set voltage levels, giving a flat gray level value for both rows.

8.5.5.1 ATPR checker

The ATPR checker checks if the values in the ATPR received by the digital domain are within an acceptable range. Due to noise and other factors, values in these rows will have variance. If there is an extreme difference, it can be due to an error in the ADC or memory and it will be detected.

Any detected error will trigger an error signal (read from register/embedded line and/or ERRB pin) and the OX03C10 can transition to safe state (if configured).

figure 8-5 ATPR checker



8.5.6 row and column identifiers

The OX03C10 supports column and row identifiers which add a row ID and column ID to each row/column of the image, as shown in **figure 8-3**.

The start, order, and/or number of rows and columns can then be checked externally if there is any mismatch caused by the processing blocks, including data buffers and data output according to expected output format. The row and column ID will be used for internal safety checks on the sensor. It is not necessary to output the extra rows and columns.

8.5.6.1 row and column ID checker

The OX03C10 can check if the row-IDs and column-IDs going out with the active image from pixel array are correct according to crop ROI settings and mirror/flip/skip/binning settings. The checker will verify the start and end row or column identifiers against the crop settings. It can also verify if they are incrementing correctly from row-to-row and column-to-column. The start, order, and/or number of rows and columns is checked if it has been altered by the processing blocks, including buffers and data output.

Any detected error will trigger an error signal (read from register/embedded line and/or ERRB pin) and the OX03C10 can transition to safe state (if configured).

8.5.7 internal reference voltage

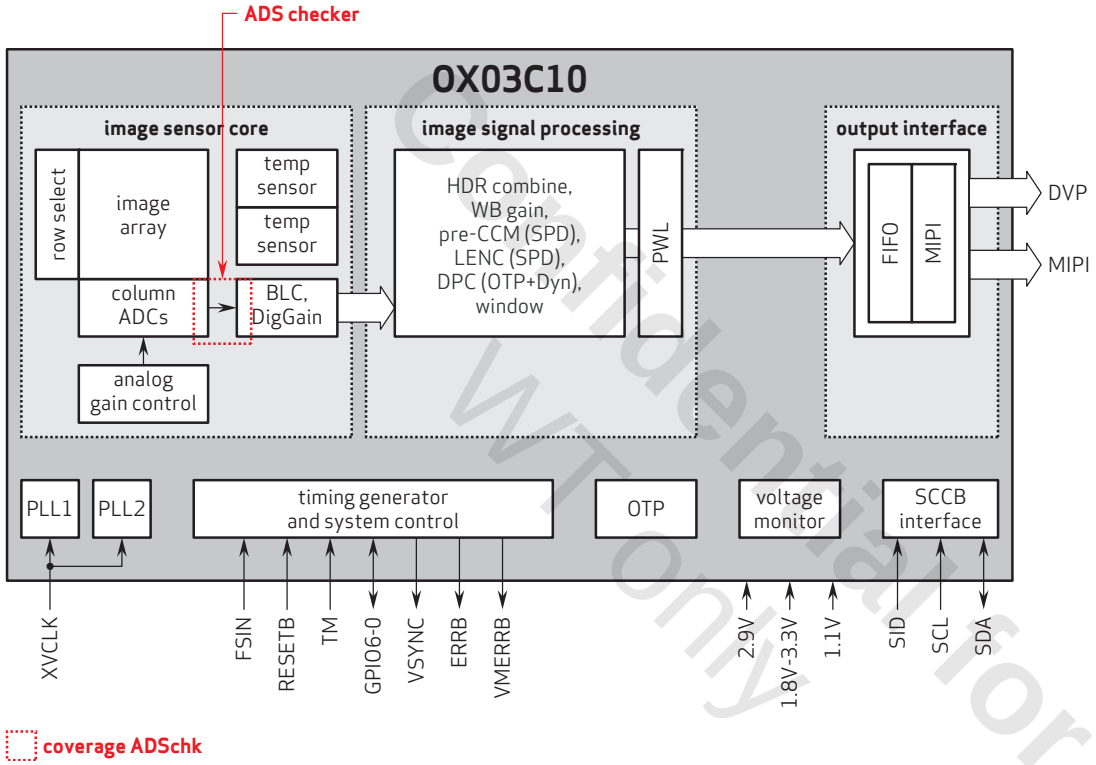
The OX03C10 internal reference monitor will check that the internal reference level for pixel control signals is within an acceptable range. Whenever an out of range voltage is detected by the comparator, an error signal (read from register/embedded line and/or ERRB pin) will be triggered and the OX03C10 can transition to safe state (if configured).

The accuracy and acceptable threshold for each comparator will be provided by OmniVision after complete characterization.

8.5.8 analog to digital sync check

The OX03C10 has a safety mechanism to check the readout and synchronization from the analog datapath output (ADCs) to the digital datapath input (BLC). The analog to digital sync check (ADSchk) uses extra rows for each frame read from pixel array and injects a pre-known pattern into the test row to check memories and buffers between ADC and BLC. If the test row readout values do not match the expected patterns, an error signal (read from register/embedded line and/or ERRB pin) is triggered and the OX03C10 can transition to safe state (if configured).

figure 8-6 ADS checker



8.5.9 digital test pattern row (DTPR)

The sensor supports six digital test pattern rows embedded with every frame for each color channel (separately). The digital test pattern rows (DTPR) are inserted early in the datapath (after ADC and before BLC) and are processed for every frame. The DTPR is used to check digital processing including BLC, ISP blocks, and output interface before MIPI output.

The test patterns are generated by a simple counter (up/down) based pattern for each color channel with configurable offset. The pixel values along the test rows increment/decrement, representing a saw-tooth like shape covering the complete data range. The initial offset (DN) to initially start counting from at the beginning of the row is configurable. When the counter reaches max value, it will restart from 0.

8.5.9.1 DTPR checker

The digital test pattern rows will be processed by digital processing blocks in two ways:

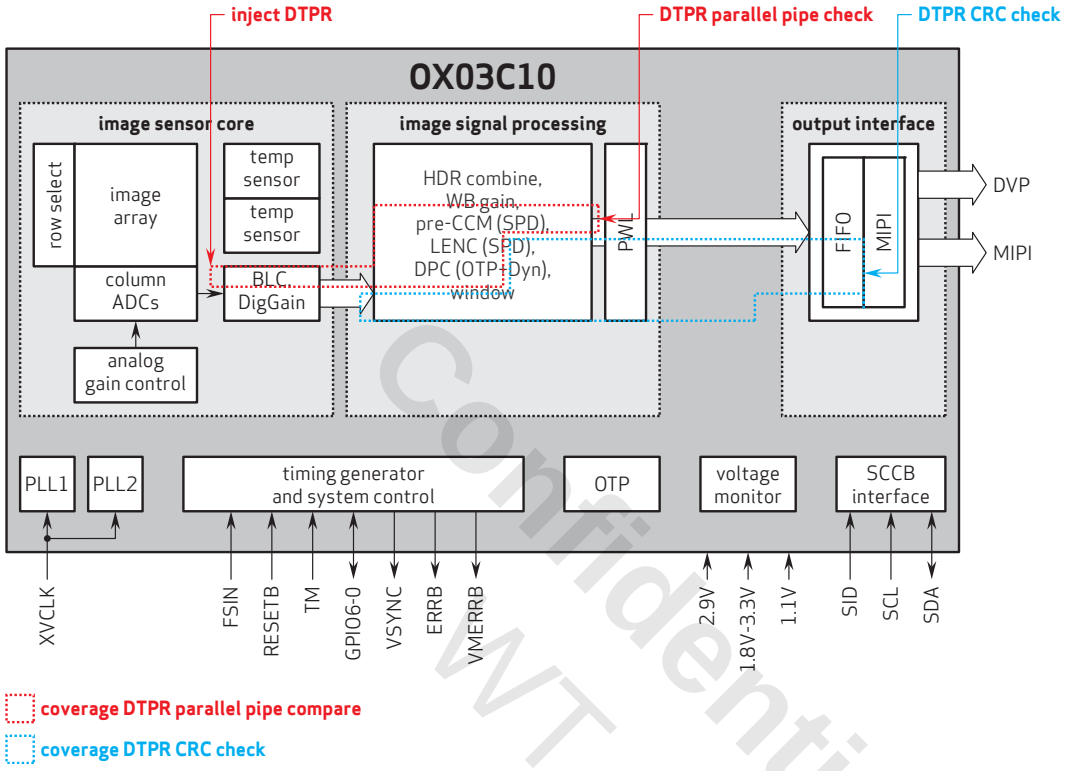
- parallel pipe comparison: Same data is inserted in two parallel pipes and a checker compares that they give the same result. Modules covered by this mode are BLC and ISP blocks with two pipelines as shown in **figure 4-1**.
- CRC check: DTPR is processed by each module and a CRC32 is calculated on pixel values and compared to an expected CRC (after output FIFO). Modules not covered by parallel pipe comparison will be covered with this mode.

Any detected error will trigger an error signal and the OX03C10 can transition to safe state (if configured).

The OX03C10 has a mechanism that checks failure within the BLC logic and detects compromised black rows. The correction value difference for each color channel is compared with the average correction value. Any mismatch that exceeds a programmable limit will trigger an error flag signal. The mismatch error flag signal indicates potential failure in BLC logic or compromised black rows.

Note that the DTPR checker functionality might not be valid for all operating modes. For example, if short exposure is disabled, a fault mask must be set accordingly to reflect the user's operating modes.

figure 8-7 DTPR checker



8.5.10 BLC checker

In addition to DTPR check, the BLC will have integrity check of the calculation. If any error is detected, an error signal (read from register/embedded line and/or ERRB pin) will be triggered and the OX03C10 can transition to safe state (if configured).

8.5.11 PLL clock monitor

The OX03C10 will monitor the internal clock generation (PLL) on-chip by checking the system core clock, SCLK/PCLK. During normal operation, the PLL clock monitor system will continuously check the output clock signal (SCLK/PCLK).

The clock monitor needs to be configured with the correct settings according to the expected clock frequency and tolerance levels before enabling. The SCLK frequency out of this range will trigger an error signal (read from register/embedded line and/or ERRB pin) and the OX03C10 can transition to safe state (if configured).

The PLL lock monitor is dependent on the XVCLK and will not detect incorrect XVCLK frequency.

8.5.11.1 PLL clock monitor integrity check

The OX03C10 PLL clock monitor has a CRC based integrity check mechanism. The monitoring system outputs a bit-wise output stream to a check sum generator (CRC) which will perform CRC calculation. The CRC calculation

stops whenever the bit-wise comparator shows a match. If CRC is not as expected, the PLL clock monitor logic is not correct. An error signal will be triggered and the OX03C10 can transition to safe state (if configured).

8.5.11.2 PLL lock state monitoring

Both PLLs in the OX03C10 sensor have an intrinsic lock function which signals when PLLs VCO frequency is settled and the propagated clocks are stable. The PLLs outputs a signal that indicates if the PLLs are in lock status. This signal goes into PLL lock checker. If PLL is not locked or out of lock any time after the timer has completed, an error signal (read from register/embedded line and/or ERRB pin) will be triggered and the OX03C10 can transition to safe state (if configured).

Usually when applying a new PLL setting, the PLLs will lose lock temporarily until a new frequency settles on the predefined setting. It is not expected that PLL settings change during streaming.

8.5.12 SCCB E2E protection

The OX03C10 has two methods to protect SCCB communication with CRC. Both methods are SCCB compatible and the host must select which method to use by register bit.

- SCCB single/sequential write with CRC
- block message read/write with packet error checking (PEC) CRC

8.5.12.1 SCCB single/sequential write with CRC

Single/sequential CRC mode is the default mode for SCCB CRC. CRC-16 is continuously calculated on write operations for single messages (address and data) or sequential messages. The CRC is updated in a dedicated SCCB register where the host can check the calculated CRC at specific intervals or through embedded line. The host must calculate the CRC before writing registers and reading back (embedded line) the SCCB CRC register for comparison after write sequence. If the CRC read from this register does not match the expected CRC calculated by host when writing, host must take necessary actions. CRC on read is not supported in this mode (see **section 6.3.1**).

8.5.12.2 block message read/write with SCCB PEC CRC

The block read/write with packet error checking (PEC) follows the SMBus ver3.0 specification. It automatically checks the CRC-8 appended for each packet for write operations and appends a CRC-8 for host to check for read operations.

If PEC detects an error on write operations, a NACK is generated and an error flag will be set if several erroneous writes are detected (see **section 6.3.2**).

8.5.13 SCCB register lock

The OX03C10 can lock access to SCCB registers after initial configuration to avoid unintentional writes which can change the OX03C10's intended operation.

To write to the locked registers an unlock bit must be written before registers can be updated. Registers that are expected to be written frequently (e.g. gain, exposure) will not be protected by SCCB register lock and does not need to be unlocked before written to.

The following is a list of unlocked registers:

- 0x3187
- 0x3500~0x350F
- 0x3540~0x354F
- 0x3580~0x358F
- 0x35C0~0x35CF
- 0x5280~0x5287
- 0x5480~0x5487
- 0x5680~0x5687
- 0x5880~0x5887
- 0x3208

8.5.14 internal register read-back check

The OX03C10 SCCB has a register read-back mechanism that will check if internal writing to SCCB registers is correct compared to received data. The internal read-back is done on separate bus to ensure correct state in register flip-flop:

- after silicon default values are loaded from ROM at startup
- after OTP load is done and registers written from OTP SRAM
- on all external SCCB writes to registers

Any detected error will trigger an error signal (read from register/embedded line and/or ERRB pin) and the OX03C10 can transition to safe state (if configured).

8.5.15 embedded data

Additional information about the set up and configuration of the sensor will be embedded in the image frame. The embedded data contains the values of a programmable list of registers (including error flags) to describe the current state of the sensor (e.g., frame counter, exposure time, and gain, etc.). The embedded data information is synchronous with the image frame.

8.5.15.1 embedded data E2E protection

To ensure E2E protection of the embedded data and mitigate transmission errors, the last entries in the embedded rows are CRC values (4 bytes).

The programming of the embedded data is protected through SCCB CRC and the storage of embedded register to send out (group hold) is also CRC protected. The latter CRC can be output on embedded line for host to check if the programmed registers for embedded line are the actual outputted registers. This CRC is also checked internally. Any detected error will trigger an error signal (read from register/embedded line and/or ERRB pin) and the OX03C10 sensor can transition to safe state (if configured). See **section 5.5.4** and **section 5.6.1** for more information.

8.5.16 SI default register check

The OX03C10 stores the silicon default registers on ROM. In addition to the ROM CRC, the correct copying from ROM to register flip flops to guarantee the OX03C10 is correctly configured at start up is ensured by internal registers read-back. It compares all ROM writes to registers with the read back register value. If the comparison fails, an error signal (read from register/embedded line and/or ERRB pin) will be triggered and the OX03C10 can transition to safe state (if configured).

8.5.17 MIPI CRC/ECC

MIPI CRC and ECC will enable the host to detect data transmission errors.

The OX03C10 MIPI CRC is a 16-bit cyclic redundancy check (CRC) calculated over each image row.

The 32-bit packet header's last byte contains ECC, which allows for one faulty bit to be corrected and up to two faulty bits to be detected in the packet header.

The ECC/CRC generation, follows the MIPI CSI-2 standard and is transmitted as part of the packet header and footer of the image data while the sensor is streaming.

The host must ensure ECC and CRC are checked and take appropriate action if any error detected.

8.5.18 output FIFO CRC

The output FIFO will pack and buffer image data from internal clock domain to output clock domain according to output format (MIPI: valid data width and number of used output lanes). The output FIFO CRC is active when streaming image data. Any detected error will trigger an error signal (read from register/embedded line and/or ERRB pin) and the OX03C10 sensor can transition to safe state (if configured).

8.5.19 ROM CRC check fail

The OX03C10 has a mechanism that calculates ROM CRC while loading and compares it with the stored CRC during start up mode. Any mismatch between the calculated CRC and the stored ROM CRC will trigger an error signal (read from register/embedded line and/or ERRB pin) and the OX03C10 can transition to safe state (if configured).

8.5.20 OTP CRC

The OX03C10 OTP memory containing wafer info, temperature sensor calibration, and OTP-DPC is protected with CRC. The CRC will be stored in OTP and will be read out to OTP RAM at start up together with normal content. The user needs to read OTP RAM data, and calculate CRC to check whether it matches expected CRC.

The OTP CRC will mitigate error in OTP, OTP load, and OTP SRAM.

8.5.21 SRAM built in self-test (MBIST)

The OX03C10 memories have a built in self-test (MBIST) wrapped on each SRAM. The MBIST is automatically run during startup mode and a pass/fail result will be available from register. Any detected error will trigger an error signal (read from register/embedded line and/or ERRB pin) and the OX03C10 sensor can transition to safe state (if configured).

8.5.22 SRAM CRC

The OX03C10 supports online CRC check on selected critical SRAMs. The CRC is calculated for all data written to the selected SRAMs and correspondingly checked when read out. The SRAM CRC is used to detect transient/permanent faults (such as stuck at fault) within the SRAM. Fault(s) detected by the SRAM CRC will trigger an error signal (read from register/embedded line and/or ERRB pin) and the OX03C10 can transition to safe state (if configured).

8.5.23 temperature sensor

The OX03C10 has two embedded temperature sensors that measure the junction temperature. The average temperature from the two sensors can be read back from SCCB register in degree Celsius (°C) and the host controller can also read the temperature values from embedded line to monitor the temperature. The range of the temperature reading is from -40°C to 125°C. The temperature reading outside this temperature range is expected to be less reliable. The host must take appropriate action when temperature reading is too high or too low.

8.5.23.1 temperature sensor integrity check

The readings from the two temperature sensors are continuously compared internally. If there is an unexpected considerable difference between the temperature sensors, an error signal (read from register/embedded line and/or ERRB pin) will be triggered and the OX03C10 can transition to safe state (if configured).

8.5.23.2 temperature sensor self-test

The OX03C10 temperature sensor has a self-test mechanism to check the temperature sensor conversion by injecting known stimuli. If the resulting temperature is not as expected, an error signal (read from register/embedded line and/or ERRB pin) will be triggered and the OX03C10 sensor can transition to safe state (if configured).

8.5.24 supply voltage monitor

The OX03C10 monitors supply voltages (AVDD, DVDD, and DOVDD) delivered to the sensor and can mitigate potential failure with:

- power traces on PCB
- sensor power pads

The measurement from the voltage monitor can be read from registers (see **table 8-2**) or from embedded lines. The real measured value = register value in decimal * 6 /4096.

table 8-2 VM supply voltages readout registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4581	VM_CTRL	0xC7	RW	Bit[2]: DVDD enable Bit[1]: DOVDD enable Bit[0]: AVDD enable
0x45A0	AVDD_RESULT	–	R	Bit[3:0]: AVDD[11:8]
0x45A1	AVDD_RESULT	–	R	Bit[7:0]: AVDD[7:0]
0x45A2	DOVDD_RESULT	–	R	Bit[3:0]: DOVDD[11:8]
0x45A3	DOVDD_RESULT	–	R	Bit[7:0]: DOVDD[7:0]

table 8-2 VM supply voltages readout registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x45A4	DVDD_RESULT	–	R	Bit[3:0]: DVDD[11:8]
0x45A5	DVDD_RESULT	–	R	Bit[7:0]: DVDD[7:0]

The voltage monitor will be calibrated by OmniVision and the offset will be stored in the OTP. To improve accuracy from voltage monitor, the offset values in OTP should be added to the values from the VM supply readout registers.

The VM needs to be enabled by SCCB register 0x4581:

- 0x4581[2] = 1: enable DVDD monitor
- 0x4581[1] = 1: enable DOVDD monitor
- 0x4581[0] = 1: enable AVDD monitor

In the event that DVDD and/or DOVDD supply is missing, the VMERRB pin will be pulled low.

8.5.24.1 voltage monitor self-test

The OX03C10 voltage monitor has a self-test mechanism to check the voltage sensor conversion by injecting known stimuli. If the resulting temperature is not as expected, an error signal (read from register/embedded line and/or ERRB pin) will be triggered and the OX03C10 can transition to safe state (if configured).

8.5.25 frame counter

The OX03C10 has a 32-bit frame counter that can be read from registers or from embedded line. The counter is triggered by internal start of frame signal which is initiated from readout of the first row by the MIPI core. The frame counter is always updated while the sensor is streaming. The user can check frame counter in embedded line, monitor correct frame number sequence, and check for any dropped frames. The frame counter is not checked on-chip and will not trigger any error signal.

8.5.26 digital pattern generator

The OX03C10 can output digital patterns to enable the host to detect transmission error and/or error in the digital datapath. The digital test patterns are only available when the OX03C10 ISP is enabled. The test patterns are injected at the start of the digital datapath and are processed as normal image data in ISP. The digital test pattern test is not a safety mechanism that can detect errors by itself and cannot transition to safe state (see **section 4.1**).

9 operating specifications

9.1 absolute maximum ratings

table 9-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-50°C to +125°C
supply voltage (with respect to ground)	AVDD	4.5V
	DVDD	3V
	DOVDD	4.5V
all input/output voltages (with respect to ground)		-0.3V to DOVDD + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to device; exposure to absolute maximum rated conditions for extended periods may affect device reliability

9.2 functional temperature

table 9-2 functional temperature

parameter	range
operating temperature[a]	-40°C to +125°C sensor junction temperature -40°C to +105°C ambient temperature

a. sensor functions in operating range; however, some image quality changes may be noticed at temperature extremes

9.3 DC characteristics

table 9-3 DC characteristics (-40°C < T_J < 125°C)

symbol	parameter	min	typ	max	unit
supply					
AVDD	supply voltage analog	2.7	2.9	3.1	V
DVDD	supply voltage digital circuit DVDD and MIPI core	1.05	1.1	1.16	V
DOVDD	supply voltage digital I/O	1.62	1.8	1.98	V
		2.97	3.3	3.63	V
I_{AVDD}	active (operating) current - sensor is streaming		66[a]		mA
I_{DVDD}			141[b]		mA
I_{DOVDD}			0.21[c]		mA
$I_{AVDD-PWDN}$	standby current[d]		10		µA
$I_{DVDD-PWDN}$			1.85		mA
$I_{DOVDD-PWDN}$			65		µA
internally derived voltages[e]					
V_{H1}	positive reference voltage 1	2.8	3.1	3.4	V
V_{H2}	positive reference voltage 2	2.6	2.8	3.0	V
V_{N1}	negative reference voltage 1	-1.8	-1.4	-0.8	V
V_{N2}	negative reference voltage 2	-1.8	-1.4	-0.8	V
digital inputs (typical conditions: AVDD = 2.9V, DOVDD = 1.8V, DVDD = 1.1V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[f]	SCL and SDA	-0.5	0	0.54	V
V_{IH}[f]	SCL and SDA	1.28	1.8	2.32	V
		2.78	3.3	3.82	V

a. based on simulation (4 captures, full resolution)
b. based on simulation (4 captures, full resolution), V_{DD-D} = 1.1V
c. based on simulation (4 captures, full resolution), V_{DD-IO} = 3.3V
d. standby current based on room temperature
e. not to be in contact with external devices, except for adjacent capacitors, reference voltages specified for operating mode
f. based on DOVDD = 1.8V

9.4 AC characteristics

figure 9-1 clock specification illustration

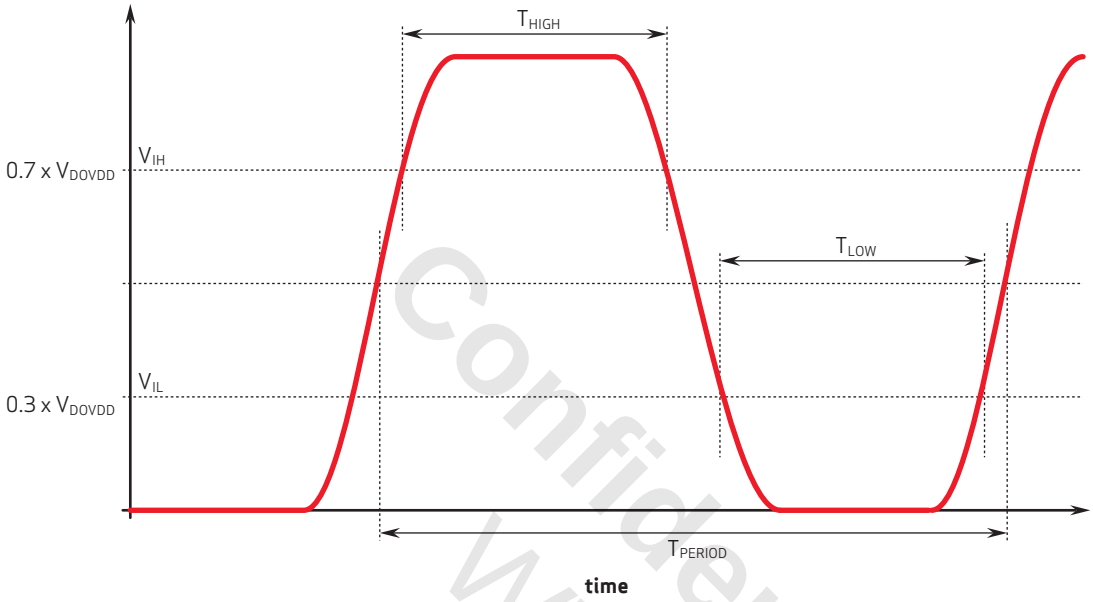


table 9-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{XVCLK}	frequency (XVCLK)	18	24	27[a]	MHz
T_XVCLK_jitter	allowed RMS jitter (XVCLK)			100	ps
C_XVCLK	input capacitance (XVCLK)			1.5	pF
T_{PERIOD}	period (XVCLK)	37	41.7	55.6	ns
T_{LOW}	low level width (XVCLK)	$0.35 \times T_{PERIOD}$		$0.65 \times T_{PERIOD}$	ns
T_{HIGH}	high level width (XVCLK)	$0.35 \times T_{PERIOD}$		$0.65 \times T_{PERIOD}$	ns

a. other frequencies can be supported via OTP trimming

10 mechanical specifications

10.1 physical specifications

figure 10-1 package specifications

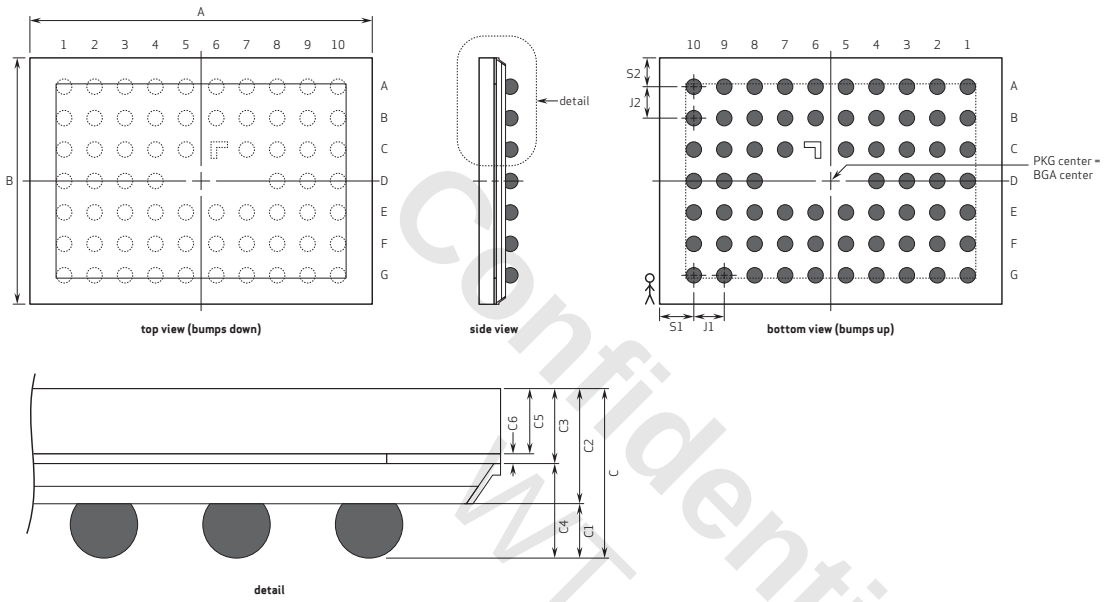


table 10-1 package dimensions (sheet 1 of 2)

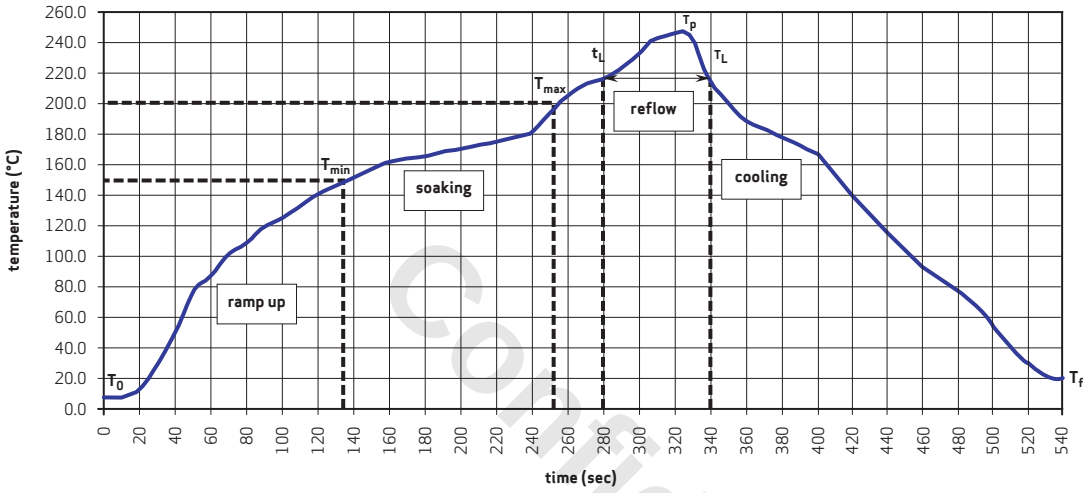
parameter	symbol	min	typ	max	unit
package body dimension x	A	6837	6862	6887	µm
package body dimension y	B	4911	4936	4961	µm
package height	C	720	780	840	µm
ball height	C1	220	250	280	µm
package body thickness	C2	495	530	565	µm
thickness of glass surface to wafer	C3	325	345	365	µm
image plane height	C4	390	435	480	µm
glass thickness	C5	285	300	315	µm
air gap between sensor and glass	C6	41	45	49	µm
ball diameter	D	280	310	340	µm
total ball count	N		66 (4 NC)		

table 10-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
pin pitch x-axis	J1		610		µm
pin pitch y-axis	J2		630		µm
edge-to-pin center distance along x	S1	656	686	716	µm
edge-to-pin center distance along y	S2	548	578	608	µm

10.2 IR reflow specifications

figure 10-2 IR/solder reflow ramp rate profile requirements



note The OX03C10 uses a lead free package.

table 10-2 reflow conditions[ab]

zone	description	exposure
ramp up A (T_0 to T_{min})	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90~150 seconds
ramp up B (t_L to T_P)	heating from 217°C to 245°C	temperature slope ≤ 3°C per second
peak temperature	maximum temperature in SMT	245°C +0/-5°C (duration max 30 sec)
reflow (t_L to T_L)	temperature higher than 217°C	30~120 seconds
ramp down A (T_P to T_L)	cooling from 245°C to 217°C	temperature slope ≤ 3°C per second
ramp down B (T_L to T_f)	cooling from 217°C to room temperature	temperature slope ≤ 6°C per second
T_0 to T_P	room temperature to peak temperature	≤ 8 minutes

a. maximum number of reflow cycles = 3

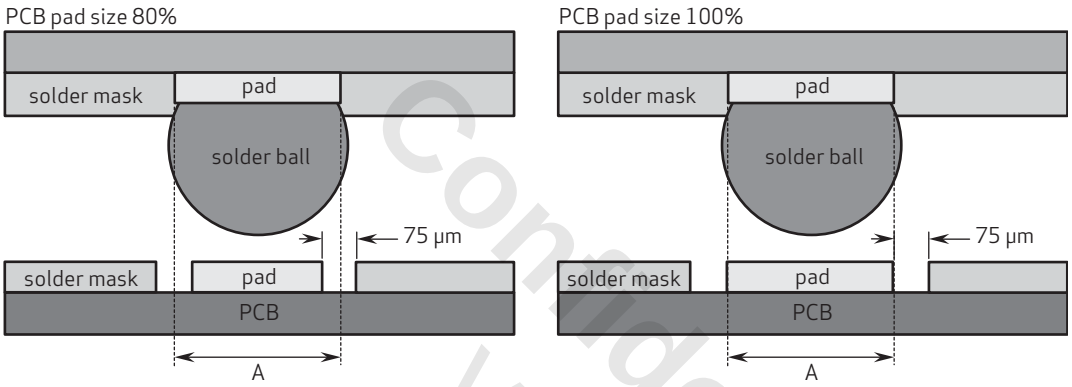
b. N2 gas reflow or control O2 gas PPM < 500 as recommendation

10.3 PCB and SMT design recommendations

10.3.1 PCB design recommendations

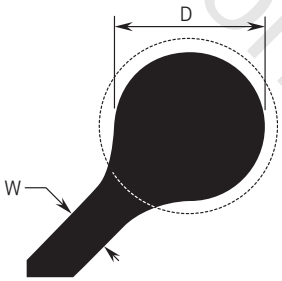
- solder pad of PCB: non solder mask defined (NSMD)
- PCB pad size: 90% ± 10% (80~100%) of package's ball pad opening
- gap between pad to neighboring solder mask: 75 µm (minimum)

figure 10-3 PCB pad example



- trace width: must be less than 1/2 ball diameter (W<1/2 D)
- recommend adding tear drop design on trace connecting to via and pad

figure 10-4 tear drop design example



- PCB material: high performance FR4 with high Tg and low CTE substrate material is recommended
- package edge to PCB edge minimum 1.0 mm is recommended

table 10-3 ball pad opening size and recommended PCB NSMD ball pad size

device name	package type	package size	CSP/BGA ball pad opening size	recommended PCB NSMD ball pad size
OX03C10	a-CSP	6862 µm x 4936 µm	250 µm	225 µm ± 25 µm

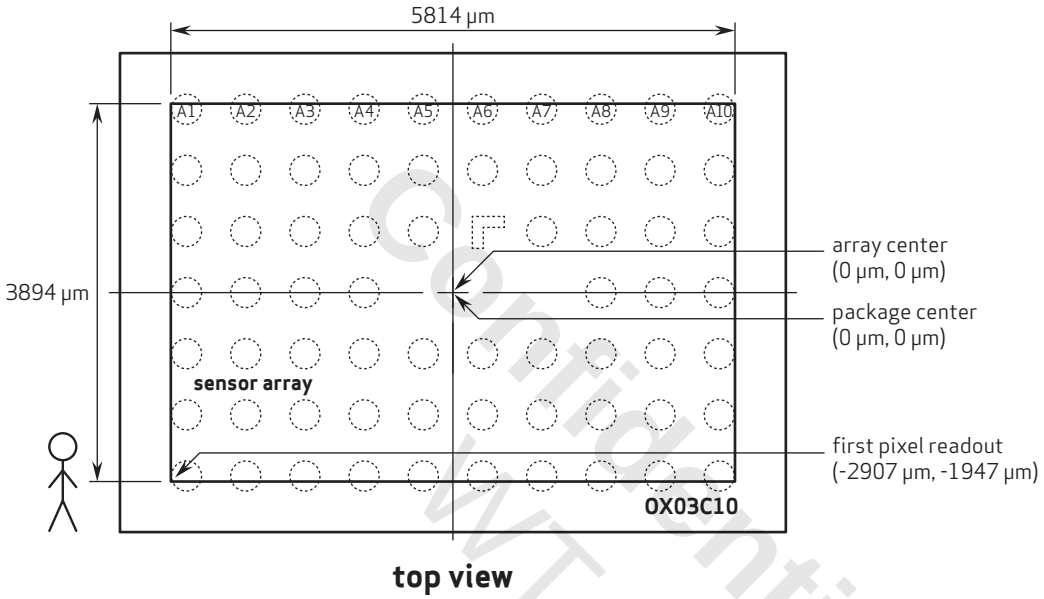
10.3.2 SMT design recommendations

- stencil: laser cut with electro-polishing
- stencil opening: 90~100% of PCB pad size
- stencil thickness: 0.08~0.15 mm
- solder material: SAC 305 is recommended
- solder paste: type 4 (20 µm to 38 µm) or finer solder sphere particle size is recommended
- SMT profile: refer to solder paste datasheet and product datasheet

11 optical specifications

11.1 sensor array center

figure 11-1 sensor array center

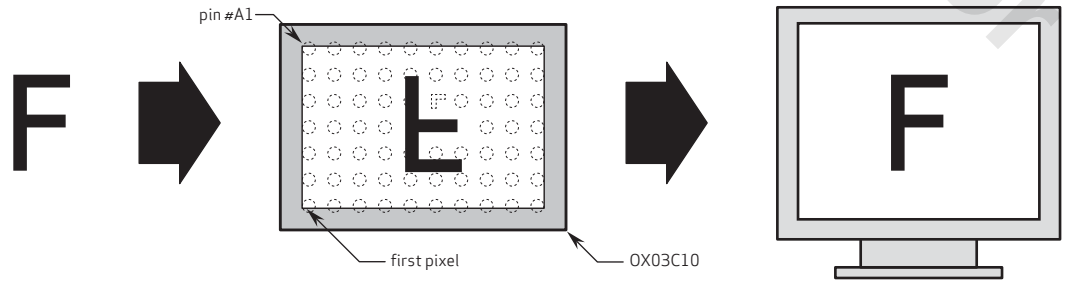


top view

note 1 this drawing is not to scale and is for reference only

note 2 as most optical assemblies mirror image, chip is typically mounted as above with first pixel at bottom left corner

figure 11-2 final image output



original image **output image**

11.2 lens chief ray angle (CRA)

figure 11-3 chief ray angle (CRA)

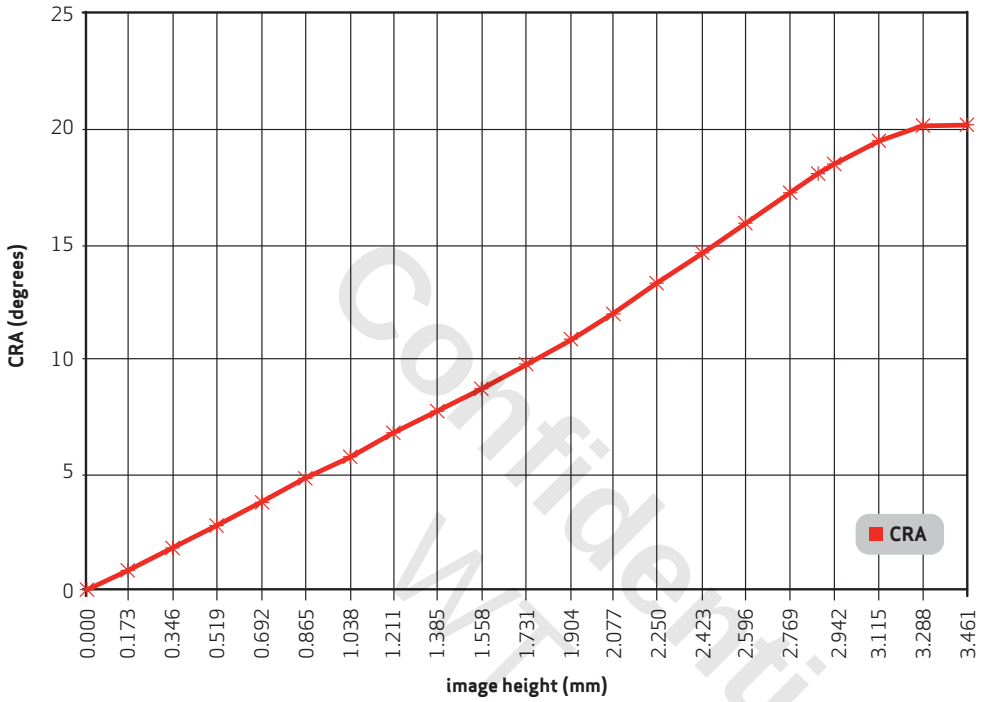


table 11-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0.00	0.000	0.000
0.05	0.173	0.835
0.10	0.346	1.792
0.15	0.519	2.800
0.20	0.692	3.818
0.25	0.865	4.821
0.30	1.038	5.803
0.35	1.211	6.771
0.40	1.385	7.741
0.45	1.558	8.733

table 11-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.50	1.731	9.769
0.55	1.904	10.867
0.60	2.077	12.040
0.65	2.250	13.290
0.70	2.423	14.601
0.75	2.596	15.944
0.80	2.769	17.263
0.85	2.942	18.477
0.90	3.115	19.474
0.95	3.288	20.110
1.00	3.461	20.200

appendix A register table

A.1 module name and address range

table A-1 module name and address range (sheet 1 of 2)

module name	address range
SYSTEM CONTROL (SC, SENSOR)	0x0100~0x010B, 0x3000~0x3CFF
PLL CONTROL (PLL_CTRL)	0x0300~0x0363
PLL MONITOR (PLL_MONITOR, PLL_LOCK)	0x0400~0x0419, 0x0440~0x0442
ROM LOADER (ROMLOADER)	0x2000~0x2008
PIXEL SIGNAL INTEGRITY CHECK (XCHK_REP)	0x2800~0x280D
SCCB CONTROL (SB_SCCB)	0x3100~0x3109
SCCB PACKET ERROR CHECK (SB_PEC)	0x3180~0x31A7
GROUP HOLD CONTROL (GRP_HOLD)	0x3200~0x324F
ASRAM CONTROL (ASRAM_TST_TOP)	0x3300~0x3318
PSV CTRL (PSV_CTRL)	0x3400~0x342F
EXPOSURE AND GAIN (AEC_PK_CORE_HCG, AEC_PK_CORE_LCG, AEC_PK_CORE_SPD, AEC_PK_CORE_VS)	0x3500~0x3522, 0x3580~0x35A2, 0x3540~0x3562, 0x35C0~0x35E2
ANALOG CONTROL (ANA_TOP)	0x3600~0x3676
TIMING CONTROL (TIMING_CTRL)	0x3800~0x3897
ANALOG TEST PATTERN ROWS CHECKER CONTROL (APC)	0x3B40~0x3B61
ONLINE PIXEL TEST CONTROL (PIXEL ASIL) (PIXELASIL_CHK)	0x3B80~0x3B9F
ONE-TIME PROGRAMMABLE CONTROL (OTP_SC)	0x3D00~0x3DA9
SRAM BIST CONTROL (BIST_231_TOP)	0x3E00~0x3E4B
PROGRAMMABLE SRAM CONTROL (PSRAM)	0x3F00~0x3F0F
BLACK LEVEL CORRECTION CONTROL (BLC_TOP)	0x4000~0x40E1
DIGITAL TEST PATTERN ROWS CONTROL (DIG_TEST_ROWS_GEN_TOP)	0x4200~0x422A
SYNC FIFO CONTROL (SYNC_FIFO)	0x4500~0x4511
VOLTAGE MONITOR CONTROL (VM_TOP)	0x4580~0x45BB
VFIFO CONTROL (VFIFO_31)	0x4600~0x4625
ROW/COLUMN UNIQUE ID CHECKER (UID_CHECK_LATE)	0x4640~0x4649
DVP CONTROL (DVP_TOP)	0x4700~0x470C

table A-1 module name and address range (sheet 2 of 2)

module name	address range
MIPI CORE CONTROL (MIPI_CORE)	0x4800~0x487E
MIPI PHY CONTROL (MIPI_PHY)	0x4880~0x488A
ISP FRAME CONTROL (FC)	0x4900~0x4904
TEMPERATURE MONITOR CONTROL (TPM)	0x4D00~0x4D63
WATCHDOG CONTROL (WATCHDOG_TOP)	0x4F00~0x4F0F
ISP CONTROL (ISP_PROC_TOP)	0x5000~0x50EB
PRE ISP CONTROL (PRE_ISP_HCG, PRE_ISP_LCG, PRE_ISP_SPD, PRE_ISP_VS)	0x5200~0x5204, 0x5400~0x5404, 0x5600~0x5604, 0x5800~0x5804
AWB GAIN CONTROL (AWB_GAIN_HCG, AWB_GAIN_LCG, AWB_GAIN_SPD, AWB_GAIN_VS)	0x5240~0x5269, 0x5440~0x5469, 0x5640~0x5669, 0x5840~0x5869
DPC CONTROL (DPC_1745_HCG, DPC_1745_LCG, DPC_1745_SPD, DPC_1745_VS)	0x52C0~0x52EF, 0x54C0~0x54EF, 0x56C0~0x56EF, 0x58C0~0x58EF
OTP DPC CONTROL (OTP_DPC_3245_TOP_HCG, OTP_DPC_3245_TOP_LCG, OTP_DPC_3245_TOP_SPD, OTP_DPC_3245_TOP_VS)	0x5300~0x5337, 0x5500~0x5537, 0x5700~0x5737, 0x5900~0x5937
HDR COMBINE CONTROL (COMBINE_3004_0, COMBINE_3004_1, COMBINE_3004_2)	0x5B80~0x5BF1, 0x5C00~0x5C71, 0x5C80~0x5CF1
STATISTICS DATA CONTROL (STATIC_1015_D2V2_0, STATIC_1015_D2V2_1, STATIC_1015_D2V2_2, STATIC_1015_D2V2_3, STATIC_1015_D2V2_4)	0x6000~0x601E, 0x6020~0x603E, 0x6040~0x605E, 0x6060~0x607E, 0x6080~0x609E
PEICEWISE LINEAR CONTROL (PWL_0245_0, PWL_0245_1)	0x5E00~0x5E85, 0x5F00~0x5F85
WINDOW CONTROL (WINDOW_D2V2)	0x6A00~0x6A2C

A.2 sensor register table

table A-2 sensor control registers (sheet 1 of 255)

address	register name	default value	R/W	description
0x0100	SMIA_R0100	0x00	RW	Bit[7:1]: Not used Bit[0]: Stream 0: software_standby 1: Streaming
0x0102	SMIA_R0102	0x00	RW	Bit[7:1]: Not used Bit[0]: truncation_stanby_mode truncation_stanby
0x0103	SMIA_R0103	0x00	RW	Bit[7:1]: Not used Bit[0]: software_reset
0x0104	SMIA_R0104	0x04	RW	Bit[7:3]: Not used Bit[2]: enter_stream_off Bit[1]: leave_safe_mode Bit[0]: enter_safe_mode
0x0105	SMIA_R0105	0x00	RW	Bit[7:2]: Not used Bit[1]: byp_start_up_otp Bypass start-up test Bit[0]: enter_sfw_stb
0x0106	SMIA_R0106	0x00	RW	Bit[7:0]: sc_state_ctrl
0x0107	SMIA_R0107	0x00	RW	Bit[7:1]: Not used Bit[0]: software_reset2 Reset to sfw_stb
0x0108	SMIA_R0108	–	R	Bit[7:4]: Not used Bit[3:0]: sc_state
0x0109	SMIA_R0109	0x00	RW	Bit[7:1]: Not used Bit[0]: leave_safe_en
0x010A	SMIA_R010A	0x10	RW	Bit[7:0]: stream_wait_h
0x010B	SMIA_R010B	0x00	RW	Bit[7:0]: stream_wait_l
0x0300	PLL1_CTRL0	0x3A	RW	Bit[7:6]: Not used Bit[5]: pll1_sel_lock Bit[4]: pll1_sel_gated Bit[3]: pll1_bp_vco_sync Bit[2]: pll1_rst Bit[1]: pll1_dither_en Bit[0]: pll1_bypass

table A-2 sensor control registers (sheet 2 of 255)

address	register name	default value	R/W	description
0x0301	PLL1_CTRL1	0xC8	RW	Bit[7]: pll1_divs Bit[6]: pll1_predivp Bit[5:4]: Reserved Bit[3]: pll1_divpix Bit[2:0]: Not used
0x0302	PLL1_CTRL2	0x21	RW	Bit[7:6]: Not used Bit[5]: pll1_div_rst_sync_en Bit[4]: pll1_bias_ext Bit[3]: Not used Bit[2:0]: pll1_cp
0x0303	PLL1_CTRL3	0x01	RW	Bit[7:3]: Not used Bit[2:0]: pll1_prediv
0x0304	PLL1_CTRL4	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pll1_loopdiv
0x0305	PLL1_CTRL5	0x2C	RW	Bit[7:0]: pll1_loopdiv
0x0306	PLL1_CTRL6	0x04	RW	Bit[7:3]: Not used Bit[2:0]: pll1_divmipi
0x0307	PLL1_CTRL7	0x01	RW	Bit[7:4]: Not used Bit[3:0]: pll1_divm
0x0308	PLL1_CTRL8	0x13	RW	Bit[7:5]: Not used Bit[4]: pll1_divs_div2 Bit[3:2]: Not used Bit[1:0]: pll1_divsp
0x0309	PLL1_CTRL9	0x03	RW	Bit[7:6]: pll1_precision Bit[5:4]: pll1_cnt_ref Bit[3:2]: Reserved Bit[1]: pll1_rst_lock_det Bit[0]: pll1_en_exti
0x0310	PLL1_CTRL10	0x00	RW	Bit[7:4]: Not used Bit[3:0]: pll1_cntstep
0x0311	PLL1_CTRL11	0x00	RW	Bit[7:3]: Not used Bit[2]: pll1_frac_en Bit[1]: pll1_sscg_3xfast Bit[0]: pll1_sscg_en
0x0312	PLL1_CTRL12	0x07	RW	Bit[7:3]: Not used Bit[2:0]: pll1_cntck
0x0313	PLL1_CTRL13	0x00	RW	Bit[7:4]: Not used Bit[3:0]: pll1_dsm
0x0314	PLL1_CTRL14	0x00	RW	Bit[7:0]: pll1_dsm
0x0315	PLL1_CTRL15	0x00	RW	Bit[7:0]: pll1_dsm

table A-2 sensor control registers (sheet 3 of 255)

address	register name	default value	R/W	description
0x0316	PLL1_CTRL16	0x00	RW	Bit[7:0]: pll1_reserve2
0x0317	PLL1_CTRL17	0x00	RW	Bit[7:0]: pll1_reserve3
0x0318	PLL1_CTRL18	0x00	RW	Bit[7:4]: Not used Bit[3:0]: pll1_reserve4
0x0320	PLL2_CTRL0	0x12	RW	Bit[7]: pll2_bp_vco_sync Bit[6]: pll2_sel_bak_divs Bit[5]: pll2_sel_bak_sa1 Bit[4]: pll2_en_extl Bit[3]: Reserved Bit[2]: pll2_rst Bit[1]: pll2_div_rst_sync_en Bit[0]: pll2_bypass
0x0321	PLL2_CTRL1	0x31	RW	Bit[7:6]: Not used Bit[5]: pll2_sel_lock Bit[4]: pll2_sel_gated Bit[3]: Not used Bit[2:0]: pll2_cp
0x0322	PLL2_CTRL2	0x03	RW	Bit[7:6]: pll2_precision Bit[5:4]: pll2_cnt_ref Bit[3:2]: Not used Bit[1]: pll2_reset_lockdet Bit[0]: Not used
0x0323	PLL2_CTRL3	0x04	RW	Bit[7:3]: Not used Bit[2:0]: pll2_prediv
0x0324	PLL2_CTRL4	0x00	RW	Bit[7:2]: Not used Bit[1:0]: pll2_divp
0x0325	PLL2_CTRL5	0xC8	RW	Bit[7:0]: pll2_divp
0x0326	PLL2_CTRL6	0x09	RW	Bit[7]: pll2_predivp Bit[6]: pll2_bias_ext Bit[5]: pll2_sa1_clk_sel Bit[4]: sa1_post_div 0: 1+r_div_sa1 Bit[3:0]: 2*(1+r_div_sa1[3:0])
0x0327	PLL2_CTRL7	0x04	RW	Bit[7:4]: Not used Bit[3:0]: pll2_divsram 1+r_divsam
0x0329	PLL2_CTRL9	0x01	RW	Bit[7:4]: Not used Bit[3:0]: pll2_divdac 1+r_divdac
0x032A	PLL2_CTRLA	0x04	RW	Bit[7:4]: Not used Bit[3:0]: pll2_divsys_pre 1+r_div_sys_pre

table A-2 sensor control registers (sheet 4 of 255)

address	register name	default value	R/W	description
0x032B	PLL2_CTRLB	0x06	RW	Bit[7:4]: Not used Bit[3:0]: pll2_divsys 1/1.5/2/2.5/3/3.5/4/4.5/5/6/7/8/9/10/1/1
0x032C	PLL2_CTRLC	0x03	RW	Bit[7:2]: Not used Bit[1:0]: pll2_sram_prediv 1+r_sram_prediv
0x032D	PLL2_CTRLD	0x01	RW	Bit[7:1]: Not used Bit[0]: pll2_sa1_prediv 1+r_sa1_prediv
0x032E	PLL2_CTRLE	0x00	RW	Bit[7:1]: Not used Bit[0]: pll2_dac_prediv 1+r_dac_prediv
0x032F	PLL2_CTRLF	0x00	RW	Bit[7:4]: Not used Bit[3:1]: pll2_reserve2 Bit[0]: pll2_sel_bak_divc
0x0330	PLL2_CTRL30	0x09	RW	Bit[7:4]: Not used Bit[3:0]: pll2_divcpu_pre 1+r_div_cpu_pre
0x0331	PLL2_CTRL31	0x04	RW	Bit[7:4]: Not used Bit[3:0]: pll2_divcpu 1/1.5/2/2.5/3/3.5/4/4.5/5/6/7/8/9/10/1/1
0x0360	MIPI_BIT_CONTROL	0x09	RW	Bit[7]: Reserved Bit[6]: lvds_bit_sel_man_en Bit[5:4]: lvds_bit_sel_man Bit[3]: Reserved_0 Bit[2:0]: mipi_bit_sel
0x0361	PLL_SMOOTHLY_CHANGE_VCO_CONTROL	0x00	RW	Bit[7:4]: Not used Bit[3]: pll1_lat_sel Bit[2]: pll3_lat_en Bit[1]: pll2_lat_en Bit[0]: pll1_lat_en

table A-2 sensor control registers (sheet 5 of 255)

address	register name	default value	R/W	description
0x0362	PLL_BASEBAND_AND_LPFRES	0x6A	RW	Bit[7:5]: pll2_lpf_res Adjust resolution in LPF to get a better phase margin for PLL 2 loop Bit[4]: pll2_bandsel Choose high band and low band for FVCO PLL 2 Bit[3:1]: pll1_lpf_res Adjust resolution in LPF to get a better phase margin for PLL 1 loop Bit[0]: pll1_bandsel Choose high band and low band for FVCO PLL 1
0x0363	PLL_SPEEDUP	0xC0	RW	Bit[7]: pll2_speedup_en Bit[6]: pll1_speedup_en Bit[5:0]: Not used
0x0400	EXPECTED_CNT_SCLK_H	0xE0	RW	Bit[7:0]: expected_cnt_sclk_h
0x0401	EXPECTED_CNT_SCLK_L	0x80	RW	Bit[7:0]: expected_cnt_sclk_l
0x0403	CRC_CHECKSUM_SCLK_H	0xDE	RW	Bit[7:0]: crc_checksum_sclk_h
0x0404	CRC_CHECKSUM_SCLK_L	0x34	RW	Bit[7:0]: crc_checksum_sclk_l
0x0405	PULSE_WIDTH_SCLK_H	0x3B	RW	Bit[7:0]: pulse_width_sclk_h
0x0406	PULSE_WIDTH_SCLK_L	0xDE	RW	Bit[7:0]: pulse_width_sclk_l
0x0407	TOLERANCE_SCLK	0x08	RW	Bit[7:0]: tolerance_sclk
0x0408	EXPECTED_CNT_PCLK_H	0xE0	RW	Bit[7:0]: expected_cnt_pclk_h
0x0409	EXPECTED_CNT_PCLK_L	0x7F	RW	Bit[7:0]: expected_cnt_pclk_l
0x040A	CRC_CHECKSUM_PCLK_H	0xDE	RW	Bit[7:0]: crc_checksum_pclk_h
0x040B	CRC_CHECKSUM_PCLK_L	0x34	RW	Bit[7:0]: crc_checksum_pclk_l
0x040C	PULSE_WIDTH_PCLK_H	0x47	RW	Bit[7:0]: pulse_width_pclk_h
0x040D	PULSE_WIDTH_PCLK_L	0xD8	RW	Bit[7:0]: pulse_width_pclk_l
0x040E	TOLERANCE_PCLK	0x08	RW	Bit[7:0]: tolerance_pclk
0x040F	FAULT_CLOCK_FLAGS_SCLK_MASK	0x00	RW	Bit[7:2]: Not used Bit[1]: clock_count_flag_sclk_mask Bit[0]: crc_checksum_flag_sclk_mask
0x0410	FAULT_CLOCK_FLAGS_PCLK_MASK	0x00	RW	Bit[7:2]: Not used Bit[1]: clock_count_flag_pclk_mask Bit[0]: crc_checksum_flag_pclk_mask
0x0411	FAULT_CLOCK_FLAGS_SCLK	–	R	Bit[7:2]: Not used Bit[1]: clock_count_flag_sclk Bit[0]: crc_checksum_flag_sclk

table A-2 sensor control registers (sheet 6 of 255)

address	register name	default value	R/W	description
0x0412	FAULT_CLOCK_FLAGS_PCLK	–	R	Bit[7:2]: Not used Bit[1]: clock_count_flag_pclk Bit[0]: crc_checksum_flag_pclk
0x0413	CNT_SCLK_H	–	R	Bit[7:0]: cnt_sclk_h
0x0414	CNT_SCLK_L	–	R	Bit[7:0]: cnt_sclk_l
0x0415	CNT_PCLK_H	–	R	Bit[7:0]: cnt_pclk_h
0x0416	CNT_PCLK_L	–	R	Bit[7:0]: cnt_pclk_l
0x0417	FAULT_CLOCK_FLAGS_SCLK_LATCH	–	R	Bit[7:2]: Not used Bit[1]: clock_count_flag_sclk_latch Bit[0]: crc_checksum_flag_sclk_latch
0x0418	FAULT_CLOCK_FLAGS_PCLK_LATCH	–	R	Bit[7:2]: Not used Bit[1]: clock_count_flag_pclk_latch Bit[0]: crc_checksum_flag_pclk_latch
0x0419	FAULT_PLL_MONITOR_STATE	–	R	Bit[7:1]: Not used Bit[0]: fault_pll_monitor_state
0x0440	FAULT_PLL_FLAGS_LATCH	–	R	Bit[7:2]: Not used Bit[1]: pll2_lock_latch Bit[0]: pll1_lock_latch
0x0441	FAULT_PLL_FLAGS_MASK	0x00	RW	Bit[7:2]: Not used Bit[1]: fault_pll2_lock_mask Bit[0]: fault_pll1_lock_mask
0x0442	FAULT_PLL_LOCK_STATE	–	R	Bit[7:1]: Not used Bit[0]: fault_pll_lock_state
0x2000~0x2008	RSVD	–	–	Reserved
0x2800	XCHK_FAILINGROW_DCG_H	–	R	Bit[7:3]: Not used Bit[2:0]: First failing row-pair address[10:8], DCG readout
0x2801	XCHK_FAILINGROW_DCG_L	–	R	Bit[7:0]: First failing row-pair address[7:0], DCG readout

table A-2 sensor control registers (sheet 7 of 255)

address	register name	default value	R/W	description
0x2802	XCHK_FAULTS_INTERNAL	–	R	Bit[7]: Not used Bit[6]: xchk_addr_differs_from_addr_rp XCHK address decoded by analog core ('row-pair-ID') differs from digital row-pair address (internal error) Bit[5]: xchk_rowaddr_invalid Multiple row-pairs were selected when decoding XCHK address (internal error, sticky) Bit[4]: xchk_txs_failed Pixel array control signal integrity check failed on TX for small diode (internal error, sticky) Bit[3]: xchk_rs_failed Pixel array control signal integrity check failed on RS (internal error, sticky) Bit[2]: xchk_txl_failed Pixel array control signal integrity check failed on TX for large diode (internal error, sticky) Bit[1]: xchk_rst_failed Pixel array control signal integrity check failed on RST (internal error, sticky) Bit[0]: xchk_dfd_failed Pixel array control signal integrity check failed on DFD (internal error, sticky)

table A-2 sensor control registers (sheet 8 of 255)

address	register name	default value	R/W	description
0x2803	XCHK_CTRL_REG	0xFC	RW	Bit[7]: rowaddr_valid_chk_en Enable check on rowaddr_valid Bit[6]: txs_chk_en Enable check on TX for small diode Bit[5]: rs_chk_en Enable check on RS Bit[4]: txl_chk_en Enable check on TX for large diode Bit[3]: rst_chk_en Enable check on RST Bit[2]: dfd_chk_en Enable check on DFD Bit[1]: skip_addr_opt_dis Disable option to skip check on rows 0 to 53 Bit[0]: xchk_inv_flag Invert interpretation of long_flag_i and short_flag_i before use
0x2804	XCHK_FAILINGROW_SPD_H	–	R	Bit[7:3]: Not used Bit[2:0]: First failing row-pair address[10:8], SPD readout
0x2805	XCHK_FAILINGROW_SPD_L	–	R	Bit[7:0]: First failing row-pair address[7:0], SPD readout
0x2806	XCHK_DIFFADDR_DIG_H	–	R	Bit[7:3]: Not used Bit[2:0]: First time in a frame when dig and ana addresses differ[10:8], dig address
0x2807	XCHK_DIFFADDR_DIG_L	–	R	Bit[7:0]: First time in a frame when dig and ana addresses differ[7:0], dig address
0x2808	XCHK_DIFFADDR_ANA_H	–	R	Bit[7:3]: Not used Bit[2:0]: First time in a frame when dig and ana addresses differ[10:8], ana address
0x2809	XCHK_DIFFADDR_ANA_L	–	R	Bit[7:0]: First time in a frame when dig and ana addresses differ[7:0], ana address

table A-2 sensor control registers (sheet 9 of 255)

address	register name	default value	R/W	description
0x280A	XCHK_FAULTS_LATCHED	–	R	Bit[7:4]: Not used Bit[3]: xchk_rowaddr_invalid_latched Multiple row-pairs were selected when decoding XCHK address (latched fault flag) Bit[2]: xchk_addr_differs_from _addr_rp_latched XCHK address decoded by analog core ('row-pair-ID') differs from digital row-pair address (latched fault flag) Bit[1]: xchk_txs_failed_latched Pixel array control signal integrity check failed on TX for small diode (latched fault flag) Bit[0]: xchk_rs_txl_rst_or_dfd_ failed_latched Pixel array control signal integrity check failed on either RS,TX for large diode, RST, or DFD (latched fault flag)
0x280B	XCHK_FAULT_MASK	0x00	RW	Bit[7:4]: Not used Bit[3]: xchk_rowaddr_invalid_mask Multiple row-pairs were selected when decoding XCHK address (mask bit) Bit[2]: xchk_addr_differs_from_ addr_rp_mask XCHK address decoded by analog core ('row-pair-ID') differs from digital row-pair address (mask bit) Bit[1]: xchk_txs_failed_mask Pixel array control signal integrity check failed on TX for small diode (mask bit) Bit[0]: xchk_rs_txl_rst_or_ dfd_failed_mask Pixel array control signal integrity check failed on either RS,TX for large diode, RST, or DFD (mask bit)

table A-2 sensor control registers (sheet 10 of 255)

address	register name	default value	R/W	description
0x280C	XCHK_IGNORE_CFG	0x7B	RW	Bit[7]: Not used Bit[6]: Disable ignoring ROWADDR_VALID check for initial few frames Bit[5]: Disable ignoring DFD OK check for initial few frames Bit[4]: Disable ignoring RST OK check for initial few frames Bit[3]: Disable ignoring TX OK check for initial few frames Bit[2]: Disable ignoring RS OK check for initial few frames Bit[1:0]: xchk_ignore_init_frames Ignore initial frames each time streaming starts
0x280D	FAULT_FLAG_ST	–	R	Bit[7:1]: Not used Bit[0]: state_o status of XCHK FAULT_FLAG module
0x3000	SC_CTRL	0x00	RW	Bit[7:2]: Not used Bit[1:0]: io_pad_oen Pad IO function enable
0x3001	SC_CTRL_1	0x03	RW	Bit[7:0]: io_pad_oen Pad IO function enable
0x3002	SC_CTRL_2	0xF8	RW	Bit[7:0]: io_pad_oen Pad IO function enable
0x3003	SC_CTRL_3	0x00	RW	Bit[7:2]: Not used Bit[1:0]: io_pad_out Pad IO select value
0x3004	SC_CTRL_4	0x00	RW	Bit[7:0]: io_pad_out Pad IO select value
0x3005	SC_CTRL_5	0x00	RW	Bit[7:0]: io_pad_out Pad IO select value
0x3006	SC_CTRL_6	0x00	RW	Bit[7:2]: Not used Bit[1:0]: io_pad_sel Pad IO select
0x3007	SC_CTRL_7	0x00	RW	Bit[7:0]: io_pad_sel Pad IO select
0x3008	SC_CTRL_8	0x00	RW	Bit[7:0]: io_pad_sel Pad IO select
0x3009	SC_CTRL_9	0x06	RW	Bit[7:0]: a_pad_pk Pad control

table A-2 sensor control registers (sheet 11 of 255)

address	register name	default value	R/W	description
0x300A	SC_CTRL_A	0x58	R	Bit[7:0]: def_snr_id Sensor ID
0x300B	SC_CTRL_B	0x01	R	Bit[7:0]: def_snr_id Sensor ID
0x300C	SC_CTRL_C	0x44	R	Bit[7:0]: def_snr_id Sensor ID
0x300D	SC_CTRL_D	0x11	RW	Bit[7]: Not used Bit[6:4]: Ppump1 clock generation division factor Bit[3]: Not used Bit[2:0]: Npump1 clock generation division factor
0x300E	SC_CTRL_E	0x11	RW	Bit[7]: Not used Bit[6:4]: Ppump2 clock generation division factor Bit[3]: Not used Bit[2:0]: Npump2 clock generation division factor
0x300F	SC_CTRL_F	0x11	RW	Bit[7]: Not used Bit[6:4]: Ppump3 clock generation division factor Bit[3]: Not used Bit[2:0]: Npump3 clock generation division factor
0x3012	SC_PHY_CTRL	0x41	RW	Bit[7:4]: mipi_lane_num Number of MIPI and LVDS lanes Bit[3]: mipi_phy_rst 0: MIPI PHY reset depends on other signals 1: MIPI PHY reset always high Bit[2]: pd_mipi_phy MIPI power down Bit[1]: Not used Bit[0]: phy_mode 0: LVDS mode 1: MIPI mode
0x3013	SC_CTRL_13	0x00	RW	Bit[7:2]: Not used Bit[1:0]: io_pad_ien Pad input enable
0x3014	SC_CTRL_14	0x00	RW	Bit[7:0]: io_pad_ien Pad input enable
0x3015	SC_CTRL_15	0x08	RW	Bit[7:0]: io_pad_ien Pad input enable

table A-2 sensor control registers (sheet 12 of 255)

address	register name	default value	R/W	description
0x3016	SC_CTRL_16	0xF0	RW	Bit[7]: SCLK enable for analog control and sensor top Bit[6]: SCLK enable for strobe function Bit[5]: Not used Bit[4]: tc_clk_en SCLK enable for timing control Bit[3]: rst_ac_dis Always reset analog control and sensor top Bit[2]: rst_stb_dis Always reset strobe Bit[1]: Not used Bit[0]: rst_tc_int_dis Always reset timing control
0x3017	SC_CTRL_17	0xF0	RW	Bit[7]: sclk_tpm_en SCLK enable for TPM Bit[6]: sclk_isp_en SCLK enable for ISP Bit[5]: arb_clk_en SCLK enable for arbitration Bit[4]: sclk_vfifo_en SCLK enable for VFIFO Bit[3]: rst_tpm_dis Always reset TPM Bit[2]: rst_isp_dis Always reset ISP Bit[1]: rst_arb_dis Always reset arbitration Bit[0]: rst_vfifo_dis Always reset VFIFO
0x3018	SC_CTRL_18	0xF0	RW	Bit[7]: cpuclk_crypto_en Bit[6]: sclk_crypto_en Bit[5]: sclk_mipi_en SCLK enable for MIPI Bit[4]: sclk_efuse_en SCLK enable for eFUSE Bit[3]: Not used Bit[2]: rst_mipi_dis Always reset MIPI Bit[1]: rst_crypto_dis Bit[0]: rst_efuse_dis Always reset OTP

table A-2 sensor control registers (sheet 13 of 255)

address	register name	default value	R/W	description
0x3019	SC_CTRL_19	0xF0	RW	Bit[7]: sclk_blc_en SCLK enable for BLC Bit[6]: sclk_ispfc_en SCLK enable for ISP FC Bit[5]: sclk_fmt_en SCLK enable for test mode Bit[4]: sclk_embline_en SCLK enable for sensor frex Bit[3]: rst_blc_dis Always reset BLC Bit[2]: rst_ispfc_dis Always reset ISP FC Bit[1]: rst_fmt_dis Always reset TEST MODE Bit[0]: rst_embline_tmp_dis Always reset sensor frex
0x301A	SC_CTRL_1A	0xF0	RW	Bit[7]: grp_clk_en SCLK enable for group hold Bit[6]: Not used Bit[5]: pclk_vfifo_en PCLK enable for VFIFO Bit[4]: pclk_mipi_en PCLK enable for MIPI Bit[3]: rst_grp_dis Always reset group hold Bit[2]: rst_mipi_sc_dis Always reset MIPI Bit[1]: Not used Bit[0]: rst_embline_sw 0: Reset for sensor frex is reset for SCCB 1: Reset for sensor frex is reset
0x301B	SC_CTRL_1B	0xB4	RW	Bit[7]: daclk_sel 0: 1/2 DAC clock 1: DAC clock Bit[6]: daclk_sw Choose SCLK for DAC clock Bit[5]: sclk_bist20_en SCLK enable for MBIST Bit[4]: sclk_snr_sync_en SCLK enable for SYNC FIFO Bit[3]: sclk_grp_sw_sft_stb_dis Disable group hold clock switch Bit[2]: DAC clock enable Bit[1]: rst_bist20_dis Always reset MBIST Bit[0]: rst_snr_sync_dis Always reset SYNC FIFO

table A-2 sensor control registers (sheet 14 of 255)

address	register name	default value	R/W	description
0x301C	SC_CTRL_1C	0x01	RW	Bit[7]: rst_asil_chk_dis Always reset pixel ASIL checker Bit[6]: Not used Bit[5]: rst_snr_sync_frex_stb_dis Disable frex function on SYNC FIFO Bit[4]: rst_embline_tmp_frex_stb_dis Disable frex function on frex Bit[3]: rst_ispfc_frex_stb_dis Disable frex function on ISP FC Bit[2]: rst_blc_frex_stb_dis Disable frex function on BLC Bit[1]: Not used Bit[0]: rst_stb_frex_stb_dis Disable frex function on strobe
0x301D	SC_CTRL_1D	0x02	RW	Bit[7]: Not used Bit[6]: rst_tpm_frex_stb_dis Disable frex function on TPM Bit[5]: rst_isp_frex_stb_dis Disable frex function on ISP Bit[4]: rst_dvp_frex_stb_dis Disable frex function on LVDS Bit[3]: rst_mipi_frex_stb_dis Disable frex function on MIPI Bit[2]: rst_fmt_frex_stb_dis Disable frex function on TEST MODE Bit[1]: rst_arb_frex_stb_dis Disable frex function on ISP FC Bit[0]: mipi_phy_rst_frex_stb_dis Disable frex function on MIPI PHY
0x301E	SC_CTRL_1E	0xB0	RW	Bit[7:6]: Not used Bit[5]: Counter clock enable Bit[4]: SRAM clock enable Bit[3]: pclk_sel 0: PCLK 1: 1/2 PCLK Bit[2:1]: Not used Bit[0]: sclk2x_sel 0: SCLK 1: 1/2 SCLK

table A-2 sensor control registers (sheet 15 of 255)

address	register name	default value	R/W	description
0x301F	SC_CTRL_1F	0xE1	RW	Bit[7]: Not used Bit[6:4]: DAC clock division factor Bit[3]: rst_lvds_dis Always reset LVDS Bit[2]: rst_lvds_frex_stb_dis Disable frex function on LVDS Bit[1]: daclk_sw2 0: DAC clock is PLL DAC clock 1: DAC clock is PLL DAC clock division result Bit[0]: cen_global 0: All SRAMS are selected at same time
0x3020	SC_CTRL_20	0x01	RW	Bit[7]: Not used Bit[6]: p_pwdn_dis Disable power down pin function on MIPI PHY Bit[5]: Not used Bit[4]: stb_rst_dis Disable software standby reset Bit[3]: Not used Bit[2]: no_wait_stop Group hold clock switch and register bus switch do not wait for SCCB stop Bit[1]: sft_stb_dis Disable software standby function on MIPI PHY Bit[0]: reg_bus_sw_en Enable register bus to go to sleep
0x3021	RSVD	–	–	Reserved
0x3022	SC_CTRL_22	0xF8	RW	Bit[7]: sclk_ba22_en SCLK enable for ASRAM TST Bit[6:4]: Not used Bit[3]: rst_ba22_dis Always reset ASRAM TST Bit[2:0]: Not used
0x3023	SC_CTRL_23	0xF0	RW	Bit[7]: sclk_psv_en SCLK enable for PSV Bit[6:4]: Not used Bit[3]: rst_psv_dis Always reset PSV Bit[2:0]: Not used
0x3024	SC_CTRL_24	0xF0	RW	Bit[7]: rst_ba22_frex_stb_dis Disable frex function on ASRAM TST Bit[6:0]: Not used

table A-2 sensor control registers (sheet 16 of 255)

address	register name	default value	R/W	description
0x3025	NOT USED	0x02	RW	Bit[7:0]: Not used
0x3026	SC_CTRL_26	0x00	RW	Bit[7:0]: Power save mode various clock gate mask[15:8]
0x3027	SC_CTRL_27	0x00	RW	Bit[7:0]: Power save mode various clock gate mask[7:0]
0x3028	SC_CTRL_28	0xF0	RW	Bit[7:6]: Not used Bit[5]: sclk_dtr_en SCLK enable for dig test pattern rows Bit[4]: sclk_uid_en SCLK enable for unique ID Bit[3]: rst_dtr_dis Always reset dig test pattern rows Bit[2]: rst_uid_dis Always reset unique ID Bit[1:0]: Not used
0x3029	SC_CTRL_29	0x84	RW	Bit[7]: sclk_vm_en SCLK enable for VM Bit[6:4]: Not used Bit[3]: rst_vm_dis Always reset VM Bit[2]: rst_tpm_wait4otp Release TPM reset only after OTP BIST done Bit[1:0]: Not used
0x302A	SC_CTRL_2A	0x00	R	Bit[7:0]: def_ver_id Sensor version ID
0x302B	SC_CTRL_2B	–	R	Bit[7:0]: d_split_id
0x302C	SC_CTRL_2C	0x00	RW	Bit[7:0]: snr_unique_id User programmable unique sensor ID
0x3035	SC_CTRL_35	0x6C	RW	Bit[7:0]: SCCB ID chosen when SID pin input is low
0x3036	SC_CTRL_36	0x42	RW	Bit[7:0]: SCCB ID2
0x3037	SC_CTRL_37	0x20	RW	Bit[7:0]: sccb_id_alt SCCB ID chosen when SID pin input is high
0x3038	SC_CTRL_38	0x00	RW	Bit[7:1]: Not used Bit[0]: SCCB ID2 detected, no acknowledge is activated

table A-2 sensor control registers (sheet 17 of 255)

address	register name	default value	R/W	description
0x3039	SC_CTRL_39	0x00	RW	Bit[7:2]: Reserved Bit[1]: Bypass state STARTUP_BIST Bit[0]: after_start_up_chk_goto _stream_off Leaving state START_UP_CHK, go to state STREAM_OFF instead of SW_STBY
0x303D	SC_CTRL_3D	–	R	Bit[7:5]: Not used Bit[4:0]: IO pad
0x303E	SC_CTRL_3E	–	R	Bit[7:5]: Not used Bit[4:0]: IO pad
0x303F	SC_CTRL_3F	–	R	Bit[7:5]: Not used Bit[4:0]: IO pad
0x3100	SB_S_REG1	0x00	RW	Bit[7:4]: Not used Bit[3]: Enable SCCB data lane delay before sample next data Bit[2:0]: sda_dly Clock counts before SCCB data lane sample data
0x3101	SB_S_REG2	0x32	RW	Bit[7:5]: Not used Bit[4]: Enable SCCB address automatically increase Bit[3]: sda_byp 0: Use posedge clock edge to SDA data lane input data sync 1: Use both clock edges to SDA data lane input data sync Bit[2]: scl_byp 0: Use posedge clock edge to SCL clock data lane input data sync 1: Use both clock edges to SCL clock lane input data sync Bit[1]: Mask glitch in SCCB Bit[0]: Mask stop sign in SCCB state machine
0x3102	SB_S_REG3	0x00	RW	Bit[7:4]: sda_num number of clock cycle in SDA data lane coming-in data Bit[3:0]: scl_num number of clock cycle in SCL clock lane coming-in data

table A-2 sensor control registers (sheet 18 of 255)

address	register name	default value	R/W	description
0x3103	SB_S_REG4	0x25	RW	Bit[7:0]: sccb_sysreg System going to stream timing control
0x3104	SB_S_REG5	0x01	RW	Bit[7:6]: Not used Bit[5]: pll_pclk_sel 0: PCLK source used in digital is from PLL1 SCLK 1: PCLK source used in digital is from PLL1 PCLK Bit[4:2]: Not used Bit[1]: pll_sclk_sel 0: SCLK source used in digital is from PLL2 SCLK 1: SCLK source used in digital is from PLL1 SCLK Bit[0]: Not used
0x3105	NOT USED	0x11	RW	Bit[7:0]: Not used
0x3106	SB_S_REG7	0x10	RW	Bit[7:0]: srb_ctrl SCLK, SRAM clock and counter clock/divided clock selection
0x3107~ 0x3108	RSVD	–	–	Reserved
0x3109	SB_S_GRANT	0x00	RW	Bit[7:1]: Not used Bit[0]: Manually trigger SCCB override grant
0x3180	SCCB_CRC_H	–	R	Bit[7:0]: SCCB CRC[15:8]
0x3181	SCCB_CRC_L	–	R	Bit[7:0]: SCCB CRC[7:0]
0x3182	PEC_CONFIG	0x10	RW	Bit[7:5]: Not used Bit[4]: verify_enable Register verification enable Bit[3]: Not used Bit[2]: pec_last_adr_inc_dis Stop address increase in last one Bit[1]: pec_nak_en Send NAK if received wrong PEC CRC Bit[0]: PEC enable
0x3183	PEC_ERROR_RATE	0xFF	RW	Bit[7:0]: PEC error rate
0x3184	PEC_ERROR_ THRESHOLD	0xFF	RW	Bit[7:0]: Error threshold for PEC function
0x3185	PEC_ERROR_CNT	–	R	Bit[7:0]: Counter of PEC errors

table A-2 sensor control registers (sheet 19 of 255)

address	register name	default value	R/W	description
0x3186	PEC_STATUS	–	R	Bit[7:3]: Not used Bit[2]: sccb_buffer_fault Buffer of SCCB is corrupted Bit[1]: sccb_verif_fault Error in register verification Bit[0]: sccb_cmd_fault Error in SCCB PEC command
0x3187	SCCB_BLOCKED_ THRESHOLD	0xFF	RW	Bit[7:0]: Threshold to SCCB blocked
0x3188	SCCB_BLOCKED_CNT	–	R	Bit[7:0]: Counter to SCCB blocked
0x3189	SCCB_FAULT_MASKED	0x00	RW	Bit[7:3]: Not used Bit[2]: sccb_buffer_fault_masked Mask SCCB buffer fault Bit[1]: sccb_verif_fault_masked Mask verification fault Bit[0]: sccb_cmd_fault_masked Mask PEC command fault
0x318A	SCCB_FAULT_STATE	–	R	Bit[7:1]: Not used Bit[0]: SCCB fault state
0x318B	SCCB_FAULT_ERROR	–	R	Bit[7:3]: Not used Bit[2]: SCCB buffer error Bit[1]: SCCB verification error Bit[0]: sccb_cmd_err PEC command error
0x318F	PEC_CRC_STATUS	–	R	Bit[7:1]: Not used Bit[0]: pec_crc_err PEC CRC check result
0x3190	MASK_ADR_1_H	0x00	RW	Bit[7:0]: Verify masked address 1H
0x3191	MASK_ADR_1_L	0x00	RW	Bit[7:0]: Verify masked address 1L
0x3192	MASK_DAT_1	0x00	RW	Bit[7:0]: vmask_dat_1 Verify masked value 1
0x3193	MASK_ADR_2_H	0x00	RW	Bit[7:0]: Verify masked address 2H
0x3194	MASK_ADR_2_L	0x00	RW	Bit[7:0]: Verify masked address 2L
0x3195	MASK_DAT_2	0x00	RW	Bit[7:0]: vmask_dat_2 Verify masked value 2
0x3196	MASK_ADR_3_H	0x00	RW	Bit[7:0]: Verify masked address 3H
0x3197	MASK_ADR_3_L	0x00	RW	Bit[7:0]: Verify masked address 3L
0x3198	MASK_DAT_3	0x00	RW	Bit[7:0]: vmask_dat_3 Verify masked value 3

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address	register name	default value	R/W	description
0x3199	MASK_ADR_4_H	0x00	RW	Bit[7:0]: Verify masked address 4H
0x319A	MASK_ADR_4_L	0x00	RW	Bit[7:0]: Verify masked address 4L
0x319B	MASK_DAT_4	0x00	RW	Bit[7:0]: vmask_dat_4 Verify masked value 4
0x319C	BMASK_ADR_1_H	0x00	RW	Bit[7:0]: Blocked masked address 1H
0x319D	BMASK_ADR_1_L	0x00	RW	Bit[7:0]: Blocked masked address 1L
0x319E	BMASK_BIT_1	0x00	RW	Bit[7:0]: Masked address bit
0x319F	BMASK_ADR_2_H	0x00	RW	Bit[7:0]: Blocked masked address 2H
0x31A0	BMASK_ADR_2_L	0x00	RW	Bit[7:0]: Blocked masked address 2L
0x31A1	BMASK_BIT_2	0x00	RW	Bit[7:0]: Masked address bit
0x31A2	BMASK_ADR_3_H	0x00	RW	Bit[7:0]: Blocked masked address 3H
0x31A3	BMASK_ADR_3_L	0x00	RW	Bit[7:0]: Blocked masked address 3L
0x31A4	BMASK_BIT_3	0x00	RW	Bit[7:0]: Masked address bit
0x31A5	BMASK_ADR_4_H	0x00	RW	Bit[7:0]: Blocked masked address 4h
0x31A6	BMASK_ADR_4_L	0x00	RW	Bit[7:0]: Blocked masked address 4L
0x31A7	BMASK_BIT_4	0x00	RW	Bit[7:0]: Masked address bit
0x3200	GRP_HOLD_CTRL_0	0x00	RW	Bit[7:0]: Ba0 Group 0 base address
0x3201	GRP_HOLD_CTRL_1	0x08	RW	Bit[7:0]: Ba1 Group 1 base address
0x3202	GRP_HOLD_CTRL_2	0x10	RW	Bit[7:0]: Ba2 Group 2 base address
0x3203	GRP_HOLD_CTRL_3	0x18	RW	Bit[7:0]: Ba3 Group 3 base address
0x3204	GRP_HOLD_CTRL_4	0x20	RW	Bit[7:0]: Ba4 Group 4 base address
0x3205	GRP_HOLD_CTRL_5	0x30	RW	Bit[7:0]: Ba5 Group 5 base address

table A-2 sensor control registers (sheet 21 of 255)

address	register name	default value	R/W	description
0x3208	GRP_HOLD_8	–	W	Bit[7:4]: group_ctrl 0000:Group hold start 0001:Group hold end 0110:H-blank group launch 1010:V-blank group launch 1110:Immediate group launch Others:Reserved Bit[3:0]: group_id 0000:Group bank 0 0001:Group bank 1 0010:Group bank 2 0011:Group bank 3 Others:Reserved
0x320A	GRP_HOLD_CTRL_A	0x00	RW	Bit[7:0]: grp0_frms Number of frames staying in group0
0x320B	GRP_HOLD_CTRL_B	0x00	RW	Bit[7:0]: grp1_frms Number of frames staying in group1
0x320C	GRP_HOLD_CTRL_C	0x00	RW	Bit[7:0]: grp2_frms Number of frames staying in group2
0x320D	GRP_HOLD_CTRL_D	0x00	RW	Bit[7:0]: grp3_frms Number of frames staying in group3
0x320E~ 0x320F	RSVD	–	–	Reserved
0x3210	GRP_HOLD_CTRL_10	0x00	RW	Bit[7]: grp_wr_sel_eco eco_sl0b, select trigger source 0: Timing ctrl 1: ISP Bit[6]: Not used Bit[5]: first_frame_context_en Bit[4]: FSIN enable in context switch Bit[3:2]: Not used Bit[1:0]: FSIN group number

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address	register name	default value	R/W	description
0x3211	GRP_HOLD_CTRL_11	0x61	RW	Bit[7]: Reserved Bit[6]: grf_vrf_en Enable read-back checking Bit[5]: Repeat context switch enable Bit[4]: Context switch enable Bit[3:2]: Not used Bit[1:0]: sw_back_grp_reg When in context switch mode, but not repeat switch, switch back group number
0x3212	GRP_HOLD_CTRL_12	0x00	RW	Bit[7:0]: Reserved
0x3213	GRP_HOLD_CTRL_13	0x02	RW	Bit[7:4]: Not used Bit[3:0]: emb_line_num Number of embedded lines
0x3214	GRP_HOLD_CTRL_14	0x00	RW	Bit[7:0]: Padding data
0x3215	GRP_HOLD_CTRL_15	0xCD	RW	Bit[7:6]: hblk_ctrl Next embedded line start options Bit[5]: padding_md2 Bit[4]: frame_cnt_trig Bit[3]: emline_eof_en Bit[2]: emline_sof_en Bit[1]: Send address in emb rows Bit[0]: tag_en Send tag in emb rows
0x3216	GRP_HOLD_CTRL_16	0xDA	RW	Bit[7:0]: Tag data
0x3217	GRP_HOLD_CTRL_17	0x09	RW	Bit[7:0]: emb_width_offset
0x3218	GRP_HOLD_CTRL_18	0x06	RW	Bit[7:6]: Reserved Bit[5]: front_emb_size_man Manual front embedded row size Bit[4]: end_emb_size_man Manual end embedded row size Bit[3]: Not used Bit[2]: mem_crc_en Output CRC of configuration for each embedded Bit[1]: emb_crc_en Bit[0]: emb_crc_dat_inv

table A-2 sensor control registers (sheet 23 of 255)

address	register name	default value	R/W	description
0x3219	MEM_CRC_FAULT_ MASKED	0x0E	RW	Bit[7:4]: Not used Bit[3]: wd_fault_inject_mask Mask manual fault injection to watchdog Bit[2]: grp_verif_fault_mask Mask read-back check fault for group 0~3 Bit[1]: grp_mem_crc_fault_mask Mask memory CRC fault for group 0~3 Bit[0]: emb_mem_crc_fault_mask Mask memory CRC fault for embedded rows
0x321A	GRP_HOLD_SRAM_T0	0x06	RW	Bit[7:6]: Not used Bit[5:0]: SRAM test control signals
0x321B	GRP_HOLD_SRAM_T1	0x06	RW	Bit[7:0]: SRAM test control signals
0x321C	EMB_SRAM_T0	0x06	RW	Bit[7:6]: Not used Bit[5:0]: emb_sram_tstctrl SRAM test control signals for embedded FIFO
0x321D	EMB_SRAM_T1	0x06	RW	Bit[7:0]: emb_sram_tstctrl SRAM test control signals for embedded FIFO
0x321E	GRP_HOLD_STATUS	–	R	Bit[7:6]: Not used Bit[5:0]: crc_status Result of CRC check for SRAM
0x321F	MEM_CRC_FAULT_ STATUS	–	R	Bit[7]: Memory fault state Bit[6:4]: Not used Bit[3]: wd_fault_inject_status Manually injected fault to watchdog Bit[2]: grp_verif_fault Read-back check fault of group 0~3 Bit[1]: grp_mem_crc_fault Memory check fault of group 0~3 Bit[0]: emb_mem_crc_fault Memory check fault of embedded rows
0x3220	GRP_HOLD_LEN_0	–	R	Bit[7:0]: len0_rd Group 0 length
0x3221	GRP_HOLD_LEN_1	–	R	Bit[7:0]: len1_rd Group 1 length

table A-2 sensor control registers (sheet 24 of 255)

address	register name	default value	R/W	description
0x3222	GRP_HOLD_LEN_2	–	R	Bit[7:0]: len2_rd Group 2 length
0x3223	GRP_HOLD_LEN_3	–	R	Bit[7:0]: len3_rd Group 3 length
0x3224	GRP_HOLD_LEN_4	–	R	Bit[7:0]: len4_rd Group 4 length
0x3225	GRP_HOLD_LEN_5	–	R	Bit[7:0]: len5_rd Group 5 length
0x3226	GRP_HOLD_CTRL_26	–	R	Bit[7:0]: Frame counter group 0
0x3227	GRP_HOLD_CTRL_27	–	R	Bit[7:0]: Frame counter group 1
0x3228	GRP_HOLD_CTRL_28	–	R	Bit[7:0]: Frame counter group 2
0x3229	GRP_HOLD_CTRL_29	–	R	Bit[7:0]: Frame counter group 3
0x322A~ 0x322C	RSVD	–	–	Reserved
0x322D	GRP_HOLD_CTRL_2D	–	R	Bit[7:0]: grp_sel_real Selected group
0x322E	GRP_HOLD_ERR_STATUS	–	R	Bit[7:3]: Not used Bit[2]: grp_verif_err Read-back check result of group 0~3 Bit[1]: grp_mem_crc_err Memory check result of group 0~3 Bit[0]: emb_mem_crc_err Memory check result of embedded rows
0x322F	WD_INJECT_FAULT	0x00	RW	Bit[7:1]: Not used Bit[0]: Inject fault to watchdog manually
0x3230	FRONT_EMB_SIZE_H	–	R	Bit[7:0]: Size of front embedded rows[15:8]
0x3231	FRONT_EMB_SIZE_L	–	R	Bit[7:0]: Size of front embedded rows[7:0]
0x3232	END_EMB_SIZE_H	–	R	Bit[7:0]: Size of end embedded rows[15:8]
0x3233	END_EMB_SIZE_L	–	R	Bit[7:0]: Size of end embedded rows[7:0]
0x3234	GRP_CRC_0_3	–	R	Bit[7:0]: Group 0 mem CRC, byte 3
0x3235	GRP_CRC_0_2	–	R	Bit[7:0]: Group 0 mem CRC, byte 2
0x3236	GRP_CRC_0_1	–	R	Bit[7:0]: Group 0 mem CRC, byte 1
0x3237	GRP_CRC_0_0	–	R	Bit[7:0]: Group 0 mem CRC, byte 0
0x3238	GRP_CRC_1_3	–	R	Bit[7:0]: Group 1 mem CRC, byte 3

table A-2 sensor control registers (sheet 25 of 255)

address	register name	default value	R/W	description
0x3239	GRP_CRC_1_2	–	R	Bit[7:0]: Group 1 mem CRC, byte 2
0x323A	GRP_CRC_1_1	–	R	Bit[7:0]: Group 1 mem CRC, byte 1
0x323B	GRP_CRC_1_0	–	R	Bit[7:0]: Group 1 mem CRC, byte 0
0x323C	GRP_CRC_2_3	–	R	Bit[7:0]: Group 2 mem CRC, byte 3
0x323D	GRP_CRC_2_2	–	R	Bit[7:0]: Group 2 mem CRC, byte 2
0x323E	GRP_CRC_2_1	–	R	Bit[7:0]: Group 2 mem CRC, byte 1
0x323F	GRP_CRC_2_0	–	R	Bit[7:0]: Group 2 mem CRC, byte 0
0x3240	GRP_CRC_3_3	–	R	Bit[7:0]: Group 3 mem CRC, byte 3
0x3241	GRP_CRC_3_2	–	R	Bit[7:0]: Group 3 mem CRC, byte 2
0x3242	GRP_CRC_3_1	–	R	Bit[7:0]: Group 3 mem CRC, byte 1
0x3243	GRP_CRC_3_0	–	R	Bit[7:0]: Group 3 mem CRC, byte 0
0x3244	GRP_CRC_4_3	–	R	Bit[7:0]: Group 4 mem CRC, byte 3
0x3245	GRP_CRC_4_2	–	R	Bit[7:0]: Group 4 mem CRC, byte 2
0x3246	GRP_CRC_4_1	–	R	Bit[7:0]: Group 4 mem CRC, byte 1
0x3247	GRP_CRC_4_0	–	R	Bit[7:0]: Group 4 mem CRC, byte 0
0x3248	GRP_CRC_5_3	–	R	Bit[7:0]: Group 5 mem CRC, byte 3
0x3249	GRP_CRC_5_2	–	R	Bit[7:0]: Group 5 mem CRC, byte 2
0x324A	GRP_CRC_5_1	–	R	Bit[7:0]: Group 5 mem CRC, byte 1
0x324B	GRP_CRC_5_0	–	R	Bit[7:0]: Group 5 mem CRC, byte 0
0x324C	FRONT_MAN_SIZE_H	0x00	RW	Bit[7:0]: Front emb manual size[15:8]
0x324D	FRONT_MAN_SIZE_L	0x00	RW	Bit[7:0]: Front emb manual size[7:0]
0x324E	END_MAN_SIZE_H	0x00	RW	Bit[7:0]: End emb manual size[15:8]
0x324F	END_MAN_SIZE_L	0x00	RW	Bit[7:0]: End emb manual size[7:0]
0x3301~ 0x3318	RSVD	–	–	Reserved
0x3400	PSV_CTRL_1	0x08	RW	Bit[7:4]: Not used Bit[3]: psv_auto_dis Disable PSV auto on function Bit[2]: PSV mode enable Bit[1:0]: Not used

table A-2 sensor control registers (sheet 26 of 255)

address	register name	default value	R/W	description
0x3401	PSV_CTRL_2	0x00	RW	Bit[7:5]: Not used Bit[4]: stream_clk_allon Do not stop clock toggling during PSV mode Bit[3:0]: Not used
0x3406	PSV_CTRL_7	0x08	RW	Bit[7:0]: stream_st_offs Equivalent number of pad clock in image output state, compared to VTS
0x3407	PSV_CTRL_8	0x08	RW	Bit[7:0]: pchg_st_offs Equivalent number of pad clock in precharge state, compared to HTS
0x3408	PSV_CTRL_9	0x01	RW	Bit[7:4]: Not used Bit[3:0]: clk_winp_offs Equivalent number of pad clock when SCLK is ready in precharge state, compared to hts
0x3409	PSV_CTRL_10	0x02	RW	Bit[7:4]: Not used Bit[3:0]: strm_rear_offs Equivalent number of pad clock after core sensor goes down and before end row of image output
0x340A	PSV_CTRL_11	0x02	RW	Bit[7:4]: Not used Bit[3:0]: pchg_rear_offs Equivalent number of pad clock after going in vertical blanking and before end row to be precharged in one frame
0x340C	PSV_CTRL_12	0x10	RW	Bit[7:0]: psv_auto_on_thresh VTS row counter threshold high byte
0x340D	PSV_CTRL_13	0x00	RW	Bit[7:0]: psv_auto_on_thresh VTS row counter threshold low byte
0x340E	PSV_CTRL_14	0x30	RW	Bit[7:0]: vblank_thresh Do not stop clock toggling during PSV mode

table A-2 sensor control registers (sheet 27 of 255)

address	register name	default value	R/W	description
0x3416	PSV_CTRL_16	0x00	RW	Bit[7:3]: Not used Bit[2]: strm_off_no_retime Do not stop clock toggling during PSV mode Bit[1]: strm_on_no_retime Do not stop clock toggling during PSV mode Bit[0]: slv_snr_strm_off Do not stop clock toggling during PSV mode
0x3417	PSV_CTRL_17	0x08	RW	Bit[7:0]: strm_chg_point_l Do not stop clock toggling during PSV mode
0x3420	PSV_CTRL_21	0x00	RW	Bit[7:0]: mipi_pll_pd_sel Select reset signal for MIPI, PLL1 and PLL2 in power save mode
0x3421	PSV_CTRL_22	0x00	RW	Bit[7:0]: Array blocks power down control in power save mode
0x3422	PSV_CTRL_23	0x00	RW	Bit[7:0]: Array blocks power down control in power save mode
0x3423	PSV_CTRL_24	0x00	RW	Bit[7:0]: Array blocks power down control in power save mode
0x3424	PSV_CTRL_25	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Array blocks power down control in power save mode
0x3425	PSV_CTRL_26	0x00	RW	Bit[7:0]: asp_pd_sel Selection of array blocks power down in power save mode
0x3426	PSV_CTRL_27	0x00	RW	Bit[7:0]: asp_pd_sel Selection of array blocks power down in power save mode
0x3427	PSV_CTRL_28	0x00	RW	Bit[7:0]: asp_pd_sel Selection of array blocks power down in power save mode
0x3428	PSV_CTRL_29	0x00	RW	Bit[7:0]: asp_pd_sel Selection of array blocks power down in power save mode
0x3429	PSV_CTRL_30	0x00	RW	Bit[7:0]: asp_pd_sel Selection of array blocks power down in power save mode

table A-2 sensor control registers (sheet 28 of 255)

address	register name	default value	R/W	description
0x342A	PSV_CTRL_31	0x00	RW	Bit[7:0]: asp_pd_sel Selection of array blocks power down in power save mode
0x342B	PSV_CTRL_32	0x00	RW	Bit[7:0]: asp_pd_sel Selection of array blocks power down in power save mode
0x342C	PSV_CTRL_33	0x00	RW	Bit[7:0]: asp_pd_hblank Output selection array during horizontal blanking
0x342D	PSV_CTRL_34	0x00	RW	Bit[7:0]: asp_pd_hblank Output selection array during horizontal blanking
0x342E	PSV_CTRL_35	0x00	RW	Bit[7:0]: asp_pd_hblank Output selection array during horizontal blanking
0x342F	PSV_CTRL_36	0x00	RW	Bit[7:4]: Not used Bit[3:0]: asp_pd_hblank Output selection array during horizontal blanking
0x3501	AEC_HCG_CTRL_01	0x00	RW	Bit[7:0]: expo_coarse[15:8] Exposure in unit of rows, high byte
0x3502	AEC_HCG_CTRL_02	0x08	RW	Bit[7:0]: expo_coarse[7:0] Exposure in unit of rows, low byte
0x3503	AEC_HCG_CTRL_03	0xA8	RW	Bit[7]: Not used Bit[6]: Digital delay one frame Bit[5]: Format change update enable Bit[4]: Real analog gain delay one frame Bit[3]: Not used Bit[2]: Fine exposure delay one frame Bit[1]: Coarse exposure delay one frame Bit[0]: Gain change control for BLC
0x3504	AEC_HCG_CTRL_04	0x08	RW	Bit[7]: Calculate sensor gain from real gain Bit[6]: Determine gain used in ISP Bit[5]: Choose place to apply digital gain in BLC or ISP IP Bit[4]: Gain delay by exposure change Bit[3]: Enable initial update Bit[2:0]: Not used
0x3505	AEC_HCG_CTRL_05	–	R	Bit[7:1]: Not used Bit[0]: Manual update enable

table A-2 sensor control registers (sheet 29 of 255)

address	register name	default value	R/W	description
0x3506	AEC_HCG_CTRL_06	0x20	RW	Bit[7:0]: expo_fine[15:8] Fine exposure high byte
0x3507	AEC_HCG_CTRL_07	0x00	RW	Bit[7:0]: expo_fine[7:0] Fine exposure low byte
0x3508	AEC_HCG_CTRL_08	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Real gain, integer part
0x3509	AEC_HCG_CTRL_09	0x00	RW	Bit[7:4]: Real gain, fractional part Bit[3:0]: Not used
0x350A	AEC_HCG_CTRL_0A	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Digital gain[19:16]
0x350B	AEC_HCG_CTRL_0B	0x00	RW	Bit[7:0]: Digital gain[15:8]
0x350C	AEC_HCG_CTRL_OC	0x00	RW	Bit[7:6]: Digital gain[7:6] Bit[5:0]: Not used
0x350D	AEC_HCG_CTRL_0D	0x00	RW	Bit[7:0]: Sensor gain map
0x350E	AEC_HCG_CTRL_0E	–	R	Bit[7:0]: expo_coarse_cur[15:8] Current coarse exposure high byte
0x350F	AEC_HCG_CTRL_0F	–	R	Bit[7:0]: expo_coarse_cur[7:0] Current coarse exposure low byte
0x3510	AEC_HCG_CTRL_10	–	R	Bit[7:0]: expo_fine_cur[15:8] Current fine exposure high byte
0x3511	AEC_HCG_CTRL_11	–	R	Bit[7:0]: expo_fine_cur[7:0] Current fine exposure low byte
0x3512	AEC_HCG_CTRL_12	–	R	Bit[7:5]: Not used Bit[4:0]: real_gain_cur_real[12:8] Current real gain for BLC high 5 bits
0x3513	AEC_HCG_CTRL_13	–	R	Bit[7:1]: real_gain_cur_real[7:1] Current real gain for BLC low 7 bits Bit[0]: Not used
0x3514	AEC_HCG_CTRL_14	–	R	Bit[7:5]: Not used Bit[4:0]: gain_cur_org[12:8] Not converted current real gain high 5 bits
0x3515	AEC_HCG_CTRL_15	–	R	Bit[7:1]: gain_cur_org[7:1] Not converted current real gain low 7 bits Bit[0]: Not used

table A-2 sensor control registers (sheet 30 of 255)

address	register name	default value	R/W	description
0x3516	AEC_HCG_CTRL_16	–	R	Bit[7:4]: Not used Bit[3:0]: snr_gain_coarse_cur Current sensor coarse gain
0x3517	AEC_HCG_CTRL_17	–	R	Bit[7:1]: snr_gain_fine_cur Current sensor fine gain Bit[0]: Not used
0x3518	AEC_HCG_CTRL_18	–	R	Bit[7:4]: Not used Bit[3:0]: Digital gain for BLC[19:16]
0x3519	AEC_HCG_CTRL_19	–	R	Bit[7:0]: Digital gain for BLC[15:8]
0x351A	AEC_HCG_CTRL_1A	–	R	Bit[7:6]: Digital gain for BLC[7:6] Bit[5:0]: Not used
0x351B	AEC_HCG_CTRL_1B	–	R	Bit[7:4]: Not used Bit[3:0]: dig_gain_mwb[19:16] Digital gain for ISP high 4 bits
0x351C	AEC_HCG_CTRL_1C	–	R	Bit[7:0]: dig_gain_mwb[15:8] Digital gain for ISP medium byte
0x351D	AEC_HCG_CTRL_1D	–	R	Bit[7:6]: dig_gain_mwb[7:6] Digital gain for ISP low 2 bits Bit[5:0]: Not used
0x351E	AEC_HCG_CTRL_1E	–	R	Bit[7:5]: Not used Bit[4:0]: Real gain for BLC[12:8]
0x351F	AEC_HCG_CTRL_1F	–	R	Bit[7:4]: Real gain for BLC[7:4] Bit[3:0]: Not used
0x3520	AEC_HCG_CTRL_20	–	R	Bit[7:0]: Real gain for ISP[17:10], format 8.10
0x3521	AEC_HCG_CTRL_21	–	R	Bit[7:0]: Real gain for ISP[9:2]
0x3522	AEC_HCG_CTRL_22	–	R	Bit[7:6]: Real gain for ISP[1:0] Bit[5:0]: Not used
0x3541	AEC_SPD_CTRL_01	0x00	RW	Bit[7:0]: expo_coarse[15:8] Exposure in unit of rows, high byte
0x3542	AEC_SPD_CTRL_02	0x04	RW	Bit[7:0]: expo_coarse[7:0] Exposure in unit of rows, Low byte
0x3543	AEC_SPD_CTRL_03	0xA8	RW	Bit[7]: Not used Bit[6]: Digital delay one frame Bit[5]: Format change update enable Bit[4]: Real analog gain delay one frame Bit[3]: Not used Bit[2]: Fine exposure delay one frame Bit[1]: Coarse exposure delay one frame Bit[0]: Gain change control for BLC

table A-2 sensor control registers (sheet 31 of 255)

address	register name	default value	R/W	description
0x3544	AEC_SPD_CTRL_04	0x08	RW	Bit[7]: Calculate sensor gain from real gain Bit[6]: Determine gain used in ISP Bit[5]: Choose place to apply digital gain in BLC or ISP IP Bit[4]: Gain delay by exposure change Bit[3]: Enable initial update Bit[2:0]: Not used
0x3545	AEC_SPD_CTRL_05	–	R	Bit[7:1]: Not used Bit[0]: Manual update enable
0x3546	AEC_SPD_CTRL_06	0x20	RW	Bit[7:0]: expo_fine[15:8] Fine exposure high byte
0x3547	AEC_SPD_CTRL_07	0x00	RW	Bit[7:0]: expo_fine[7:0] Fine exposure low byte
0x3548	AEC_SPD_CTRL_08	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Real gain, integer part
0x3549	AEC_SPD_CTRL_09	0x00	RW	Bit[7:4]: Real gain, fractional part Bit[3:0]: Not used
0x354A	AEC_SPD_CTRL_0A	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Digital gain[19:16]
0x354B	AEC_SPD_CTRL_0B	0x00	RW	Bit[7:0]: Digital gain[15:8]
0x354C	AEC_SPD_CTRL_OC	0x00	RW	Bit[7:6]: Digital gain[7:6] Bit[5:0]: Not used
0x354D	AEC_SPD_CTRL_0D	0x00	RW	Bit[7:0]: Sensor gain map
0x354E	AEC_SPD_CTRL_0E	–	R	Bit[7:0]: expo_coarse_cur[15:8] Current coarse exposure high byte
0x354F	AEC_SPD_CTRL_0F	–	R	Bit[7:0]: expo_coarse_cur[7:0] Current coarse exposure low byte
0x3550	AEC_SPD_CTRL_10	–	R	Bit[7:0]: expo_fine_cur[15:8] Current fine exposure high byte
0x3551	AEC_SPD_CTRL_11	–	R	Bit[7:0]: expo_fine_cur[7:0] Current fine exposure low byte
0x3552	AEC_SPD_CTRL_12	–	R	Bit[7:5]: Not used Bit[4:0]: real_gain_cur_real[12:8] Current real gain for BLC high 5 bits
0x3553	AEC_SPD_CTRL_13	–	R	Bit[7:1]: real_gain_cur_real[7:1] Current real gain for BLC low 7 bits Bit[0]: Not used

table A-2 sensor control registers (sheet 32 of 255)

address	register name	default value	R/W	description
0x3554	AEC_SPD_CTRL_14	–	R	Bit[7:5]: Not used Bit[4:0]: gain_cur_org[12:8] Not converted current real gain high 4 bit
0x3555	AEC_SPD_CTRL_15	–	R	Bit[7:1]: gain_cur_org[7:1] Not converted current real gain low 7 bit Bit[0]: Not used
0x3556	AEC_SPD_CTRL_16	–	R	Bit[7:4]: Not used Bit[3:0]: snr_gain_coarse_cur Current sensor coarse gain
0x3557	AEC_SPD_CTRL_17	–	R	Bit[7:1]: snr_gain_fine_cur Current sensor fine gain Bit[0]: Not used
0x3558	AEC_SPD_CTRL_18	–	R	Bit[7:4]: Not used Bit[3:0]: Digital gain for BLC[19:16]
0x3559	AEC_SPD_CTRL_19	–	R	Bit[7:0]: Digital gain for BLC[15:8]
0x355A	AEC_SPD_CTRL_1A	–	R	Bit[7:6]: Digital gain for BLC[7:6] Bit[5:0]: Not used
0x355B	AEC_SPD_CTRL_1B	–	R	Bit[7:4]: Not used Bit[3:0]: dig_gain_mwb[19:16] Digital gain for ISP high 4 bit
0x355C	AEC_SPD_CTRL_1C	–	R	Bit[7:0]: dig_gain_mwb[15:8] Digital gain for ISP medium byte
0x355D	AEC_SPD_CTRL_1D	–	R	Bit[7:6]: dig_gain_mwb[7:6] Digital gain for ISP low 2 bit Bit[5:0]: Not used
0x355E	AEC_SPD_CTRL_1E	–	R	Bit[7:5]: Not used Bit[4:0]: Real gain for BLC[12:8]
0x355F	AEC_SPD_CTRL_1F	–	R	Bit[7:4]: Real gain for BLC[7:4] Bit[3:0]: Not used
0x3560	AEC_SPD_CTRL_20	–	R	Bit[7:0]: Real gain for ISP[17:10], format 8.10
0x3561	AEC_SPD_CTRL_21	–	R	Bit[7:0]: Real gain for ISP[9:2]
0x3562	AEC_SPD_CTRL_22	–	R	Bit[7:6]: Real gain for ISP[1:0] Bit[5:0]: Not used
0x3581	AEC_LCG_CTRL_01	0x00	RW	Bit[7:0]: expo_coarse[15:8] Exposure in unit of rows, high byte

table A-2 sensor control registers (sheet 33 of 255)

address	register name	default value	R/W	description
0x3582	AEC_LCG_CTRL_02	0x40	RW	Bit[7:0]: expo_coarse[7:0] Exposure in unit of rows, low byte
0x3583	AEC_LCG_CTRL_03	0xA8	RW	Bit[7]: Not used Bit[6]: Digital delay one frame Bit[5]: Format change update enable Bit[4]: Real analog gain delay one frame Bit[3]: Not used Bit[2]: Fine exposure delay one frame Bit[1]: Coarse exposure delay one frame Bit[0]: Gain change control for BLC
0x3584	AEC_LCG_CTRL_04	0x08	RW	Bit[7]: Calculate sensor gain from real gain Bit[6]: Determine gain used in ISP Bit[5]: Choose place to apply digital gain in BLC or ISP IP Bit[4]: Gain delay by exposure change Bit[3]: Enable initial update Bit[2:0]: Not used
0x3585	AEC_LCG_CTRL_05	–	R	Bit[7:1]: Not used Bit[0]: Manual update enable
0x3586	AEC_LCG_CTRL_06	0x40	RW	Bit[7:0]: expo_fine[15:8] Fine exposure high byte
0x3587	AEC_LCG_CTRL_07	0x00	RW	Bit[7:0]: expo_fine[7:0] Fine exposure low byte
0x3588	AEC_LCG_CTRL_08	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: Real gain, integer part
0x3589	AEC_LCG_CTRL_09	0x00	RW	Bit[7:4]: Real gain, fractional part Bit[3:0]: Not used
0x358A	AEC_LCG_CTRL_0A	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Digital gain[19:16]
0x358B	AEC_LCG_CTRL_0B	0x00	RW	Bit[7:0]: Digital gain[15:8]
0x358C	AEC_LCG_CTRL_OC	0x00	RW	Bit[7:6]: Digital gain[7:6] Bit[5:0]: Not used
0x358D	AEC_LCG_CTRL_0D	0x00	RW	Bit[7:0]: Sensor gain map
0x358E	AEC_LCG_CTRL_0E	–	R	Bit[7:0]: expo_coarse_cur[15:8] Current coarse exposure high byte
0x358F	AEC_LCG_CTRL_0F	–	R	Bit[7:0]: expo_coarse_cur[7:0] Current coarse exposure low byte
0x3590	AEC_LCG_CTRL_10	–	R	Bit[7:0]: expo_fine_cur[15:8] Current fine exposure high byte

table A-2 sensor control registers (sheet 34 of 255)

address	register name	default value	R/W	description
0x3591	AEC_LCG_CTRL_11	–	R	Bit[7:0]: expo_fine_cur[7:0] Current fine exposure low byte
0x3592	AEC_LCG_CTRL_12	–	R	Bit[7:5]: Not used Bit[4:0]: real_gain_cur_real[12:8] Current real gain for BLC high 5 bit
0x3593	AEC_LCG_CTRL_13	–	R	Bit[7:1]: real_gain_cur_real[7:1] Current real gain for BLC low 7 bit Bit[0]: Not used
0x3594	AEC_LCG_CTRL_14	–	R	Bit[7:5]: Not used Bit[4:0]: gain_cur_org[12:8] Not converted current real gain high 5 bit
0x3595	AEC_LCG_CTRL_15	–	R	Bit[7:1]: gain_cur_org[7:1] Not converted current real gain low 7 bit Bit[0]: Not used
0x3596	AEC_LCG_CTRL_16	–	R	Bit[7:4]: Not used Bit[3:0]: snr_gain_coarse_cur Current sensor coarse gain
0x3597	AEC_LCG_CTRL_17	–	R	Bit[7:1]: snr_gain_fine_cur Current sensor fine gain Bit[0]: Not used
0x3598	AEC_LCG_CTRL_18	–	R	Bit[7:4]: Not used Bit[3:0]: Digital gain for BLC[19:16]
0x3599	AEC_LCG_CTRL_19	–	R	Bit[7:0]: Digital gain for BLC[15:8]
0x359A	AEC_LCG_CTRL_1A	–	R	Bit[7:6]: Digital gain for BLC[7:6] Bit[5:0]: Not used
0x359B	AEC_LCG_CTRL_1B	–	R	Bit[7:4]: Not used Bit[3:0]: dig_gain_mwb[19:16] Digital gain for ISP high 4 bit
0x359C	AEC_LCG_CTRL_1C	–	R	Bit[7:0]: dig_gain_mwb[15:8] Digital gain for ISP medium byte
0x359D	AEC_LCG_CTRL_1D	–	R	Bit[7:6]: dig_gain_mwb[7:6] Digital gain for ISP low 2 bit Bit[5:0]: Not used
0x359E	AEC_LCG_CTRL_1E	–	R	Bit[7:5]: Not used Bit[4:0]: Real gain for BLC[12:8]
0x359F	AEC_LCG_CTRL_1F	–	R	Bit[7:4]: Real gain for BLC[7:4] Bit[3:0]: Not used

table A-2 sensor control registers (sheet 35 of 255)

address	register name	default value	R/W	description
0x35A0	AEC_LCG_CTRL_20	–	R	Bit[7:0]: Real gain for ISP[17:10], format 8.10
0x35A1	AEC_LCG_CTRL_21	–	R	Bit[7:0]: Real gain for ISP[9:2]
0x35A2	AEC_LCG_CTRL_22	–	R	Bit[7:6]: Real gain for ISP[1:0] Bit[5:0]: Not used
0x35C1	AEC_VS_CTRL_01	0x00	RW	Bit[7:0]: expo_coarse[15:8] Exposure in unit of rows, high byte
0x35C2	AEC_VS_CTRL_02	0x02	RW	Bit[7:0]: expo_coarse[7:0] Exposure in unit of rows, Low byte
0x35C3	AEC_VS_CTRL_03	0xA8	RW	Bit[7]: Not used Bit[6]: Digital delay one frame Bit[5]: Format change update enable Bit[4]: Real analog gain delay one frame Bit[3]: Not used Bit[2]: Fine exposure delay one frame Bit[1]: Coarse exposure delay one frame Bit[0]: Gain change control for BLC
0x35C4	AEC_VS_CTRL_04	0x08	RW	Bit[7]: Calculate sensor gain from real gain Bit[6]: Determine gain used in ISP Bit[5]: Choose place to apply digital gain in BLC or ISP IP Bit[4]: Gain delay by exposure change Bit[3]: Enable initial update Bit[2:0]: Not used
0x35C5	AEC_VS_CTRL_05	–	R	Bit[7:1]: Not used Bit[0]: Manual update enable
0x35C6	AEC_VS_CTRL_06	0xB0	RW	Bit[7:0]: expo_fine[15:8] Fine exposure high byte
0x35C7	AEC_VS_CTRL_07	0x00	RW	Bit[7:0]: expo_fine[7:0] Fine exposure low byte
0x35C8	AEC_VS_CTRL_08	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Real gain, integer part
0x35C9	AEC_VS_CTRL_09	0x00	RW	Bit[7:4]: Real gain, fractional part Bit[3:0]: Not used
0x35CA	AEC_VS_CTRL_0A	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Digital gain[19:16]
0x35CB	AEC_VS_CTRL_0B	0x00	RW	Bit[7:0]: Digital gain[15:8]
0x35CC	AEC_VS_CTRL_OC	0x00	RW	Bit[7:6]: Digital gain[7:6] Bit[5:0]: Not used

table A-2 sensor control registers (sheet 36 of 255)

address	register name	default value	R/W	description
0x35CD	AEC_VS_CTRL_0D	0x00	RW	Bit[7:0]: Sensor gain map
0x35CE	AEC_VS_CTRL_0E	–	R	Bit[7:0]: expo_coarse_cur[15:8] Current coarse exposure high byte
0x35CF	AEC_VS_CTRL_0F	–	R	Bit[7:0]: expo_coarse_cur[7:0] Current coarse exposure low byte
0x35D0	AEC_VS_CTRL_10	–	R	Bit[7:0]: expo_fine_cur[15:8] Current fine exposure high byte
0x35D1	AEC_VS_CTRL_11	–	R	Bit[7:0]: expo_fine_cur[7:0] Current fine exposure low byte
0x35D2	AEC_VS_CTRL_12	–	R	Bit[7:5]: Not used Bit[4:0]: real_gain_cur_real[12:8] Current real gain for BLC high 5 bit
0x35D3	AEC_VS_CTRL_13	–	R	Bit[7:1]: real_gain_cur_real[7:1] Current real gain for BLC low 7 bit Bit[0]: Not used
0x35D4	AEC_VS_CTRL_14	–	R	Bit[7:5]: Not used Bit[4:0]: gain_cur_org[12:8] Not converted current real gain high 5 bit
0x35D5	AEC_VS_CTRL_15	–	R	Bit[7:1]: gain_cur_org[7:1] Not converted current real gain low 7 bit Bit[0]: Not used
0x35D6	AEC_VS_CTRL_16	–	R	Bit[7:4]: Not used Bit[3:0]: snr_gain_coarse_cur Current sensor coarse gain
0x35D7	AEC_VS_CTRL_17	–	R	Bit[7:1]: snr_gain_fine_cur Current sensor fine gain Bit[0]: Not used
0x35D8	AEC_VS_CTRL_18	–	R	Bit[7:4]: Not used Bit[3:0]: Digital gain for BLC[19:16]
0x35D9	AEC_VS_CTRL_19	–	R	Bit[7:0]: Digital gain for BLC[15:8]
0x35DA	AEC_VS_CTRL_1A	–	R	Bit[7:6]: Digital gain for BLC[7:6] Bit[5:0]: Not used
0x35DB	AEC_VS_CTRL_1B	–	R	Bit[7:4]: Not used Bit[3:0]: dig_gain_mwb[19:16] Digital gain for ISP high 4 bit
0x35DC	AEC_VS_CTRL_1C	–	R	Bit[7:0]: dig_gain_mwb[15:8] Digital gain for ISP medium byte

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address	register name	default value	R/W	description
0x35DD	AEC_VS_CTRL_1D	–	R	Bit[7:6]: dig_gain_mwb[7:6] Digital gain for ISP low 2 bit Bit[5:0]: Not used
0x35DE	AEC_VS_CTRL_1E	–	R	Bit[7:5]: Not used Bit[4:0]: Real gain for BLC[12:8]
0x35DF	AEC_VS_CTRL_1F	–	R	Bit[7:4]: Real gain for BLC[7:4] Bit[3:0]: Not used
0x35E0	AEC_VS_CTRL_20	–	R	Bit[7:0]: Real gain for ISP[17:10], format 8.10
0x35E1	AEC_VS_CTRL_21	–	R	Bit[7:0]: Real gain for ISP[9:2]
0x35E2	AEC_VS_CTRL_22	–	R	Bit[7:6]: Real gain for ISP[1:0] Bit[5:0]: Not used
0x3600~ 0x37FF	RSVD	–	–	Reserved
0x3800	X_ADDR_START_INT_H	0x00	RW	Bit[7:0]: Horizontal start address[15:8]
0x3801	X_ADDR_START_INT_L	0x00	RW	Bit[7:0]: Horizontal start address[7:0]
0x3802	Y_ADDR_START_INT_H	0x00	RW	Bit[7:0]: Vertical start address[15:8]
0x3803	Y_ADDR_START_INT_L	0x04	RW	Bit[7:0]: Vertical start address[7:0]
0x3804	X_ADDR_END_INT_H	0x07	RW	Bit[7:0]: Horizontal end address[15:8]
0x3805	X_ADDR_END_INT_L	0x9F	RW	Bit[7:0]: Horizontal end address[7:0]
0x3806	Y_ADDR_END_INT_H	0x05	RW	Bit[7:0]: Vertical end address[15:8]
0x3807	Y_ADDR_END_INT_L	0x0B	RW	Bit[7:0]: Vertical end address[7:0]
0x3808	X_OUTPUT_SIZE_INT_H	0x07	RW	Bit[7:0]: Horizontal output size for final image[15:8]
0x3809	X_OUTPUT_SIZE_INT_L	0x80	RW	Bit[7:0]: Horizontal output size for final image[7:0]
0x380A	Y_OUTPUT_SIZE_INT_H	0x05	RW	Bit[7:0]: Vertical output size for final image[15:8]
0x380B	Y_OUTPUT_SIZE_INT_L	0x00	RW	Bit[7:0]: Vertical output size for final image[7:0]
0x380C	HTS_DCG_H	0x04	RW	Bit[7:0]: Portion of row time used for long exposure control and readout[15:8], in units of SCLK cycles

table A-2 sensor control registers (sheet 38 of 255)

address	register name	default value	R/W	description
0x380D	HTS_DCG_L	0x47	RW	Bit[7:0]: Portion of row time used for long exposure control and readout[7:0], in units of SCLK cycles
0x380E	VTS_H	0x02	RW	Bit[7:0]: Total number of rows per frame[15:8]
0x380F	VTS_L	0xAE	RW	Bit[7:0]: Total number of rows per frame[7:0]
0x3810	ISP_X_WIN_INT_H	0x00	RW	Bit[7:0]: Number of pixels to be cut off at horizontal beginning of image[15:8]
0x3811	ISP_X_WIN_INT_L	0x08	RW	Bit[7:0]: Number of pixels to be cut off at horizontal beginning of image[7:0]
0x3812	ISP_Y_WIN_INT_H	0x00	RW	Bit[7:0]: Number of rows to be cut off at vertical beginning of image[15:8]
0x3813	ISP_Y_WIN_INT_L	0x04	RW	Bit[7:0]: Number of rows to be cut off at vertical beginning of image[7:0]
0x3814	INC_INT3	0x01	RW	Bit[7:0]: Increase steps in horizontal odd position (x_odd_inc)
0x3815	INC_INT2	0x01	RW	Bit[7:0]: Increase steps in horizontal even position (x_even_inc)
0x3816	INC_INT1	0x01	RW	Bit[7:0]: Increase steps in vertical odd position (y_odd_inc)
0x3817	INC_INT0	0x01	RW	Bit[7:0]: Increase steps in vertical even position (y_even_inc)
0x3818	VSYNC_RISE_CCNT_H	0x00	RW	Bit[7:0]: Column counter value for VSYNC rising edge[15:8]
0x3819	VSYNC_RISE_CCNT_L	0x00	RW	Bit[7:0]: Column counter value for VSYNC rising edge[7:0]
0x381A	VSYNC_RISE_RCNT_H	0x00	RW	Bit[7:0]: Row counter value for VSYNC rising edge[15:8]
0x381B	VSYNC_RISE_RCNT_L	0x01	RW	Bit[7:0]: Row counter value for VSYNC rising edge[7:0]
0x381C	TIMING_CTRL_REG_1C	0x18	RW	Bit[7:5]: ablc_adj Bit[4]: format_lat_dis Disable registering format bits Bit[3]: tc_sof_sel Bit[2]: Not used Bit[1]: New stagger HDR mode enable Bit[0]: vref_img_rev

table A-2 sensor control registers (sheet 39 of 255)

address	register name	default value	R/W	description
0x381D	TIMING_CTRL_REG_1D	0x00	RW	Bit[7:6]: Not used Bit[5]: man_blc_num_sel Bit[4:0]: man_blc_num
0x381E	Y_INC_ISP_0	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Increase steps in vertical odd position (y_odd_inc), separate control for ISP due to double row readout
0x381F	Y_INC_ISP_1	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Increase steps in vertical even position (y_even_inc), separate control for ISP due to double row readout
0x3820	TIMING_CTRL_REG_20	0x00	RW	Bit[7]: Not used Bit[6]: vflip_blc Zero and black lines flip enable Bit[5]: Horizontal mirror enable Bit[4:3]: Not used Bit[2]: Vflip Image lines flip enable Bit[1:0]: Not used
0x3821	READ_MODE	0x19	RW	Bit[7:6]: dig_hbin Bit[5]: Not used Bit[4]: Dual conversion gain long capture enable Bit[3]: stg_hdr_en Staggered Vshort capture enable Bit[2]: stg_hdr2_en Staggered Short capture enable, cannot be used with split_pix_en Bit[1]: short_out_dis Disable short capture data readout from ASRAM Bit[0]: split_pix_en SPD Short capture enable, cannot be used with stg_hdr2_en

table A-2 sensor control registers (sheet 40 of 255)

address	register name	default value	R/W	description
0x3822	TIMING_CTRL_REG_22	0x13	RW	Bit[7]: tc_r_offs Bit[6]: ls_sel Select to output VSYNC in long exposure Bit[5]: Enable mode to fix timing counter before coming of external frame sync signal Bit[4]: vts_add_dis Disable VTS auto increase mode Bit[3:0]: grp_adj Number of rows before frame end for group launch
0x3823	TIMING_CTRL_REG_23	0x08	RW	Bit[7]: ext_vsync_re Reverse external VSYNC pulse Bit[6]: ext_vsync_en Enable to receive external VSYNC pulse Bit[4]: Enable to set row counter initial value manually Bit[3:0]: ext_vsync_div If this number is n, it means every n frames sensor will enable one external VSYNC pulse
0x3824	TC_CS_INIT_H	0x00	RW	Bit[7:0]: Column counter initial value[15:8]
0x3825	TC_CS_INIT_L	0x20	RW	Bit[7:0]: Column counter initial value[7:0]
0x3826	TC_R_INIT_MAN_H	0x00	RW	Bit[7:0]: Row counter initial value[15:8]
0x3827	TC_R_INIT_MAN_L	0x08	RW	Bit[7:0]: Row counter initial value[7:0]
0x3828	TIMING_CTRL_REG_28	0x36	RW	Bit[7]: Not used Bit[6:0]: zblc_num First active row address
0x382A	TC_R_INT_ADJ	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Number of rows adjusted for row counter initial value (range 0~15)
0x382B	FVTS_H	0x00	RW	Bit[7:0]: Fractional VTS[15:8] (every fvts row, rowtime is HTS+2 instead of HTS SCLK cycles)
0x382C	FVTS_L	0x00	RW	Bit[7:0]: Fractional VTS[7:0] (every fvts row, rowtime is HTS+2 instead of HTS SCLK cycles)
0x382D	VTS_INC	0x00	RW	Bit[7:0]: Number of rows to be added when exposure is greater than VTS
0x3830	TC_R_H	–	R	Bit[7:0]: Row counter value[15:8]

table A-2 sensor control registers (sheet 41 of 255)

address	register name	default value	R/W	description
0x3831	TC_R_HCG	–	R	Bit[7:0]: Row counter value[7:0]
0x3832	VSYNC_WIDTH	0x00	RW	Bit[7:4]: VSYNC width in units of rowtime, except 0 means 1 TCLK cycle, note it is in bits Bit[3:0]: Not used
0x3833	TIMING_CTRL_REG_33	0x01	RW	Bit[7:3]: Not used Bit[2]: stg_hdr_grp_wr_opt Bit[1]: stg_sleep_nomask Bit[0]: stg_grphold_nomask
0x3834	TIMING_CTRL_REG_34	0x00	RW	Bit[7:4]: context_sel Select to enable VSYNC output at certain group launch group Bit[3:0]: Not used
0x3836	THRESHOLD_VTS_SUB_H	0x1F	RW	Bit[7:0]: Threshold VTS for adjusment[15:8]
0x3837	THRESHOLD_VTS_SUB_L	0x40	RW	Bit[7:0]: Threshold VTS for adjustment[7:0]
0x3838~ 0x383C	NOT USED	0x48	RW	Bit[7:0]: Not used
0x383D	AUTO_SIZE_CTRL	0x00	RW	Bit[7:6]: Not used Bit[5]: Flip auto cut enable Bit[4]: Mirror auto cut enable Bit[3:0]: Not used
0x383E	TIMING_CTRL_REG_3E	0x00	RW	Bit[7]: vsync_ext_rst_dis Disable external VSYNC to reset timing counter value Bit[6:0]: Not used
0x3842	TIMING_CTRL_REG_42	0x00	RW	Bit[7:6]: Not used Bit[5]: vs_flag_rev Reverse very short flag Bit[4]: flag_rev Reverse long flag Bit[3:0]: Not used
0x3843~ 0x3844	NOT USED	0x00	RW	Bit[7:0]: Not used
0x3845	M_SOF_R_CNT_H	0x00	RW	Bit[7:0]: m_sof_r_cnt[15:8]
0x3846	M_SOF_R_CNT_L	0x03	RW	Bit[7:0]: m_sof_r_cnt[7:0]
0x3847	M_EOF_R_CNT_H	0x04	RW	Bit[7:0]: m_eof_r_cnt[15:8]
0x3848	M_EOF_R_CNT_L	0x60	RW	Bit[7:0]: m_eof_r_cnt[7:0]
0x3849	M_CS_CNT_H	0x02	RW	Bit[7:0]: m_cs_cnt[15:8]

table A-2 sensor control registers (sheet 42 of 255)

address	register name	default value	R/W	description
0x384A	M_CS_CNT_L	0x40	RW	Bit[7:0]: m_cs_cnt[7:0]
0x384C	HTS_SPD_H	0x02	RW	Bit[7:0]: Portion of row time used for short exposure control and readout[15:8], in units of SCLK cycles
0x384D	HTS_SPD_L	0x0D	RW	Bit[7:0]: Portion of row time used for Short exposure control and readout[7:0], in units of SCLK cycles
0x384E	L_CS_CNT_H	0x00	RW	Bit[7:0]: l_cs_cnt[15:8]
0x384F	L_CS_CNT_L	0x40	RW	Bit[7:0]: l_cs_cnt[7:0]
0x3850	DUMMY_SOF_R_CNT_H	0x00	RW	Bit[7:0]: dummy_sof_r_cnt[15:8]
0x3851	DUMMY_SOF_R_CNT_L	0x42	RW	Bit[7:0]: dummy_sof_r_cnt[7:0]
0x3852	DUMMY_EOF_R_CNT_H	0x00	RW	Bit[7:0]: dummy_eof_r_cnt[15:8]
0x3853	DUMMY_EOF_R_CNT_L	0x40	RW	Bit[7:0]: dummy_eof_r_cnt[7:0]
0x3854	S_SOF_R_CNT_H	0x00	RW	Bit[7:0]: s_sof_r_cnt[15:8]
0x3855	S_SOF_R_CNT_L	0x05	RW	Bit[7:0]: s_sof_r_cnt[7:0]
0x3856	S_EOF_R_CNT_H	0x00	RW	Bit[7:0]: s_eof_r_cnt[15:8]
0x3857	S_EOF_R_CNT_L	0x04	RW	Bit[7:0]: s_eof_r_cnt[7:0]
0x3858	TIMING_CTRL_REG_58	0x04	RW	Bit[7]: Not used Bit[6]: dummy_seof_manu_en Bit[5]: long_flag_dummy Bit[4]: long_flag_vs Bit[3]: long_flag_s Bit[2]: long_flag_l Bit[1]: sof_eof_manu_en Bit[0]: hdr_comb_en
0x3859	L_SOF_R_CNT_H	0x00	RW	Bit[7:0]: l_sof_r_cnt[15:8]
0x385A	L_SOF_R_CNT_L	0x03	RW	Bit[7:0]: l_sof_r_cnt[7:0]
0x385B	L_EOF_R_CNT_H	0x04	RW	Bit[7:0]: l_eof_r_cnt[15:8]
0x385C	L_EOF_R_CNT_L	0x60	RW	Bit[7:0]: l_eof_r_cnt[7:0]
0x385D	VS_SOF_R_CNT_H	0x00	RW	Bit[7:0]: vs_sof_r_cnt[15:8]
0x385E	VS_SOF_R_CNT_L	0x12	RW	Bit[7:0]: vs_sof_r_cnt[7:0]
0x385F	VS_EOF_R_CNT_H	0x00	RW	Bit[7:0]: vs_eof_r_cnt[15:8]
0x3860	VS_EOF_R_CNT_L	0x10	RW	Bit[7:0]: vs_eof_r_cnt[7:0]
0x3861	S_CS_CNT_H	0x00	RW	Bit[7:0]: s_cs_cnt[15:8]

table A-2 sensor control registers (sheet 43 of 255)

address	register name	default value	R/W	description
0x3862	S_CS_CNT_L	0x40	RW	Bit[7:0]: s_cs_cnt[7:0]
0x3863	VS_CS_CNT_H	0x00	RW	Bit[7:0]: vs_cs_cnt[15:8]
0x3864	VS_CS_CNT_L	0x40	RW	Bit[7:0]: vs_cs_cnt[7:0]
0x3865	DUMMY_CS_CNT_H	0x00	RW	Bit[7:0]: dummy_cs_cnt[15:8]
0x3866	DUMMY_CS_CNT_L	0x40	RW	Bit[7:0]: dummy_cs_cnt[7:0]
0x3867	TIMING_CTRL_REG_67	0x31	RW	Bit[7:6]: Not used Bit[5]: vshort_flag_dummy Bit[4]: vshort_flag_vs Bit[3]: vshort_flag_s Bit[2]: vshort_flag_l Bit[1]: vshort_flag_m Bit[0]: long_flag_m
0x386C	TC_R_VS_LAT_H	–	R	Bit[7:0]: Latched row counter value for very short exposure part[15:8]
0x386D	TC_R_VS_LAT_L	–	R	Bit[7:0]: Latched row counter value for very short exposure part[7:0]
0x386E	TOTAL_HTS_H	–	R	Bit[7:0]: Latched total HTS value[15:8]
0x386F	TOTAL_HTS_L	–	R	Bit[7:0]: Latched total HTS value[7:0]
0x3871	TC_R_HCGAT_H	–	R	Bit[7:0]: Latched row counter value for long exposure part[15:8]
0x3872	TC_R_HCGAT_L	–	R	Bit[7:0]: Latched row counter value for long exposure part[7:0]
0x3873	TC_R_SPD_LAT_H	–	R	Bit[7:0]: Latched row counter value for short exposure part[15:8]
0x3874	TC_R_SPD_LAT_L	–	R	Bit[7:0]: Latched row counter value for short exposure part[7:0]
0x3875~ 0x387E	NOT USED	–	R	Bit[7:0]: Not used
0x3880	VTS_ADJ_DIR	–	R	Bit[7:0]: VTS adjust direction because of frame sync 0: Increase 1: Decrease

table A-2 sensor control registers (sheet 44 of 255)

address	register name	default value	R/W	description
0x3881	TIMING_CTRL_REG_81	0x02	RW	Bit[7:6]: Not used Bit[5:4]: hdr_num 0: Long/short 1: Long/medium/short Bit[3]: ext_vsync_rst_sensor_timing_en Enable reset sensor timing by external VSYNC Bit[2]: ext_vsync_adj_vts_en Enable mode to adjust VTS by external VSYNC Bit[1:0]: VTS adjust threshold VTS will be adjusted only if difference of row counters in two sensors is larger than this threshold
0x3882	SYNC_ROW_CNT_ADJ_H	0x00	RW	Bit[7:0]: Number of rows before frame end to set for row comparison between two sensors[15:8]
0x3883	SYNC_ROW_CNT_ADJ_L	0x08	RW	Bit[7:0]: Number of rows before frame end to set for row comparison between two sensors[7:0]
0x388C	HTS_VS_H	0x02	RW	Bit[7:0]: Portion of row time used for very short exposure control and readout, in units of SCLK cycles[15:8]
0x388D	HTS_VS_L	0x2B	RW	Bit[7:0]: Portion of row time used for very short exposure control and readout, in units of SCLK cycles[7:0]
0x388E	SYNC_CS_CNT	0x01	RW	Bit[7:0]: sync_cs_cnt
0x388F	SYNC_CS_CNT_8F	0x00	RW	Bit[7:0]: sync_cs_cnt
0x3890	FSYNC_CS_THRESHOLD	0x00	RW	Bit[7:0]: fsync_cs_threshold
0x3891	FSYNC_CS_THRESHOLD_91	0x20	RW	Bit[7:0]: fsync_cs_threshold
0x3892	TIMING_CTRL_REG_92	0x40	RW	Bit[7:4]: fsin_glitch_filter_num Number of filter step Bit[3]: Not used Bit[2]: fsync_cs_adj_en Bit[1:0]: vsync_ps
0x3894	REAL_HTS_H	–	R	Bit[7:0]: Real using HTS
0x3895	REAL_HTS_L	–	R	Bit[7:0]: Real using HTS
0x3896	REAL_VTS_H	–	R	Bit[7:0]: Real using VTS

table A-2 sensor control registers (sheet 45 of 255)

address	register name	default value	R/W	description
0x3897	REAL_VTS_L	–	R	Bit[7:0]: Real using VTS
0x3B40	APC_CALC_RANGE_H_H	0x0F	RW	Bit[7:4]: Not used Bit[3:0]: High calculation range[11:8]
0x3B41	APC_CALC_RANGE_H_L	0x80	RW	Bit[7:0]: High calculation range[7:0]
0x3B42	APC_CALC_RANGE_L_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Low calculation range[11:8]
0x3B43	APC_CALC_RANGE_L_L	0x80	RW	Bit[7:0]: Low calculation range[7:0]
0x3B44	APC_CHECK_MARGIN_H_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: High margin[11:8]
0x3B45	APC_CHECK_MARGIN_H_L	0xC0	RW	Bit[7:0]: High margin[7:0]
0x3B46	APC_CHECK_MARGIN_L_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Low margin[11:8]
0x3B47	APC_CHECK_MARGIN_L_L	0xC0	RW	Bit[7:0]: Low margin[7:0]
0x3B48	APC_LVL_SIG_0	0x18	RW	Bit[7:5]: Not used Bit[4:0]: Analog test row signal level (option 0)
0x3B49	APC_LVL_SIG_1	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Analog test row signal level (option 1)
0x3B4A	APC_LVL_SIG_2	0x3C	RW	Bit[7:5]: Not used Bit[4:0]: Analog test row signal level (option 2)
0x3B4B	APC_LVL_SIG_3_AND_SEL	0x2D	RW	Bit[7]: Not used Bit[6:5]: Select switching control for APC levels 00: Fix at option 0 01: apc_level_trigger_i rising 10: sof_vs 11: apc_href_post_vs falling Bit[4:0]: Analog test row signal level (option 3)
0x3B4C	APC_FAULT_MASK_H	0x00	RW	Bit[7:2]: Not used Bit[1]: apc_chk1_defunct_mask (mask for fault) Self-test failed in APC checker no 1 (checks data from ADC bank 1) Bit[0]: apc_chk0_defunct_mask (mask for fault) Self-test failed in APC checker 0 (checks data from ADC bank 0)

table A-2 sensor control registers (sheet 46 of 255)

address	register name	default value	R/W	description
0x3B4D	APC_FAULT_MASK_L	0x00	RW	Bit[7]: apc_improper_input_flags_ vs1_mask (mask for fault) Improper input flags to APC module, VS exposure Bit[6]: apc_improper_input_flags_ m1_mas (mask for fault) Improper input flags to APC module, M exposure Bit[5]: apc_improper_input_flags_ l0_mask (mask for fault) Improper input flags to APC module, L exposure Bit[4]: apc_err_wide_vs1_mask (mask for fault) Pixels outside wide range set for average, ADC bank 1, VS1 exposure Bit[3]: apc_err_wide_m1_mask (mask for fault) Pixels outside wide range set for average, ADC bank 1, M exposure Bit[2]: apc_err_wide_l0_mask (mask for fault) Pixels outside wide range set for average, ADC bank 0, L exposure Bit[1]: apc_err_narrow_m1_mask (mask for fault) Pixels outside narrow margin around average, ADC bank 1, M exposure Bit[0]: apc_err_narrow_l0_mask (mask for fault) Pixels outside narrow margin around average, ADC bank 0, L exposure
0x3B4E	APC_FAULT_LIVE_H	–	R	Bit[7:2]: Not used Bit[1]: apc_chk1_defunct_live (live) Self-test failed in APC checker no 1 (checks data from ADC bank 1) Bit[0]: apc_chk0_defunct_live (live) Self-test failed in APC checker 0 (checks data from ADC bank 0)

table A-2 sensor control registers (sheet 47 of 255)

address	register name	default value	R/W	description
0x3B4F	APC_FAULT_LIVE_L	–	R	Bit[7]: apc_improper_input_flags_ vs1_live (live) Improper input flags to APC module, VS exposure Bit[6]: apc_improper_input_flags_ m1_live (live) Improper input flags to APC module, M exposure Bit[5]: apc_improper_input_flags_l0_live (live) Improper input flags to APC module, L exposure Bit[4]: apc_err_wide_vs1_live (live) Pixels outside wide range set for average, ADC bank 1, VS1 exposure Bit[3]: apc_err_wide_m1_live (live) Pixels outside wide range set for average, ADC bank 1, M exposure Bit[2]: apc_err_wide_l0_live (live) Pixels outside wide range set for average, ADC bank 0, L exposure Bit[1]: apc_err_narrow_m1_live (live) Pixels outside narrow margin around average, ADC bank 1, M exposure Bit[0]: apc_err_narrow_l0_live (live) Pixels outside narrow margin around average, ADC bank 0, L exposure
0x3B50	APC_FAULT_LATCHED_H	–	R	Bit[7:3]: Not used Bit[2]: apc_fault_flag_state State of fault_flag module in APC Bit[1]: apc_chk1_defunct_flatched (latched at fault) Self-test failed in APC checker no 1 (checks data from ADC bank 1) Bit[0]: apc_chk0_defunct_flatched (latched at fault) Self-test failed in APC checker 0 (checks data from ADC bank 0)

table A-2 sensor control registers (sheet 48 of 255)

address	register name	default value	R/W	description
0x3B51	APC_FAULT_LATCHED_L	–	R	Bit[7]: apc_improper_input_flags_vs1_flatched (latched at fault) Improper input flags to APC module, VS exposure Bit[6]: apc_improper_input_flags_m1_flatched (latched at fault) Improper input flags to APC module, M exposure Bit[5]: apc_improper_input_flags_l0_flatched (latched at fault) Improper input flags to APC module, L exposure Bit[4]: apc_err_wide_vs1_flatched (latched at fault) Pixels outside wide range set for average, ADC bank 1, VS1 exposure Bit[3]: apc_err_wide_m1_flatched (latched at fault) Pixels outside wide range set for average, ADC bank 1, M exposure Bit[2]: apc_err_wide_l0_flatched (latched at fault) Pixels outside wide range set for average, ADC bank 0, L exposure Bit[1]: apc_err_narrow_m1_flatched (latched at fault) Pixels outside narrow margin around average, ADC bank 1, M exposure Bit[0]: apc_err_narrow_l0_flatched (latched at fault) Pixels outside narrow margin around average, ADC bank 0, L exposure
0x3B52	APC_ERROR_COUNT_0_LIVE	–	R	Bit[7:0]: Number of errors detected (live), ADC bank 0, if > 255n 255
0x3B53	APC_ERROR_COUNT_1_LIVE	–	R	Bit[7:0]: Number of errors detected (live), ADC bank 1, if > 255n 255
0x3B54	APC_AVG_L0_LIVE_H	–	R	Bit[7:4]: Not used Bit[3:0]: apc_average_l0_live_h[15:8] (live) Average value from ADC bank 0, L exposure (high byte)
0x3B55	APC_AVG_L0_LIVE_L	–	R	Bit[7:0]: apc_average_l0_live_l[7:0] (live) Average value from ADC bank 0, L exposure, (low byte)

table A-2 sensor control registers (sheet 49 of 255)

address	register name	default value	R/W	description
0x3B56	APC_AVG_M1_LIVE_H	–	R	Bit[7:4]: Not used Bit[3:0]: apc_average_m1_live_h[15:8] (live) Average value from ADC bank 1, M exposure (high byte)
0x3B57	APC_AVG_M1_LIVE_L	–	R	Bit[7:0]: apc_average_m1_live_l[7:0] (live) Average value from ADC bank 1, M exposure (low byte)
0x3B58	APC_AVG_VS1_LIVE_H	–	R	Bit[7:4]: Not used Bit[3:0]: apc_average_vs1_live_h[15:8] (live) Average value from ADC bank 1, VS1 exposure (high byte)
0x3B59	APC_AVG_VS1_LIVE_L	–	R	Bit[7:0]: apc_average_vs1_live_l[7:0] (live) Average value from ADC bank 1, VS1 exposure (low byte)
0x3B5A	APC_ERROR_COUNT_0_ LATCHED	–	R	Bit[7:0]: Number of errors detected (latched at fault), ADC bank 0, if > 255n 255
0x3B5B	APC_ERROR_COUNT_1_ LATCHED	–	R	Bit[7:0]: Number of errors detected (latched at fault), ADC bank 1, if > 255n 255
0x3B5C	APC_AVG_L0_LATCHED_H	–	R	Bit[7:4]: Not used Bit[3:0]: apc_average_l0_latched_h[15:8] (latched at fault) Average value from ADC bank 0, L exposure (high byte)
0x3B5D	APC_AVG_L0_LATCHED_L	–	R	Bit[7:0]: apc_average_l0_latched_l[7:0] (latched at fault) Average value from ADC bank 0, L exposure (low byte)
0x3B5E	APC_AVG_M1_LATCHED_ H	–	R	Bit[7:4]: Not used Bit[3:0]: apc_average_m1_ latched_h[15:8] (latched at fault) Average value from ADC bank 1, M exposure (high byte)
0x3B5F	APC_AVG_M1_LATCHED_L	–	R	Bit[7:0]: apc_average_m1_latched_l[7:0] (latched at fault) Average value from ADC bank 1, M exposure (low byte)

table A-2 sensor control registers (sheet 50 of 255)

address	register name	default value	R/W	description
0x3B60	APC_AVG_VS1_LATCHED_H	–	R	Bit[7:4]: Not used Bit[3:0]: apc_average_vs1_latched_h[15:8] (latched at fault) Average value from ADC bank 1, VS1 exposure (high byte)
0x3B61	APC_AVG_VS1_LATCHED_L	–	R	Bit[7:0]: apc_average_vs1_latched_l[7:0] (latched at fault) Average value from ADC bank 1, VS1 exposure (low byte)
0x3B80	PIXASIL_ROI_FAILED_NR_TH_H1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Failing-pixels threshold in ROI for issuing error signal[19:16], 4 MSBs
0x3B81	PIXASIL_ROI_FAILED_NR_TH_H2	0x03	RW	Bit[7:0]: Failing-pixels threshold in ROI for issuing error signal[15:8]
0x3B82	PIXASIL_ROI_FAILED_NR_TH_L	0xE8	RW	Bit[7:0]: Failing-pixels threshold in ROI for issuing error signal[7:0]
0x3B83	PIXASIL_FRAME_FAILED_NR_TH_H1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Failing-pixels threshold in full-frame for issuing error signal[19:16], 4 MSBs
0x3B84	PIXASIL_FRAME_FAILED_NR_TH_H2	0x03	RW	Bit[7:0]: Failing-pixels threshold in full-frame for issuing error signal[15:8]
0x3B85	PIXASIL_FRAME_FAILED_NR_TH_L	0xE8	RW	Bit[7:0]: Failing-pixels threshold in full-frame for issuing error signal[7:0]
0x3B86	A_PIXASIL_ROI_Y_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: a_roi_y_start ROI row start location, 4 MSBs
0x3B87	A_PIXASIL_ROI_Y_L	0x00	RW	Bit[7:0]: a_roi_y_start ROI row start location[7:0]
0x3B88	A_PIXASIL_ROI_X_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: a_roi_x_start ROI column start location, 4 MSBs
0x3B89	A_PIXASIL_ROI_X_L	0x00	RW	Bit[7:0]: a_roi_x_start[7:0] ROI column start location, Low byte
0x3B8A	A_PIXASIL_ROI_Y_SIZE_H	0x04	RW	Bit[7:4]: Not used Bit[3:0]: ROI row size, 4 MSBs

table A-2 sensor control registers (sheet 51 of 255)

address	register name	default value	R/W	description
0x3B8B	A_PIXASIL_ROI_Y_SIZE_L	0xFF	RW	Bit[7:0]: ROI row size[7:0] ROI rows = start + size
0x3B8C	A_PIXASIL_ROI_X_SIZE_H	0x07	RW	Bit[7:4]: Not used Bit[3:0]: ROI column size, 4 MSBs
0x3B8D	A_PIXASIL_ROI_X_SIZE_L	0x7F	RW	Bit[7:0]: ROI column size[7:0] ROI columns = start + size
0x3B8E	B_PIXASIL_ROI_Y_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: b_roi_y_start ROI row start location, 4 MSBs
0x3B8F	B_PIXASIL_ROI_Y_L	0x00	RW	Bit[7:0]: b_roi_y_start[7:0] ROI row start location, low byte
0x3B90	B_PIXASIL_ROI_X_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: b_roi_x_start ROI column start location, 4 MSBs
0x3B91	B_PIXASIL_ROI_X_L	0x00	RW	Bit[7:0]: b_roi_x_start[7:0] ROI column start location, low byte
0x3B92	B_PIXASIL_ROI_Y_SIZE_H	0x04	RW	Bit[7:4]: Not used Bit[3:0]: ROI row size, 4 MSBs
0x3B93	B_PIXASIL_ROI_Y_SIZE_L	0xFF	RW	Bit[7:0]: ROI row size[7:0] ROI rows = start + size
0x3B94	B_PIXASIL_ROI_X_SIZE_H	0x07	RW	Bit[7:4]: Not used Bit[3:0]: ROI column size, 4 MSBs
0x3B95	B_PIXASIL_ROI_X_SIZE_L	0x7F	RW	Bit[7:0]: ROI Column size[7:0] ROI Columns = start + size
0x3B96	PIXASIL_FAIL_FLAG_ STATUS	–	R	Bit[7:4]: Not used Bit[3]: SEL_ROI frame-synchronized status, read this before setting next ROI Bit[2]: pixasil_frame_fail_flag Latched last time fault was detected – number of failing pixels in full-frame exceeded threshold value Bit[1]: pixasil_atr_fail_flag Latched last time fault was detected - All pixels are not faulty in first two rows Bit[0]: Latched last time fault was detected – Number of failing pixels in ROI exceeded threshold

table A-2 sensor control registers (sheet 52 of 255)

address	register name	default value	R/W	description
0x3B97	TOTAL_ROI_PIXASIL_FAULTS_H1	–	R	Bit[7:4]: Not used Bit[3:0]: Total pixel ASIL faults detected in ROI[19:16]
0x3B98	TOTAL_ROI_PIXASIL_FAULTS_H2	–	R	Bit[7:0]: Total pixel ASIL faults detected in ROI[15:8]
0x3B99	TOTAL_ROI_PIXASIL_FAULTS_L	–	R	Bit[7:0]: Total pixel ASIL faults detected in ROI[7:0]
0x3B9A	TOTAL_FRAME_PIXASIL_FAULTS_H1	–	R	Bit[7:4]: Not used Bit[3:0]: Total pixel ASIL faults detected in current[19:16]
0x3B9B	TOTAL_FRAME_PIXASIL_FAULTS_H2	–	R	Bit[7:0]: Total pixel ASIL faults detected in current[15:8]
0x3B9C	TOTAL_FRAME_PIXASIL_FAULTS_L	–	R	Bit[7:0]: Total pixel ASIL faults detected in current[7:0]
0x3B9D	PIXASIL_STATUS	0x01	RW	Bit[7:3]: Not used Bit[2]: Inject PIXASIL fault manually to take system to safe state Bit[1]: ROI select bit 0: A ROI 1: B ROI Bit[0]: Pixel ASIL is enabled
0x3B9E	PIXASIL_FAULT_MASK	0x08	RW	Bit[7:4]: Not used Bit[3]: Mask manual injection of PIXASIL fault Bit[2]: Mask pixasil_frame_fail_flag Bit[1]: Mask PIXASIL atr fail_flag Bit[0]: Mask PIXASIL fail flag
0x3B9F	PIXASIL_FAULT_LATCH	–	R	Bit[7:4]: Not used Bit[3]: latch_inject_pixasil_fault Watchdog manually injected fault status Bit[2]: fault_flag modules fault_latch_o for pixasil_frame_fail_flag Bit[1]: fault_flag modules fault_latch_o for pixasil_atr_fail_flag Bit[0]: fault_flag modules fault_latch_o for pixasil_fail_flag
0x3C00~ 0x3CFF	RSVD	–	–	Reserved
0x3D80	OTP_PGEN	–	R	Bit[7]: otp_pgenb_n 0: Not in OTP program 1: In OTP program Bit[6:0]: Not used

table A-2 sensor control registers (sheet 53 of 255)

address	register name	default value	R/W	description
0x3D81	OTP_LOAD	–	R	Bit[7]: otp_load 0: Not in OTP load 1: In OTP load Bit[6]: Not used Bit[5]: OTP BIST function error flag Bit[4]: otp_bist_done OTP BIST is done or error is found Bit[3:1]: Not used Bit[0]: OTP load trigger (0x3D81[0] = 1)
0x3D82	OTP_PGM_CTR	0xBC	RW	Bit[7:0]: Timing length of OTP strobe/8 for program operation
0x3D83	OTP_REG83	0x08	RW	Bit[7:4]: Not used Bit[3:0]: rd_ctrl Timing length of OTP strobe for read operation
0x3D84	OTP_MODE	0x00	RW	Bit[7]: pgm_dis Disable OTP program Bit[6]: manu_mode_en 0: OTP all-byte mode 1: OTP manual mode Bit[5:0]: Not used

table A-2 sensor control registers (sheet 54 of 255)

address	register name	default value	R/W	description
0x3D85	OTP_BIST_AUTOLOAD_CTRL	0x0B	RW	Bit[7]: otp_ldbist_dis Disable OTP load BIST which will compare and check data written to OTP SRAM Bit[6]: otp_bist_comp_val Compared value with OTP load data during OTP BIST function, assigned by user Bit[5]: otp_bist_sel OTP load data compare with value 0x3D85[6] 0: OTP load data compare with SRAM buffer data Bit[4]: otp_bist_en 0: OTP BIST function disable 1: OTP BIST function enable Bit[3]: pwup_load_en 0: OTP auto-load only first time (when bit[2] = 1) 1: OTP auto-load every time state STREAM_ON is entered Bit[2]: otp_in_streaming_en OTP auto-load at entering STREAM_ON is governed by bit[3], 0 = OTP auto-load never takes place in state STREAM_ON, new bit in 0x01D10 Note: OTP loading always takes place at START_UP_OTP Bit[1]: hw_ld_setting_en System all-byte automatic load setting operation enable Bit[0]: sw_ld_setting_en System 0x3D81[0] = 1 triggered load setting operation enable
0x3D87	OTP_WAIT	0x0A	RW	Bit[7:4]: Not used Bit[3:0]: Ps2cs Waiting time after 0x3D80[0] = 1 and before OTP starts programing
0x3D88	OTP_ADR_STT_PT_H	0x00	RW	Bit[7:0]: Start global address[15:8]
0x3D89	OTP_ADR_STT_PT_L	0x00	RW	Bit[7:0]: Start global address[7:0]
0x3D8A	OTP_ADDR_END_PT_H	0x03	RW	Bit[7:0]: End global address[15:8]
0x3D8B	OTP_ADR_END_PT_L	0xFF	RW	Bit[7:0]: End global address[7:0]

table A-2 sensor control registers (sheet 55 of 255)

address	register name	default value	R/W	description
0x3D8C	OTP_SET_ADDR_STT_PT_H	0x00	RW	Bit[7:0]: setting_adr_stt_pt_h[15:8] OTP load setting start address high byte
0x3D8D	OTP_SET_ADDR_STT_PT_L	0x26	RW	Bit[7:0]: setting_adr_stt_pt_l OTP load setting start address low byte
0x3D8E	OTP_BIST_ERR_ADR_H	–	R	Bit[7:0]: OTP BIST first address[15:8] where error is reported, 0 means no error
0x3D8F	OTP_BIST_ERR_ADR_L	–	R	Bit[7:0]: OTP BIST first address[7:0] where error is reported, 0 means no error
0x3D90	OTP_ADR_BASE_H	0x00	RW	Bit[7:0]: OTP base address[15:8] Used when SRAM buffer size is smaller than OTP size
0x3D91	OTP_ADR_BASE_L	0x00	RW	Bit[7:0]: OTP base address[7:0] Used when SRAM buffer size is smaller than OTP size
0x3D92	OTP_PGEN_92	0xE2	RW	Bit[7:4]: t_pgenb_end Waiting time after OTP finishes programming and before OTP programming sign is pulled up Bit[3:0]: t_pgenb_start Waiting time after 0x3D80[0] = 1 and before OTP programming sign is pulled down
0x3D93	OTP_VDDQ	0x46	RW	Bit[7:4]: t_vddq_end Waiting time after OTP finishes programming and before OTP VDDQ control is pulled down Bit[3:0]: t_vddq_start Waiting time after 0x3D80[0] = 1 and before OTP VDDQ control is pulled up
0x3D94	OTP_STROBE_GAP_PGM	0x14	RW	Bit[7:0]: Number of SCLK cycle of gap between two OTP strobes for OTP program
0x3D95	OTP_STROBE_GAP_LOAD	0x06	RW	Bit[7:4]: Not used Bit[3:0]: Number of SCLK cycle of gap between two OTP strobes for OTP load

table A-2 sensor control registers (sheet 56 of 255)

address	register name	default value	R/W	description
0x3D96	OTP_CRC_CTR	0x01	RW	Bit[7:2]: Not used Bit[1]: Reset OTP CRC error flag and reported result Bit[0]: crc_chk_en OTP CRC function enable during OTP load operation
0x3D97	OTP_CRC_STT_ADR0_H	0x00	RW	Bit[7:0]: OTP CRC first address segment start address[15:8]
0x3D98	OTP_CRC_STT_ADR0_L	0x24	RW	Bit[7:0]: OTP CRC first address segment start address[7:0]
0x3D99	OTP_CRC_END_ADR0_H	0x00	RW	Bit[7:0]: OTP CRC first address segment end address[15:8]
0x3D9A	OTP_CRC_END_ADR0_L	0x6D	RW	Bit[7:0]: OTP CRC first address segment end address[7:0]
0x3D9B	OTP_CRC_STT_ADR1_H	0x00	RW	Bit[7:0]: OTP CRC second address segment start address[15:8]
0x3D9C	OTP_CRC_STT_ADR1_L	0x6E	RW	Bit[7:0]: OTP CRC second address segment start address[7:0]
0x3D9D	OTP_CRC_END_ADR1_H	0x03	RW	Bit[7:0]: OTP CRC second address segment end address[15:8]
0x3D9E	OTP_CRC_END_ADR1_L	0xFF	RW	Bit[7:0]: OTP CRC second address segment end address[7:0]
0x3D9F	OTP_CRC_STT_ADR2_H	0x00	RW	Bit[7:0]: OTP CRC third address segment start address[15:8]
0x3DA0	OTP_CRC_STT_ADR2_L	0x10	RW	Bit[7:0]: OTP CRC third address segment start address[7:0]
0x3DA1	OTP_CRC_END_ADR2_H	0x00	RW	Bit[7:0]: OTP CRC third address segment end address[15:8]
0x3DA2	OTP_CRC_END_ADR2_L	0x23	RW	Bit[7:0]: OTP CRC third address segment end address[7:0]

table A-2 sensor control registers (sheet 57 of 255)

address	register name	default value	R/W	description
0x3DA3	OTP_CRC_ADR_ERR	–	R	Bit[7]: OTP SRAM load and compare MBIST passed Bit[6]: Not used Bit[5]: verify_err Error flag reports read-back check Bit[4]: crc_adr2_err Error flag reported in first address segment Bit[3]: crc_adr1_err Error flag reported in second address segment Bit[2]: crc_adr0_err Error flag reported in third address segment Bit[1:0]: crc_err_cnt Number of address segments which have errors
0x3DA4	OTP_SLOPE_CTR	0x20	RW	Bit[7:6]: Not used Bit[5]: ef_vq_pwup_en_o OTP VQ_PWUP is enabled (default will be driver by P_RST_B in analog) Bit[4]: ef_slope_ctrl_all0 OTP VQPS ef_slope_ctrl always low Bit[3]: sreg_ldo_pd Register setting OTP LDO function (not used) Bit[2:1]: ef_slope_sreg OTP VQPS slope control Bit[0]: ef_slope_ctrl_all1 OTP VQPS ef_slope_ctrl always high, has no reset sequence with digital and analog reset
0x3DA5	OTP_SRAM_T0	0x06	RW	Bit[7:6]: Not used Bit[5:0]: SRAM test control signals
0x3DA6	OTP_SRAM_T1	0x06	RW	Bit[7:0]: SRAM test control signals

table A-2 sensor control registers (sheet 58 of 255)

address	register name	default value	R/W	description
0x3DA7	OTP_FAULT_MASKED	0x40	RW	Bit[7]: Not used Bit[6]: wd_fault_inject_mask Masked manual fault injection to watchdog Bit[5]: verify_err_masked Masked read-back check error Bit[4]: crc_adr2_err_masked Masked error flag in third address segment Bit[3]: crc_adr1_err_masked Masked error flag in second address segment Bit[2]: crc_adr0_err_masked Masked error flag in first address segment Bit[1:0]: Not used
0x3DA8	OTP_FAULT_STATUS	–	R	Bit[7]: Not used Bit[6]: Status of injected fault to watchdog Bit[5]: verify_fault Read-back verification fault Bit[4]: crc_adr2_fault First address segment CRC fault Bit[3]: crc_adr1_fault Second address segment CRC fault Bit[2]: crc_adr0_fault Third address segment CRC fault Bit[1]: Not used Bit[0]: OTP fault state
0x3DA9	OTP_WD_INJECT_FAULT	0x00	RW	Bit[7:1]: Not used Bit[0]: wd_otp_inject_fault Injects a fault to watchdog manually
0x3E00~ 0x3F0F	RSVD	–	–	Reserved

table A-2 sensor control registers (sheet 59 of 255)

address	register name	default value	R/W	description
0x4000	BLC_CTRL_0	0x78	RW	Bit[7]: off_trig_en Enable triggering of BLC update after offset out of range Bit[6]: exp_chg_trig_en Enable triggering of BLC update after exposure changes Bit[5]: gain_chg_trig_en Enable triggering of BLC update after gain changes Bit[4]: fmt_chg_trig_en Enable triggering of BLC update after format changes Bit[3]: rst_trig_en Enable triggering of BLC update after reset release Bit[2]: Manual trigger BLC update Bit[1]: off_frz_en BLC update freeze Bit[0]: off_always_up BLC update every frames
0x4001	BLC_CTRL_1	0x2B	RW	Bit[7]: zero_ln_out_en Enable of zero row output Bit[6]: blk_ln_out_en Enable of black row output Bit[5]: Dither function enable Bit[4]: off_man_en Use manual offset value for BL correction Bit[3]: Median filter enable Bit[2]: Zero banding correction (ZBC) enable Bit[1]: Dark current BLC function enable Bit[0]: BLC enable (MSB pass-through if disabled)
0x4002	HWIN_OFF_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Black row calculated window start offset[11:8]
0x4003	HWIN_OFF_L	0x80	RW	Bit[7:0]: Black row calculated window start offset[7:0]
0x4004	HWIN_PAD_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Black row calculated window end offset[11:8]
0x4005	HWIN_PAD_L	0x80	RW	Bit[7:0]: Black row calculated window end offset[7:0]

table A-2 sensor control registers (sheet 60 of 255)

address	register name	default value	R/W	description
0x4006	HSIZE_MAN_H	0x0F	RW	Bit[7:4]: Not used Bit[3:0]: Manual horizontal size[11:8], overrides input (hsize_i)
0x4007	HSIZE_MAN_L	0x00	RW	Bit[7:0]: Manual horizontal size[7:0], overrides input (hsize_i)
0x4008	ZL_START	0x04	RW	Bit[7:5]: Not used Bit[4:0]: Zero line start row
0x4009	ZL_END	0x07	RW	Bit[7:5]: Not used Bit[4:0]: Zero line end row
0x400A	ZERO_LN_NUM	0x08	RW	Bit[7:5]: Not used Bit[4:0]: Manual number of zero lines, overrides input (zero_ln_num_i) if enabled (ln_num_man)
0x400B	BL_START	0x02	RW	Bit[7:5]: Not used Bit[4:0]: Black row select start
0x400C	BL_END	0x0F	RW	Bit[7:5]: Not used Bit[4:0]: Black row select end
0x400D	BLK_LN_NUM	0x10	RW	Bit[7:5]: Not used Bit[4:0]: Manual number of black lines, overrides input (black_ln_num_i) if enabled (ln_num_man)
0x400E	OFF_LIM_TH_L_H	0x03	RW	Bit[7:4]: Not used Bit[3:0]: Offset limit threshold L expo (absolute maximum offset)
0x400F	OFF_LIM_TH_L_L	0x6F	RW	Bit[7:0]: Offset limit threshold L expo (absolute maximum offset)
0x4010	REG_BLC_28	0x6F	RW	Bit[7]: Not used Bit[6]: lim_bits_en Bit[5]: Black level threshold enable (row averaging discards samples larger than threshold) Bit[4]: thres_lcgan_en Manual black level threshold enable Bit[3:0]: Accumulator stats threshold histogram cutoff
0x4011	THRES_DELTA_CUTOFF	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Accumulator stats threshold delta cutoff
0x4012	THRES_DELTA	0x30	RW	Bit[7:0]: Accumulator stats threshold delta

table A-2 sensor control registers (sheet 61 of 255)

address	register name	default value	R/W	description
0x4013	THRES_HCGINE	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Accumulator stats threshold line
0x4014	THRES_LCGAN_H	0x0F	RW	Bit[7:4]: Not used Bit[3:0]: Accumulator manual black Level threshold[11:8]
0x4015	THRES_LCGAN_L	0xFF	RW	Bit[7:0]: Accumulator manual black Level threshold[7:0]
0x4016	MF_TH	0x00	RW	Bit[7]: Not used Bit[6:0]: Median filter threshold
0x4017	CCHS_CTRL	0x07	RW	Bit[7:4]: Not used Bit[3:2]: zbc_cchs Number of color channels to process for ZBC, default 1 Bit[1:0]: blc_cchs Number of color channels to process for BLC, default 4
0x4018	BLC_CTRL_3	0x12	RW	Bit[7]: img_gfirst_rvs Reverse order of columns in active pixels Bit[6]: blk_rblue_rvs Reverse order of rows in black pixels Bit[5]: img_rblue_rvs Reverse order of rows in active pixels Bit[4]: Insert dummy flag on zero/black lines while zero/black line output is enabled Bit[3]: hsize_man_en Override hsize input with manual register values Bit[2]: In_num_man Override zero and black line input with manual register values Bit[1]: rst_trig_opt Bit[0]: man_avg_en Enable EWMA frame to frame averaging

table A-2 sensor control registers (sheet 62 of 255)

address	register name	default value	R/W	description
0x4019	BLC_CRTL_4	0xFF	RW	Bit[7]: Reserved Bit[6]: Offset change (out of range) multi frame update enable Bit[5]: Format change multi frame update enable Bit[4]: Gain change multi frame update enable Bit[3]: Reset multi frame update mode Bit[2]: Offset change (out of range) multi frame update mode Bit[1]: Format change multi frame update mode Bit[0]: Gain change multi frame update mode
0x401A	RST_TRIG_FN	0x08	RW	Bit[7:0]: Number of frames to update after reset trigger
0x401B	FMT_TRIG_FN	0x02	RW	Bit[7:0]: Number of frames to update after format trigger
0x401C	GAIN_TRIG_FN	0x02	RW	Bit[7:0]: Number of frames to update after gain trigger
0x401D	OFF_TRIG_FN	0x02	RW	Bit[7:0]: Number of frames to update after offset trigger (out of range)
0x401E	OFF_TRIG_TH_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Offset trigger (out of range) threshold[17:16]
0x401F	OFF_TRIG_TH_L	0x04	RW	Bit[7:0]: Offset Trigger (out of range) threshold[15:8]
0x4020	BLC_CTRL_5	0x18	RW	Bit[7]: Absolute offset limit (clips color aspect ratio) Bit[6]: zb_out_en Enable of zero banding pixels output Bit[5]: Reserved Bit[4]: Bypass 10 MSB or 10 LSB, applies to bypass_flag and blc_en = 0 Bit[3]: gain_trig_beh Bit[2]: format_trig_beh Bit[1]: cmp_mirror_man_en Enable manual horizontal order of k-coefficient and d-value (disable automatic order) Bit[0]: cmp_mirror_man Manual horizontal order (mirrored = 1) of k-coefficient and d-value

table A-2 sensor control registers (sheet 63 of 255)

address	register name	default value	R/W	description
0x4021	BLC_CTRL_6	0x05	RW	Bit[7:3]: Not used Bit[2]: vs_use_l_comp Very short exposure use long exposure d-value and k-coefficient Bit[1]: s_use_l_comp Short exposure use long exposure d-value and k-coefficient Bit[0]: m_use_l_comp Mid exposure use long exposure d-value and k-coefficient
0x4022	OFF_AVG_WEIGHT_A	0x30	RW	Bit[7:0]: Alpha value A for frame to frame EMWA-filter (format: 1.7)
0x4023	OFF_AVG_WEIGHT_B	0x10	RW	Bit[7:0]: Alpha value B for frame to frame EMWA-filter (format: 1.7)
0x4024	RND_GAIN_TH_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Analog gain threshold for dithering[9:8] (format: 6.4)
0x4025	RND_GAIN_TH_L	0x00	RW	Bit[7:0]: Analog gain threshold for dithering[7:0] (format: 6.4)
0x4026	BLK_LVL_TARGET_HCG_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Black level target for L expo
0x4027	BLK_LVL_TARGET_HCG_L	0x40	RW	Bit[7:0]: Black level target for L expo
0x4028	BLK_LVL_TARGET_LCG_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Black level target for M expo
0x4029	BLK_LVL_TARGET_LCG_L	0x40	RW	Bit[7:0]: Black level target for M expo
0x402A	BLK_LVL_TARGET_SPD_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Black level target for S expo
0x402B	BLK_LVL_TARGET_SPD_L	0x40	RW	Bit[7:0]: Black level target for S expo
0x402C	BLK_LVL_TARGET_VS_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Black level target for VS expo
0x402D	BLK_LVL_TARGET_VS_L	0x40	RW	Bit[7:0]: Black level target for VS expo
0x402E	D_VALUE_B_L	0x00	RW	Bit[7:0]: Offset compensation d-value for long exposure B pixels (format s3.4)
0x402F	D_VALUE_CB_HCG	0x00	RW	Bit[7:0]: Offset compensation d-value for long exposure Gb pixels (format s3.4)
0x4030	D_VALUE_CR_HCG	0x00	RW	Bit[7:0]: Offset compensation d-value for long exposure Gr pixels (format s3.4)

table A-2 sensor control registers (sheet 64 of 255)

address	register name	default value	R/W	description
0x4031	D_VALUE_R_HCG	0x00	RW	Bit[7:0]: Offset compensation d-value for long exposure R pixels (format s3.4)
0x4032	D_VALUE_B_SPD	0x00	RW	Bit[7:0]: Offset compensation d-value for short exposure B pixels (format s3.4)
0x4033	D_VALUE_CB_SPD	0x00	RW	Bit[7:0]: Offset compensation d-value for short exposure Gb pixels (format s3.4)
0x4034	D_VALUE_CR_SPD	0x00	RW	Bit[7:0]: Offset compensation d-value for short exposure Gr pixels (format s3.4)
0x4035	D_VALUE_R_SPD	0x00	RW	Bit[7:0]: Offset compensation d-value for short exposure R pixels (format s3.4)
0x4036	D_VALUE_B_LCG	0x00	RW	Bit[7:0]: Offset compensation d-value for Very Short exposure B pixels (format s3.4)
0x4037	D_VALUE_CB_LCG	0x00	RW	Bit[7:0]: Offset compensation d-value for mid exposure Gb pixels (format s3.4)
0x4038	D_VALUE_CR_LCG	0x00	RW	Bit[7:0]: Offset compensation d-value for mid exposure Gr pixels (format s3.4)
0x4039	D_VALUE_R_LCG	0x00	RW	Bit[7:0]: Offset compensation d-value for mid exposure R pixels (format s3.4)
0x403A	D_VALUE_B_VS	0x00	RW	Bit[7:0]: Offset compensation d-value for very short exposure B pixels (format s3.4)
0x403B	D_VALUE_CB_VS	0x00	RW	Bit[7:0]: Offset compensation d-value for very short exposure Gb pixels (format s3.4)
0x403C	D_VALUE_CR_VS	0x00	RW	Bit[7:0]: Offset compensation d-value for very short exposure Gr pixels (format s3.4)
0x403D	D_VALUE_R_VS	0x00	RW	Bit[7:0]: Offset compensation d-value for very short exposure R pixels (format s3.4)

table A-2 sensor control registers (sheet 65 of 255)

address	register name	default value	R/W	description
0x403E	KCOEF_B_HCGH	0x02	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_b_l Long exposure B channel k-coefficient (format 1.9)
0x403F	KCOEF_B_HCGL	0x00	RW	Bit[7:0]: Long exposure B channel k-coefficient
0x4040	KCOEF_CB_HCG_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Long exposure Gb channel k-coefficient (format 1.9)
0x4041	KCOEF_CB_HCG_L	0x00	RW	Bit[7:0]: Long exposure Gb channel k-coefficient
0x4042	KCOEF_CR_HCG_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Long exposure Gr channel k-coefficient (format 1.9)
0x4043	KCOEF_CR_HCG_L	0x00	RW	Bit[7:0]: Long exposure Gr channel k-coefficient
0x4044	KCOEF_R_HCG_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Long exposure R channel k-coefficient (format 1.9)
0x4045	KCOEF_R_HCG_L	0x00	RW	Bit[7:0]: Long exposure R channel k-coefficient
0x4046	KCOEF_B_SPD_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Short exposure B channel k-coefficient (format 1.9)
0x4047	KCOEF_B_SPD_L	0x00	RW	Bit[7:0]: Short exposure B channel k-coefficient
0x4048	KCOEF_CB_SPD_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Short exposure Gb channel k-coefficient (format 1.9)
0x4049	KCOEF_CB_SPD_L	0x00	RW	Bit[7:0]: Short exposure Gb channel k-coefficient
0x404A	KCOEF_CR_SPD_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Short exposure Gr channel k-coefficient (format 1.9)
0x404B	KCOEF_CR_SPD_L	0x00	RW	Bit[7:0]: Short exposure Gr channel k-coefficient
0x404C	KCOEF_R_SPD_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Short exposure R channel k-coefficient (format 1.9)

table A-2 sensor control registers (sheet 66 of 255)

address	register name	default value	R/W	description
0x404D	KCOEF_R_SPD_L	0x00	RW	Bit[7:0]: Short exposure R channel k-coefficient
0x404E	KCOEF_B_LCG_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Mid exposure B channel k-coefficient (format 1.9)
0x404F	KCOEF_B_LCG_L	0x00	RW	Bit[7:0]: Mid exposure B channel k-coefficient
0x4050	KCOEF_CB_LCG_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Mid exposure Gb channel k-coefficient (format 1.9)
0x4051	KCOEF_CB_LCG_L	0x00	RW	Bit[7:0]: Mid exposure Gb channel k-coefficient
0x4052	KCOEF_CR_LCG_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Midd exposure Gr channel k-coefficient (format 1.9)
0x4053	KCOEF_CR_LCG_L	0x00	RW	Bit[7:0]: Mid exposure Gr channel k-coefficient
0x4054	KCOEF_R_LCG_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Mid exposure R channel k-coefficient (format 1.9)
0x4055	KCOEF_R_LCG_L	0x00	RW	Bit[7:0]: Mid exposure R channel k-coefficient
0x4056	KCOEF_B_VS_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Very short exposure B channel k-coefficient (format 1.9)
0x4057	KCOEF_B_VS_L	0x00	RW	Bit[7:0]: Very short exposure B channel k-coefficient
0x4058	KCOEF_CB_VS_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Very short exposure Gb channel k-coefficient (format 1.9)
0x4059	KCOEF_CB_VS_L	0x00	RW	Bit[7:0]: Very short exposure Gb channel k-coefficient
0x405A	KCOEF_CR_VS_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Very short exposure Gr channel k-coefficient (format 1.9)
0x405B	KCOEF_CR_VS_L	0x00	RW	Bit[7:0]: Very short exposure Gr channel k-coefficient
0x405C	KCOEF_R_VS_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Very short exposure R channel k-coefficient (format 1.9)

table A-2 sensor control registers (sheet 67 of 255)

address	register name	default value	R/W	description
0x405D	KCOEF_R_VS_L	0x00	RW	Bit[7:0]: Very short exposure R channel k-coefficient
0x405E	OFF_MAN_B_HCGH	0x00	RW	Bit[7:4]: Not used Bit[3:0]: off_man_b_l Manual offset for L expo, B channel
0x405F	OFF_MAN_B_HCGL	0x00	RW	Bit[7:0]: Manual offset for L expo, B channel
0x4060	OFF_MAN_CB_HCG_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual offset for L expo, Gb channel
0x4061	OFF_MAN_CB_HCG_L	0x00	RW	Bit[7:0]: Manual offset for L expo, Gb channel
0x4062	OFF_MAN_CR_HCG_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual offset for L expo, Gr channel
0x4063	OFF_MAN_CR_HCG_L	0x00	RW	Bit[7:0]: Manual offset for L expo, Gr channel
0x4064	OFF_MAN_R_HCG_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual offset for L expo, R channel
0x4065	OFF_MAN_R_HCG_L	0x00	RW	Bit[7:0]: Manual offset for L expo, R channel
0x4066	OFF_MAN_B_LCG_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual offset for M expo, B channel
0x4067	OFF_MAN_B_LCG_L	0x00	RW	Bit[7:0]: Manual offset for M expo, B channel
0x4068	OFF_MAN_CB_LCG_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual offset for M expo, Gb channel
0x4069	OFF_MAN_CB_LCG_L	0x00	RW	Bit[7:0]: Manual offset for M expo, Gb channel
0x406A	OFF_MAN_CR_LCG_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual offset for M expo, Gr channel
0x406B	OFF_MAN_CR_LCG_L	0x00	RW	Bit[7:0]: Manual offset for M expo, Gr channel

table A-2 sensor control registers (sheet 68 of 255)

address	register name	default value	R/W	description
0x406C	OFF_MAN_R_LCG_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual offset for M expo, R channel
0x406D	OFF_MAN_R_LCG_L	0x00	RW	Bit[7:0]: Manual offset for M expo, R channel
0x406E	OFF_MAN_B_SPD_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual offset for S expo, B channel
0x406F	OFF_MAN_B_SPD_L	0x00	RW	Bit[7:0]: Manual offset for S expo, B channel
0x4070	OFF_MAN_CB_SPD_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual offset for S expo, Gb channel
0x4071	OFF_MAN_CB_SPD_L	0x00	RW	Bit[7:0]: Manual offset for S expo, Gb channel
0x4072	OFF_MAN_CR_SPD_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual offset for S expo, Gr channel
0x4073	OFF_MAN_CR_SPD_L	0x00	RW	Bit[7:0]: Manual offset for S expo, Gr channel
0x4074	OFF_MAN_R_SPD_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual offset for S expo, R channel
0x4075	OFF_MAN_R_SPD_L	0x00	RW	Bit[7:0]: Manual offset for S expo, R channel
0x4076	OFF_MAN_B_VS_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual offset for VS expo, B channel
0x4077	OFF_MAN_B_VS_L	0x00	RW	Bit[7:0]: Manual offset for VS expo, B channel
0x4078	OFF_MAN_CB_VS_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual offset for VS expo, Gb channel
0x4079	OFF_MAN_CB_VS_L	0x00	RW	Bit[7:0]: Manual offset for VS expo, Gb channel
0x407A	OFF_MAN_CR_VS_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual offset for VS expo, Gr channel
0x407B	OFF_MAN_CR_VS_L	0x00	RW	Bit[7:0]: Manual offset for VS expo, Gr channel

table A-2 sensor control registers (sheet 69 of 255)

address	register name	default value	R/W	description
0x407C	OFF_MAN_R_VS_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual offset for VS expo, R channel
0x407D	OFF_MAN_R_VS_L	0x00	RW	Bit[7:0]: Manual offset for VS expo, R channel
0x407E	FAULT_MASK_H	0xCC	RW	Pipe #0/1 Bit[7:6]: Row ID 0/1 Bit[5]: GR_off_err Bit[4]: GB_off_err Bit[3]: ZB_dig_B_err Bit[2]: ZB_dig_A_err Bit[1]: UDI_err Bit[0]: hwin_overrun_err
0x407F	FAULT_MASK_L	0x18	RW	Pipe #0/1 Bit[7:6]: row_acc_err Bit[5]: busy_err Bit[4:3]: zbc_calc_sm_l/m or s/vs Bit[2:1]: blc_calc_sm_l/m or s/vs Bit[0]: sel_err
0x4080	DIFF_THRES_H	0xFF	RW	Bit[7:0]: Channel diff threshold[15:8]
0x4081	DIFF_THRES_HCG	0xFF	RW	Bit[7:0]: Channel diff threshold[7:0]
0x4082	OFF_LIM_TH_M_H	0x03	RW	Bit[7:4]: Not used Bit[3:0]: Offset limit threshold M expo (absolute maximum offset)
0x4083	OFF_LIM_TH_M_L	0x6F	RW	Bit[7:0]: Offset limit threshold M expo (absolute maximum offset)
0x4084	OFF_LIM_TH_S_H	0x03	RW	Bit[7:4]: Not used Bit[3:0]: Offset limit threshold S expo (absolute maximum offset)
0x4085	OFF_LIM_TH_S_L	0x6F	RW	Bit[7:0]: Offset limit threshold S expo (absolute maximum offset)
0x4086	OFF_LIM_TH_VS_H	0x03	RW	Bit[7:4]: Not used Bit[3:0]: Offset limit threshold VS expo (absolute maximum offset)
0x4087	OFF_LIM_TH_VS_L	0x6F	RW	Bit[7:0]: Offset limit threshold VS expo (absolute maximum offset)
0x4088	BLC_OFFSET_B_HCGH	–	R	Bit[7:0]: blc_offset_b_l Calculated offset for L expo, B channel (format: 10.4)
0x4089	BLC_OFFSET_B_HCGL	–	R	Bit[7:0]: Calculated offset for L expo, B channel

table A-2 sensor control registers (sheet 70 of 255)

address	register name	default value	R/W	description
0x408A	BLC_OFFSET_CB_HCG_H	–	R	Bit[7:0]: Calculated offset for L expo, Gb channel (format: 10.4)
0x408B	BLC_OFFSET_CB_HCG_L	–	R	Bit[7:0]: Calculated offset for L expo, Gb channel
0x408C	BLC_OFFSET_CR_HCG_H	–	R	Bit[7:0]: Calculated offset for L expo, Gr channel (format: 10.4)
0x408E	BLC_OFFSET_CR_HCG_L	–	R	Bit[7:0]: Calculated offset for L expo, Gr channel
0x408F	BLC_OFFSET_R_HCG_H	–	R	Bit[7:0]: Calculated offset for L expo, R channel (format: 10.4)
0x4090	BLC_OFFSET_R_HCG_L	–	R	Bit[7:0]: Calculated offset for L expo, R channel
0x4091	BLC_OFFSET_B_LCG_H	–	R	Bit[7:0]: Calculated offset for M expo, B channel (format: 10.4)
0x4092	BLC_OFFSET_B_LCG_L	–	R	Bit[7:0]: Calculated offset for M expo, B channel
0x4093	BLC_OFFSET_CB_LCG_H	–	R	Bit[7:0]: Calculated offset for M expo, Gb channel (format: 10.4)
0x4094	BLC_OFFSET_CB_LCG_L	–	R	Bit[7:0]: Calculated offset for M expo, Gb channel
0x4095	BLC_OFFSET_CR_LCG_H	–	R	Bit[7:0]: Calculated offset for M expo, Gr channel (format: 10.4)
0x4096	BLC_OFFSET_CR_LCG_L	–	R	Bit[7:0]: Calculated offset for M expo, Gr channel
0x4097	BLC_OFFSET_R_LCG_H	–	R	Bit[7:0]: Calculated offset for M expo, R channel (format: 10.4)
0x4098	BLC_OFFSET_R_LCG_L	–	R	Bit[7:0]: Calculated offset for M expo, R channel
0x4099	BLC_OFFSET_B_SPD_H	–	R	Bit[7:0]: Calculated offset for S expo, B channel (format: 10.4)
0x409A	BLC_OFFSET_B_SPD_L	–	R	Bit[7:0]: Calculated offset for S expo, B channel
0x409B	BLC_OFFSET_CB_SPD_H	–	R	Bit[7:0]: Calculated offset for S expo, Gb channel (format: 10.4)
0x409C	BLC_OFFSET_CB_SPD_L	–	R	Bit[7:0]: Calculated offset for S expo, Gb channel
0x409D	BLC_OFFSET_CR_SPD_H	–	R	Bit[7:0]: Calculated offset for S expo, Gr channel (format: 10.4)

table A-2 sensor control registers (sheet 71 of 255)

address	register name	default value	R/W	description
0x409E	BLC_OFFSET_CR_SPD_L	–	R	Bit[7:0]: Calculated offset for S expo, Gr channel
0x409F	BLC_OFFSET_R_SPD_H	–	R	Bit[7:0]: Calculated offset for S expo, R channel (format: 10.4)
0x40A0	BLC_OFFSET_R_SPD_L	–	R	Bit[7:0]: Calculated offset for S expo, R channel
0x40A1	BLC_OFFSET_B_VS_H	–	R	Bit[7:0]: Calculated offset for VS expo, B channel (format: 10.4)
0x40A2	BLC_OFFSET_B_VS_L	–	R	Bit[7:0]: Calculated offset for VS expo, B channel
0x40A3	BLC_OFFSET_CB_VS_H	–	R	Bit[7:0]: Calculated offset for VS expo, Gb channel (format: 10.4)
0x40A4	BLC_OFFSET_CB_VS_L	–	R	Bit[7:0]: Calculated offset for VS expo, Gb channel
0x40A5	BLC_OFFSET_CR_VS_H	–	R	Bit[7:0]: Calculated offset for VS expo, Gr channel (format: 10.4)
0x40A6	BLC_OFFSET_CR_VS_L	–	R	Bit[7:0]: Calculated offset for VS expo, Gr channel
0x40A7	BLC_OFFSET_R_VS_H	–	R	Bit[7:0]: Calculated offset for VS expo, R channel (format: 10.4)
0x40A8	BLC_OFFSET_R_VS_L	–	R	Bit[7:0]: Calculated offset for VS expo, R channel
0x40A9	COMP_DC_B_HCGH	–	R	Bit[7:6]: Not used Bit[5:0]: Compensated dark current for L expo, B channel (format: 10.4)
0x40AA	COMP_DC_B_HCGL	–	R	Bit[7:0]: Compensated dark current for L expo, B channel
0x40AB	COMP_DC_CB_HCG_H	–	R	Bit[7:6]: Not used Bit[5:0]: Compensated dark current for L expo, Gb channel (format: 10.4)
0x40AC	COMP_DC_CB_HCG_L	–	R	Bit[7:0]: Compensated dark current for L expo, Gb channel
0x40AD	COMP_DC_CR_HCG_H	–	R	Bit[7:6]: Not used Bit[5:0]: Compensated dark current for L expo, Gr channel (format: 10.4)
0x40AE	COMP_DC_CR_HCG_L	–	R	Bit[7:0]: Compensated dark current for L expo, Gr channel

table A-2 sensor control registers (sheet 72 of 255)

address	register name	default value	R/W	description
0x40AF	COMP_DC_R_HCG_H	–	R	Bit[7:6]: Not used Bit[5:0]: Compensated dark current for L expo, R channel (format: 10.4)
0x40B0	COMP_DC_R_HCG_L	–	R	Bit[7:0]: Compensated dark current for L expo, R channel
0x40B1	COMP_DC_B_LCG_H	–	R	Bit[7:6]: Not used Bit[5:0]: Compensated dark current for M expo, B channel (format: 10.4)
0x40B2	COMP_DC_B_LCG_L	–	R	Bit[7:0]: Compensated dark current for M expo, B channel
0x40B3	COMP_DC_CB_LCG_H	–	R	Bit[7:6]: Not used Bit[5:0]: Compensated dark current for M expo, Gb channel (format: 10.4)
0x40B4	COMP_DC_CB_LCG_L	–	R	Bit[7:0]: Compensated dark current for M expo, Gb channel
0x40B5	COMP_DC_CR_LCG_H	–	R	Bit[7:6]: Not used Bit[5:0]: Compensated dark current for M expo, Gr channel (format: 10.4)
0x40B6	COMP_DC_CR_LCG_L	–	R	Bit[7:0]: Compensated dark current for M expo, Gr channel
0x40B7	COMP_DC_R_LCG_H	–	R	Bit[7:6]: Not used Bit[5:0]: Compensated dark current for M expo, R channel (format: 10.4)
0x40B8	COMP_DC_R_LCG_L	–	R	Bit[7:0]: Compensated dark current for M expo, R channel
0x40B9	COMP_DC_B_SPD_H	–	R	Bit[7:6]: Not used Bit[5:0]: Compensated dark current for S expo, B channel (format: 10.4)
0x40BA	COMP_DC_B_SPD_L	–	R	Bit[7:0]: Compensated dark current for S expo, B channel
0x40BB	COMP_DC_CB_SPD_H	–	R	Bit[7:6]: Not used Bit[5:0]: Compensated dark current for S expo, Gb channel (format: 10.4)
0x40BC	COMP_DC_CB_SPD_L	–	R	Bit[7:0]: Compensated dark current for S expo, Gb channel
0x40BD	COMP_DC_CR_SPD_H	–	R	Bit[7:6]: Not used Bit[5:0]: Compensated dark current for S expo, Gr channel (format: 10.4)
0x40BE	COMP_DC_CR_SPD_L	–	R	Bit[7:0]: Compensated dark current for S expo, Gr channel

table A-2 sensor control registers (sheet 73 of 255)

address	register name	default value	R/W	description
0x40BF	COMP_DC_R_SPD_H	–	R	Bit[7:6]: Not used Bit[5:0]: Compensated dark current for S expo, R channel (format: 10.4)
0x40C0	COMP_DC_R_SPD_L	–	R	Bit[7:0]: Compensated dark current for S expo, R channel
0x40C1	COMP_DC_B_VS_H	–	R	Bit[7:6]: Not used Bit[5:0]: Compensated dark current for VS expo, B channel (format: 10.4)
0x40C2	COMP_DC_B_VS_L	–	R	Bit[7:0]: Compensated dark current for VS expo, B channel
0x40C3	COMP_DC_CB_VS_H	–	R	Bit[7:6]: Not used Bit[5:0]: Compensated dark current for VS expo, Gb channel (format: 10.4)
0x40C4	COMP_DC_CB_VS_L	–	R	Bit[7:0]: Compensated dark current for VS expo, Gb channel
0x40C5	COMP_DC_CR_VS_H	–	R	Bit[7:6]: Not used Bit[5:0]: Compensated dark current for VS expo, Gr channel (format: 10.4)
0x40C6	COMP_DC_CR_VS_L	–	R	Bit[7:0]: Compensated dark current for VS expo, Gr channel
0x40C7	COMP_DC_R_VS_H	–	R	Bit[7:6]: Not used Bit[5:0]: Compensated dark current for VS expo, R channel (format: 10.4)
0x40C8	COMP_DC_R_VS_L	–	R	Bit[7:0]: Compensated dark current for VS expo, R channel
0x40C9	THRES_HCG_H	–	R	Bit[7:6]: Not used Bit[5:0]: Accumulator black level threshold used for L[13:8]
0x40CA	THRES_HCG_L	–	R	Bit[7:0]: Accumulator black level threshold used for L[7:0]
0x40CB	THRES_LCG_H	–	R	Bit[7:6]: Not used Bit[5:0]: Accumulator black level threshold used for M[13:8]
0x40CC	THRES_LCG_L	–	R	Bit[7:0]: Accumulator black level threshold used for M[7:0]
0x40CD	THRES_SPD_H	–	R	Bit[7:6]: Not used Bit[5:0]: Accumulator black level threshold used for S[13:8]
0x40CE	THRES_SPD_L	–	R	Bit[7:0]: Accumulator black level threshold used for S[7:0]

table A-2 sensor control registers (sheet 74 of 255)

address	register name	default value	R/W	description
0x40CF	THRES_VS_H	–	R	Bit[7:6]: Not used Bit[5:0]: Accumulator black level threshold used for Vs[13:8]
0x40D0	THRES_VS_L	–	R	Bit[7:0]: Accumulator black level threshold used for VS[7:0]
0x40D1	ZB_OFFSET_HCG_H	–	R	Bit[7:0]: Zero banding level in black rows used for long exposure[15:8]
0x40D2	ZB_OFFSET_HCG_L	–	R	Bit[7:0]: Zero banding level in black rows used for long exposure[7:0]
0x40D3	ZB_OFFSET_LCG_H	–	R	Bit[7:0]: Zero banding level in black rows used for mid exposure[15:8]
0x40D4	ZB_OFFSET_LCG_L	–	R	Bit[7:0]: Zero banding level in black rows used for mid exposure[7:0]
0x40D5	ZB_OFFSET_SPD_H	–	R	Bit[7:0]: Zero banding level in black rows used for short exposure[15:8]
0x40D6	ZB_OFFSET_SPD_L	–	R	Bit[7:0]: Zero banding level in black rows used for short exposure[7:0]
0x40D7	ZB_OFFSET_VS_H	–	R	Bit[7:0]: Zero banding level in black rows used for very short exposure[15:8]
0x40D8	ZB_OFFSET_VS_L	–	R	Bit[7:0]: Zero banding level in black rows used for very short exposure[7:0]
0x40D9	FAULT_PIPE_0_H	–	R	Pipe #0 Bit[7:6]: Not used Bit[5]: GR_off_err Bit[4]: GB_off_err Bit[3]: ZB_dig_B_err Bit[2]: ZB_dig_A_err Bit[1]: UDI_err Bit[0]: hwin_overrun_err
0x40DA	FAULT_PIPE_0_L	–	R	Pipe #0: Bit[7:6]: row_acc_err Bit[5]: busy_err Bit[4:3]: zbc_calc_sm_l/m or s/vs Bit[2:1]: blc_calc_sm_l/m or s/vs Bit[0]: sel_err

table A-2 sensor control registers (sheet 75 of 255)

address	register name	default value	R/W	description
0x40DB	FAULT_PIPE_1_H	–	R	Pipe #1: Bit[7:6]: Not used Bit[5]: GR_off_err Bit[4]: GB_off_err Bit[3]: ZB_dig_B_err Bit[2]: ZB_dig_A_err Bit[1]: UDI_err Bit[0]: hwin_overrun_err
0x40DC	FAULT_PIPE_1_L	–	R	Pipe #1 Bit[7:6]: row_acc_err Bit[5]: busy_err Bit[4:3]: zbc_calc_sm_l/m or s/vs Bit[2:1]: blc_calc_sm_l/m or s/vs Bit[0]: sel_err
0x40DD	FAULT_LATCH_PIPE_0_H	–	R	Pipe #0 Bit[7:6]: Not used Bit[5]: GR_off_err Bit[4]: GB_off_err Bit[3]: ZB_dig_B_err Bit[2]: ZB_dig_A_err Bit[1]: UDI_err Bit[0]: hwin_overrun_err
0x40DE	FAULT_LATCH_PIPE_0_L	–	R	Pipe #0 Bit[7:6]: row_acc_err Bit[5]: busy_err Bit[4:3]: zbc_calc_sm_l/m or s/vs Bit[2:1]: blc_calc_sm_l/m or s/vs Bit[0]: sel_err
0x40DF	FAULT_LATCH_PIPE_1_H	–	R	Pipe #1 Bit[7:6]: Not used Bit[5]: GR_off_err Bit[4]: GB_off_err Bit[3]: ZB_dig_B_err Bit[2]: ZB_dig_A_err Bit[1]: UDI_err Bit[0]: hwin_overrun_err
0x40E0	FAULT_LATCH_PIPE_1_L	–	R	Pipe #1 Bit[7:6]: row_acc_err Bit[5]: busy_err Bit[4:3]: zbc_calc_sm_l/m or s/vs Bit[2:1]: blc_calc_sm_l/m or s/vs Bit[0]: sel_err
0x40E1	STATUS	–	R	Bit[7:2]: Not used Bit[1:0]: State machine state 0: Reset latch 1: Error latch

table A-2 sensor control registers (sheet 76 of 255)

address	register name	default value	R/W	description
0x4200	DTR_B_OFFS	0x00	RW	Bit[7:2]: Not used Bit[1:0]: B channel offset[9:8]
0x4201	DTR_B_OFFS_1	0x00	RW	Bit[7:0]: B channel offset[7:0]
0x4202	DTR_CB_OFFS	0x00	RW	Bit[7:2]: Not used Bit[1:0]: GB channel offset[9:8]
0x4203	DTR_CB_OFFS_3	0x00	RW	Bit[7:0]: GB channel offset[7:0]
0x4204	DTR_R_OFFS	0x00	RW	Bit[7:2]: Not used Bit[1:0]: R channel offset[9:8]
0x4205	DTR_R_OFFS_5	0x00	RW	Bit[7:0]: R channel offset[7:0]
0x4206	DTR_CR_OFFS	0x00	RW	Bit[7:2]: Not used Bit[1:0]: GR channel offset[9:8]
0x4207	DTR_CR_OFFS_7	0x00	RW	Bit[7:0]: GR channel offset[7:0]
0x4208	DTR_COLOR_CONFIG	0x00	RW	Bit[7]: B counter shift (1 means 2x) Bit[6]: Gb counter shift (1 means 2x) Bit[5]: R counter shift (1 means 2x) Bit[4]: Gr counter shift (1 means 2x) Bit[3]: B counter direction (0 means up) Bit[2]: Gb counter direction (0 means up) Bit[1]: R counter direction (0 means up) Bit[0]: Gr counter direction (0 means up)
0x4209	REGION1_OFFSET	0x00	RW	Bit[7:0]: Additional offset in row region 1
0x420A	REGION2_OFFSET	0x00	RW	Bit[7:0]: Additional offset in row region 2
0x420B	REGION3_OFFSET	0x00	RW	Bit[7:0]: Additional offset in row region 3
0x420C	REGION_CONFIG	0x00	RW	Bit[7:4]: region_direction_inv Invert direction in region Bit[3:0]: region_shift_inv Change shift in region
0x420D	ROW_OFFSET	0x00	RW	Bit[7:0]: Additional offset added every second row (applied to full 12-bit value)
0x420E	DTR_CRC_REF_A	0xFF	RW	Bit[7:0]: Digital test row CRC reference value (a)
0x420F	DTR_CRC_REF_A_F	0xFF	RW	Bit[7:0]: Digital test row CRC reference value (a)
0x4210	DTR_CRC_REF_A_10	0xFF	RW	Bit[7:0]: Digital test row CRC reference value (a)
0x4211	DTR_CRC_REF_A_11	0xFF	RW	Bit[7:0]: Digital test row CRC reference value (a)

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address	register name	default value	R/W	description
0x4212	DTR_CRC_REF_B	0xFF	RW	Bit[7:0]: Digital test row CRC reference value (b)
0x4213	DTR_CRC_REF_B_13	0xFF	RW	Bit[7:0]: Digital test row CRC reference value (b)
0x4214	DTR_CRC_REF_B_14	0xFF	RW	Bit[7:0]: Digital test row CRC reference value (b)
0x4215	DTR_CRC_REF_B_15	0xFF	RW	Bit[7:0]: Digital test row CRC reference value (b)
0x4216	DTR_WHITE_PIX_CONF	0xFF	RW	Bit[7]: Enable white pixel generation Bit[6:0]: white_pix_val MSBs of white pixels (LSBs are all 1)
0x4217	DTR_BLACK_PIX_CONF	0x80	RW	Bit[7]: Enable black pixel generation Bit[6:0]: black_pix_val MSBs of black pixels (LSBs are all 0)
0x4218	DTR_BLC_OFFS_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Zero point of BLC Output data will have this as lower value (row offset applied on top of this)
0x4219	DTR_BLC_OFFS_L	0x00	RW	Bit[7:0]: Zero point of BLC Output data will have this as lower value (row offset applied on top of this)
0x421A	DTR_CRC_CALC	–	R	Bit[7:0]: dig_test_row_crc_cal Digital test row CRC
0x421B	DTR_CRC_CALC_1B	–	R	Bit[7:0]: dig_test_row_crc_cal Digital test row CRC
0x421C	DTR_CRC_CALC_1C	–	R	Bit[7:0]: dig_test_row_crc_cal Digital test row CRC
0x421D	DTR_CRC_CALC_1D	–	R	Bit[7:0]: dig_test_row_crc_cal Digital test row CRC
0x421E	DTR_FAULT_MASK	0x02	RW	Bit[7]: parallel_gain_test_cal_err_mask_26 Bit[6]: dpc_test_cal_err_mask_25 Bit[5]: scip_test_err_mask_24 Bit[4]: dpc_test_err_mask_23 Bit[3]: otp_test_err_mask_22 Bit[2]: awbg_test_err_mask_21 Bit[1]: pre_isp_test_err_mask_20 Bit[0]: stat_test_crc_err_mask_17

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address	register name	default value	R/W	description
0x421F	DTR_FAULT_MASK_1F	0x75	RW	Bit[7]: single_gain_test_cal_err_mask_16 Bit[6]: awb_revs_test_cal_err_mask_15 Bit[5]: pwl_test_cal_err_mask_14 Bit[4]: lfm_test_cal_err_mask_13 Bit[3]: combine_test_cal_err_mask_12 Bit[2]: lenc_test_cal_err_mask_11 Bit[1]: retiming_mem_crc_err0_mask_9 Bit[0]: post_bin_mem_crc_err0_mask_8
0x4220	DTR_FAULT_MASK_20	0xE1	RW	Bit[7]: retiming_mem_crc_err1_mask_7 Bit[6]: post_bin_mem_crc_err1_mask_6 Bit[5]: lfm_mem_crc_err_mask_5 Bit[4]: scip_mem_crc_err_mask_4 Bit[3]: d2v2tov2_mem_crc_err_mask_3 Bit[2]: dpc_mem_crc_err_mask_2 Bit[1]: sync_buff_crc_err_i_mask_1 Bit[0]: Reserved
0x4221	DTR_FAULT_MASK_21	0x05	RW	Bit[7]: dpc_err_flag_o_mask Bit[6]: dig_test_row_crc_fault_a_mask Digital test row a CRC fault mask Bit[5]: dig_test_row_crc_fault_b_lcgask Digital test row b CRC fault mask Bit[4]: dtr_fault_flags_mask_reserved_bit4 Bit[3]: dtr_fault_flags_mask_reserved_bit3 Bit[2]: prematrix_test_cal_err_mask_19 Bit[1]: xtc_test_cal_err_mask_18 Bit[0]: sc_mem_crc_err_mask_10
0x4222	DTR_FAULT_LATCH	–	R	Bit[7]: parallel_gain_test_cal_err_latch_26 Bit[6]: dpc_test_cal_err_latch_25 Bit[5]: scip_test_err_latch_24 Bit[4]: dpc_test_err_latch_23 Bit[3]: otp_test_err_latch_22 Bit[2]: awbg_test_err_latch_21 Bit[1]: pre_isp_test_err_latch_20 Bit[0]: stat_test_crc_err_latch_17
0x4223	DTR_FAULT_LATCH_23	–	R	Bit[7]: single_gain_test_cal_err_latch_16 Bit[6]: awb_revs_test_cal_err_latch_15 Bit[5]: pwl_test_cal_err_latch_14 Bit[4]: lfm_test_cal_err_latch_13 Bit[3]: combine_test_cal_err_latch_12 Bit[2]: lenc_test_cal_err_latch_11 Bit[1]: retiming_mem_crc_err0_latch_9 Bit[0]: post_bin_mem_crc_err0_latch_8

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address	register name	default value	R/W	description
0x4224	DTR_FAULT_LATCH_24	–	R	Bit[7]: retiming_mem_crc_err1_latch_7 Bit[6]: post_bin_mem_crc_err1_latch_6 Bit[5]: lfm_mem_crc_err_latch_5 Bit[4]: scip_mem_crc_err_latch_4 Bit[3]: d2v2tov2_mem_crc_err_latch_3 Bit[2]: dpc_mem_crc_err_latch_2 Bit[1]: sync_buff_crc_err_i_latch_1 Bit[0]: Reserved
0x4225	DTR_FAULT_LATCH_25	–	R	Bit[7]: dpc_err_flag_o_latch Bit[6]: dig_test_row_crc_fault_a_latch Digital test row a CRC fault latched Bit[5]: dig_test_row_crc_fault_b_latch Digital test row b CRC fault latched Bit[4]: dtr_fault_flags_latch_ reserved_bit4 Bit[3]: dtr_fault_flags_latch_ reserved_bit3 Bit[2]: prematrix_test_cal_err_latch_19 Bit[1]: xtc_test_cal_err_latch_18 Bit[0]: sc_mem_crc_err_latch_10
0x4226	DTR_FAULT_FLAGS	–	R	Bit[7]: parallel_gain_test_cal_err_26 Bit[6]: dpc_test_cal_err_25 Bit[5]: scip_test_err_24 Bit[4]: dpc_test_err_23 Bit[3]: otp_test_err_22 Bit[2]: awbg_test_err_21 Bit[1]: pre_isp_test_err_20 Bit[0]: stat_test_crc_err_17
0x4227	DTR_FAULT_FLAGS_27	–	R	Bit[7]: single_gain_test_cal_err_16 Bit[6]: awb_revs_test_cal_err_15 Bit[5]: pwl_test_cal_err_14 Bit[4]: lfm_test_cal_err_13 Bit[3]: combine_test_cal_err_12 Bit[2]: lenc_test_cal_err_11 Bit[1]: retiming_mem_crc_err0_9 Bit[0]: post_bin_mem_crc_err0_8
0x4228	DTR_FAULT_FLAGS_28	–	R	Bit[7]: retiming_mem_crc_err1_7 Bit[6]: post_bin_mem_crc_err1_6 Bit[5]: lfm_mem_crc_err_5 Bit[4]: scip_mem_crc_err_4 Bit[3]: d2v2tov2_mem_crc_err_3 Bit[2]: dpc_mem_crc_err_2 Bit[1]: sync_buff_crc_err_i_1 Bit[0]: Reserved

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address	register name	default value	R/W	description
0x4229	DTR_FAULT_FLAGS_29	–	R	Bit[7]: dpc_err_flag_o Bit[6]: dig_test_row_crc_fault_a Digital test row a CRC fault Bit[5]: dig_test_row_crc_fault_b Digital test row b CRC fault Bit[4]: dtr_fault_flags_reserved_bit4 Bit[3]: dtr_fault_flags_reserved_bit3 Bit[2]: prematrix_test_cal_err_19 Bit[1]: xtc_test_cal_err_18 Bit[0]: sc_mem_crc_err_10
0x422A	DTR_STATE	–	R	Bit[7:1]: Not used Bit[0]: dig_test_row_fault_state
0x4300	TESTMODE_BIT_SWAP_CTRL	0x00	RW	Bit[7:6]: reserved_7_6 Bit[5:3]: Bit swap control 0x1: Complete bit reversal (0:23) 0x2: 10-bit data reverse (9:0 23:10) 0x3: 8-bit data reverse (7:0 23:8), otherwise no bit swap Bit[2:0]: reserved_2_1_0
0x4301	TESTMODE_CLIP_MAX_HI	0x0F	RW	Bit[7:0]: Clipping max value[23:16]
0x4302	TESTMODE_CLIP_MAX_MID	0xFF	RW	Bit[7:0]: Clipping max value[15:8]
0x4303	TESTMODE_CLIP_MAX_LO	0xFF	RW	Bit[7:0]: Clipping max value[7:0]
0x4304	TESTMODE_CLIP_MIN_HI	0x00	RW	Bit[7:0]: Clipping min value[23:16]
0x4305	TESTMODE_CLIP_MIN_MID	0x00	RW	Bit[7:0]: Clipping min value[15:8]
0x4306	TESTMODE_CLIP_MIN_LO	0x00	RW	Bit[7:0]: Clipping min value[7:0]
0x4307	FORMAT_REG	0x03	RW	Bit[7:2]: Not used Bit[1:0]: emb_trigger_sync Select SOF to trigger embedded reading

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address	register name	default value	R/W	description
0x4308	FORMAT_REG_8	0x13	RW	Bit[7]: mipi_dummy_out_dis Block dummy at MIPI output Bit[6]: dummy_out_en Enable dummy line output from MIPI Bit[5]: win_dummy_seof_en SOF/EOF selection for dummy channel 0: From timing control 1: From window Bit[4]: late_eof_en Use EOF at end of col-ID rows even if not output Bit[3:2]: Not used Bit[1]: rip_sof_ispfc_en Ispfc SOF select Bit[0]: rip_sof_vfifo_en Vfifo SOF select
0x4309	FORMAT_REG_9	0x00	RW	Bit[7]: fm_ch_man_en Manual enable channels Bit[6:4]: Not used Bit[3]: fm_vs_ch_en Manual enable VS channel Bit[2]: fm_s_ch_en Manual enable S channel Bit[1]: fm_m_ch_en Manual enable M channel Bit[0]: fm_l_ch_en Manual enable L channel
0x430A	FORMAT_REG_A	0xF3	RW	Bit[7]: vfifo_vs_ch_en Enable data into vfifo for VS channel Bit[6]: vfifo_s_ch_en Enable data into vfifo for S channel Bit[5]: vfifo_m_ch_en Enable data into vfifo for M channel Bit[4]: vfifo_l_ch_en Enable data into vfifo for L channel Bit[3]: Reserved Bit[2]: novch_en New stagger HDR enable Bit[1]: isp_expo_sh 0: Feed only coarse exposure to ISP 1: Feed 15 bits coarse and one bit fine exposure to ISP Bit[0]: vc_align_en Stagger HDR align enable

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address	register name	default value	R/W	description
0x430B	FORMAT_REG_B	0x00	RW	Bit[7:4]: Not used Bit[3]: Bit shift and clip enable Bit[2:0]: bit_shift_mode 0x1: Shift 1 bit 0x2: Shift 2 bits 0x3: Shift 3 bits
0x430C	FORMAT_REG_C	0x00	RW	Bit[7]: Fix timing enable Bit[6]: Not used Bit[5]: Fix timing SOF reset Bit[4:0]: Sof2ready adjust
0x430D	FORMAT_REG_D	0x13	RW	Bit[7]: MIPI data type same as image Bit[6]: Embedded data LSB first Bit[5:0]: emb_top_dt Top embedded data type
0x430E	FORMAT_REG_E	0x94	RW	Bit[7:6]: Not used Bit[5:0]: emb_bottom_dt Bottom embedded data type
0x430F	FORMAT_REG_F	0x57	RW	Bit[7]: Digital test row output enable Bit[6]: Statistic row output enable Bit[5:0]: mipi_stat_row_dt Statistic row data type
0x4310	FORMAT_REG_10	0x95	RW	Bit[7]: rip_eof_ispfc_en Ispfc EOF select Bit[6]: Analog test row output enable Bit[5:0]: mipi_ana_test_row_dt Analog test row data type
0x4311	FORMAT_REG_11	0x16	RW	Bit[7]: Row id output enable Bit[6]: colid_row_out Column ID output enable Bit[5:0]: mipi_colid_row_dt Column ID data type
0x4312	FORMAT_REG_12	0x00	RW	Bit[7:0]: hts_pclk[15:8]
0x4313	FORMAT_REG_13	0x00	RW	Bit[7:0]: hts_pclk[7:0]
0x4314	FORMAT_REG_14	0x00	RW	Bit[7:0]: y_output_size_man[15:8] Y output size high byte
0x4315	FORMAT_REG_15	0x00	RW	Bit[7:0]: y_output_size_man[7:0] Y output size low byte
0x4316	FORMAT_REG_16	0x00	RW	Bit[7]: Not used Bit[6:4]: ISP work mode Bit[3:1]: Not used Bit[0]: hdr_vsize_man_en HDR vsize select

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address	register name	default value	R/W	description
0x4317	FORMAT_REG_17	0x38	RW	Bit[7:6]: Not used Bit[5]: Front embedded row enable Bit[4]: End embedded row enable Bit[3]: emb_end_on_first Send end embedded lines on first frame instead of last Bit[2:0]: Not used
0x4318	FORMAT_REG_18	0x12	RW	Bit[7:6]: Not used Bit[5:0]: mipi_dig_test_row_dt Digital test row data type
0x4319	FORMAT_REG_19	0x00	RW	Bit[7]: mipi_bitw_force1 Force vfifo/MIPI bitwidth for other group1 Bit[6]: mipi_bitw_force0 Force vfifo/MIPI bitwidth for other group1 Bit[5]: Not used Bit[4]: spd_out_en Enable outputting separate SPD channel Bit[3]: lfm_bit_out_en Enable outputting LFM bit on SPD channel Bit[2]: Reserved Bit[1]: spd_in_comb_en Use SPD in combine Bit[0]: hdr_combine_en Enable DCG combine
0x431A	FORMAT_REG_1A	0x00	RW	Bit[7:4]: mipi_bitw_man1 0x0: 8 bits 0x1: 10 bits 0x2: 12 bits 0x3: 14 bits 0x4: 16 bits 0x5: 20 bits 0x8~0x11: 24 bits Bit[3:0]: mipi_bitw_man0 0x0: 8 bits 0x1: 10 bits 0x2: 12 bits 0x3: 14 bits 0x4: 16 bits 0x5: 20 bits 0x8~0x11:24 bits

table A-2 sensor control registers (sheet 84 of 255)

address	register name	default value	R/W	description
0x431B	FORMAT_REG_1B	0x00	RW	Bit[7:4]: mipi_format_group_sel Each bit selects format group for one MIPI channel Bit[3:0]: vfifo_format_group_sel Each bit selects format group for one vfifo channel
0x431C	FORMAT_REG_1C	0x2A	RW	Bit[7]: Not used Bit[6]: mipi_imgdt_force0 Force MIPI image data type (see r_mipi_imgdt_man) Bit[5:0]: mipi_imgdt_man0 Image data type if manually selected
0x431D	FORMAT_REG_1D	0x2A	RW	Bit[7]: Not used Bit[6]: mipi_imgdt_force1 Force MIPI image data type (see r_mipi_imgdt_man) Bit[5:0]: mipi_imgdt_man1 Image data type if manually selected
0x431E	FORMAT_REG_1E	0x11	RW	Bit[7]: Not used Bit[6]: Dummy data type enable Bit[5:0]: Dummy data type
0x431F	FORMAT_REG_1F	0x00	RW	Bit[7:6]: pack24bit_sel Select one of 4 packing options for 24 bit format Bit[5]: pwl0_en Enable PWL for first channel Bit[4:3]: pwl0_bits PWL mode (12/14/16/20) for first channel Bit[2]: pwl1_en Enable PWL for second channel Bit[1:0]: pwl1_bits PWL mode (12/14/16/20) for second channel

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address	register name	default value	R/W	description
0x4320	FORMAT_REG_20	0x19	RW	Bit[7]: pack24_mipi8_eco eco_sl0b Fix 24b packing in RAW8 mode Bit[6]: x_size0_switch_en_eco eco_sl0b Fix bz382 Bit[5]: emb_dmy_masked_eco eco_sl0b Fix bz361 Bit[4]: x_size_latch_en_eco eco_sl0c Fix bz473, latch size information for vfifo and MIPI_TX Bit[3]: x_size_shift_en_eco eco_sl0c Fix bz473, shift size information from vfifo to MIPI_TX Bit[2]: Not used Bit[1:0]: lfm_channel_sel Select channel for LFM bit
0x4321	Y_VS_OFFS_H	–	R	Bit[7:0]: VS staggered offset in rows
0x4322	Y_VS_OFFS_L	–	R	Bit[7:0]: VS staggered offset in rows
0x4323	DTR_CRC_CALC_FM	0x80	RW	Bit[7:4]: dtr_mask Mask bits for L M S VS channels Bit[3:2]: dtr_end Last channel for digital test row calculation Bit[1:0]: Not used
0x4324	FORMAT_MISC_CTRL	0x00	RW	Bit[7:3]: Not used Bit[2]: Enable watchdog fault insertion on column UID rows (last 2x2 pixel) Bit[1]: Reserved Bit[0]: mipi_dvp_select Enable DVP and disable MIPI
0x4500~ 0x4511	RSVD	–	–	Reserved
0x4580	R_VM_CTRL0	0xF8	RW	Bit[7:4]: Div Ratio of p_clk to vm_clk Bit[3:1]: cnt_bit Nr of clock, in multiple of 512 in each sampling period Bit[0]: clk_re Revert vm_clk

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address	register name	default value	R/W	description
0x4581	R_VM_CTRL1	0xE7	RW	Bit[7]: tester_enable Bit[6:5]: tester_thresh Maximum acceptable difference in tester Bit[4:3]: Not used Bit[2]: snr_2_en Bit[1]: snr_1_en Bit[0]: snr_0_en
0x4582	R_VM_CTRL2	0x00	RW	Bit[7:5]: Not used Bit[4:3]: vm_cp_check_sel 00: Always in stream 01: During active frames 10: At SOF 11: At EOF Bit[2:0]: Not used
0x4583	R_VOL_0_MIN	0x00	RW	Bit[7:4]: Not used Bit[3:0]: vol_0_min
0x4584	R_VOL_0_MIN_4	0x00	RW	Bit[7:0]: Voltage 0 date lower bound
0x4585	R_VOL_0_MAX	0x0F	RW	Bit[7:4]: Not used Bit[3:0]: vol_0_max
0x4586	R_VOL_0_MAX_6	0xFF	RW	Bit[7:0]: Voltage 0 date higher bound
0x4587	R_VOL_1_MIN	0x00	RW	Bit[7:4]: Not used Bit[3:0]: vol_1_min
0x4588	R_VOL_1_MIN_8	0x00	RW	Bit[7:0]: Voltage 1 date lower bound
0x4589	R_VOL_1_MAX	0x0F	RW	Bit[7:4]: Not used Bit[3:0]: vol_1_max
0x458A	R_VOL_1_MAX_A	0xFF	RW	Bit[7:0]: Voltage 1 date higher bound
0x458B	R_VOL_2_MIN	0x00	RW	Bit[7:4]: Not used Bit[3:0]: vol_2_min
0x458C	R_VOL_2_MIN_C	0x00	RW	Bit[7:0]: Voltage 2 date lower bound
0x458D	R_VOL_2_MAX	0x0F	RW	Bit[7:4]: Not used Bit[3:0]: vol_2_max
0x458E	R_VOL_2_MAX_E	0xFF	RW	Bit[7:0]: Voltage 2 date higher bound
0x458F	R_TEST_CYCLE_H	0x00	RW	Bit[7:0]: Test cycle[15:8]
0x4590	R_TEST_CYCLE_L	0x20	RW	Bit[7:0]: Test cycle[7:0]
0x4591	R_CLK_MUSK_NUM	0x09	RW	Bit[7:4]: Not used Bit[3:0]: clk_musk_num
0x4592	R_CLK_MUSK_NUM_12	0x60	RW	Bit[7:0]: clk_musk_num

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address	register name	default value	R/W	description
0x4593	R_VM_ANALOG_ CONTROL_REG	0x18	RW	Bit[7:0]: vm_analog_control_reg
0x4594	R_STOP_UPDATE_VM	0x00	RW	Bit[7:1]: Not used Bit[0]: stop_update
0x4597	VOLTAGE_MONITOR_ FAULT_MASK	0x00	RW	Bit[7:6]: Not used Bit[5:3]: Voltage monitor BIST fault masks Bit[2:0]: vm_alarm_fault_mask Voltage monitor fault masks (out of range voltage)
0x4598	VM_CP_FAULT_MASK	0x00	RW	Bit[7:4]: vm_cp_startup_fault_mask Voltage monitor charge pump comparator fault masks (startup checks) Bit[3:0]: Voltage monitor charge pump comparator fault masks
0x4599	NP1_THR_REG	0x0F	RW	Bit[7:4]: vm_np1_thr_start Startup check threshold for NP1 Bit[3:0]: vm_np1_thr_func Functional threshold for NP1
0x459A	NP2_THR_REG	0x0F	RW	Bit[7:4]: vm_np2_thr_start Startup check threshold for NP2 Bit[3:0]: vm_np2_thr_func Functional threshold for NP2
0x459B	PP1_THR_REG	0xF0	RW	Bit[7:4]: vm_pp1_thr_start Startup check threshold for PP1 Bit[3:0]: vm_pp1_thr_func Functional threshold for PP1
0x459C	PP2_THR_REG	0xF0	RW	Bit[7:4]: vm_pp2_thr_start Startup check threshold for PP2 Bit[3:0]: vm_pp2_thr_func Functional threshold for PP2
0x45A0	R_VOL_0_RESULT	–	R	Bit[7:4]: Not used Bit[3:0]: vol_0_result
0x45A1	R_VOL_0_RESULT_21	–	R	Bit[7:0]: Voltage read out data (without VM-BIST value)
0x45A2	R_VOL_1_RESULT	–	R	Bit[7:4]: Not used Bit[3:0]: vol_1_result
0x45A3	R_VOL_1_RESULT_23	–	R	Bit[7:0]: Voltage read out data (without VM-BIST value)
0x45A4	R_VOL_2_RESULT	–	R	Bit[7:4]: Not used Bit[3:0]: vol_2_result

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address	register name	default value	R/W	description
0x45A5	R_VOL_2_RESULT_25	–	R	Bit[7:0]: Voltage read out data (without VM-BIST value)
0x45A6	R_VOL_0_TEST_RESULT	–	R	Bit[7:4]: Not used Bit[3:0]: vol_0_test_result
0x45A7	R_VOL_0_TEST_RESULT_27	–	R	Bit[7:0]: Voltage read out data (with VM-BIST value)
0x45A8	R_VOL_1_TEST_RESULT	–	R	Bit[7:4]: Not used Bit[3:0]: vol_1_test_result
0x45A9	R_VOL_1_TEST_RESULT_29	–	R	Bit[7:0]: Voltage read out data (with VM-BIST value)
0x45AA	R_VOL_2_TEST_RESULT	–	R	Bit[7:4]: Not used Bit[3:0]: vol_2_test_result
0x45AB	R_VOL_2_TEST_RESULT_2B	–	R	Bit[7:0]: Voltage read out data (with VM-BIST value)
0x45AC	R_DB_0_REAL_H	–	R	Bit[7:0]: Voltage sensor readout[15:8]
0x45AD	R_DB_0_REAL_L	–	R	Bit[7:0]: Voltage sensor readout[7:0]
0x45AE	R_DB_1_REAL_H	–	R	Bit[7:0]: Voltage sensor readout[15:8]
0x45AF	R_DB_1_REAL_L	–	R	Bit[7:0]: Voltage sensor readout[7:0]
0x45B0	R_DB_2_REAL_H	–	R	Bit[7:0]: Voltage sensor readout[15:8]
0x45B1	R_DB_2_REAL_L	–	R	Bit[7:0]: Voltage sensor readout[7:0]
0x45B2	VM_FAULTS	–	R	Bit[7:6]: Not used Bit[5:3]: Voltage monitor bist faults Bit[2:0]: vm_alarm_fault Voltage monitor faults (out of range voltage)
0x45B3	VM_CP_FAULTS	–	R	Bit[7:4]: vm_cp_startup_fault Charge pump comparator faults (startup check) Bit[3:0]: Charge pump comparator faults
0x45B4	VM_FAULTS_LATCH	–	R	Bit[7]: Not used Bit[6]: vm_fault_state State of VM fault flag block Bit[5:3]: vm_bist_fault_latch Voltage monitor bist faults Bit[2:0]: vm_alarm_fault_latch Voltage monitor faults (out of range voltage)

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address	register name	default value	R/W	description
0x45B5	VM_CP_FAULTS_LATCH	–	R	Bit[7:4]: vm_cp_startup_fault_latch Charge pump comparator faults (startup check) Bit[3:0]: Charge pump comparator faults
0x45B6	R_OFFSET_S0_H	0x00	RW	Bit[7:0]: s0_calibration_offset
0x45B7	R_OFFSET_S0_L	0x00	RW	Bit[7:0]: s0_calibration_offset
0x45B8	R_OFFSET_S1_H	0x00	RW	Bit[7:0]: s1_calibration_offset
0x45B9	R_OFFSET_S1_L	0x00	RW	Bit[7:0]: s1_calibration_offset
0x45BA	R_OFFSET_S2_H	0x00	RW	Bit[7:0]: s2_calibration_offset
0x45BB	R_OFFSET_S2_L	0x00	RW	Bit[7:0]: s2_calibration_offset
0x4600	VFIFO_REG00	0x00	RW	Bit[7:0]: auto_start_adjust[15:8] Start point adjustment in auto mode high byte
0x4601	VFIFO_REG01	0x00	RW	Bit[7:0]: auto_start_adjust[7:0] Start point adjustment in auto mode low byte
0x4602	VFIFO_REG02	0x00	RW	Bit[7:5]: Reserved Bit[4]: sof_dly_en Delay SOF until finish sending Bit[3]: SOF clear disable Bit[2]: BIST selection Bit[1]: SRAM high frequency mode enable Bit[0]: RAM bypass
0x4603	VFIFO_REG03	0x11	RW	Bit[7]: lfm_reverse Bit[6]: data_switch_en Bit[5]: hsize_switch_en Switch hsize0_i and hsize1_i Bit[4]: Frame rst enable Bit[3]: Discard CRC error count Bit[2]: Reset CRC error count Bit[1]: man_start_mode Start manual mode enable Bit[0]: fo_rd_en_wr_cnd For read write condition enable
0x4604	VFIFO_REG04	0x00	RW	Bit[7:0]: Reserved
0x4605	VFIFO_REG05	0x01	RW	Bit[7:0]: CRC error threshold
0x4606	VFIFO_REG06	0x06	RW	Bit[7:6]: Not used Bit[5:0]: SRAM BIST rm[15:8]
0x4607	VFIFO_REG07	0x06	RW	Bit[7:0]: SRAM BIST rm[7:0]

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address	register name	default value	R/W	description
0x4608	VFIFO_REG08	0x00	RW	Bit[7:0]: line_gap_man[15:8] Manual line gap high byte
0x4609	VFIFO_REG09	0x0A	RW	Bit[7:0]: line_gap_man[7:0] Manual line gap low byte
0x460A	VFIFO_FAULT_MASKED	0x30	RW	Bit[7:6]: Not used Bit[5]: vfifo_fault_lfm1_masked Masked fault in lower LFM data fault Bit[4]: vfifo_fault_lfm0_masked Masked fault in upper LFM data fault Bit[3]: vfifo_fault_odd1_masked Masked fault in lower rows odd data fault Bit[2]: vfifo_fault_even1_masked Masked fault in lower rows even data fault Bit[1]: vfifo_fault_odd0_masked Masked fault in upper rows odd data fault Bit[0]: vfifo_fault_even0_masked Masked fault in upper rows even data fault
0x460C	VFIFO_FCNT_MAX3	0xFF	RW	Bit[7:0]: Frame counter max value byte 3
0x460D	VFIFO_FCNT_MAX2	0xFF	RW	Bit[7:0]: Frame counter max value byte 2
0x460E	VFIFO_FCNT_MAX1	0xFF	RW	Bit[7:0]: Frame counter max value byte 1
0x460F	VFIFO_FCNT_MAX0	0xFF	RW	Bit[7:0]: Frame counter max value byte 0
0x4610	VFIFO_REG10	0x00	RW	Bit[7:0]: Hsize0 image manual start point[15:8]
0x4611	VFIFO_REG11	0x70	RW	Bit[7:0]: Hsize0 image manual start point[7:0]
0x4612	VFIFO_REG12	0x01	RW	Bit[7:0]: Hsize0 LFM manual start point[15:8]
0x4613	VFIFO_REG13	0x00	RW	Bit[7:0]: Hsize0 LFM manual start point[7:0]
0x4614	VFIFO_REG14	0x00	RW	Bit[7:0]: Hsize1 image manual start point[15:8]
0x4615	VFIFO_REG15	0x70	RW	Bit[7:0]: Hsize1 image manual start point[7:0]
0x4616	VFIFO_REG16	0x01	RW	Bit[7:0]: Hsize1 LFM manual start point[15:8]

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address	register name	default value	R/W	description
0x4617	VFIFO_REG17	0x00	RW	Bit[7:0]: Hsize1 LFM manual start point[7:0]
0x4618	VFIFO_REG18	–	R	Bit[7:0]: image_crc_error0_even Image upper line even data CRC error
0x4619	VFIFO_REG19	–	R	Bit[7:0]: image_crc_error0_odd Image upper line odd CRC error
0x461A	VFIFO_REG1A	–	R	Bit[7:0]: image_crc_error1_even Image lower line even data CRC error
0x461B	VFIFO_REG1B	–	R	Bit[7:0]: image_crc_error1_odd Image lower line odd CRC error
0x461C	VFIFO_REG1C	–	R	Bit[7:0]: lfm_crc_error0 Image upper line LFM data CRC error
0x461D	VFIFO_REG1D	–	R	Bit[7:0]: lfm_crc_error1 Image lower line LFM data CRC error
0x461E	VFIFO_REG1E	–	R	Bit[7]: ram3_overflow This register can only be manually cleaned Bit[6]: ram2_overflow Bit[5]: ram1_overflow Bit[4]: ram0_overflow Bit[3]: ram3_underflow Bit[2]: ram2_underflow Bit[1]: ram1_underflow Bit[0]: ram0_underflow
0x461F	VFIFO_REG1F	–	R	Bit[7:1]: Not used Bit[0]: fo_underflow This register can only be manually cleaned
0x4620	VFIFO_FCNT3	–	R	Bit[7:0]: Frame counter byte 3
0x4621	VFIFO_FCNT2	–	R	Bit[7:0]: Frame counter byte 2
0x4622	VFIFO_FCNT1	–	R	Bit[7:0]: Frame counter byte 1
0x4623	VFIFO_FCNT0	–	R	Bit[7:0]: Frame counter byte 0

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address	register name	default value	R/W	description
0x4624	VFIFO_CRC_ERROR	–	R	Bit[7:6]: Not used Bit[5]: vfifo_crc_lfm1 CRC error in lower LFM data Bit[4]: vfifo_crc_lfm0 CRC error in upper LFM data Bit[3]: vfifo_crc_odd1 CRC error in lower rows odd data Bit[2]: vfifo_crc_even1 CRC error in lower rows even data Bit[1]: vfifo_crc_odd0 CRC error in upper rows odd data Bit[0]: vfifo_crc_even0 CRC error in upper rows even data
0x4625	VFIFO_FAULT	–	R	Bit[7]: Vfifio fault state Bit[6]: Not used Bit[5]: vfifo_fault_lfm1 Lower rows LFM data fault Bit[4]: vfifo_fault_lfm0 Upper rows LFM data fault Bit[3]: vfifo_fault_odd1 Lower rows odd data fault Bit[2]: vfifo_fault_even1 Lower rows even data fault Bit[1]: vfifo_fault_odd0 Upper rows odd data fault Bit[0]: vfifo_fault_even0 Upper rows even data fault
0x4640	UID_LATE_CTRL0	0x40	RW	Bit[7]: uid_flip_auto_cut_en Separate flip-auto-cut enable bit for UID module, must match one in Window module Bit[6]: uid_mirror_auto_cut_en Separate mirror-auto-cut enable bit for UID module, must match one in Window module Bit[5]: uid_vskip This bit and global vertical skip setting must match for late UID row-ID check to pass Bit[4:2]: Reserved Bit[1]: uid_vflip This bit and global vertical flip setting must match for late UID row-ID check to pass Bit[0]: uid_mirror This bit and global horizontal mirror setting must match for late UID column-ID check to pass

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address	register name	default value	R/W	description
0x4641	UID_LATE_CTRL1	0x12	RW	Bit[7]: vs_is_last Bit[6]: s_is_last Bit[5]: m_is_last Bit[4]: l_is_last Bit[3]: Reserved Bit[2:0]: Expected number of exposures per row (needed for row ID check counter), 1, 2, 3, 4 will be taken as-is, 0, 5, 6, 7 will be understood as 4 Default is 2 (COMB + S)
0x4642	UID_LATE_FAULTMASK1	0x00	RW	Bit[7]: uid_late_rw_sparebit1 Bit[6]: uid_late_rw_sparebit2 Bit[5]: uid_late_rw_sparebit3 Bit[4]: rowid_end_fault_common_mask Bit[3]: rowid_step_fault_mask_vs Bit[2]: rowid_step_fault_mask_s Bit[1]: rowid_step_fault_mask_m Bit[0]: rowid_step_fault_mask_l
0x4643	UID_LATE_FAULTMASK2	0x00	RW	Bit[7]: colid_end_fault_mask_vs Bit[6]: colid_end_fault_mask_s Bit[5]: colid_end_fault_mask_m Bit[4]: colid_end_fault_mask_l Bit[3]: colid_step_fault_mask_vs Bit[2]: colid_step_fault_mask_s Bit[1]: colid_step_fault_mask_m Bit[0]: colid_step_fault_mask_l

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address	register name	default value	R/W	description
0x4644	UID_LATE_DIAG_ LATCHED1	–	R	Bit[7]: uid_late_ro_sparebit1 Bit[6]: colid_fault_flag_state Bit[5]: rowid_fault_flag_state Bit[4]: rowid_end_fault_common After windowing, row-ID end value was not as expected, for one or more exposures Bit[3]: rowid_step_fault_vs After windowing, row-ID start value or increment step was not as expected, VS exposure Bit[2]: rowid_step_fault_s After windowing, row-ID start value or increment step was not as expected, S exposure Bit[1]: rowid_step_fault_m After windowing, row-ID start value or increment step was not as expected, M exposure Bit[0]: rowid_step_fault_l After windowing, row-ID start value or increment step was not as expected, L exposure

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address	register name	default value	R/W	description
0x4645	UID_LATE_DIAG_ LATCHED2	–	R	Bit[7]: colid_end_fault_vs After windowing, col-ID end value was not as expected, VS exposure Bit[6]: colid_end_fault_s After windowing, col-ID end value was not as expected, S exposure Bit[5]: colid_end_fault_m After windowing, col-ID end value was not as expected, M exposure Bit[4]: colid_end_fault_l After windowing, col-ID end value was not as expected, L exposure Bit[3]: colid_step_fault_vs After windowing, col-ID start value or increment step was not as expected, VS exposure Bit[2]: colid_step_fault_s After windowing, col-ID start value or increment step was not as expected, S exposure Bit[1]: colid_step_fault_m After windowing, col-ID start value or increment step was not as expected, M exposure Bit[0]: colid_step_fault_l After windowing, col-ID start value or increment step was not as expected, L exposure
0x4646	UID_LATE_FAULTMASK3	0x00	RW	Bit[7:0]: Reserved
0x4647	UID_LATE_DIAG_ LATCHED3	–	R	Bit[7:0]: Reserved

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address	register name	default value	R/W	description
0x4648	UID_LATE_CTRL2	0x00	RW	Bit[7]: uid_late_rw_sparebit5 Bit[6]: uid_post_bin1_mono_en This bit must match its sister bit in ISP_PROC Bit[5]: uid_post_bin1_h_en This bit must match its sister bit in ISP_PROC Bit[4]: uid_post_bin1_v_en This bit must match its sister bit in ISP_PROC Bit[3]: uid_late_rw_sparebit6 Bit[2]: uid_post_bin0_mono_en This bit must match its sister bit in ISP_PROC Bit[1]: uid_post_bin0_h_en This bit must match its sister bit in ISP_PROC Bit[0]: uid_post_bin0_v_en This bit must match its sister bit in ISP_PROC
0x4649	UID_LATE_CTRL3	0x03	RW	Bit[7:2]: Not used Bit[1]: uid_flip_keep_view_en This bit must match its sister bit in window Bit[0]: uid_mirror_keep_view_en This bit must match its sister bit in window
0x4700	VSYNC_WIDTH_LINE_H	0x00	RW	Bit[7:0]: vsync_width_line_h
0x4701	VSYNC_WIDTH_LINE_L	0x00	RW	Bit[7:0]: vsync_width_line_l
0x4702	VSYNC_WIDTH_PIXEL_H	0x02	RW	Bit[7:0]: vsync_width_pixel_h
0x4703	VSYNC_WIDTH_PIXEL_L	0x00	RW	Bit[7:0]: vsync_width_pixel_l
0x4704	VSYNC_DELAY_H	0x00	RW	Bit[7:0]: vsync_delay_h
0x4705	VSYNC_DELAY_M	0x01	RW	Bit[7:0]: vsync_delay_m
0x4706	VSYNC_DELAY_L	0x00	RW	Bit[7:0]: vsync_delay_l

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address	register name	default value	R/W	description
0x4707	POLARITY_CTRL	0x00	RW	Bit[7]: clk_ddr_mode_enable Not used Bit[6]: bit_reverse_enable Invert output bits Bit[5]: vsync_gate_clk_enable Not used Bit[4]: href_gate_clk_enable Not used Bit[3]: no_frst_for_fifo Not used Bit[2]: href_polarity 0: Active high 1: Active low Bit[1]: vsync_polarity 0: Active high 1: Active low Bit[0]: pclk_polarity Not used
0x4708	MOTO_ORDER	0x00	RW	Bit[7]: fifo_bypass_mode Not used Bit[6:4]: Reserved Bit[3]: moto_test_mode When set, only change moto data every other clock Bit[2]: moto_test_bit10 Enable 10-bit test Bit[1]: moto_test_bit8 Enable 8-bit test Bit[0]: moto_test_enable Enable moto test
0x4709	BYP_SELECT	0x00	RW	Bit[7:6]: Not used Bit[5]: data_bit_shift Used in moto mode to select between bit swap methods when using 16 bits Bit[4]: href_sel Not used Bit[3:0]: bypass_sel Not used
0x470A	R_FIFO	0x00	RW	Bit[7:2]: Not used Bit[1]: dvp_sync_pclk_pol Invert output PCLK within DVP_SYNC module Bit[0]: dvp_sync_pll_pclk_inv Invert input PLL PCLK within DVP_SYNC module

table A-2 sensor control registers (sheet 98 of 255)

address	register name	default value	R/W	description
0x470B	CHANNEL_SELECT	0x0F	RW	Bit[7:4]: Not used Bit[3]: channel3_sel Bit[2]: channel2_sel Bit[1]: channel1_sel Bit[0]: channel0_sel
0x470C	DVP_SYNC_CONTROL	0x01	RW	Bit[7:2]: Not used Bit[1]: dvp_bypass Bit[0]: dvp_vsync_en
0x4800	MIPI_CTRL00	0x04	RW	Bit[7]: sc_valid_opt Select sc_valid Bit[6]: vertical_en Enable vertical clock gating Bit[5]: gate_sc_en Enable clock gating Bit[4]: line_sync_en Enable line sync Bit[3]: Not used Bit[2]: pclk_inv Invert output PCLK Bit[1]: first_bit First bit is 1 Bit[0]: lpx_p_sel Select manual parameter or auto parameter
0x4802	MIPI_CTRL02	0x00	RW	Bit[7]: hs_prepare_sel Select manual parameter or auto parameter Bit[6]: clk_prepare_sel Select manual parameter or auto parameter Bit[5]: clk_post_sel Select manual parameter or auto parameter Bit[4]: clk_trail_sel Select manual parameter or auto parameter Bit[3]: hs_exit_sel Select manual parameter or auto parameter Bit[2]: hs_zero_sel Select manual parameter or auto parameter Bit[1]: hs_trail_sel Select manual parameter or auto parameter Bit[0]: clk_zero_sel Select manual parameter or auto parameter

table A-2 sensor control registers (sheet 99 of 255)

address	register name	default value	R/W	description
0x4803	MIPI_CTRL03	0x00	RW	Bit[7]: test_en Bit[6:1]: Not used Bit[0]: dphy_test_escape_en
0x4804	MIPI_CTRL04	0xB6	RW	Bit[7:0]: mipi_phy_test_pattern
0x4805	MIPI_CTRL05	0x00	RW	Bit[7:6]: Not used Bit[5]: mipi_pkt_slp_en Option for pre-sleep Bit[4]: slp_change_en Option for pre-sleep Bit[3]: lpda_retim_manu Retiming Bit[2]: lpda_retim_sel Retiming Bit[1]: lpck_retim_manu Retiming Bit[0]: lpck_retim_sel Retiming
0x4806	MIPI_CTRL06	0x40	RW	Bit[7:6]: clk_data_pattern Bit[5]: clk_trail_data Bit[4]: pu_mark_en_o Enable power up mark Bit[3]: mipi_remot_rst_o Remote reset Bit[2]: mipi_susp_o Suspend Bit[1]: smia_lane_ch_en_o Enable SMIA lane Bit[0]: tx_lsb_first_o Output TXLSB first
0x4807	MIPI_CTRL07	0x03	RW	Bit[7:6]: Not used Bit[5:4]: clk_lane_swap_phy Clock lane switch ctrl for PHY Bit[3:0]: sw_t_lpx_o Ultra low power mode state delay
0x4808	MIPI_CTRL08	0x18	RW	Bit[7:0]: wkup_dly_o Wakeup delay
0x4809	MIPI_CTRL09	0x4C	RW	Bit[7]: lptx_pd_mode_man_en Manual control enable for lptx_pd_mode_sl Bit[6]: lptx_pd_mode_man Bit[5:0]: lptx_pd_ovlap

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address	register name	default value	R/W	description
0x480A	MIPI_TMG_CTRL	0x22	RW	Bit[7]: pkt_bit14_opt Bit[6]: frame_blk_out_opt Bit[5]: pre_sleep_opt Bit[4:2]: Reserved Bit[1]: line_act_enable Bit[0]: wc_sel_opt
0x480B	MIPI_LANE_CTRL	0x10	RW	Bit[7]: lane1_pn_swap Bit[6:4]: lane1_swap Bit[3]: lane0_pn_swap Bit[2:0]: lane0_swap
0x480C	MIPI_LANE_CTRLC	0x80	RW	Bit[7:5]: clk_lane_swap Bit[4]: lane_num_man_en Bit[3:0]: lane_num_man
0x480E	MIPI_CTRL0E	0x04	RW	Bit[7]: ring_cnt_err_opt_o Bit[6]: clk_lane_pn_swap Bit[5:4]: frm_end_time_opt Bit[3]: Enable data type2 Bit[2]: Enable img2 Bit[1:0]: Reserved
0x480F	MIPI_TMG_CTRL_F	0x32	RW	Bit[7]: lane3_pn_swap Bit[6:4]: lane3_swap Bit[3]: lane2_pn_swap Bit[2:0]: lane2_swap
0x4810	MIPI_CTRL10	0xFF	RW	Bit[7:0]: fcnt_max[15:8] Max frame count value high byte
0x4811	MIPI_CTRL11	0xFF	RW	Bit[7:0]: fcnt_max[7:0] Max frame count value low byte
0x4812	MIPI_CTRL04_12	0x12	RW	Bit[7:6]: Not used Bit[5:0]: emb_dt
0x4813	MIPI_CTRL13	0xE4	RW	Bit[7:6]: VC3 Virtual channel ID Bit[5:4]: VC2 Virtual channel ID Bit[3:2]: VC1 Virtual channel ID Bit[1:0]: VC0 Virtual channel ID
0x4814	MIPI_CTRL14	0x2A	RW	Bit[7]: Not used Bit[6]: lpkt_dt_sel Data type select Bit[5:0]: dt_man0 Data type

table A-2 sensor control registers (sheet 101 of 255)

address	register name	default value	R/W	description
0x4815	MIPI_CTRL15	0x2B	RW	Bit[7:6]: Not used Bit[5:0]: dt_man1 Data type
0x4816	MIPI_CTRL16	0x2B	RW	Bit[7:6]: Not used Bit[5:0]: dt_man2 Data type
0x4817	MIPI_CTRL17	0x00	RW	Bit[7:6]: fcnt_sel Bit[5:4]: lcnt_sel Bit[3:2]: frame_act_sel Bit[1:0]: last_sel
0x4818	MIPI_CTRL18	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_zero_min MIPI parameter value
0x4819	MIPI_CTRL19	0x70	RW	Bit[7:0]: hs_zero_min MIPI parameter value
0x481A	MIPI_CTRL1A	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_trail_min MIPI parameter value
0x481B	MIPI_CTRL1B	0x3C	RW	Bit[7:0]: hs_trail_min MIPI parameter value
0x481C	MIPI_CTRL1C	0x01	RW	Bit[7:2]: Not used Bit[1:0]: clk_zero_min MIPI parameter value
0x481D	MIPI_CTRL1D	0x2C	RW	Bit[7:0]: clk_zero_min MIPI parameter value
0x481E	MIPI_CTRL1E	0x5F	RW	Bit[7:0]: clk_prepare_max MIPI parameter value
0x481F	MIPI_CTRL1F	0x30	RW	Bit[7:0]: clk_prepare_min MIPI parameter value
0x4820	MIPI_CTRL20	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_post_min MIPI parameter value
0x4821	MIPI_CTRL21	0x3C	RW	Bit[7:0]: clk_post_min MIPI parameter value
0x4822	MIPI_CTRL22	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_trail_min MIPI parameter value
0x4823	MIPI_CTRL23	0x3C	RW	Bit[7:0]: clk_trail_min MIPI parameter value

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address	register name	default value	R/W	description
0x4824	SOF_PCLK_I	0x00	RW	Bit[7:2]: Not used Bit[1:0]: lpx_p_min MIPI parameter value
0x4825	MIPI_CTRL25	0x32	RW	Bit[7:0]: lpx_p_min MIPI parameter value
0x4826	MIPI_CTRL26	0x32	RW	Bit[7:0]: hs_prepare_min MIPI parameter value
0x4827	MIPI_CTRL27	0x55	RW	Bit[7:0]: hs_prepare_max MIPI parameter value
0x4828	MIPI_CTRL28	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_exit_min MIPI parameter value
0x4829	MIPI_CTRL29	0x64	RW	Bit[7:0]: hs_exit_min MIPI parameter value
0x482A	MIPI_CTRL2A	0x06	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_zero_min MIPI parameter value
0x482B	MIPI_CTRL2B	0x04	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_trail_min MIPI parameter value
0x482C	MIPI_CTRL2C	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_zero_min MIPI parameter value
0x482D	MIPI_CTRL2D	0x00	RW	Bit[7:4]: ui_clk_prepare_max MIPI parameter value Bit[3:0]: ui_clk_prepare_min MIPI parameter value
0x482E	MIPI_CTRL2E	0x34	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_post_min MIPI parameter value
0x482F	MIPI_CTRL2F	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_trail_min MIPI parameter value
0x4830	MIPI_CTRL30	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_lpx_p_min MIPI parameter value
0x4831	MIPI_CTRL31	0x64	RW	Bit[7:4]: ui_hs_prepare_max MIPI parameter value Bit[3:0]: ui_hs_prepare_min MIPI parameter value

table A-2 sensor control registers (sheet 103 of 255)

address	register name	default value	R/W	description
0x4832	MIPI_CTRL32	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_exit_min MIPI parameter value
0x4833	MIPI_CTRL33	0x15	RW	Bit[7:6]: Not used Bit[5:0]: Pkt FIFO ready mark
0x4834	MIPI_CTRL34	0x02	RW	Bit[7]: Not used Bit[6]: dphy_preamble_en Bit[5:0]: t_dphy_preamble
0x4835	MIPI_CTRL34_35	0x55	RW	Bit[7:0]: dphy_preamble_data
0x4837	MIPI_CTRL37	0x0D	RW	Bit[7:0]: MIPI PCLK period Should be changed when PCLK frequency changes
0x4838	MIPI_CTRL38	0x00	RW	Bit[7]: Low power select for lane0 Bit[6]: lp_dir_man0 Low power direction for lane0 Bit[5]: lp_p0_out Lp p0 for lane0 Bit[4]: lp_n0_out Lp n0 for lane0 Bit[3]: Low power select for lane1 Bit[2]: lp_dir_man1 Low power direction for lane1 Bit[1]: lp_p1_out Lp p0 for lane1 Bit[0]: lp_n1_out Lp n0 for lane1
0x4839	MIPI_CTRL39	0x00	RW	Bit[7]: Low power select for lane2 Bit[6]: lp_dir_man2 Low power direction for lane2 Bit[5]: lp_p2_out Lp p0 for lane2 Bit[4]: lp_n2_out Lp n0 for lane2 Bit[3]: Low power select for lane3 Bit[2]: lp_dir_man3 Low power direction for lane3 Bit[1]: lp_p3_out Lp p0 for lane3 Bit[0]: lp_n3_out Lp n0 for lane0
0x483C	MIPI_CTRL3C	0x10	RW	Bit[7:0]: t_clk_pre MIPI parameter value

table A-2 sensor control registers (sheet 104 of 255)

address	register name	default value	R/W	description
0x483D	MIPI_CTRL3D	0x00	RW	Bit[7:4]: Not used Bit[3]: lp_ck_sel0 Low power select for clock lane Bit[2]: Not used Bit[1]: lp_ck_p_out0 Lp clock lane p Bit[0]: lp_ck_n_out0 Lp clock lane n
0x483E	MIPI_CTRL3E	–	R	Bit[7:0]: fcnt_rd[15:8] Frame count value high byte
0x483F	MIPI_CTRL3F	–	R	Bit[7:0]: fcnt_rd[7:0] Frame count value low byte
0x484A	MIPI_CTRL4A	0x3F	RW	Bit[7:6]: Not used Bit[5]: slp_lp_pon_man Sleep powerdown select Bit[4]: slp_lp_pon_da lp_pon data Bit[3]: slp_lp_pon_ck_da lp_pon clock lane data Bit[2]: mipi_slpst_man Manual sleep state Bit[1]: slpst_clk_lane Clock lane sleep state Bit[0]: slpst_data_lane Data lane sleep state
0x484B	MIPI_CTRL4B	0x47	RW	Bit[7]: Not used Bit[6]: line_start_sel 0: Line start short packet from vfifo non-empty 1: Line start short packet from vfifo ready Bit[5]: r_eof_man EOF select Bit[4]: Virtual channel select Bit[3]: Data scramble enable Bit[2]: eof_busy_en EOF busy select Bit[1]: Clock start select Bit[0]: SOF select
0x484C	MIPI_CTRL4C	0x00	RW	Bit[7:1]: Not used Bit[0]: fcnt_inact Disable frame count
0x484E	MIPI_CTRL4E	0x10	RW	Bit[7:0]: Frame end delay

table A-2 sensor control registers (sheet 105 of 255)

address	register name	default value	R/W	description
0x484F	MIPI_CTRL4F	0x00	RW	Bit[7:4]: vc_height_sel Bit[3:1]: Not used Bit[0]: line_sleep_en
0x4850	MIPI_CTRL50	0x42	RW	Bit[7]: Not used Bit[6]: dphy12_frm_blk_opt Bit[5]: Deskew output enable Bit[4]: Deskew manual trigger Bit[3]: Initial deskew disable Bit[2]: Frame deskew disable Bit[1]: alt_cal_dis Bit[0]: DPHY1, 2 enable
0x4851	MIPI_CTRL51	0xAA	RW	Bit[7:0]: dskew_hsdat Deskew data
0x4852	MIPI_CTRL52	0xFF	RW	Bit[7:0]: Deskew sync data
0x4853	MIPI_CTRL53	0x8A	RW	Bit[7:0]: Deskew start delay
0x4854	MIPI_CTRL54	0x05	RW	Bit[7:0]: Frame deskew width
0x4855	MIPI_CTRL55	0x1C	RW	Bit[7:0]: Initial deskew width
0x4856	MIPI_CTRL56	0x01	RW	Bit[7:0]: Frame deskew interval
0x4857	MIPI_CTRL57	0x08	RW	Bit[7:4]: Not used Bit[3]: hs_same_time Bit[2:1]: Not used Bit[0]: deskew_en_man
0x4858	MIPI_CTRL58	0x1C	RW	Bit[7:0]: alt_deskew_width
0x4860	MIPI_CTRL60	0x00	RW	Bit[7:6]: mipi_cphy_dis CPHY disable Bit[5:1]: Not used Bit[0]: mipi_cphy_en CPHY enable
0x4861	MIPI_CTRL61	0xEC	RW	Bit[7]: esc_flag_sel2 CPHY escape flag Bit[6]: esc_flag_sel1 CPHY escape flag Bit[5]: Not used Bit[4]: crc_sel_reg Bit[3]: cphy_pheader_order_sel Bit[2]: cphy_eot_same_time Bit[1]: cphy_trail_data_man Bit[0]: cphy_trail_man_en
0x4862	MIPI_CTRL62	0x04	RW	Bit[7:0]: t_pre_begin_reg CPHY parameter

table A-2 sensor control registers (sheet 106 of 255)

address	register name	default value	R/W	description
0x4863	MIPI_CTRL63	0x01	RW	Bit[7:0]: t_pre_end_reg CPHY parameter
0x4864	MIPI_CTRL64	0x00	RW	Bit[7:0]: t_prog_seq_reg CPHY programmable sequence
0x4865	MIPI_CTRL65	0x66	RW	Bit[7:0]: prog_dat1_reg CPHY programmable data1
0x4866	MIPI_CTRL66	0x99	RW	Bit[7:0]: prog_dat2_reg CPHY programmable data
0x4867	MIPI_CTRL67	0x88	RW	Bit[7:0]: prog_dat3_reg CPHY programmable data3
0x4868	MIPI_CTRL68	0xAA	RW	Bit[7:0]: prog_dat4_reg CPHY programmable data4
0x4869	MIPI_CTRL69	0xFF	RW	Bit[7:0]: preamb_data1_reg CPHY preamble data1
0x486A	MIPI_CTRL6A	0x3F	RW	Bit[7:0]: preamb_data2_reg CPHY preamble data2
0x486B	MIPI_CTRL6B	0x84	RW	Bit[7:0]: sync_dat1_reg CPHY sync data1
0x486C	MIPI_CTRL6C	0x36	RW	Bit[7:0]: sync_dat2_reg CPHY sync data2
0x486D	MIPI_CTRL6D	0x00	RW	Bit[7:0]: cphy_rsvdat_reg Reverse data for CPHY
0x486E	MIPI_CTRL6E	0x84	RW	Bit[7:0]: esc_data1_reg CPHY escape data1
0x486F	MIPI_CTRL6F	0x36	RW	Bit[7:0]: esc_data2_reg CPHY escape data2
0x4870	MIPI_CTRL70	0x00	RW	Bit[7]: giic_ctrl_en Bit[6:0]: Not used
0x4871	MIPI_CTRL71	0x10	RW	Bit[7]: Not used Bit[6:4]: prbs_deg_opt 0x0: prbs_disable 0x1: Deg92 0x2: Deg113 0x3: Deg16 0x4: Deg18 0x5: 4444pattern Bit[3]: Not used Bit[2]: dphy_prbs9_opt Bit[1:0]: cphy_prbs_order Output sequence option for prbs

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address	register name	default value	R/W	description
0x4872	MIPI_CTRL72	0x00	RW	Bit[7:2]: Not used Bit[1:0]: prbs_seed_lane0
0x4873	MIPI_CTRL73	0x00	RW	Bit[7:0]: prbs_seed_lane0
0x4874	MIPI_CTRL74	0xFF	RW	Bit[7:0]: prbs_seed_lane0
0x4875	MIPI_CTRL75	0x00	RW	Bit[7:0]: prbs_seed_lane1
0x4876	MIPI_CTRL76	0xFE	RW	Bit[7:0]: prbs_seed_lane1
0x4877	MIPI_CTRL77	0x00	RW	Bit[7:0]: prbs_seed_lane2
0x4878	MIPI_CTRL78	0xFD	RW	Bit[7:0]: prbs_seed_lane2
0x4879	MIPI_CTRL79	0x00	RW	Bit[7:0]: prbs_seed_lane3
0x487A	MIPI_CTRL7A	0xFC	RW	Bit[7:0]: prbs_seed_lane3
0x487B	MIPI_CTRL7B	0x00	RW	Bit[7:2]: Not used Bit[1]: crc_fault_inj_cont Enable injecting CRC fault in every packet (Continuously) Bit[0]: Enable CRC fault injection
0x487C	MIPI_CTRL7C	0x7F	RW	Bit[7]: Not used Bit[6:0]: Line number that a CRC fault is injected[14:8]
0x487D	MIPI_CTRL7D	0xFF	RW	Bit[7:0]: Line number that a CRC fault is injected[7:0]
0x487E	MIPI_CTRL7E	–	R	Bit[7:1]: Not used Bit[0]: fault_inj_done Status of CRC fault injection
0x4880~ 0x488A	RSVD	–	–	Reserved

table A-2 sensor control registers (sheet 108 of 255)

address	register name	default value	R/W	description
0x4900	FC_REG1	0x08	RW	Bit[7:4]: Not used Bit[3]: sof_after_line0 0: When zero lines are output, place where SOF arises is before zero line 1: When zero lines are output, place where SOF arises regardless of zero lines Bit[2]: fcnt_eof_sel 0: FC output SOF delay 6 SCLK cycle based on input SOF 1: FC output SOF does not delay based on input SOF Bit[1]: fcnt_mask_dis 0: Enable frame counter mask 1: Disable frame counter mask Bit[0]: Manual frame counter reset
0x4901	FC_REG2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: If frame_off_no = Number of displayed frames before first masked frame, if frame_off_no != number of displayed frames before each burst of masked frames
0x4902	FC_REG3	0x00	RW	Bit[7:4]: Not used Bit[3:0]: If frame_on_no = Number of masked frames before first displayed frame, if frame_on_no != number of masked frames after each burst of displayed frames

table A-2 sensor control registers (sheet 109 of 255)

address	register name	default value	R/W	description
0x4903	FC_REG4	0x81	RW	Bit[7]: zero_line_mask_dis Disable mask for zero lines Bit[6]: Not used Bit[5]: data_mask_dis Even when frame is supposed to be masked, data is not masked Bit[4]: valid_mask_dis Even when frame is supposed to be masked, valid signals are not masked Bit[3]: href_mask_dis Even when frame is supposed to be masked, HREF signals are not masked Bit[2]: eof_mask_dis Even when frame is supposed to be masked, EOF signals are not masked Bit[1]: sof_mask_dis Even when frame is supposed to be masked, SOF signals are not masked Bit[0]: all_mask_dis Even when frame is supposed to be masked, none of data/valid/HREF/EOF/SOF are masked
0x4904	FC_REG5	0x01	RW	Bit[7:4]: Not used Bit[3]: sof_vs_sel Use SOF of VS as main SOF Bit[2]: sof_s_sel Use SOF of S as main SOF Bit[1]: sof_m_sel Use SOF of M as main SOF Bit[0]: sof_l_sel Use SOF of L as main SOF
0x4D00	TPM_REG_0	0x4A	RW	Bit[7:0]: tpm_slope
0x4D01	TPM_REG_1	0x18	RW	Bit[7:0]: tpm_slope
0x4D02	TPM_REG_2	0xBB	RW	Bit[7:0]: tpm_offset
0x4D03	TPM_REG_3	0xDE	RW	Bit[7:0]: tpm_offset
0x4D04	TPM_REG_4	0x93	RW	Bit[7:0]: tpm_offset
0x4D05	TPM_REG_5	0xFF	RW	Bit[7:0]: tpm_offset

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address	register name	default value	R/W	description
0x4D06	TPM_REG_6	0x88	RW	Bit[7:4]: tpm_clk divisor Bit[3:1]: cnt_bit Db period Bit[0]: clk_re Reverse output clock
0x4D07	TPM_REG_7	0x31	RW	Bit[7]: Stall Bit[6]: int_on_failure Generate interrupt when alarm or failure is asserted Bit[5]: sof_update_en Bit[4]: tpm_cont Continuous updating Bit[3]: pd_tpm_snr Bit[2]: format_slope Bit[1]: mul_div_sel Bit[0]: shift_ave
0x4D08	TPM_REG_8	0x63	RW	Bit[7]: sccb_read_sel Bit[6:5]: tester_fail_thersh Bit[4:0]: shift_bit
0x4D09	TPM_REG_9	0xDF	RW	Bit[7]: tester_enable Bit[6]: alarm_en Bit[5]: calc_para_restart Bit[4]: calc_para_mode Bit[3]: tpm_en_0 Bit[2]: tpm_en_1 Bit[1]: tpm_use_0 Bit[0]: tpm_use_1
0x4D0A	DB_LOW_H	0x78	RW	Bit[7:0]: db_low
0x4D0B	DB_LOW_L	0x98	RW	Bit[7:0]: db_low
0x4D0C	DB_HIGH_H	0xCA	RW	Bit[7:0]: db_high
0x4D0D	DB_HIGH_L	0x30	RW	Bit[7:0]: db_high
0x4D0E	DB_LOW_0_H	0x78	RW	Bit[7:0]: db_low_0
0x4D0F	DB_LOW_0_L	0x98	RW	Bit[7:0]: db_low_0
0x4D10	DB_HIGH_0_H	0xCA	RW	Bit[7:0]: db_high_0
0x4D11	DB_HIGH_0_L	0x30	RW	Bit[7:0]: db_high_0
0x4D12	TPM_REG_0E	0xFF	RW	Bit[7:0]: max_difference
0x4D13	TPM_REG_0F	0xE8	RW	Bit[7:0]: temp_low
0x4D14	TPM_REG_10	0x00	RW	Bit[7:0]: temp_low
0x4D15	TPM_REG_11	0x78	RW	Bit[7:0]: temp_high

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address	register name	default value	R/W	description
0x4D16	TPM_REG_12	0x00	RW	Bit[7:0]: temp_high
0x4D17	TPM_REG_13	0x00	RW	Bit[7:0]: tpm_min
0x4D18	TPM_REG_14	0xFF	RW	Bit[7:0]: tpm_max
0x4D19	TPM_REG_15	0x00	RW	Bit[7:0]: test_cycle_h
0x4D1A	TPM_REG_16	0x20	RW	Bit[7:0]: test_cycle_l
0x4D1B	TPM_REG_17	–	R	Bit[7:0]: tpm_int
0x4D1C	TPM_REG_18	–	R	Bit[7:0]: tpm_dec
0x4D1D	TPM_REG_19	–	R	Bit[7:0]: db_num
0x4D1E	TPM_REG_1A	–	R	Bit[7:0]: tpm_a_calc
0x4D1F	TPM_REG_1B	–	R	Bit[7:0]: tpm_a_calc
0x4D20	TPM_REG_1C	–	R	Bit[7:0]: tpm_b_calc
0x4D21	TPM_REG_1D	–	R	Bit[7:0]: tpm_b_calc
0x4D22	TPM_REG_1E	–	R	Bit[7:0]: tpm_b_calc
0x4D23	TPM_REG_1F	–	R	Bit[7:0]: tpm_b_calc
0x4D24	TPM_REG_20	–	R	Bit[7:0]: db_real_0
0x4D25	TPM_REG_21	–	R	Bit[7:0]: db_real_0
0x4D26	TPM_REG_22	–	R	Bit[7:0]: db_real_1
0x4D27	TPM_REG_23	–	R	Bit[7:0]: db_real_1 Separate calibration sensor 1
0x4D28	TPM_REG_24	–	R	Bit[7:4]: Not used Bit[3]: out_of_range Bit[2]: alarm_cel Bit[1]: Alarm Bit[0]: Failed
0x4D29	TPM_REG_25	0x0E	RW	Bit[7:4]: Reserved Bit[3]: calibration_1 Bit[2]: calibration_0 Bit[1]: out_of_range_en Bit[0]: tpm_option_eco
0x4D2A	TPM_REG_26	–	R	Bit[7:0]: tpm_int_rdout
0x4D2B	TPM_REG_27	–	R	Bit[7:0]: tpm_dec_rdout
0x4D2C	TPM_REG_28	–	R	Bit[7:0]: tpm0_int
0x4D2D	TPM_REG_29	–	R	Bit[7:0]: tpm0_dec

table A-2 sensor control registers (sheet 112 of 255)

address	register name	default value	R/W	description
0x4D2E	TPM_REG_2A	–	R	Bit[7:0]: tpm1_int
0x4D2F	TPM_REG_2B	–	R	Bit[7:0]: tpm1_dec
0x4D30	TPM_REG_2C	0xFF	RW	Bit[7:0]: max_diff_int
0x4D31	TPM_REG_2D	0xFF	RW	Bit[7:0]: max_diff_dec
0x4D32	TPM_REG_32	0xE8	RW	Bit[7:0]: temp_low_0
0x4D33	TPM_REG_33	0x00	RW	Bit[7:0]: temp_low_0
0x4D34	TPM_REG_34	0x78	RW	Bit[7:0]: temp_high_0
0x4D35	TPM_REG_35	0x00	RW	Bit[7:0]: temp_high_0
0x4D36	TPM_REG_36	0x78	RW	Bit[7:0]: db_low_1
0x4D37	TPM_REG_37	0x98	RW	Bit[7:0]: db_low_1
0x4D38	TPM_REG_38	0xCA	RW	Bit[7:0]: db_high_1
0x4D39	TPM_REG_39	0x30	RW	Bit[7:0]: db_high_1
0x4D3A	TPM_REG_3A	0xE8	RW	Bit[7:0]: temp_low_1
0x4D3B	TPM_REG_3B	0x00	RW	Bit[7:0]: temp_low_1
0x4D3C	TPM_REG_3C	0x78	RW	Bit[7:0]: temp_high_1
0x4D3D	TPM_REG_3D	0x00	RW	Bit[7:0]: temp_high_1
0x4D3E	TPM_REG_3E	0x4A	RW	Bit[7:0]: tpm_slope_0
0x4D3F	TPM_REG_3F	0x18	RW	Bit[7:0]: tpm_slope_0
0x4D40	TPM_REG_40	0xBB	RW	Bit[7:0]: tpm_offset_0
0x4D41	TPM_REG_41	0xDE	RW	Bit[7:0]: tpm_offset_0
0x4D42	TPM_REG_42	0x93	RW	Bit[7:0]: tpm_offset_0
0x4D43	TPM_REG_43	0xFF	RW	Bit[7:0]: tpm_offset_0
0x4D44	TPM_REG_44	0x4A	RW	Bit[7:0]: tpm_slope_1
0x4D45	TPM_REG_45	0x18	RW	Bit[7:0]: tpm_slope_1
0x4D46	TPM_REG_46	0xBB	RW	Bit[7:0]: tpm_offset_1
0x4D47	TPM_REG_47	0xDE	RW	Bit[7:0]: tpm_offset_1
0x4D48	TPM_REG_48	0x93	RW	Bit[7:0]: tpm_offset_1
0x4D49	TPM_REG_49	0xFF	RW	Bit[7:0]: tpm_offset_1
0x4D4A	TPM_REG_4A	–	R	Bit[7:0]: tpm_a_s0_calc
0x4D4B	TPM_REG_4B	–	R	Bit[7:0]: tpm_a_s0_calc

table A-2 sensor control registers (sheet 113 of 255)

address	register name	default value	R/W	description
0x4D4C	TPM_REG_4C	–	R	Bit[7:0]: tpm_b_spd0_calc
0x4D4D	TPM_REG_4D	–	R	Bit[7:0]: tpm_b_spd0_calc
0x4D4E	TPM_REG_4E	–	R	Bit[7:0]: tpm_b_spd0_calc
0x4D4F	TPM_REG_4F	–	R	Bit[7:0]: tpm_b_spd0_calc
0x4D50	TPM_REG_50	–	R	Bit[7:0]: tpm_a_s1_calc
0x4D51	TPM_REG_51	–	R	Bit[7:0]: tpm_a_s1_calc
0x4D52	TPM_REG_52	–	R	Bit[7:0]: tpm_b_spd1_calc
0x4D53	TPM_REG_53	–	R	Bit[7:0]: tpm_b_spd1_calc
0x4D54	TPM_REG_54	–	R	Bit[7:0]: tpm_b_spd1_calc
0x4D55	TPM_REG_55	–	R	Bit[7:0]: tpm_b_spd1_calc
0x4D56	TPM_REG_56	–	R	Bit[7:0]: tpm0_int_rdout
0x4D57	TPM_REG_57	–	R	Bit[7:0]: tpm0_dec_rdout
0x4D58	TPM_REG_58	–	R	Bit[7:0]: tpm1_int_rdout
0x4D59	TPM_REG_59	–	R	Bit[7:0]: tpm1_dec_rdout
0x4D5A	TPM_REG_5A	0x10	RW	Bit[7:5]: Not used Bit[4]: wd_fault_inject_mask Bit[3]: fault_out_of_range_mask Bit[2]: fault_alarm_cel_mask Bit[1]: fault_alarm_mask Bit[0]: fault_failed_mask
0x4D5B	TPM_REG_5B	–	R	Bit[7:5]: Not used Bit[4]: wd_injected_fault_latch Bit[3]: fault_out_of_range_latch Bit[2]: fault_alarm_cel_latch Bit[1]: fault_alarm_latch Bit[0]: fault_failed_latch
0x4D5C	TPM_REG_5C	–	R	Bit[7:1]: Not used Bit[0]: fault_tpm_state
0x4D5D	TPM_WD_INJECT_FAULT	0x02	RW	Bit[7:2]: Not used Bit[1]: man_self_test_param_en Bit[0]: wd_tpm_inject_fault
0x4D5E	TPM_ST_SLOPE_H	0x4A	RW	Bit[7:0]: tpm_self_test_slope
0x4D5F	TPM_ST_SLOPE_L	0x18	RW	Bit[7:0]: tpm_self_test_slope
0x4D60	TPM_ST_OFFSET_1	0xBB	RW	Bit[7:0]: tpm_self_test_offset
0x4D61	TPM_ST_OFFSET_2	0xDE	RW	Bit[7:0]: tpm_self_test_offset

table A-2 sensor control registers (sheet 114 of 255)

address	register name	default value	R/W	description
0x4D62	TPM_ST_OFFSET_3	0x93	RW	Bit[7:0]: tpm_self_test_offset
0x4D63	TPM_ST_OFFSET_4	0xFF	RW	Bit[7:0]: tpm_self_test_offset
0x4F00	FAULT_MASK_2	0x3F	RW	Bit[7:6]: Not used Bit[5]: blc_fault_1_mask BLC fault, pipe 1 Bit[4]: sensor_chk_fault_mask Sensor timing control fault Bit[3]: errb_o_fault_mask ERRB pad fault Bit[2]: fault_o_fault_mask Fault output fault Bit[1]: grf_fault_mask Group hold fault Bit[0]: row_uid_fault_mask Row-ID fault after windowing
0x4F01	FAULT_MASK_1	0xFF	RW	Bit[7]: col_uid_fault_mask Column-ID fault after windowing Bit[6]: dtr_fault_mask Digital test row fault Bit[5]: apc_fault_mask Analog test pattern row fault Bit[4]: sync_fifo_fault_mask Sync-FIFO fault Bit[3]: xdec_chk_fault_mask X-decoder checker fault Bit[2]: vfifo_fault_mask Bit[1]: blc_fault_0_mask BLC fault, pipe 0 Bit[0]: sccb_fault_mask I2C readback fault
0x4F02	FAULT_MASK_0	0xFF	RW	Bit[7]: otp_fault_mask Bit[6]: tpm_fault_mask Temperature sensor fault Bit[5]: romloader_fault_mask Bit[4]: pll_monitor_fault_mask Bit[3]: pll_fault_mask PLL lock fault Bit[2]: vm_fault_mask Voltage monitor fault Bit[1]: pixel_asil_fault_mask Online pixel ASIL fault Bit[0]: mbist_fault_mask

table A-2 sensor control registers (sheet 115 of 255)

address	register name	default value	R/W	description
0x4F03	WATCHDOG_CTRL_1	0x20	RW	Bit[7:6]: vsync_sel Select VSYNC 00: Long (default) 01: Mid 10: Short 11: Very short Bit[5]: Sticky ERRB pad Bit[4]: rev_fault Dual fault signal reverse Bit[3:2]: Mask dual fault signal Bit[1]: rev_errb Pad fault signal reverse Bit[0]: mask_errb Mask pad fault signal
0x4F04	WATCHDOG_CTRL_2	0xE0	RW	Bit[7]: reg2_sticky_clear_en Enable sticky fault flag clear by register2 read to 0x4F0E, default disabled Bit[6]: reg_sticky_clear_en Enable sticky fault flag clear by register read to 0x4F0E, default enabled Bit[5]: sticky_fault_flags Do not use (always high) Bit[4]: enable_streaming Enable startup fault_flag module (disable will keep it in wait state) Bit[3]: enable_startup Enable startup fault_flag module (disable will keep it in wait state) Bit[2:1]: Dummy bit Do not change (replaces VSYNC with long EOF) Bit[0]: fault_clear Clear all fault latches (need to set to 1 and 0)
0x4F05	COUNTER_CTRL	0x13	RW	Bit[7:4]: Watchdog blocks fault output while VSYNC count is less than VSYNC's register value Bit[3:0]: Initial value of diff counter (count down), counter value equal to zero asserts fault flag

table A-2 sensor control registers (sheet 116 of 255)

address	register name	default value	R/W	description
0x4F06	FAULT_LATCH_2	–	R	Bit[7:6]: Not used Bit[5]: blc_fault_1_latch BLC fault, pipe 1 Bit[4]: sensor_chk_fault_latch Sensor timing control fault Bit[3]: errb_o_fault_latch ERRB pad fault Bit[2]: fault_o_fault_latch Fault output fault Bit[1]: grf_fault_latch Group hold fault Bit[0]: row_uid_fault_latch Row-ID fault after windowing
0x4F07	FAULT_LATCH_1	–	R	Bit[7]: col_uid_fault_latch Column-ID fault after windowing Bit[6]: dtr_fault_latch Digital test row fault Bit[5]: apc_fault_latch Analog test pattern row fault Bit[4]: sync_fifo_fault_latch Sync-FIFO fault Bit[3]: xdec_chk_fault_latch X-decoder checker fault Bit[2]: vfifo_fault_latch Bit[1]: blc_fault_0_latch BLC fault, pipe 0 Bit[0]: sccb_fault_latch I2C readback fault
0x4F08	FAULT_LATCH_0	–	R	Bit[7]: otp_fault_latch Bit[6]: tpm_fault_latch Temperature sensor fault Bit[5]: romloader_fault_latch Bit[4]: pll_monitor_fault_latch Bit[3]: pll_fault_latch PLL lock fault Bit[2]: vm_fault_latch Voltage monitor fault Bit[1]: pixel_asil_fault_latch Online pixel ASIL fault Bit[0]: mbist_fault_latch

table A-2 sensor control registers (sheet 117 of 255)

address	register name	default value	R/W	description
0x4F09	FAULT_2	–	R	Bit[7:6]: Not used Bit[5]: BLC fault, pipe 1 Bit[4]: sensor_chk_fault Sensor timing control fault Bit[3]: errb_o_fault ERRB pad fault Bit[2]: Fault output fault Bit[1]: grf_fault Group hold fault Bit[0]: row_uid_fault Row-ID fault after windowing
0x4F0A	FAULT_1	–	R	Bit[7]: Column-ID fault after windowing Bit[6]: Digital test row fault Bit[5]: apc_fault Analog test pattern row fault Bit[4]: Sync-FIFO fault Bit[3]: X-decoder checker fault Bit[2]: VFIFO fault Bit[1]: BLC fault, pipe 0 Bit[0]: sccb_fault I2C readback fault
0x4F0B	FAULT_0	–	R	Bit[7]: OTP fault Bit[6]: tpm_fault Temperature sensor fault Bit[5]: ROM loader fault Bit[4]: PLL monitor fault Bit[3]: PLL lock fault Bit[2]: Voltage monitor fault Bit[1]: Online pixel ASIL fault Bit[0]: MBIST fault
0x4F0C	STICKY_FAULT_CLEAR	–	R	Bit[7:1]: Not used Bit[0]: Unmasked sticky faults or'd (read will unstick faults)
0x4F0D	TPM_READOUT_H	–	R	Bit[7:0]: Temperature sensor readout (integer)
0x4F0E	TPM_READOUT_L	–	R	Bit[7:0]: Temperature sensor readout (decimal)

table A-2 sensor control registers (sheet 118 of 255)

address	register name	default value	R/W	description
0x4F0F	STATUS_F	–	R	Bit[7]: Not used Bit[6]: Fault status of startup tests Bit[5]: Fault status of streaming tests Bit[4]: State machine state 0: Reset latch 1: Error latch for startup tests Bit[3]: State machine state 0: Reset latch 1: Error latch for streaming tests Bit[2]: State of ERRB output Bit[1:0]: State of fault outputs
0x5000	ISP_CTRL_00	0x8F	RW	Bit[7]: Output size latch (by get_ready) Operation enable Bit[6]: Output stream 1 post RAW binning mono mode enable Bit[5:3]: Reserved Bit[2]: para_latch_en Latch (by get_ready) operation enable Bit[1]: ctrl_latch_en Latch (by VSYNC) operation enable Bit[0]: ISP enable
0x5001	ISP_CTRL_01	0x75	RW	Bit[7]: gain_iterate_en Bit[6]: rst_protect_en HREF before 1st VSYNC mask enable Bit[5]: Digital gain work enable Bit[4]: spd_used_in_combine Bit[3]: Reserved Bit[2]: Split mode Bit[1]: bypass_combine Bit[0]: LFM's timing go with main combine
0x5002	ISP_CTRL_02	0x3F	RW	Bit[7]: PWL 1 enable Bit[6]: PWL 0 enable Bit[5]: Re-timing enable Bit[4]: Statistic block 4 enable Bit[3]: Statistic block 3 enable Bit[2]: Statistic block 2 enable Bit[1]: Statistic block 1 enable Bit[0]: Statistic block 0 enable

table A-2 sensor control registers (sheet 119 of 255)

address	register name	default value	R/W	description
0x5003	ISP_CTRL_03	0xFA	RW	Bit[7]: awb_revs_en Reverse AWB Gain enable Bit[6]: LFM enable Bit[5]: Combine enable Bit[4]: Pre-Matrix enable Bit[3]: Combine sync buffer enable Bit[2]: LENC enable Bit[1]: HDR sync buffer enable Bit[0]: Reserved
0x5004	ISP_CTRL_04	0x3E	RW	Bit[7]: Reserved Bit[6]: Sampcorr enable Bit[5]: XTC enable Bit[4]: scip_l_en L channel SCIP enable Bit[3]: dpc_l_en L channel DPC enable Bit[2]: otp_l_en L channel OTP_DPC enable Bit[1]: awb_gain_l_en L channel AWB gain enable Bit[0]: pre_isp_l_en L channel pre ISP enable
0x5005	ISP_CTRL_05	0x1E	RW	Bit[7:5]: Reserved Bit[4]: scip_m_en M channel SCIP enable Bit[3]: dpc_m_en M channel DPC enable Bit[2]: otp_m_en M channel OTP_DPC enable Bit[1]: awb_gain_m_en M channel AWB gain enable Bit[0]: pre_isp_m_en M channel pre ISP enable
0x5006	ISP_CTRL_06	0x1E	RW	Bit[7:5]: Reserved Bit[4]: scip_s_en S channel SCIP enable Bit[3]: dpc_s_en S channel DPC enable Bit[2]: otp_s_en S channel OTP_DPC enable Bit[1]: awb_gain_s_en S channel AWB gain enable Bit[0]: pre_isp_s_en S channel pre ISP enable

table A-2 sensor control registers (sheet 120 of 255)

address	register name	default value	R/W	description
0x5007	ISP_CTRL_07	0x1E	RW	Bit[7:5]: Reserved Bit[4]: scip_v_en V channel SCIP enable Bit[3]: dpc_v_en V channel DPC enable Bit[2]: otp_v_en V channel OTP_DPC enable Bit[1]: awb_gain_v_en V channel AWB gain enable Bit[0]: pre_isp_v_en V channel pre ISP enable
0x5008	POST_RAW_BIN_CTRL	0x00	RW	Bit[7]: Ifm_bin_mode 0: All bits or with each other 1: All bits and with each other Bit[6]: post_bin1_mono_en Output stream 1 post RAW binning mono mode enable Bit[5]: post_bin1_h_en Output stream 1 post RAW H binning enable Bit[4]: post_bin1_v_en Output stream 1 post RAW V binning enable Bit[3]: Reserved Bit[2]: post_bin0_mono_en Output stream 0 post RAW binning mono mode enable Bit[1]: post_bin0_h_en Output stream 0 post RAW H binning enable Bit[0]: post_bin0_v_en0 Output stream 0 Post RAW V binning enable
0x5009	TEST_CTRL_EN0	0x1F	RW	Bit[7:5]: Reserved Bit[4]: stat4_test_en Statistic block test enable Bit[3]: stat3_test_en Statistic block test enable Bit[2]: stat2_test_en Statistic block test enable Bit[1]: stat1_test_en Statistic block test enable Bit[0]: stat0_test_en Statistic block test enable

table A-2 sensor control registers (sheet 121 of 255)

address	register name	default value	R/W	description
0x500A	TEST_CTRL_EN1	0x3F	RW	Bit[7:6]: Reserved Bit[5]: Sampcorrection test enable Bit[4]: XTC test enable Bit[3]: pwl1_test_en PWL test enable Bit[2]: pwl0_test_en PWL test enable Bit[1]: LFM test enable Bit[0]: awb_revs_test_en Reverse AWB gain test enable
0x500B	TEST_CTRL_EN2	0xFF	RW	Bit[7]: Combine test enable Bit[6]: Pre-matrix test enable Bit[5]: SCIP test enable Bit[4]: DPC test enable Bit[3]: OTP_DPC test enable Bit[2]: LENC test enable Bit[1]: AWB gain test enable Bit[0]: Pre ISP test enable
0x500C	RSVD	–	–	Reserved
0x500D	RESERVE_0D	0x01	RW	Bit[7:3]: Reserved Bit[2:1]: awb_copy_mode Switch for and operation Bit[0]: Output mode latch (by VSYNC) operation enable
0x500E	GT_CLK0	0x00	RW	Bit[7]: pipe_en_latch_dis_combine0 Combine's pipe enable latch disable Bit[6]: pipe_en_latch_dis_pre_matrix0 Pre-matrix's pipe enable latch disable Bit[5]: pipe_en_latch_dis_scip0 SCIP'S pipe enable latch disable Bit[4]: pipe_en_latch_dis_dpc0 DPC'S pipe enable latch disable Bit[3]: pipe_en_latch_dis_otp0 OTP'S pipe enable latch disable Bit[2]: pipe_en_latch_dis_lenc0 LENC'S pipe enable latch disable Bit[1]: pipe_en_latch_dis_awbg0 AWBG'S pipe enable latch disable Bit[0]: pipe_en_latch_dis_pre_isp0 Pre-ISP's pipe enable latch disable

table A-2 sensor control registers (sheet 122 of 255)

address	register name	default value	R/W	description
0x500F	GT_CLK1	0x00	RW	Bit[7:6]: Reserved Bit[5]: pipe_en_latch_dis_sc Sampcorr's pipe enable latch disable Bit[4]: pipe_en_latch_dis_xtc XTC's pipe enable latch disable Bit[3]: pipe_en_latch_dis_pwl PWL's pipe enable latch disable Bit[2]: pipe_en_latch_dis_post_bin Post-bin's pipe enable latch disable Bit[1]: pipe_en_latch_dis_rawb Reverse-AWB's pipe enable latch disable Bit[0]: pipe_en_latch_dis_lfm LFM's pipe enable latch disable
0x5010	L_SCALE_GAIN_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Conversion gain scale for long exposure
0x5011	L_SCALE_GAIN_L	0x40	RW	Bit[7:0]: Conversion gain scale for long exposure
0x5012	M_SCALE_GAIN_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Conversion gain scale for mid exposure
0x5013	M_SCALE_GAIN_L	0x40	RW	Bit[7:0]: Conversion gain scale for mid exposure
0x5014	S_SCALE_GAIN_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Conversion gain scale for short exposure
0x5015	S_SCALE_GAIN_L	0x40	RW	Bit[7:0]: Conversion gain scale for short exposure
0x5016	V_SCALE_GAIN_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Conversion gain scale for very short exposure
0x5017	V_SCALE_GAIN_L	0x40	RW	Bit[7:0]: Conversion gain scale for very short exposure
0x5019	L_SENSITIVITY0	0x00	RW	Bit[7:1]: Not used Bit[0]: Reversed
0x501A	L_SENSITIVITY1	0xFF	RW	Bit[7:0]: Sensitivity ratio for long exposure
0x501B	L_SENSITIVITY2	0xFF	RW	Bit[7:0]: Sensitivity ratio for long exposure
0x501D	M_SENSITIVITY0	0x00	RW	Bit[7:1]: Not used Bit[0]: Reversed

table A-2 sensor control registers (sheet 123 of 255)

address	register name	default value	R/W	description
0x501E	M_SENSITIVITY1	0x24	RW	Bit[7:0]: Sensitivity ratio for mid exposure
0x501F	M_SENSITIVITY2	0x92	RW	Bit[7:0]: Sensitivity ratio for mid exposure
0x5021	S_SENSITIVITY0	0x00	RW	Bit[7:1]: Not used Bit[0]: Reversed
0x5022	S_SENSITIVITY1	0x00	RW	Bit[7:0]: Sensitivity ratio for short exposure
0x5023	S_SENSITIVITY2	0x56	RW	Bit[7:0]: Sensitivity ratio for short exposure
0x5025	V_SENSITIVITY0	0x00	RW	Bit[7:1]: Not used Bit[0]: Reversed
0x5026	V_SENSITIVITY1	0x24	RW	Bit[7:0]: Sensitivity ratio for very short exposure
0x5027	V_SENSITIVITY2	0x92	RW	Bit[7:0]: Sensitivity ratio for very short exposure
0x5028	CLK_GT_CTRL1	0x10	RW	Bit[7]: dis_ck_gt_sc Sampcorr clock gate disable Bit[6]: dis_ck_gt_xtc XTC clock gate disable Bit[5]: ISP golbal CLK enable Bit[4]: ISP golbal CLK gate Bit[3]: Reserved Bit[2]: dis_ck_gt_top ISP_TOP clock gate disable Bit[1]: dis_ck_gt_retiming Re-timing clock gate disable Bit[0]: dis_ck_gt_v2tod2v2 V2tod2v2 clock gate disable
0x5029	CLK_GT_CTRL2	0x00	RW	Bit[7]: dis_ck_gt_stat Statistic clock gate disable Bit[6]: dis_ck_gt_pwl PWL clock gate disable Bit[5]: dis_ck_gt_awb_revs Reverse AWB gain clock gate disable Bit[4]: dis_ck_gt_post_bin Post RAW binning clock gate disable Bit[3]: dis_ck_gt_lfm LFM clock gate disable Bit[2]: dis_ck_gt_combine Combine clock gate disable Bit[1]: dis_ck_gt_pre_matrix Pre-matrix clock gate disable Bit[0]: dis_ck_gt_scip SCIP clock gate disable

table A-2 sensor control registers (sheet 124 of 255)

address	register name	default value	R/W	description
0x502A	CLK_GT_CTRL3	0x00	RW	Bit[7]: dis_ck_gt_d2v2tov2 D2v2tov2 buffer clock gate disable Bit[6]: dis_ck_gt_dpc DPC clock gate disable Bit[5]: dis_ck_gt_otp OTP-DPC clock gate disable Bit[4]: dis_ck_gt_lenc LENC clock gate disable Bit[3]: dis_ck_gt_awb AWB gain clock gate disable Bit[2]: dis_ck_gt_pre_isp Pre ISP clock gate disable Bit[1]: dis_ck_gt_sync_buf HDR sync buffer clock gate disable Bit[0]: Reserved
0x502B	MAN_CTRL_EN1	0x80	RW	Bit[7]: glb_cen_sram Global SRAM CEN Bit[6]: Manual test enable Use test line's enable or use active line's enable Bit[5]: Manual set pipe size enable Bit[4]: man_gain_rst_en Manual reset gain/expo calculation enable Bit[3]: Manual set output format enable Bit[2]: Manual set work mode enable Bit[1]: Manual set output dummy line number enable Bit[0]: Manual set CFA pattern enable
0x502C	MAN_CTRL_EN2	0x00	RW	Bit[7]: Manual set V channel BLC enable Bit[6]: Manual set S channel BLC enable Bit[5]: Manual set M channel BLC enable Bit[4]: Manual set L channel BLC enable Bit[3]: Manual set V channel exposure index enable Bit[2]: Manual set S channel exposure index enable Bit[1]: Manual set M channel exposure index enable Bit[0]: Manual set L channel exposure index enable

table A-2 sensor control registers (sheet 125 of 255)

address	register name	default value	R/W	description
0x502D	MAN_CTRL_EN3	0x00	RW	Bit[7]: Manual set V channel camera exposure enable Bit[6]: Manual set S channel camera exposure enable Bit[5]: Manual set M channel camera exposure enable Bit[4]: Manual set L channel camera exposure enable Bit[3]: Manual set V channel convert gain enable Bit[2]: Manual set S channel convert gain enable Bit[1]: Manual set M channel convert gain enable Bit[0]: Manual set L channel convert gain enable
0x502E	MAN_EOF0	0x00	RW	Bit[7:6]: S timing output EOF select 00: Proc 01: Pre-ISP 10: DPC 11: Statistic done Bit[5:4]: S timing output SOF select 00: Proc 01: Pre-ISP Others:S VSYNC Bit[3:2]: L timing output EOF select 00: Proc 01: Pre-ISP 10: DPC 11: Statistic done Bit[1:0]: L timing output SOF select 00: Proc 01: Pre-ISP Others:L VSYNC

table A-2 sensor control registers (sheet 126 of 255)

address	register name	default value	R/W	description
0x502F	MAN_EOF1	0x00	RW	Bit[7:6]: V timing output EOF select 00: Proc 01: Pre-ISP 10: DPC 11: Statistic done Bit[5:4]: V timing output SOF select 00: Proc 01: Pre-ISP Others:S VSYNC Bit[3:2]: M timing output EOF select 00: Proc 01: Pre-ISP 10: DPC 11: Statistic done Bit[1:0]: M timing output SOF select 00: Proc 01: Pre-ISP Others:L VSYNC
0x5030	MAN_GAIN_HCG0	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Manual convert gain for L channel
0x5031	MAN_GAIN_HCG1	0x00	RW	Bit[7:0]: Manual convert gain for L channel
0x5032	MAN_GAIN_LCG0	0x00	RW	Bit[7:6]: Not used Bit[5:0]: man_m_convert_gain Manual convert gain for M channel
0x5033	MAN_GAIN_LCG1	0x00	RW	Bit[7:0]: man_m_convert_gain Manual convert gain for M channel
0x5034	MAN_GAIN_SPD0	0x00	RW	Bit[7:6]: Not used Bit[5:0]: man_s_convert_gain Manual convert gain for S channel
0x5035	MAN_GAIN_SPD1	0x00	RW	Bit[7:0]: man_s_convert_gain Manual convert gain for S channel
0x5036	MAN_GAIN_VS0	0x00	RW	Bit[7:6]: Not used Bit[5:0]: man_v_convert_gain Manual convert gain for V channel
0x5037	MAN_GAIN_VS1	0x00	RW	Bit[7:0]: man_v_convert_gain Manual convert gain for V channel
0x5038	MAN_EXP_L0	0x00	RW	Bit[7:0]: Manual camera exposure for L channel
0x5039	MAN_EXP_L1	0x00	RW	Bit[7:0]: Manual camera exposure for L channel

table A-2 sensor control registers (sheet 127 of 255)

address	register name	default value	R/W	description
0x503A	MAN_EXP_M0	0x00	RW	Bit[7:0]: man_m_cam_expo Manual camera exposure for M channel
0x503B	MAN_EXP_M1	0x00	RW	Bit[7:0]: man_m_cam_expo Manual camera exposure for M channel
0x503C	MAN_EXP_S0	0x00	RW	Bit[7:0]: man_s_cam_expo Manual camera exposure for S channel
0x503D	MAN_EXP_S1	0x00	RW	Bit[7:0]: man_s_cam_expo Manual camera exposure for S channel
0x503E	MAN_EXP_V0	0x00	RW	Bit[7:0]: man_v_cam_expo Manual camera exposure for V channel
0x503F	MAN_EXP_V1	0x00	RW	Bit[7:0]: man_v_cam_expo Manual camera exposure for V channel
0x5040	MAN_BLC_HCG0	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual BLC for L channel
0x5041	MAN_BLC_HCG1	0x00	RW	Bit[7:0]: Manual BLC for L channel
0x5042	MAN_BLC_LCG0	0x00	RW	Bit[7:2]: Not used Bit[1:0]: man_m_blc Manual BLC for M channel
0x5043	MAN_BLC_LCG1	0x00	RW	Bit[7:0]: man_m_blc Manual BLC for M channel
0x5044	MAN_BLC_SPD0	0x00	RW	Bit[7:2]: Not used Bit[1:0]: man_s_blc Manual BLC for S channel
0x5045	MAN_BLC_SPD1	0x00	RW	Bit[7:0]: man_s_blc Manual BLC for S channel
0x5046	MAN_BLC_VS0	0x00	RW	Bit[7:2]: Not used Bit[1:0]: man_v_blc Manual BLC for V channel
0x5047	MAN_BLC_VS1	0x00	RW	Bit[7:0]: man_v_blc Manual BLC for V channel
0x504B	MAN_EXP_IDX_HCG0	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Manual exposure index for L channel

table A-2 sensor control registers (sheet 128 of 255)

address	register name	default value	R/W	description
0x504C	MAN_EXP_IDX_HCG1	0x00	RW	Bit[7:0]: Manual exposure index for L channel
0x504D	MAN_EXP_IDX_HCG2	0x00	RW	Bit[7:0]: Manual exposure index for L channel
0x504E	MAN_EXP_IDX_HCG3	0x00	RW	Bit[7:0]: Manual exposure index for L channel
0x504F	MAN_EXP_IDX_HCG4	0x00	RW	Bit[7:0]: Manual exposure index for L channel
0x5053	MAN_EXP_IDX_LCG0	0x00	RW	Bit[7:6]: Not used Bit[5:0]: man_m_expo_idx Manual exposure index for M channel
0x5054	MAN_EXP_IDX_LCG1	0x00	RW	Bit[7:0]: man_m_expo_idx Manual exposure index for M channel
0x5055	MAN_EXP_IDX_LCG2	0x00	RW	Bit[7:0]: man_m_expo_idx Manual exposure index for M channel
0x5056	MAN_EXP_IDX_LCG3	0x00	RW	Bit[7:0]: man_m_expo_idx Manual exposure index for M channel
0x5057	MAN_EXP_IDX_LCG4	0x00	RW	Bit[7:0]: man_m_expo_idx Manual exposure index for M channel
0x505B	MAN_EXP_IDX_SPD0	0x00	RW	Bit[7:6]: Not used Bit[5:0]: man_s_expo_idx Manual exposure index for S channel
0x505C	MAN_EXP_IDX_SPD1	0x00	RW	Bit[7:0]: man_s_expo_idx Manual exposure index for S channel
0x505D	MAN_EXP_IDX_SPD2	0x00	RW	Bit[7:0]: man_s_expo_idx Manual exposure index for S channel
0x505E	MAN_EXP_IDX_SPD3	0x00	RW	Bit[7:0]: man_s_expo_idx Manual exposure index for S channel
0x505F	MAN_EXP_IDX_SPD4	0x00	RW	Bit[7:0]: man_s_expo_idx Manual exposure index for S channel

table A-2 sensor control registers (sheet 129 of 255)

address	register name	default value	R/W	description
0x5063	MAN_EXP_IDX_VS0	0x00	RW	Bit[7:6]: Not used Bit[5:0]: man_v_expo_idx Manual exposure index for V channel
0x5064	MAN_EXP_IDX_VS1	0x00	RW	Bit[7:0]: man_v_expo_idx Manual exposure index for V channel
0x5065	MAN_EXP_IDX_VS2	0x00	RW	Bit[7:0]: man_v_expo_idx Manual exposure index for V channel
0x5066	MAN_EXP_IDX_VS3	0x00	RW	Bit[7:0]: man_v_expo_idx Manual exposure index for V channel
0x5067	MAN_EXP_IDX_VS4	0x00	RW	Bit[7:0]: man_v_expo_idx Manual exposure index for V channel
0x5068	MAN_VSIZE0	0x00	RW	Bit[7:0]: Manual pipe process (before post-binning) V size
0x5069	MAN_VSIZE1	0x00	RW	Bit[7:0]: Manual pipe process (before post-binning) V size
0x506A	MAN_HSIZE0	0x00	RW	Bit[7:0]: Manual pipe process (before post-binning) H size
0x506B	MAN_HSIZE1	0x00	RW	Bit[7:0]: Manual pipe process (before post-binning) H size
0x506C	MAN_RETIMING0	0x00	RW	Bit[7:1]: Not used Bit[0]: man_retim_dmy Manual dmy enable for re-timing
0x506D	MAN_RETIMING1	0x00	RW	Bit[7:2]: Reserved Bit[1]: Manual bg_gain enable for LENC and PMX Bit[0]: Manual dummy hblank number enable for re-timing
0x506E	MAN_RETIMING2	0x01	RW	Bit[7:0]: Manual dummy hblank number for re-timing
0x506F	MAN_RETIMING3	0x00	RW	Bit[7:0]: Manual dummy hblank number for re-timing
0x5070	RESERVE_70	0x00	RW	Bit[7:0]: Reserved
0x5071	MAN_DMY_LINE_NUM	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual dummy line number

table A-2 sensor control registers (sheet 130 of 255)

address	register name	default value	R/W	description
0x5072	MAN_SETTING0	0x00	RW	Bit[7:6]: Manual CFA pattern Bit[5:4]: Manual ISP output format Bit[3]: Not used Bit[2:0]: Manual work mode
0x5073	MAN_POST_BIN_CTRL	0x00	RW	Bit[7:2]: Reserved Bit[1]: Manual PWL1 enable 0: Auto control by output mode 1: Manual control Bit[0]: Manual post bin1 enable 0: Auto control by output mode 1: Manual control
0x5074	MAN_CMB_MODE	0x04	RW	Bit[7]: Not used Bit[6]: Manual combine out option 0: Combine out 1: Non-combine out Bit[5:4]: man_cmb_bypass_sel Manual select exposure out when in non-combine out mode Bit[3]: man_cmb_expo_mode_en Manual expo mode enable for combine Bit[2:0]: man_cmb_expo_mode Manual expo mode for combine 001: 2 expo 010: 3 expo 011: Expo Others:Not Used
0x5075	MAN_CMB_MODE_75	0x1B	RW	Bit[7:6]: Manual combine L exposure in 00: L 01: M 10: S 11: V Bit[5:4]: Manual combine M exposure in 00: L 01: M 10: S 11: V Bit[3:2]: Manual combine S exposure in 00: L 01: M 10: S 11: V Bit[1:0]: Manual combine V exposure in 00: L 01: M 10: S 11: V

table A-2 sensor control registers (sheet 131 of 255)

address	register name	default value	R/W	description
0x5076	MAN_ST_ERR0	0x00	RW	Manual Start Frame Error Enable for Single Pipe Bit[7]: Prematrix Bit[6]: XTC Bit[5]: Single gain Bit[4]: AWB reverse Bit[3]: PWL Bit[2]: LFM Bit[1]: Combine Bit[0]: LENC
0x5077	MAN_ST_ERR1	0x00	RW	Bit[7:2]: Not used Bit[1:0]: man_p_st_err_en Manual start frame error enable for parallel pipe [1] Parallel gain [0] DPC
0x507A	STAT_CRC_GLD0	0x00	RW	Bit[7:0]: stat_crc_gld_data Golden data for statistic CRC check
0x507B	STAT_CRC_GLD1	0x00	RW	Bit[7:0]: stat_crc_gld_data Golden data for statistic CRC check
0x507C	MAN_GAIN_HCGEN0	0x00	RW	Bit[7:0]: Manual b_gain for len and PMX
0x507D	MAN_GAIN_HCGEN1	0x00	RW	Bit[7:0]: Manual b_gain for len and PMX
0x507E	MAN_GAIN_HCGEN2	0x00	RW	Bit[7:0]: Manual r_gain for len and PMX
0x507F	MAN_GAIN_HCGEN2_7F	0x00	RW	Bit[7:0]: Manual r_gain for len and PMX
0x5080	SVN_REV0	–	R	Bit[7:0]: ISP releases SVN revision number
0x5081	SVN_REV1	–	R	Bit[7:0]: ISP releases SVN revision number
0x5082	SVN_REV2	–	R	Bit[7:0]: ISP releases SVN revision number
0x5083	SVN_REV3	–	R	Bit[7:0]: ISP releases SVN revision number
0x5084	HSIZE0	–	R	Bit[7:0]: ro_pipe_hsize Read out pipe process (before post-binning) V Size
0x5085	HSIZE1	–	R	Bit[7:0]: ro_pipe_hsize Read out pipe process (before post-binning) V Size
0x5086	VSIZE0	–	R	Bit[7:0]: ro_pipe_vsize Read out pipe process (before post-binning) H Size

table A-2 sensor control registers (sheet 132 of 255)

address	register name	default value	R/W	description
0x5087	VSIZE1	–	R	Bit[7:0]: ro_pipe_vsize Read out pipe process (before post-binning) H Size
0x5088	MAN_GAIN_HCG0_88	–	R	Bit[7:6]: Not used Bit[5:0]: ro_l_convert_gain Read out convert gain for L channel
0x5089	MAN_GAIN_HCG1_89	–	R	Bit[7:0]: ro_l_convert_gain Read out convert gain for L channel
0x508A	MAN_GAIN_LCG0_8A	–	R	Bit[7:6]: Not used Bit[5:0]: ro_m_convert_gain Read out convert gain for M channel
0x508B	MAN_GAIN_LCG1_8B	–	R	Bit[7:0]: ro_m_convert_gain Read out convert gain for M channel
0x508C	MAN_GAIN_SPD0_8C	–	R	Bit[7:6]: Not used Bit[5:0]: ro_s_convert_gain Read out convert gain for S channel
0x508D	MAN_GAIN_SPD1_8D	–	R	Bit[7:0]: ro_s_convert_gain Read out convert gain for S channel
0x508E	MAN_GAIN_VS0_8E	–	R	Bit[7:6]: Not used Bit[5:0]: ro_v_convert_gain Read out convert gain for V channel
0x508F	MAN_GAIN_VS1_8F	–	R	Bit[7:0]: ro_v_convert_gain Read out convert gain for V channel
0x5090	RO_EXP_HCG0	–	R	Bit[7:0]: ro_l_cam_expo Read out camera exposure for L channel
0x5091	RO_EXP_HCG1	–	R	Bit[7:0]: ro_l_cam_expo Read out camera exposure for L channel
0x5092	RO_EXP_LCG0	–	R	Bit[7:0]: ro_m_cam_expo Read out camera exposure for M channel

table A-2 sensor control registers (sheet 133 of 255)

address	register name	default value	R/W	description
0x5093	RO_EXP_LCG1	–	R	Bit[7:0]: ro_m_cam_expo Read out camera exposure for M channel
0x5094	RO_EXP_SPD0	–	R	Bit[7:0]: ro_s_cam_expo Read out camera exposure for S channel
0x5095	RO_EXP_SPD1	–	R	Bit[7:0]: ro_s_cam_expo Read out camera exposure for S channel
0x5096	RO_EXP_VS0	–	R	Bit[7:0]: ro_v_cam_expo Read out camera exposure for V channel
0x5097	RO_EXP_VS1	–	R	Bit[7:0]: ro_v_cam_expo Read out camera exposure for V channel
0x5098	RO_BLC_L0	–	R	Bit[7:2]: Not used Bit[1:0]: ro_l_blc Read out BLC for L channel
0x5099	RO_BLC_L1	–	R	Bit[7:0]: ro_l_blc Read out BLC for L channel
0x509A	RO_BLC_M0	–	R	Bit[7:2]: Not used Bit[1:0]: ro_m_blc Read out BLC for M channel
0x509B	RO_BLC_M1	–	R	Bit[7:0]: ro_m_blc Read out BLC for M channel
0x509C	RO_BLC_S0	–	R	Bit[7:2]: Not used Bit[1:0]: ro_s_blc Read out BLC for S channel
0x509D	RO_BLC_S1	–	R	Bit[7:0]: ro_s_blc Read out BLC for S channel
0x509E	RO_BLC_V0	–	R	Bit[7:2]: Not used Bit[1:0]: ro_v_blc Read out BLC for V channel
0x509F	RO_BLC_V1	–	R	Bit[7:0]: ro_v_blc Read out BLC for V channel
0x50A3	RO_EXP_IDX_HCG0	–	R	Bit[7:6]: Not used Bit[5:0]: ro_l_expo_idx Read out exposure index for L channel

table A-2 sensor control registers (sheet 134 of 255)

address	register name	default value	R/W	description
0x50A4	RO_EXP_IDX_HCG1	–	R	Bit[7:0]: ro_l_expo_idx Read out exposure index for L channel
0x50A5	RO_EXP_IDX_HCG2	–	R	Bit[7:0]: ro_l_expo_idx Read out exposure index for L channel
0x50A6	RO_EXP_IDX_HCG3	–	R	Bit[7:0]: ro_l_expo_idx Read out exposure index for L channel
0x50A7	RO_EXP_IDX_HCG4	–	R	Bit[7:0]: ro_l_expo_idx Read out exposure index for L channel
0x50AB	RO_EXP_IDX_LCG0	–	R	Bit[7:6]: Not used Bit[5:0]: ro_m_expo_idx Read out exposure index for M channel
0x50AC	RO_EXP_IDX_LCG1	–	R	Bit[7:0]: ro_m_expo_idx Read out exposure index for M channel
0x50AD	RO_EXP_IDX_LCG2	–	R	Bit[7:0]: ro_m_expo_idx Read out exposure index for M channel
0x50AE	RO_EXP_IDX_LCG3	–	R	Bit[7:0]: ro_m_expo_idx Read out exposure index for M channel
0x50AF	RO_EXP_IDX_LCG4	–	R	Bit[7:0]: ro_m_expo_idx Read out exposure index for M channel
0x50B3	RO_EXP_IDX_SPD0	–	R	Bit[7:6]: Not used Bit[5:0]: ro_s_expo_idx Read out exposure index for S channel
0x50B4	RO_EXP_IDX_SPD1	–	R	Bit[7:0]: ro_s_expo_idx Read out exposure index for S channel
0x50B5	RO_EXP_IDX_SPD2	–	R	Bit[7:0]: ro_s_expo_idx Read out exposure index for S channel
0x50B6	RO_EXP_IDX_SPD3	–	R	Bit[7:0]: ro_s_expo_idx Read out exposure index for S channel

table A-2 sensor control registers (sheet 135 of 255)

address	register name	default value	R/W	description
0x50B7	RO_EXP_IDX_SPD4	–	R	Bit[7:0]: ro_s_expo_idx Read out exposure index for S channel
0x50BB	RO_EXP_IDX_VS0	–	R	Bit[7:6]: Not used Bit[5:0]: ro_v_expo_idx Read out exposure index for V channel
0x50BC	RO_EXP_IDX_VS1	–	R	Bit[7:0]: ro_v_expo_idx Read out exposure index for V channel
0x50BD	RO_EXP_IDX_VS2	–	R	Bit[7:0]: ro_v_expo_idx Read out exposure index for V channel
0x50BE	RO_EXP_IDX_VS3	–	R	Bit[7:0]: ro_v_expo_idx Read out exposure index for V channel
0x50BF	RO_EXP_IDX_VS4	–	R	Bit[7:0]: ro_v_expo_idx Read out exposure index for V channel
0x50C0	RO_AWBG_HCG_B0	–	R	Bit[7:0]: ro_l_awbg_b Read out L channel AWB B gain
0x50C1	RO_AWBG_HCG_B1	–	R	Bit[7:0]: ro_l_awbg_b Read out L channel AWB B gain
0x50C2	RO_AWBG_HCG_GB0	–	R	Bit[7:0]: ro_l_awbg_gb Read out L channel AWB Gb gain
0x50C3	RO_AWBG_HCG_GB1	–	R	Bit[7:0]: ro_l_awbg_gb Read out L channel AWB Gb gain
0x50C4	RO_AWBG_HCG_GR0	–	R	Bit[7:0]: ro_l_awbg_gr Read out L channel AWB Gr gain
0x50C5	RO_AWBG_HCG_GR1	–	R	Bit[7:0]: ro_l_awbg_gr Read out L channel AWB Gr gain
0x50C6	RO_AWBG_HCG_R0	–	R	Bit[7:0]: ro_l_awbg_r Read out L channel AWB R gain
0x50C7	RO_AWBG_HCG_R1	–	R	Bit[7:0]: ro_l_awbg_r Read out L channel AWB R gain
0x50C8	RO_AWBG_LCG_B0	–	R	Bit[7:0]: ro_m_awbg_b Read out M channel AWB B gain
0x50C9	RO_AWBG_LCG_B1	–	R	Bit[7:0]: ro_m_awbg_b Read out M channel AWB B gain

table A-2 sensor control registers (sheet 136 of 255)

address	register name	default value	R/W	description
0x50CA	RO_AWBG_LCG_GB0	–	R	Bit[7:0]: ro_m_awbg_gb Read out M channel AWB Gb gain
0x50CB	RO_AWBG_LCG_GB1	–	R	Bit[7:0]: ro_m_awbg_gb Read out M channel AWB Gb gain
0x50CC	RO_AWBG_LCG_GR0	–	R	Bit[7:0]: ro_m_awbg_gr Read out M channel AWB Gr gain
0x50CD	RO_AWBG_LCG_GR1	–	R	Bit[7:0]: ro_m_awbg_gr Read out M channel AWB Gr gain
0x50CE	RO_AWBG_LCG_R0	–	R	Bit[7:0]: ro_m_awbg_r Read out M channel AWB R gain
0x50CF	RO_AWBG_LCG_R1	–	R	Bit[7:0]: ro_m_awbg_r Read out M channel AWB R gain
0x50D0	RO_AWBG_SPD_B0	–	R	Bit[7:0]: ro_s_awbg_b Read out S channel AWB B gain
0x50D1	RO_AWBG_SPD_B1	–	R	Bit[7:0]: ro_s_awbg_b Read out S channel AWB B gain
0x50D2	RO_AWBG_SPD_GB0	–	R	Bit[7:0]: ro_s_awbg_gb Read out S channel AWB Gb gain
0x50D3	RO_AWBG_SPD_GB1	–	R	Bit[7:0]: ro_s_awbg_gb Read out S channel AWB Gb gain
0x50D4	RO_AWBG_SPD_GR0	–	R	Bit[7:0]: ro_s_awbg_gr Read out S channel AWB Gr gain
0x50D5	RO_AWBG_SPD_GR1	–	R	Bit[7:0]: ro_s_awbg_gr Read out S channel AWB Gr gain
0x50D6	RO_AWBG_SPD_R0	–	R	Bit[7:0]: ro_s_awbg_r Read out S channel AWB R gain
0x50D7	RO_AWBG_SPD_R1	–	R	Bit[7:0]: ro_s_awbg_r Read out S channel AWB R gain
0x50D8	RO_AWBG_VS_B0	–	R	Bit[7:0]: ro_v_awbg_b Read out V channel AWB B gain
0x50D9	RO_AWBG_VS_B1	–	R	Bit[7:0]: ro_v_awbg_b Read out V channel AWB B gain
0x50DA	RO_AWBG_VS_GB0	–	R	Bit[7:0]: ro_v_awbg_gb Read out V channel AWB Gb gain
0x50DB	RO_AWBG_VS_GB1	–	R	Bit[7:0]: ro_v_awbg_gb Read out V channel AWB Gb gain
0x50DC	RO_AWBG_VS_GR0	–	R	Bit[7:0]: ro_v_awbg_gr Read out V channel AWB Gr gain

table A-2 sensor control registers (sheet 137 of 255)

address	register name	default value	R/W	description
0x50DD	RO_AWBG_VS_GR1	–	R	Bit[7:0]: ro_v_awbg_gr Read out V channel AWB Gr gain
0x50DE	RO_AWBG_VS_R0	–	R	Bit[7:0]: ro_v_awbg_r Read out V channel AWB R gain
0x50DF	RO_AWBG_VS_R1	–	R	Bit[7:0]: ro_v_awbg_r Read out V channel AWB R gain
0x50E0	RO_TEST_ERR_STATUS0	–	R	Bit[7:0]: ro_test_single_err Test line, single pipe check err status
0x50E1	RO_TEST_ERR_STATUS1	–	R	Bit[7:0]: ro_test_parallel_err Test line, parallel pipe check err status
0x50E2	RO_TEST_ERR_STATUS2	–	R	Bit[7:0]: ro_test_mem_err Test line, memory check err status
0x50E3	RO_TEST_ERR_STATUS3	–	R	Bit[7:0]: ro_test_mem_err Test line, memory check err status
0x50E7	RO_SORT_INDEX	–	R	Bit[7:6]: ro_sort_index_L Sort index 00: Original L 01: Original M 10: Original S 11: Original V Bit[5:4]: ro_sort_index_M Sort index 00: Original L 01: Original M 10: Original S 11: Original V Bit[3:2]: ro_sort_index_S Sort index 00: Original L 01: Original M 10: Original S 11: Original V Bit[1:0]: ro_sort_index_V Sort index 00: Original L 01: Original M 10: Original S 11: Original V
0x50EA	STAT_CRC_RST0	–	R	Bit[7:0]: ro_stat_crc_rst_data Result for statistic CRC check
0x50EB	STAT_CRC_RST1	–	R	Bit[7:0]: ro_stat_crc_rst_data Result for statistic CRC check

table A-2 sensor control registers (sheet 138 of 255)

address	register name	default value	R/W	description
0x5100	SYNC_BUFF_0	0x00	RW	Bit[7:6]: Not used Bit[5]: disable_test_en Disable test line Bit[4]: disable_bypass_en Disable bypass line Bit[3]: disable_dumy_en Disable dummy line Bit[2:1]: blk_sel 00: isp_blank_i 01: sync_buff calculated by itself 10: Manual hblank 11: Not used Bit[0]: work_mode manual enable
0x5101	SYNC_BUFF_1	0x10	RW	Bit[7:5]: Not used Bit[4]: dmy_cal_opt Bit[3]: Not used Bit[2:0]: work_mode_man Manual work_mode
0x5102	SYNC_BUFF_2	0x00	RW	Bit[7:0]: man_href_h Manual length of first HREF
0x5103	SYNC_BUFF_3	0x00	RW	Bit[7:0]: man_href_h Manual length of first HREF
0x5106	SYNC_BUFF_6	0x00	RW	Bit[7:0]: Manual blank
0x5107	SYNC_BUFF_7	0x00	RW	Bit[7:0]: Manual blank
0x5108	SYNC_BUFF_8	–	R	Bit[7:0]: ro_hsize Hsize read out
0x5109	SYNC_BUFF_9	–	R	Bit[7:0]: ro_hsize Hsize read out
0x510A	SYNC_BUFF_A	–	R	Bit[7:0]: ro_vsize Vsize read out
0x510B	SYNC_BUFF_B	–	R	Bit[7:0]: ro_vsize Vsize read out
0x510C	SYNC_BUFF_C	–	R	Bit[7:0]: ro_lcnt_in Input L expo ln_cnt
0x510D	SYNC_BUFF_D	–	R	Bit[7:0]: ro_lcnt_in Input L expo ln_cnt
0x510E	SYNC_BUFF_E	–	R	Bit[7:0]: ro_scnt_in Input S expo ln_cnt
0x510F	SYNC_BUFF_F	–	R	Bit[7:0]: ro_scnt_in Input S expo ln_cnt

table A-2 sensor control registers (sheet 139 of 255)

address	register name	default value	R/W	description
0x5110	SYNC_BUFF_10	–	R	Bit[7:0]: ro_mcnt_in Input M expo ln_cnt
0x5111	SYNC_BUFF_11	–	R	Bit[7:0]: ro_mcnt_in Input M expo ln_cnt
0x5112	SYNC_BUFF_12	–	R	Bit[7:0]: ro_vcnt_in Input V expo ln_cnt
0x5113	SYNC_BUFF_13	–	R	Bit[7:0]: ro_vcnt_in Input V expo ln_cnt
0x5114	SYNC_BUFF_14	–	R	Bit[7:0]: ro_lcnt_out Output L expo ln_cnt
0x5115	SYNC_BUFF_15	–	R	Bit[7:0]: ro_lcnt_out Output L expo ln_cnt
0x5116	SYNC_BUFF_16	–	R	Bit[7:0]: ro_scnt_out Output S expo ln_cnt
0x5117	SYNC_BUFF_17	–	R	Bit[7:0]: ro_scnt_out Output S expo ln_cnt
0x5118	SYNC_BUFF_18	–	R	Bit[7:0]: ro_mcnt_out Output M expo ln_cnt
0x5119	SYNC_BUFF_19	–	R	Bit[7:0]: ro_mcnt_out Output M expo ln_cnt
0x511A	SYNC_BUFF_1A	–	R	Bit[7:0]: ro_vcnt_out Output V expo ln_cnt
0x511B	SYNC_BUFF_1B	–	R	Bit[7:0]: ro_vcnt_out Output V expo ln_cnt
0x511D	SYNC_BUFF_1D	–	R	Bit[7:1]: Not used Bit[0]: ro_ln_err ln_cnt error flag
0x511E	SYNC_BUFF_1E	–	R	Bit[7:1]: Not used Bit[0]: ro_p0_crc_err Pipe0 CRC error flag
0x511F	SYNC_BUFF_1F	–	R	Bit[7:1]: Not used Bit[0]: ro_p1_crc_err Pipe1 CRC error flag
0x5180	CDEFECTPIXELOTP FILTER_NEW_L_0	0x80	RW	Cluster_00 Bit[7]: cluster0_flag Bit[6:5]: cluster0_xtype Bit[4:3]: cluster0_ytype Bit[2]: cluster0_low_gain Bit[1:0]: cluster0_pdtype

table A-2 sensor control registers (sheet 140 of 255)

address	register name	default value	R/W	description
0x5181	CDEFECTPIXELOTP FILTER_NEW_L_1	0x0B	RW	Bit[7:0]: Cluster_01[7:0] cluster0_x_coordinate[15:4]
0x5182	CDEFECTPIXELOTP FILTER_NEW_L_2	0xF0	RW	Bit[7:0]: Cluster_02[7:4] cluster0_x_coordinate[3:0]
0x5183	CDEFECTPIXELOTP FILTER_NEW_L_3	0x20	RW	Cluster_03 Bit[7:6]: Not used Bit[5]: cluster0_fix_replace_enable Bit[4]: cluster0_fix_replace_ptn Bit[3:0]: cluster0_y_coordinate[3:0]
0x5184	CDEFECTPIXELOTP FILTER_NEW_L_4	0x86	RW	Bit[7:0]: cluster_10
0x5185	CDEFECTPIXELOTP FILTER_NEW_L_5	0x10	RW	Bit[7:0]: cluster_11
0x5186	CDEFECTPIXELOTP FILTER_NEW_L_6	0x00	RW	Bit[7:0]: cluster_12
0x5187	CDEFECTPIXELOTP FILTER_NEW_L_7	0x30	RW	Cluster_13 Bit[7:6]: Not used Bit[5]: fix_replace_enable Bit[4]: fix_replace_ptn Bit[3:0]: y_org
0x5188	CDEFECTPIXELOTP FILTER_NEW_L_8	0x85	RW	Bit[7:0]: cluster_20
0x5189	CDEFECTPIXELOTP FILTER_NEW_L_9	0x07	RW	Bit[7:0]: cluster_21
0x518A	CDEFECTPIXELOTP FILTER_NEW_L_A	0xD0	RW	Bit[7:0]: cluster_22
0x518B	CDEFECTPIXELOTP FILTER_NEW_L_B	0x01	RW	Cluster_23 Bit[7:6]: Not used Bit[5]: fix_replace_enable Bit[4]: fix_replace_ptn Bit[3:0]: y_org
0x518C	CDEFECTPIXELOTP FILTER_NEW_L_C	0x81	RW	Bit[7:0]: cluster_30
0x518D	CDEFECTPIXELOTP FILTER_NEW_L_D	0x0B	RW	Bit[7:0]: cluster_31
0x518E	CDEFECTPIXELOTP FILTER_NEW_L_E	0xD0	RW	Bit[7:0]: cluster_32

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address	register name	default value	R/W	description
0x518F	CDEFECTPIXELOTP FILTER_NEW_L_F	0x01	RW	Cluster_33 Bit[7:6]: Not used Bit[5]: fix_replace_enable Bit[4]: fix_replace_ptn Bit[3:0]: y_org
0x5190	CDEFECTPIXELOTP FILTER_NEW_L_10	0x86	RW	Bit[7:0]: cluster_40
0x5191	CDEFECTPIXELOTP FILTER_NEW_L_11	0x04	RW	Bit[7:0]: cluster_41
0x5192	CDEFECTPIXELOTP FILTER_NEW_L_12	0x10	RW	Bit[7:0]: cluster_42
0x5193	CDEFECTPIXELOTP FILTER_NEW_L_13	0x02	RW	Cluster_43 Bit[7:6]: Not used Bit[5]: fix_replace_enable Bit[4]: fix_replace_ptn Bit[3:0]: y_org
0x5194	CDEFECTPIXELOTP FILTER_NEW_L_14	0x85	RW	Bit[7:0]: cluster_50
0x5195	CDEFECTPIXELOTP FILTER_NEW_L_15	0x09	RW	Bit[7:0]: cluster_51
0x5196	CDEFECTPIXELOTP FILTER_NEW_L_16	0x80	RW	Bit[7:0]: cluster_52
0x5197	CDEFECTPIXELOTP FILTER_NEW_L_17	0x32	RW	Cluster_53 Bit[7:6]: Not used Bit[5]: fix_replace_enable Bit[4]: fix_replace_ptn Bit[3:0]: y_org
0x5198	CDEFECTPIXELOTP FILTER_NEW_L_18	0x81	RW	Bit[7:0]: cluster_60
0x5199	CDEFECTPIXELOTP FILTER_NEW_L_19	0x04	RW	Bit[7:0]: cluster_61
0x519A	CDEFECTPIXELOTP FILTER_NEW_L_1A	0x20	RW	Bit[7:0]: cluster_62
0x519B	CDEFECTPIXELOTP FILTER_NEW_L_1B	0x33	RW	Cluster_63 Bit[7:6]: Not used Bit[5]: fix_replace_enable Bit[4]: fix_replace_ptn Bit[3:0]: y_org
0x519C	CDEFECTPIXELOTP FILTER_NEW_L_1C	0x86	RW	Bit[7:0]: cluster_70

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address	register name	default value	R/W	description
0x519D	CDEFECTPIXELOTP FILTER_NEW_L_1D	0x09	RW	Bit[7:0]: cluster_71
0x519E	CDEFECTPIXELOTP FILTER_NEW_L_1E	0xB0	RW	Bit[7:0]: cluster_72
0x519F	CDEFECTPIXELOTP FILTER_NEW_L_1F	0x03	RW	Cluster_73 Bit[7:6]: Not used Bit[5]: fix_replace_enable Bit[4]: fix_replace_ptn Bit[3:0]: y_org
0x51A0	CDEFECTPIXELOTP FILTER_NEW_L_20	0x85	RW	Bit[7:0]: cluster_80
0x51A1	CDEFECTPIXELOTP FILTER_NEW_L_21	0x01	RW	Bit[7:0]: cluster_81
0x51A2	CDEFECTPIXELOTP FILTER_NEW_L_22	0x90	RW	Bit[7:0]: cluster_82
0x51A3	CDEFECTPIXELOTP FILTER_NEW_L_23	0x04	RW	Cluster_83 Bit[7:6]: Not used Bit[5]: fix_replace_enable Bit[4]: fix_replace_ptn Bit[3:0]: y_org
0x51A4	CDEFECTPIXELOTP FILTER_NEW_L_24	0x86	RW	Bit[7:0]: cluster_90
0x51A5	CDEFECTPIXELOTP FILTER_NEW_L_25	0x16	RW	Bit[7:0]: cluster_91
0x51A6	CDEFECTPIXELOTP FILTER_NEW_L_26	0x80	RW	Bit[7:0]: cluster_92
0x51A7	CDEFECTPIXELOTP FILTER_NEW_L_27	0x04	RW	Cluster_93 Bit[7:6]: Not used Bit[5]: fix_replace_enable Bit[4]: fix_replace_ptn Bit[3:0]: y_org
0x51A8	CDEFECTPIXELOTP FILTER_NEW_L_28	0x82	RW	Bit[7:0]: cluster_a0
0x51A9	CDEFECTPIXELOTP FILTER_NEW_L_29	0x06	RW	Bit[7:0]: cluster_a1
0x51AA	CDEFECTPIXELOTP FILTER_NEW_L_2A	0x60	RW	Bit[7:0]: cluster_a2

table A-2 sensor control registers (sheet 143 of 255)

address	register name	default value	R/W	description
0x51AB	CDEFECTPIXELOTP FILTER_NEW_L_2B	0x05	RW	Cluster_a3 Bit[7:6]: Not used Bit[5]: fix_replace_enable Bit[4]: fix_replace_ptn Bit[3:0]: y_org
0x51AC	CDEFECTPIXELOTP FILTER_NEW_L_2C	0x84	RW	Bit[7:0]: cluster_b0
0x51AD	CDEFECTPIXELOTP FILTER_NEW_L_2D	0x10	RW	Bit[7:0]: cluster_b1
0x51AE	CDEFECTPIXELOTP FILTER_NEW_L_2E	0x00	RW	Bit[7:0]: cluster_b2
0x51AF	CDEFECTPIXELOTP FILTER_NEW_L_2F	0x05	RW	Cluster_b3 Bit[7:6]: Not used Bit[5]: fix_replace_enable Bit[4]: fix_replace_ptn Bit[3:0]: y_org
0x5200	PRE_RAWBIN_HCG_0	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight0
0x5201	PRE_RAWBIN_HCG_1	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight1
0x5202	PRE_RAWBIN_HCG_2	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight2
0x5203	PRE_RAWBIN_HCG_3	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight3
0x5204	PRE_RAWBIN_HCG_4	0x00	RW	Bit[7:1]: Not used Bit[0]: blc_contr_en
0x5240	PRE_ISP_0_HCG	0x0F	RW	Bit[7:6]: Not used Bit[5:4]: bar_style Bit[3]: isp_test Clear last four bits of image data to 0 Bit[2]: Transparent mode enable Combine test data and image data together Bit[1]: Rolling bar mode enable Bit[0]: Test pattern enable
0x5241	PRE_ISP_1_HCG	0x00	RW	Bit[7:4]: Not used Bit[3]: Bayer constant test pattern enable Bit[2:0]: Test image select 0, color bar
0x5242	PRE_ISP_2_HCG	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bayer_const_b

table A-2 sensor control registers (sheet 144 of 255)

address	register name	default value	R/W	description
0x5243	PRE_ISP_3_HCG	0x00	RW	Bit[7:0]: bayer_const_b Constant pixel value for B channel
0x5244	PRE_ISP_4_HCG	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bayer_const_gb
0x5245	PRE_ISP_5_HCG	0x00	RW	Bit[7:0]: bayer_const_gb Constant pixel value for Gb channel
0x5246	PRE_ISP_6_HCG	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bayer_const_gr
0x5247	PRE_ISP_7_HCG	0x00	RW	Bit[7:0]: bayer_const_gr Constant pixel value for Gr channel
0x5248	PRE_ISP_8_HCG	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bayer_const_r
0x5249	PRE_ISP_9_HCG	0x00	RW	Bit[7:0]: bayer_const_r Constant pixel value for R channel
0x524A	PRE_ISP_A_HCG	0x00	RW	Bit[7]: Not used Bit[6]: start_man_en Manual X direction start and Y direction start of sensor array enable 0: Disable 1: Enable Bit[5]: Offset manual enable 0: Disable 1: Enable Bit[4]: Flip option for Y offset Bit[3]: Mirror option for Y offset Bit[2]: end_man Manual X direction end and Y direction end of sensor array enable 0: Disable 1: Enable Bit[1]: Digital test row bypass enable Bit[0]: Window cut enable 0: Disable 1: Enable
0x524B	PRE_ISP_B_HCG	0x00	RW	Bit[7:6]: Not used Bit[5:1]: X direction skip step manual enable 0: Disable 1: Enable Bit[0]: x_skip_man_en X direction skip step value

table A-2 sensor control registers (sheet 145 of 255)

address	register name	default value	R/W	description
0x524C	PRE_ISP_C_HCG	0x00	RW	Bit[7:6]: Not used Bit[5:1]: y_skip_man X direction skip step manual enable 0: Disable 1: Enable Bit[0]: y_skip_man_en X direction skip step value
0x524D	PRE_ISP_D_HCG	0x00	RW	Bit[7:0]: ln_number
0x524E	PRE_ISP_E_HCG	0x00	RW	Bit[7:0]: Line number interrupt
0x524F	PRE_ISP_F_HCG	0x00	RW	Bit[7:0]: man_x_offset
0x5250	PRE_ISP_1_HCG0	0x00	RW	Bit[7:0]: Manual X direction offset in sensor array
0x5251	PRE_ISP_1_HCG1	0x00	RW	Bit[7:0]: man_y_offset
0x5252	PRE_ISP_1_HCG2	0x00	RW	Bit[7:0]: Manual Y direction offset in sensor array
0x5253	PRE_ISP_1_HCG3	0x00	RW	Bit[7:0]: man_x_start
0x5254	PRE_ISP_1_HCG4	0x00	RW	Bit[7:0]: Manual X start in sensor array
0x5255	PRE_ISP_1_HCG5	0x00	RW	Bit[7:0]: man_y_start
0x5256	PRE_ISP_1_HCG6	0x00	RW	Bit[7:0]: Manual Y start in sensor array
0x5257	PRE_ISP_1_HCG7	0x00	RW	Bit[7:0]: man_x_end
0x5258	PRE_ISP_1_HCG8	0x00	RW	Bit[7:0]: man_x_end Manual Y direction offset in sensor array
0x5259	PRE_ISP_1_HCG9	0x00	RW	Bit[7:0]: man_y_end
0x525A	PRE_ISP_1_HCGA	0x00	RW	Bit[7:0]: man_y_end Manual Y direction offset in sensor array
0x525B	PRE_ISP_1_HCGB	0x0F	RW	Bit[7:0]: Ratio fraction part
0x525C	PRE_ISP_HCG_ISP_CTRL_RO_0	–	R	Bit[7:5]: Not used Bit[4:0]: x_even_inc X direction increase step of even points
0x525D	PRE_ISP_HCG_ISP_CTRL_RO_1	–	R	Bit[7:5]: Not used Bit[4:0]: x_odd_inc X direction increase step of odd points

table A-2 sensor control registers (sheet 146 of 255)

address	register name	default value	R/W	description
0x525E	PRE_ISP_HCG_ISP_CTRL_RO_2	–	R	Bit[7:5]: Not used Bit[4:0]: y_even_inc Y direction increase step of even points
0x525F	PRE_ISP_HCG_ISP_CTRL_RO_3	–	R	Bit[7:5]: Not used Bit[4:0]: y_odd_inc Y direction increase step of odd points
0x5260	PRE_ISP_HCG_ISP_CTRL_RO_4	–	R	Bit[7:0]: X direction offset in sensor array
0x5261	PRE_ISP_HCG_ISP_CTRL_RO_5	–	R	Bit[7:0]: x_offset X direction increase step of odd points
0x5262	PRE_ISP_HCG_ISP_CTRL_RO_6	–	R	Bit[7:0]: Y direction offset in sensor array
0x5263	PRE_ISP_HCG_ISP_CTRL_RO_7	–	R	Bit[7:0]: y_offset Y direction increase step of odd points
0x5264	PRE_ISP_HCG_ISP_CTRL_RO_8	–	R	Bit[7:0]: Pixel counter
0x5265	PRE_ISP_HCG_ISP_CTRL_RO_9	–	R	Bit[7:0]: Pixel counter
0x5266	PRE_ISP_HCG_ISP_CTRL_RO_A	–	R	Bit[7:0]: Line counter
0x5267	PRE_ISP_HCG_ISP_CTRL_RO_B	–	R	Bit[7:0]: Line counter
0x5268	PRE_ISP_HCG_ISP_CTRL_RO_C	–	R	Bit[7:0]: Software version
0x5269	PRE_ISP_HCG_ISP_CTRL_RO_D	–	R	Bit[7:0]: Hardware version
0x5280	AWB_GAIN_HCG_0	0x04	RW	Bit[7:0]: Manual AWB gain[0]
0x5281	AWB_GAIN_HCG_1	0x00	RW	Bit[7:0]: Manual AWB gain[0]
0x5282	AWB_GAIN_HCG_2	0x04	RW	Bit[7:0]: Manual AWB gain[1]
0x5283	AWB_GAIN_HCG_3	0x00	RW	Bit[7:0]: Manual AWB gain[1]
0x5284	AWB_GAIN_HCG_4	0x04	RW	Bit[7:0]: Manual AWB gain[2]
0x5285	AWB_GAIN_HCG_5	0x00	RW	Bit[7:0]: Manual AWB gain[2]
0x5286	AWB_GAIN_HCG_6	0x04	RW	Bit[7:0]: Manual AWB gain[3]

table A-2 sensor control registers (sheet 147 of 255)

address	register name	default value	R/W	description
0x5287	AWB_GAIN_HCG_7	0x00	RW	Bit[7:0]: Manual AWB gain[3]
0x5288	AWB_GAIN_HCG_8	0x00	RW	Bit[7:5]: Not used Bit[4]: gain_man_en Manual gain enable Bit[3]: blc_man_en Manual BLC enable Bit[2]: cfa_ptn_man_en Manual CFA pattern enable Bit[1:0]: cfa_ptn_man Manual CFA pattern
0x5289	AWB_GAIN_HCG_9	0x00	RW	Bit[7:2]: Not used Bit[1:0]: blc_man Manual BLC
0x528A	AWB_GAIN_HCG_10	0x00	RW	Bit[7:0]: blc_man Manual BLC
0x5290	AWB_GAIN_HCG_11	–	R	Bit[7:0]: Version
0x5291	AWB_GAIN_HCG_12	–	R	Bit[7:0]: Version
0x52C0	DPC_HCG_NUM_0	0x33	RW	Bit[7:6]: correct_opt Option to correct G/Br pixel Bit[5:4]: Edge filling option Bit[3]: manual_mode_en Enable manual mode Bit[2]: Enable cross cluster correction Bit[1]: Enable black pixel correction Bit[0]: Enable white pixel correction
0x52C1	DPC_HCG_NUM_1	0x88	RW	Bit[7:4]: couplet_bgain_margin Black couplet defect pixel correction gain margin Bit[3:0]: couplet_wgain_margin White couplet defect pixel correction gain margin
0x52C2	DPC_HCG_NUM_2	0x88	RW	Bit[7:4]: cluster_b_th Black couplet threshold ratio Bit[3:0]: cluster_w_th White couplet threshold ratio
0x52C3	DPC_HCG_NUM_3	0x08	RW	Bit[7:0]: couplet_wgain_th White couplet defect pixel correction gain threshold
0x52C4	DPC_HCG_NUM_4	0x08	RW	Bit[7:0]: couplet_bgain_th Black couplet defect pixel correction gain threshold
0x52C5	DPC_HCG_NUM_5	0xFF	RW	Bit[7:0]: Saturation threshold

table A-2 sensor control registers (sheet 148 of 255)

address	register name	default value	R/W	description
0x52C6	DPC_HCG_0	0x00	RW	Bit[7:4]: dp_num_list0 Max allowed defect pixel list0 Bit[3:0]: dp_num_list1 Max allowed defect pixel list1
0x52C7	DPC_HCG_1	0x12	RW	Bit[7:4]: dp_num_list2 Max allowed defect pixel list2 Bit[3:0]: dp_num_list3 Max allowed defect pixel list3
0x52C8	DPC_HCG_2	0x04	RW	Bit[7:0]: w_th_list0 White pixel threshold list
0x52C9	DPC_HCG_3	0x04	RW	Bit[7:0]: w_th_list1 White pixel threshold list
0x52CA	DPC_HCG_4	0x04	RW	Bit[7:0]: w_th_list2 White pixel threshold list
0x52CB	DPC_HCG_5	0x04	RW	Bit[7:0]: w_th_list3 White pixel threshold list
0x52CC	DPC_HCG_6	0x04	RW	Bit[7:0]: b_th_list0 Black pixel threshold list
0x52CD	DPC_HCG_7	0x04	RW	Bit[7:0]: b_th_list1 Black pixel threshold list
0x52CE	DPC_HCG_8	0x04	RW	Bit[7:0]: b_th_list2 Black pixel threshold list
0x52CF	DPC_HCG_9	0x04	RW	Bit[7:0]: b_th_list3 Black pixel threshold list
0x52D0	DPC_HCG_A	0x03	RW	Bit[7:0]: gain_list0 Gain control point
0x52D1	DPC_HCG_B	0x08	RW	Bit[7:0]: gain_list1 Gain control point
0x52D2	DPC_HCG_C	0x0C	RW	Bit[7:0]: gain_list2 Gain control point
0x52D4	DPC_HCG_14	0x00	RW	Bit[7:4]: Not used Bit[3:0]: roi_start_x ROI top left X location
0x52D5	DPC_HCG_15	0x00	RW	Bit[7:0]: roi_start_x
0x52D6	DPC_HCG_16	0x00	RW	Bit[7:4]: Not used Bit[3:0]: roi_start_y ROI top left Y location
0x52D7	DPC_HCG_17	0x00	RW	Bit[7:0]: roi_start_y

table A-2 sensor control registers (sheet 149 of 255)

address	register name	default value	R/W	description
0x52D8	DPC_HCG_18	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI width
0x52D9	DPC_HCG_19	0x0F	RW	Bit[7:0]: roi_width
0x52DA	DPC_HCG_1A	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI height
0x52DB	DPC_HCG_1B	0x0F	RW	Bit[7:0]: roi_height
0x52DC	DPC_HCG_1C	0xFF	RW	Bit[7:0]: roi_dp_num Number of DP locations can be saved
0x52DD	DPC_HCG_1D	0xFF	RW	Bit[7:0]: roi_dp_num
0x52DE	DPC_HCG_1E	0xFF	RW	Bit[7:0]: roi_dp_num
0x52E6	DPC_HCG_26	–	R	Bit[7:0]: w_th
0x52E7	DPC_HCG_27	–	R	Bit[7:0]: b_th
0x52E8	DPC_HCG_28	–	R	Bit[7:4]: Not used Bit[3:0]: max_dp_num
0x52E9	DPC_HCG_29	–	R	Bit[7:2]: Not used Bit[1]: couplet_w_en Bit[0]: couplet_b_en
0x52EA	DPC_HCG_2A	–	R	Bit[7:0]: DPCount
0x52EB	DPC_HCG_2B	–	R	Bit[7:0]: DPCount
0x52EC	DPC_HCG_2C	–	R	Bit[7:0]: DPCount
0x52ED	DPC_HCG_2D	–	R	Bit[7:0]: DPROICount
0x52EE	DPC_HCG_2E	–	R	Bit[7:0]: DPROICount
0x52EF	DPC_HCG_2F	–	R	Bit[7:0]: DPROICount
0x5300	OTP_DPC_HCG_0	0x02	RW	Bit[7]: Mirror option Bit[6]: Flip option Bit[5]: Disable mirror and flip Bit[4]: Auto mode using gain enable Bit[3]: Auto mode using exposure enable Bit[2]: ThresEn Detection enable Bit[1]: Fixed pattern selection Bit[0]: Fixed pattern enable

table A-2 sensor control registers (sheet 150 of 255)

address	register name	default value	R/W	description
0x5301	OTP_DPC_HCG_1	0x10	RW	Bit[7:5]: Not used Bit[4]: GainSelect Gain-dependent OTPDPC cluster enable Bit[3]: EnableBWBin2 BW binning mode Bit[2]: Disable binning Bit[1]: Manual increase step enable Bit[0]: Manual offset enable
0x5302	OTP_DPC_HCG_2	0x30	RW	Bit[7]: Reserved Bit[6:4]: Recovery method selection Bit[3:2]: Horizontal binning mode Bit[1:0]: Vertical binning mode
0x5303	OTP_DPC_HCG_3	0x18	RW	Bit[7:4]: GainSelectThres Gain-dependent threshold Bit[3:0]: OTPThres Detection threshold
0x5304	OTP_DPC_HCG_4	0x01	RW	Bit[7:5]: Not used Bit[4:0]: ManualXEvenInc Manual X even step
0x5305	OTP_DPC_HCG_5	0x01	RW	Bit[7:5]: Not used Bit[4:0]: ManualXOddInc Manual X odd step
0x5306	OTP_DPC_HCG_6	0x01	RW	Bit[7:5]: Not used Bit[4:0]: ManualYEvenInc Manual Y even step
0x5307	OTP_DPC_HCG_7	0x01	RW	Bit[7:5]: Not used Bit[4:0]: ManualYOddInc Manual Y odd step
0x5309	OTP_DPC_HCG_8	0x07	RW	Bit[7:6]: Not used Bit[5:0]: GainLimit Gain threshold
0x530A	OTP_DPC_HCG_A	0x00	RW	Bit[7]: Not used Bit[6:0]: ExposureLimit Exposure threshold
0x530B	OTP_DPC_HCG_B	0x00	RW	Bit[7:0]: ExposureLimit Exposure threshold
0x530C	OTP_DPC_HCG_C	0x00	RW	Bit[7:0]: Manual X offset
0x530D	OTP_DPC_HCG_D	0x00	RW	Bit[7:0]: Manual X offset
0x530E	OTP_DPC_HCG_E	0x00	RW	Bit[7:0]: Manual Y offset
0x530F	OTP_DPC_HCG_F	0x00	RW	Bit[7:0]: Manual Y offset

table A-2 sensor control registers (sheet 151 of 255)

address	register name	default value	R/W	description
0x5310	OTP_DPC_HCG_10	0x00	RW	Bit[7]: flip_mirror_man_en Bit[6]: flip_man Bit[5]: mirror_man Bit[4]: Cluster data bypass enable Bit[3]: Work mode manual enable Bit[2:0]: Work mode manual
0x5311	OTP_DPC_HCG_11	0x00	RW	Bit[7]: Not used Bit[6]: dis_proc_gate Disable detect and remove blocks' clock gating option Bit[5]: dis_mem_rd_gate Disable get_cluster block's clock gating option Bit[4]: dis_start_gate Disable start frame process logic clock gating option Bit[3]: dis_buf3_gate Disable cluster_buf 3 of long exposure block's clock gating option Bit[2]: dis_buf2_gate Disable cluster_buf 2 of long exposure block's clock gating option Bit[1]: dis_buf1_gate Disable cluster_buf 1 of long exposure block's clock gating option Bit[0]: dis_buf0_gate Disable cluster_buf 0 of long exposure block's clock gating option

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address	register name	default value	R/W	description
0x5312	OTP_DPC_HCG_12	0x00	RW	Bit[7]: y_bin_man_en Manual Y direction binning enable Bit[6]: y_bin4_man Manual Y direction bin4 enable, reserved Bit[5]: y_bin3_man Manual Y direction bin3 enable, reserved Bit[4]: y_bin2_man Manual Y direction bin2 enable Bit[3]: x_bin_man_en Manual X direction binning enable Bit[2]: x_bin4_man Manual X direction bin4 enable, reserved Bit[1]: x_bin3_man Manual X direction bin3 enable, reserved Bit[0]: x_bin2_man Manual X direction bin2 enable
0x5313	OTP_DPC_HCG_13	0x00	RW	Bit[7]: Not used Bit[6]: OTP eFUSE DEBUG mode enable Read out data of debug address in eFUSE Bit[5]: Manual size enable Bit[4]: bwbin2_man_en Bit[3]: y_bwbin2_man Manual Y direction BW binning enable Bit[2]: x_bwbin2_man Manual X direction BW binning enable Bit[1]: position_debug_en Replace detected defect pixel with its position in sensor array Bit[0]: Position counter select 0: H counter 1: V counter
0x5314	OTP_DPC_HCG_14	0x70	RW	Bit[7:0]: OTP eFUSE start address
0x5315	OTP_DPC_HCG_15	0x70	RW	Bit[7:0]: OTP eFUSE start address
0x5316	OTP_DPC_HCG_16	0x73	RW	Bit[7:0]: OTP eFUSE end address
0x5317	OTP_DPC_HCG_17	0xFF	RW	Bit[7:0]: OTP eFUSE end address
0x5318	OTP_DPC_HCG_18	0x05	RW	Bit[7:0]: Manual X direction end in sensor array

table A-2 sensor control registers (sheet 153 of 255)

address	register name	default value	R/W	description
0x5319	OTP_DPC_HCG_19	0x38	RW	Bit[7:0]: Manual X direction end in sensor array
0x531A	OTP_DPC_HCG_1A	0x00	RW	Bit[7:0]: OTP eFUSE debug address
0x531B	OTP_DPC_HCG_1B	0x00	RW	Bit[7:0]: OTP eFUSE debug address
0x531C	OTP_DPC_HCG_1C	0x00	RW	Bit[7:0]: Manual vsize
0x531D	OTP_DPC_HCG_1D	0x00	RW	Bit[7:0]: Manual vsize
0x531E	OTP_DPC_HCG_1E	0x00	RW	Bit[7:0]: Manual hsize
0x531F	OTP_DPC_HCG_1F	0x00	RW	Bit[7:0]: Manual hsize
0x5320	OTP_DPC_HCG_20	–	R	Bit[7:0]: Hsize[15:8]
0x5321	OTP_DPC_HCG_21	–	R	Bit[7:0]: Hsize[7:0]
0x5322	OTP_DPC_HCG_22	–	R	Bit[7:0]: Vsize[15:8]
0x5323	OTP_DPC_HCG_23	–	R	Bit[7:0]: Vsize[7:0]
0x5324	OTP_DPC_HCG_24	–	R	Bit[7:0]: X direction offset in sensor array
0x5325	OTP_DPC_HCG_25	–	R	Bit[7:0]: X direction offset in sensor array
0x5326	OTP_DPC_HCG_26	–	R	Bit[7:0]: Y direction offset in sensor array
0x5327	OTP_DPC_HCG_27	–	R	Bit[7:0]: Y direction offset in sensor array
0x5329	OTP_DPC_HCG_29	–	R	Bit[7]: ro_y_bwbin2 Y direction BW binning Bit[6]: Y direction bin4 Bit[5]: Y direction bin3 Bit[4]: Y direction bin2 Bit[3]: ro_x_bwbin2 X direction BW binning Bit[2]: X direction bin4 Bit[1]: X direction bin3 Bit[0]: X direction bin2
0x532A	OTP_DPC_HCG_2A	–	R	Bit[7:0]: X direction end position in sensor array
0x532B	OTP_DPC_HCG_2B	–	R	Bit[7:0]: X direction end position in sensor array
0x532C	OTP_DPC_HCG_2C	–	R	Bit[7:5]: Not used Bit[4:0]: ro_x_even_inc X direction increase step of even points

table A-2 sensor control registers (sheet 154 of 255)

address	register name	default value	R/W	description
0x532D	OTP_DPC_HCG_2D	–	R	Bit[7:5]: Not used Bit[4:0]: ro_x_odd_inc X direction increase step of odd points
0x532E	OTP_DPC_HCG_2E	–	R	Bit[7:5]: Not used Bit[4:0]: ro_y_even_inc Y direction increase step of even points
0x532F	OTP_DPC_HCG_2F	–	R	Bit[7:5]: Not used Bit[4:0]: ro_y_odd_inc Y direction increase step of odd points
0x5331	OTP_DPC_HCG_31	–	R	Bit[7:0]: ro_debug_data Data of debug address in OTP eFUSE
0x5332	OTP_DPC_HCG_32	–	R	Bit[7:0]: Software version
0x5333	OTP_DPC_HCG_33	–	R	Bit[7:0]: Hardware version
0x5337	OTP_DPC_HCG_37	–	R	Bit[7:4]: Not used Bit[3:0]: work_mode 0000:For 1-expo 0001:For 2-expo 0010:For 3-expo Others:Not used
0x5400	PRE_RAWBIN_LCG_0	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight0
0x5401	PRE_RAWBIN_LCG_1	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight1
0x5402	PRE_RAWBIN_LCG_2	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight2
0x5403	PRE_RAWBIN_LCG_3	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight3
0x5404	PRE_RAWBIN_LCG_4	0x00	RW	Bit[7:1]: Not used Bit[0]: blc_contr_en

table A-2 sensor control registers (sheet 155 of 255)

address	register name	default value	R/W	description
0x5440	PRE_ISP_0_LCG	0x0F	RW	Bit[7:6]: Not used Bit[5:4]: bar_style Bit[3]: isp_test Clear last four bits of image data to 0 Bit[2]: Transparent mode enable Combine test data and image data together Bit[1]: Rolling bar mode enable Bit[0]: Test pattern enable
0x5441	PRE_ISP_1_LCG	0x00	RW	Bit[7:4]: Not used Bit[3]: Bayer constant test pattern enable Bit[2:0]: Test image select 0, color bar
0x5442	PRE_ISP_2_LCG	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bayer_const_b
0x5443	PRE_ISP_3_LCG	0x00	RW	Bit[7:0]: bayer_const_b Constant pixel value for B channel
0x5444	PRE_ISP_4_LCG	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bayer_const_gb
0x5445	PRE_ISP_5_LCG	0x00	RW	Bit[7:0]: bayer_const_gb Constant pixel value for Gb channel
0x5446	PRE_ISP_6_LCG	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bayer_const_gr
0x5447	PRE_ISP_7_LCG	0x00	RW	Bit[7:0]: bayer_const_gr Constant pixel value for Gr channel
0x5448	PRE_ISP_8_LCG	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bayer_const_r
0x5449	PRE_ISP_9_LCG	0x00	RW	Bit[7:0]: bayer_const_r Constant pixel value for R channel

table A-2 sensor control registers (sheet 156 of 255)

address	register name	default value	R/W	description
0x544A	PRE_ISP_A_LCG	0x00	RW	Bit[7]: Not used Bit[6]: start_man_en Manual X direction start and Y direction start of sensor array enable 0: Disable 1: Enable Bit[5]: Offset manual enable 0: Disable 1: Enable Bit[4]: Flip option for Y offset Bit[3]: Mirror option for Y offset Bit[2]: end_man Manual X direction end and Y direction end of sensor array enable 0: Disable 1: Enable Bit[1]: Digital test row bypass enable Bit[0]: Window cut enable 0: Disable 1: Enable
0x544B	PRE_ISP_B_LCG	0x00	RW	Bit[7:6]: Not used Bit[5:1]: X direction skip step manual enable 0: Disable 1: Enable Bit[0]: x_skip_man_en X direction skip step value
0x544C	PRE_ISP_C_LCG	0x00	RW	Bit[7:6]: Not used Bit[5:1]: y_skip_man X direction skip step manual enable 0: Disable 1: Enable Bit[0]: y_skip_man_en X direction skip step value
0x544D	PRE_ISP_D_LCG	0x00	RW	Bit[7:0]: In_number
0x544E	PRE_ISP_E_LCG	0x00	RW	Bit[7:0]: Line number interrupt
0x544F	PRE_ISP_F_LCG	0x00	RW	Bit[7:0]: man_x_offset
0x5450	PRE_ISP_1_LCG0	0x00	RW	Bit[7:0]: Manual X direction offset in sensor array
0x5451	PRE_ISP_1_LCG1	0x00	RW	Bit[7:0]: man_y_offset
0x5452	PRE_ISP_1_LCG2	0x00	RW	Bit[7:0]: Manual Y direction offset in sensor array

table A-2 sensor control registers (sheet 157 of 255)

address	register name	default value	R/W	description
0x5453	PRE_ISP_1_LCG3	0x00	RW	Bit[7:0]: man_x_start
0x5454	PRE_ISP_1_LCG4	0x00	RW	Bit[7:0]: Manual X start in sensor array
0x5455	PRE_ISP_1_LCG5	0x00	RW	Bit[7:0]: man_y_start
0x5456	PRE_ISP_1_LCG6	0x00	RW	Bit[7:0]: Manual Y start in sensor array
0x5457	PRE_ISP_1_LCG7	0x00	RW	Bit[7:0]: man_x_end
0x5458	PRE_ISP_1_LCG8	0x00	RW	Bit[7:0]: man_x_end Manual Y direction offset in sensor array
0x5459	PRE_ISP_1_LCG9	0x00	RW	Bit[7:0]: man_y_end
0x545A	PRE_ISP_1_LCGA	0x00	RW	Bit[7:0]: man_y_end Manual Y direction offset in sensor array
0x545B	PRE_ISP_1_LCGB	0x0F	RW	Bit[7:0]: Ratio fraction part
0x545C	PRE_ISP_LCG_ISP_CTRL_RO_0	–	R	Bit[7:5]: Not used Bit[4:0]: x_even_inc X direction increase step of even points
0x545D	PRE_ISP_LCG_ISP_CTRL_RO_1	–	R	Bit[7:5]: Not used Bit[4:0]: x_odd_inc X direction increase step of odd points
0x545E	PRE_ISP_LCG_ISP_CTRL_RO_2	–	R	Bit[7:5]: Not used Bit[4:0]: y_even_inc Y direction increase step of even points
0x545F	PRE_ISP_LCG_ISP_CTRL_RO_3	–	R	Bit[7:5]: Not used Bit[4:0]: y_odd_inc Y direction increase step of odd points
0x5460	PRE_ISP_LCG_ISP_CTRL_RO_4	–	R	Bit[7:0]: X direction offset in sensor array
0x5461	PRE_ISP_LCG_ISP_CTRL_RO_5	–	R	Bit[7:0]: x_offset X direction increase step of odd points
0x5462	PRE_ISP_LCG_ISP_CTRL_RO_6	–	R	Bit[7:0]: Y direction offset in sensor array
0x5463	PRE_ISP_LCG_ISP_CTRL_RO_7	–	R	Bit[7:0]: y_offset Y direction increase step of odd points

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address	register name	default value	R/W	description
0x5464	PRE_ISP_LCG_ISP_CTRL_RO_8	–	R	Bit[7:0]: Pixel counter
0x5465	PRE_ISP_LCG_ISP_CTRL_RO_9	–	R	Bit[7:0]: Pixel counter
0x5466	PRE_ISP_LCG_ISP_CTRL_RO_A	–	R	Bit[7:0]: Line counter
0x5467	PRE_ISP_LCG_ISP_CTRL_RO_B	–	R	Bit[7:0]: Line counter
0x5468	PRE_ISP_LCG_ISP_CTRL_RO_C	–	R	Bit[7:0]: Software version
0x5469	PRE_ISP_LCG_ISP_CTRL_RO_D	–	R	Bit[7:0]: Hardware version
0x5480	AWB_GAIN_LCG_0	0x04	RW	Bit[7:0]: Manual AWB gain[0]
0x5481	AWB_GAIN_LCG_1	0x00	RW	Bit[7:0]: Manual AWB gain[0]
0x5482	AWB_GAIN_LCG_2	0x04	RW	Bit[7:0]: Manual AWB gain[1]
0x5483	AWB_GAIN_LCG_3	0x00	RW	Bit[7:0]: Manual AWB gain[1]
0x5484	AWB_GAIN_LCG_4	0x04	RW	Bit[7:0]: Manual AWB gain[2]
0x5485	AWB_GAIN_LCG_5	0x00	RW	Bit[7:0]: Manual AWB gain[2]
0x5486	AWB_GAIN_LCG_6	0x04	RW	Bit[7:0]: Manual AWB gain[3]
0x5487	AWB_GAIN_LCG_7	0x00	RW	Bit[7:0]: Manual AWB gain[3]
0x5488	AWB_GAIN_LCG_8	0x00	RW	Bit[7:5]: Not used Bit[4]: gain_man_en Manual gain enable Bit[3]: blc_man_en Manual BLC enable Bit[2]: cfa_ptn_man_en Manual CFA pattern enable Bit[1:0]: cfa_ptn_man Manual CFA pattern
0x5489	AWB_GAIN_LCG_9	0x00	RW	Bit[7:2]: Not used Bit[1:0]: blc_man Manual BLC
0x548A	AWB_GAIN_LCG_10	0x00	RW	Bit[7:0]: blc_man Manual BLC
0x5490	AWB_GAIN_LCG_11	–	R	Bit[7:0]: Version
0x5491	AWB_GAIN_LCG_12	–	R	Bit[7:0]: Version

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address	register name	default value	R/W	description
0x54C0	DPC_LCG_NUM_0	0x33	RW	Bit[7:6]: correct_opt Option to correct G/Br pixel Bit[5:4]: Edge filling option Bit[3]: manual_mode_en Enable manual mode Bit[2]: Enable cross cluster correction Bit[1]: Enable black pixel correction Bit[0]: Enable white pixel correction
0x54C1	DPC_LCG_NUM_1	0x88	RW	Bit[7:4]: couplet_bgain_margin Black couplet defect pixel correction gain margin Bit[3:0]: couplet_wgain_margin White couplet defect pixel correction gain margin
0x54C2	DPC_LCG_NUM_2	0x88	RW	Bit[7:4]: cluster_b_th Black couplet threshold ratio Bit[3:0]: cluster_w_th White couplet threshold ratio
0x54C3	DPC_LCG_NUM_3	0x08	RW	Bit[7:0]: couplet_wgain_th White couplet defect pixel correction gain threshold
0x54C4	DPC_LCG_NUM_4	0x08	RW	Bit[7:0]: couplet_bgain_th Black couplet defect pixel correction gain threshold
0x54C5	DPC_LCG_NUM_5	0xFF	RW	Bit[7:0]: Saturation threshold
0x54C6	DPC_LCG_0	0x00	RW	Bit[7:4]: dp_num_list0 Max allowed defect pixel list0 Bit[3:0]: dp_num_list1 Max allowed defect pixel list1
0x54C7	DPC_LCG_1	0x12	RW	Bit[7:4]: dp_num_list2 Max allowed defect pixel list2 Bit[3:0]: dp_num_list3 Max allowed defect pixel list3
0x54C8	DPC_LCG_2	0x04	RW	Bit[7:0]: w_th_list0 White pixel threshold list
0x54C9	DPC_LCG_3	0x04	RW	Bit[7:0]: w_th_list1 White pixel threshold list
0x54CA	DPC_LCG_4	0x04	RW	Bit[7:0]: w_th_list2 White pixel threshold list
0x54CB	DPC_LCG_5	0x04	RW	Bit[7:0]: w_th_list3 White pixel threshold list

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address	register name	default value	R/W	description
0x54CC	DPC_LCG_6	0x04	RW	Bit[7:0]: b_th_list0 Black pixel threshold list
0x54CD	DPC_LCG_7	0x04	RW	Bit[7:0]: b_th_list1 Black pixel threshold list
0x54CE	DPC_LCG_8	0x04	RW	Bit[7:0]: b_th_list2 Black pixel threshold list
0x54CF	DPC_LCG_9	0x04	RW	Bit[7:0]: b_th_list3 Black pixel threshold list
0x54D0	DPC_LCG_A	0x03	RW	Bit[7:0]: gain_list0 Gain control point
0x54D1	DPC_LCG_B	0x08	RW	Bit[7:0]: gain_list1 Gain control point
0x54D2	DPC_LCG_C	0x0C	RW	Bit[7:0]: gain_list2 Gain control point
0x54D4	DPC_LCG_14	0x00	RW	Bit[7:4]: Not used Bit[3:0]: roi_start_x ROI top left X location
0x54D5	DPC_LCG_15	0x00	RW	Bit[7:0]: roi_start_x
0x54D6	DPC_LCG_16	0x00	RW	Bit[7:4]: Not used Bit[3:0]: roi_start_y ROI top left Y location
0x54D7	DPC_LCG_17	0x00	RW	Bit[7:0]: roi_start_y
0x54D8	DPC_LCG_18	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI width
0x54D9	DPC_LCG_19	0x0F	RW	Bit[7:0]: roi_width
0x54DA	DPC_LCG_1A	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI height
0x54DB	DPC_LCG_1B	0x0F	RW	Bit[7:0]: roi_height
0x54DC	DPC_LCG_1C	0xFF	RW	Bit[7:0]: roi_dp_num Number of DP locations can be saved
0x54DD	DPC_LCG_1D	0xFF	RW	Bit[7:0]: roi_dp_num
0x54DE	DPC_LCG_1E	0xFF	RW	Bit[7:0]: roi_dp_num
0x54E6	DPC_LCG_26	–	R	Bit[7:0]: w_th
0x54E7	DPC_LCG_27	–	R	Bit[7:0]: b_th

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address	register name	default value	R/W	description
0x54E8	DPC_LCG_28	–	R	Bit[7:4]: Not used Bit[3:0]: max_dp_num
0x54E9	DPC_LCG_29	–	R	Bit[7:2]: Not used Bit[1]: couplet_w_en Bit[0]: couplet_b_en
0x54EA	DPC_LCG_2A	–	R	Bit[7:0]: DPCount
0x54EB	DPC_LCG_2B	–	R	Bit[7:0]: DPCount
0x54EC	DPC_LCG_2C	–	R	Bit[7:0]: DPCount
0x54ED	DPC_LCG_2D	–	R	Bit[7:0]: DPROICount
0x54EE	DPC_LCG_2E	–	R	Bit[7:0]: DPROICount
0x54EF	DPC_LCG_2F	–	R	Bit[7:0]: DPROICount
0x5500	OTP_DPC_LCG_0	0x02	RW	Bit[7]: Mirror option Bit[6]: Flip option Bit[5]: Disable mirror and flip Bit[4]: Auto mode using gain enable Bit[3]: Auto mode using exposure enable Bit[2]: ThresEn Detection enable Bit[1]: Fixed pattern selection Bit[0]: Fixed pattern enable
0x5501	OTP_DPC_LCG_1	0x10	RW	Bit[7:5]: Not used Bit[4]: GainSelect Gain-dependent OTPDPC cluster enable Bit[3]: EnableBWBin2 BW binning mode Bit[2]: Disable binning Bit[1]: Manual increase step enable Bit[0]: Manual offset enable
0x5502	OTP_DPC_LCG_2	0x30	RW	Bit[7]: Reserved Bit[6:4]: Recovery method selection Bit[3:2]: Horizontal binning mode Bit[1:0]: Vertical binning mode
0x5503	OTP_DPC_LCG_3	0x18	RW	Bit[7:4]: GainSelectThres Gain-dependent threshold Bit[3:0]: OTPThres Detection threshold
0x5504	OTP_DPC_LCG_4	0x01	RW	Bit[7:5]: Not used Bit[4:0]: ManualXEvenInc Manual X even step

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address	register name	default value	R/W	description
0x5505	OTP_DPC_LCG_5	0x01	RW	Bit[7:5]: Not used Bit[4:0]: ManualXOddInc Manual X odd step
0x5506	OTP_DPC_LCG_6	0x01	RW	Bit[7:5]: Not used Bit[4:0]: ManualYEvenInc Manual Y even step
0x5507	OTP_DPC_LCG_7	0x01	RW	Bit[7:5]: Not used Bit[4:0]: ManualYOddInc Manual Y odd step
0x5509	OTP_DPC_LCG_8	0x07	RW	Bit[7:6]: Not used Bit[5:0]: GainLimit Gain threshold
0x550A	OTP_DPC_LCG_A	0x00	RW	Bit[7]: Not used Bit[6:0]: ExposureLimit Exposure threshold
0x550B	OTP_DPC_LCG_B	0x00	RW	Bit[7:0]: ExposureLimit Exposure threshold
0x550C	OTP_DPC_LCG_C	0x00	RW	Bit[7:0]: Manual X offset
0x550D	OTP_DPC_LCG_D	0x00	RW	Bit[7:0]: Manual X offset
0x550E	OTP_DPC_LCG_E	0x00	RW	Bit[7:0]: Manual Y offset
0x550F	OTP_DPC_LCG_F	0x00	RW	Bit[7:0]: Manual Y offset
0x5510	OTP_DPC_LCG_10	0x00	RW	Bit[7]: flip_mirror_man_en Bit[6]: flip_man Bit[5]: mirror_man Bit[4]: Cluster data bypass enable Bit[3]: Work mode manual enable Bit[2:0]: Work mode manual

table A-2 sensor control registers (sheet 163 of 255)

address	register name	default value	R/W	description
0x5511	OTP_DPC_LCG_11	0x00	RW	Bit[7]: Not used Bit[6]: dis_proc_gate Disable detect and remove blocks' clock gating option Bit[5]: dis_mem_rd_gate Disable get_cluster block's clock gating option Bit[4]: dis_start_gate Disable start frame process logic clock gating option Bit[3]: dis_buf3_gate Disable cluster_buf 3 of long exposure block's clock gating option Bit[2]: dis_buf2_gate Disable cluster_buf 2 of long exposure block's clock gating option Bit[1]: dis_buf1_gate Disable cluster_buf 1 of long exposure block's clock gating option Bit[0]: dis_buf0_gate Disable cluster_buf 0 of long exposure block's clock gating option
0x5512	OTP_DPC_LCG_12	0x00	RW	Bit[7]: y_bin_man_en Manual Y direction binning enable Bit[6]: y_bin4_man Manual Y direction bin4 enable, reserved Bit[5]: y_bin3_man Manual Y direction bin3 enable, reserved Bit[4]: y_bin2_man Manual Y direction bin2 enable Bit[3]: x_bin_man_en Manual X direction binning enable Bit[2]: x_bin4_man Manual X direction bin4 enable, reserved Bit[1]: x_bin3_man Manual X direction bin3 enable, reserved Bit[0]: x_bin2_man Manual X direction bin2 enable

table A-2 sensor control registers (sheet 164 of 255)

address	register name	default value	R/W	description
0x5513	OTP_DPC_LCG_13	0x00	RW	Bit[7]: Not used Bit[6]: OTP eFUSE debug mode enable, read out data of debug address in eFUSE Bit[5]: Manual size enable Bit[4]: bwbin2_man_en Bit[3]: y_bwbin2_man Manual Y direction BW binning enable Bit[2]: x_bwbin2_man Manual X direction BW binning enable Bit[1]: position_debug_en Replace detected defect pixel with its position in sensor array Bit[0]: Position counter select 0: H counter 1: V counter
0x5514	OTP_DPC_LCG_14	0x00	RW	Bit[7:0]: OTP eFUSE start address
0x5515	OTP_DPC_LCG_15	0x00	RW	Bit[7:0]: OTP eFUSE start address
0x5516	OTP_DPC_LCG_16	0xFF	RW	Bit[7:0]: OTP eFUSE end address
0x5517	OTP_DPC_LCG_17	0xFF	RW	Bit[7:0]: OTP eFUSE end address
0x5518	OTP_DPC_LCG_18	0x05	RW	Bit[7:0]: Manual X direction end in sensor array
0x5519	OTP_DPC_LCG_19	0x38	RW	Bit[7:0]: Manual X direction end in sensor array
0x551A	OTP_DPC_LCG_1A	0x00	RW	Bit[7:0]: OTP eFUSE debug address
0x551B	OTP_DPC_LCG_1B	0x00	RW	Bit[7:0]: OTP eFUSE debug address
0x551C	OTP_DPC_LCG_1C	0x00	RW	Bit[7:0]: Manual vsize
0x551D	OTP_DPC_LCG_1D	0x00	RW	Bit[7:0]: Manual vsize
0x551E	OTP_DPC_LCG_1E	0x00	RW	Bit[7:0]: Manual hsize
0x551F	OTP_DPC_LCG_1F	0x00	RW	Bit[7:0]: Manual hsize
0x5520	OTP_DPC_LCG_20	–	R	Bit[7:0]: Hsize[15:8]
0x5521	OTP_DPC_LCG_21	–	R	Bit[7:0]: Hsize[7:0]
0x5522	OTP_DPC_LCG_22	–	R	Bit[7:0]: Vsize[15:8]
0x5523	OTP_DPC_LCG_23	–	R	Bit[7:0]: Vsize[7:0]
0x5524	OTP_DPC_LCG_24	–	R	Bit[7:0]: X direction offset in sensor array
0x5525	OTP_DPC_LCG_25	–	R	Bit[7:0]: X direction offset in sensor array

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address	register name	default value	R/W	description
0x5526	OTP_DPC_LCG_26	–	R	Bit[7:0]: Y direction offset in sensor array
0x5527	OTP_DPC_LCG_27	–	R	Bit[7:0]: Y direction offset in sensor array
0x5529	OTP_DPC_LCG_29	–	R	Bit[7]: ro_y_bwbin2 Y direction BW binning Bit[6]: Y direction bin4 Bit[5]: Y direction bin3 Bit[4]: Y direction bin2 Bit[3]: ro_x_bwbin2 X direction BW binning Bit[2]: X direction bin4 Bit[1]: X direction bin3 Bit[0]: X direction bin2
0x552A	OTP_DPC_LCG_2A	–	R	Bit[7:0]: X direction end position in sensor array
0x552B	OTP_DPC_LCG_2B	–	R	Bit[7:0]: X direction end position in sensor array
0x552C	OTP_DPC_LCG_2C	–	R	Bit[7:5]: Not used Bit[4:0]: ro_x_even_inc X direction increase step of even points
0x552D	OTP_DPC_LCG_2D	–	R	Bit[7:5]: Not used Bit[4:0]: ro_x_odd_inc X direction increase step of odd points
0x552E	OTP_DPC_LCG_2E	–	R	Bit[7:5]: Not used Bit[4:0]: ro_y_even_inc Y direction increase step of even points
0x552F	OTP_DPC_LCG_2F	–	R	Bit[7:5]: Not used Bit[4:0]: ro_y_odd_inc Y direction increase step of odd points
0x5531	OTP_DPC_LCG_31	–	R	Bit[7:0]: ro_debug_data Data of debug address in OTP eFUSE
0x5532	OTP_DPC_LCG_32	–	R	Bit[7:0]: Software version
0x5533	OTP_DPC_LCG_33	–	R	Bit[7:0]: Hardware version

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address	register name	default value	R/W	description
0x5537	OTP_DPC_LCG_37	–	R	Bit[7:4]: Not used Bit[3:0]: work_mode 0000:For 1-expo 0001:For 2-expo 0010:For 3-expo Others: Not used
0x5600	PRE_RAWBIN_SPD_0	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight0
0x5601	PRE_RAWBIN_SPD_1	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight1
0x5602	PRE_RAWBIN_SPD_2	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight2
0x5603	PRE_RAWBIN_SPD_3	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight3
0x5604	PRE_RAWBIN_SPD_4	0x00	RW	Bit[7:1]: Not used Bit[0]: blc_contr_en
0x5640	PRE_ISP_0_SPD	0x0F	RW	Bit[7:6]: Not used Bit[5:4]: bar_style Bit[3]: isp_test Clear last four bits of image data to 0 Bit[2]: Transparent mode enable Combine test data and image data together Bit[1]: Rolling bar mode enable Bit[0]: Test pattern enable
0x5641	PRE_ISP_1_SPD	0x00	RW	Bit[7:4]: Not used Bit[3]: Bayer constant test pattern enable Bit[2:0]: Test image select 0, color bar
0x5642	PRE_ISP_2_SPD	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bayer_const_b
0x5643	PRE_ISP_3_SPD	0x00	RW	Bit[7:0]: bayer_const_b Constant pixel value for B channel
0x5644	PRE_ISP_4_SPD	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bayer_const_gb
0x5645	PRE_ISP_5_SPD	0x00	RW	Bit[7:0]: bayer_const_gb Constant pixel value for Gb channel
0x5646	PRE_ISP_6_SPD	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bayer_const_gr

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address	register name	default value	R/W	description
0x5647	PRE_ISP_7_SPD	0x00	RW	Bit[7:0]: bayer_const_gr Constant pixel value for Gr channel
0x5648	PRE_ISP_8_SPD	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bayer_const_r
0x5649	PRE_ISP_9_SPD	0x00	RW	Bit[7:0]: bayer_const_r Constant pixel value for R channel
0x564A	PRE_ISP_A_SPD	0x00	RW	Bit[7]: Not used Bit[6]: start_man_en Manual X direction start and Y direction start of sensor array enable 0: Disable 1: Enable Bit[5]: Offset manual enable 0: Disable 1: Enable Bit[4]: Flip option for Y offset Bit[3]: Mirror option for Y offset Bit[2]: end_man Manual X direction end and Y direction end of sensor array enable 0: Disable 1: Enable Bit[1]: Digital test row bypass enable Bit[0]: Window cut enable 0: Disable 1: Enable
0x564B	PRE_ISP_B_SPD	0x00	RW	Bit[7:6]: Not used Bit[5:1]: X direction skip step manual enable 0: Disable 1: Enable Bit[0]: x_skip_man_en X direction skip step value
0x564C	PRE_ISP_C_SPD	0x00	RW	Bit[7:6]: Not used Bit[5:1]: y_skip_man X direction skip step manual enable 0: Disable 1: Enable Bit[0]: y_skip_man_en X direction skip step value
0x564D	PRE_ISP_D_SPD	0x00	RW	Bit[7:0]: ln_number
0x564E	PRE_ISP_E_SPD	0x00	RW	Bit[7:0]: Line number interrupt

table A-2 sensor control registers (sheet 168 of 255)

address	register name	default value	R/W	description
0x564F	PRE_ISP_F_SPD	0x00	RW	Bit[7:0]: man_x_offset
0x5650	PRE_ISP_1_SPD0	0x00	RW	Bit[7:0]: Manual X direction offset in sensor array
0x5651	PRE_ISP_1_SPD1	0x00	RW	Bit[7:0]: man_y_offset
0x5652	PRE_ISP_1_SPD2	0x00	RW	Bit[7:0]: Manual Y direction offset in sensor array
0x5653	PRE_ISP_1_SPD3	0x00	RW	Bit[7:0]: man_x_start
0x5654	PRE_ISP_1_SPD4	0x00	RW	Bit[7:0]: Manual X start in sensor array
0x5655	PRE_ISP_1_SPD5	0x00	RW	Bit[7:0]: man_y_start
0x5656	PRE_ISP_1_SPD6	0x00	RW	Bit[7:0]: Manual Y start in sensor array
0x5657	PRE_ISP_1_SPD7	0x00	RW	Bit[7:0]: man_x_end
0x5658	PRE_ISP_1_SPD8	0x00	RW	Bit[7:0]: man_x_end Manual Y direction offset in sensor array
0x5659	PRE_ISP_1_SPD9	0x00	RW	Bit[7:0]: man_y_end
0x565A	PRE_ISP_1_SPDA	0x00	RW	Bit[7:0]: man_y_end Manual Y direction offset in sensor array
0x565B	PRE_ISP_1_SPDB	0x0F	RW	Bit[7:0]: Ratio fraction part
0x565C	PRE_ISP_SPD_ISP_CTRL_RO_0	–	R	Bit[7:5]: Not used Bit[4:0]: x_even_inc X direction increase step of even points
0x565D	PRE_ISP_SPD_ISP_CTRL_RO_1	–	R	Bit[7:5]: Not used Bit[4:0]: x_odd_inc X direction increase step of odd points
0x565E	PRE_ISP_SPD_ISP_CTRL_RO_2	–	R	Bit[7:5]: Not used Bit[4:0]: y_even_inc Y direction increase step of even points
0x565F	PRE_ISP_SPD_ISP_CTRL_RO_3	–	R	Bit[7:5]: Not used Bit[4:0]: y_odd_inc Y direction increase step of odd points
0x5660	PRE_ISP_SPD_ISP_CTRL_RO_4	–	R	Bit[7:0]: X direction offset in sensor array

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address	register name	default value	R/W	description
0x5661	PRE_ISP_SPD_ISP_CTRL_RO_5	–	R	Bit[7:0]: x_offset X direction increase step of odd points
0x5662	PRE_ISP_SPD_ISP_CTRL_RO_6	–	R	Bit[7:0]: Y direction offset in sensor array
0x5663	PRE_ISP_SPD_ISP_CTRL_RO_7	–	R	Bit[7:0]: y_offset Y direction increase step of odd points
0x5664	PRE_ISP_SPD_ISP_CTRL_RO_8	–	R	Bit[7:0]: Pixel counter
0x5665	PRE_ISP_SPD_ISP_CTRL_RO_9	–	R	Bit[7:0]: Pixel counter
0x5666	PRE_ISP_SPD_ISP_CTRL_RO_A	–	R	Bit[7:0]: Line counter
0x5667	PRE_ISP_SPD_ISP_CTRL_RO_B	–	R	Bit[7:0]: Line counter
0x5668	PRE_ISP_SPD_ISP_CTRL_RO_C	–	R	Bit[7:0]: Software version
0x5669	PRE_ISP_SPD_ISP_CTRL_RO_D	–	R	Bit[7:0]: Hardware version
0x5680	AWB_GAIN_SPD_0	0x04	RW	Bit[7:0]: Manual AWB gain[0]
0x5681	AWB_GAIN_SPD_1	0x00	RW	Bit[7:0]: Manual AWB gain[0]
0x5682	AWB_GAIN_SPD_2	0x04	RW	Bit[7:0]: Manual AWB gain[1]
0x5683	AWB_GAIN_SPD_3	0x00	RW	Bit[7:0]: Manual AWB gain[1]
0x5684	AWB_GAIN_SPD_4	0x04	RW	Bit[7:0]: Manual AWB gain[2]
0x5685	AWB_GAIN_SPD_5	0x00	RW	Bit[7:0]: Manual AWB gain[2]
0x5686	AWB_GAIN_SPD_6	0x04	RW	Bit[7:0]: Manual AWB gain[3]
0x5687	AWB_GAIN_SPD_7	0x00	RW	Bit[7:0]: Manual AWB gain[3]
0x5688	AWB_GAIN_SPD_8	0x00	RW	Bit[7:5]: Not used Bit[4]: gain_man_en Manual gain enable Bit[3]: blc_man_en Manual BLC enable Bit[2]: cfa_ptn_man_en Manual CFA pattern enable Bit[1:0]: cfa_ptn_man Manual CFA pattern

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address	register name	default value	R/W	description
0x5689	AWB_GAIN_SPD_9	0x00	RW	Bit[7:2]: Not used Bit[1:0]: blc_man Manual BLC
0x568A	AWB_GAIN_SPD_10	0x00	RW	Bit[7:0]: blc_man Manual BLC
0x5690	AWB_GAIN_SPD_11	–	R	Bit[7:0]: Version
0x5691	AWB_GAIN_SPD_12	–	R	Bit[7:0]: Version
0x56C0	DPC_SPD_NUM_0	0x33	RW	Bit[7:6]: correct_opt Option to correct G/Br pixel Bit[5:4]: Edge filling option Bit[3]: manual_mode_en Enable manual mode Bit[2]: Enable cross cluster correction Bit[1]: Enable black pixel correction Bit[0]: Enable white pixel correction
0x56C1	DPC_SPD_NUM_1	0x88	RW	Bit[7:4]: couplet_bgain_margin Black couplet defect pixel correction gain margin Bit[3:0]: couplet_wgain_margin White couplet defect pixel correction gain margin
0x56C2	DPC_SPD_NUM_2	0x88	RW	Bit[7:4]: cluster_b_th Black couplet threshold ratio Bit[3:0]: cluster_w_th White couplet threshold ratio
0x56C3	DPC_SPD_NUM_3	0x08	RW	Bit[7:0]: couplet_wgain_th White couplet defect pixel correction gain threshold
0x56C4	DPC_SPD_NUM_4	0x08	RW	Bit[7:0]: couplet_bgain_th Black couplet defect pixel correction gain threshold
0x56C5	DPC_SPD_NUM_5	0xFF	RW	Bit[7:0]: Saturation threshold
0x56C6	DPC_SPD_0	0x00	RW	Bit[7:4]: dp_num_list0 Max allowed defect pixel list0 Bit[3:0]: dp_num_list1 Max allowed defect pixel list1
0x56C7	DPC_SPD_1	0x12	RW	Bit[7:4]: dp_num_list2 Max allowed defect pixel list2 Bit[3:0]: dp_num_list3 Max allowed defect pixel list3
0x56C8	DPC_SPD_2	0x04	RW	Bit[7:0]: w_th_list0 White pixel threshold list

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address	register name	default value	R/W	description
0x56C9	DPC_SPD_3	0x04	RW	Bit[7:0]: w_th_list1 White pixel threshold list
0x56CA	DPC_SPD_4	0x04	RW	Bit[7:0]: w_th_list2 White pixel threshold list
0x56CB	DPC_SPD_5	0x04	RW	Bit[7:0]: w_th_list3 White pixel threshold list
0x56CC	DPC_SPD_6	0x04	RW	Bit[7:0]: b_th_list0 Black pixel threshold list
0x56CD	DPC_SPD_7	0x04	RW	Bit[7:0]: b_th_list1 Black pixel threshold list
0x56CE	DPC_SPD_8	0x04	RW	Bit[7:0]: b_th_list2 Black pixel threshold list
0x56CF	DPC_SPD_9	0x04	RW	Bit[7:0]: b_th_list3 Black pixel threshold list
0x56D0	DPC_SPD_A	0x03	RW	Bit[7:0]: gain_list0 Gain control point
0x56D1	DPC_SPD_B	0x08	RW	Bit[7:0]: gain_list1 Gain control point
0x56D2	DPC_SPD_C	0x0C	RW	Bit[7:0]: gain_list2 Gain control point
0x56D4	DPC_SPD_14	0x00	RW	Bit[7:4]: Not used Bit[3:0]: roi_start_x ROI top left X location
0x56D5	DPC_SPD_15	0x00	RW	Bit[7:0]: roi_start_x
0x56D6	DPC_SPD_16	0x00	RW	Bit[7:4]: Not used Bit[3:0]: roi_start_y ROI top left Y location
0x56D7	DPC_SPD_17	0x00	RW	Bit[7:0]: roi_start_y
0x56D8	DPC_SPD_18	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI width
0x56D9	DPC_SPD_19	0x0F	RW	Bit[7:0]: roi_width
0x56DA	DPC_SPD_1A	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI height
0x56DB	DPC_SPD_1B	0x0F	RW	Bit[7:0]: roi_height
0x56DC	DPC_SPD_1C	0xFF	RW	Bit[7:0]: roi_dp_num Number of DP locations can be saved

table A-2 sensor control registers (sheet 172 of 255)

address	register name	default value	R/W	description
0x56DD	DPC_SPD_1D	0xFF	RW	Bit[7:0]: roi_dp_num
0x56DE	DPC_SPD_1E	0xFF	RW	Bit[7:0]: roi_dp_num
0x56E6	DPC_SPD_26	–	R	Bit[7:0]: w_th
0x56E7	DPC_SPD_27	–	R	Bit[7:0]: b_th
0x56E8	DPC_SPD_28	–	R	Bit[7:4]: Not used Bit[3:0]: max_dp_num
0x56E9	DPC_SPD_29	–	R	Bit[7:2]: Not used Bit[1]: couplet_w_en Bit[0]: couplet_b_en
0x56EA	DPC_SPD_2A	–	R	Bit[7:0]: DPCount
0x56EB	DPC_SPD_2B	–	R	Bit[7:0]: DPCount
0x56EC	DPC_SPD_2C	–	R	Bit[7:0]: DPCount
0x56ED	DPC_SPD_2D	–	R	Bit[7:0]: DPROICount
0x56EE	DPC_SPD_2E	–	R	Bit[7:0]: DPROICount
0x56EF	DPC_SPD_2F	–	R	Bit[7:0]: DPROICount
0x5700	OTP_DPC_SPD_0	0x02	RW	Bit[7]: Mirror option Bit[6]: Flip option Bit[5]: Disable mirror and flip Bit[4]: Auto mode using gain enable Bit[3]: Auto mode using exposure enable Bit[2]: ThresEn Detection enable Bit[1]: Fixed pattern selection Bit[0]: Fixed pattern enable
0x5701	OTP_DPC_SPD_1	0x10	RW	Bit[7:5]: Not used Bit[4]: GainSelect Gain-dependent OTPDPC cluster enable Bit[3]: EnableBWBin2 BW binning mode Bit[2]: Disable binning Bit[1]: Manual increase step enable Bit[0]: Manual offset enable
0x5702	OTP_DPC_SPD_2	0x30	RW	Bit[7]: Reserved Bit[6:4]: Recovery method selection Bit[3:2]: Horizontal binning mode Bit[1:0]: Vertical binning mode

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address	register name	default value	R/W	description
0x5703	OTP_DPC_SPD_3	0x18	RW	Bit[7:4]: GainSelectThres Gain-dependent threshold Bit[3:0]: OTPThres Detection threshold
0x5704	OTP_DPC_SPD_4	0x01	RW	Bit[7:5]: Not used Bit[4:0]: ManualXEvenInc Manual X even step
0x5705	OTP_DPC_SPD_5	0x01	RW	Bit[7:5]: Not used Bit[4:0]: ManualXOddInc Manual X odd step
0x5706	OTP_DPC_SPD_6	0x01	RW	Bit[7:5]: Not used Bit[4:0]: ManualYEvenInc Manual Y even step
0x5707	OTP_DPC_SPD_7	0x01	RW	Bit[7:5]: Not used Bit[4:0]: ManualYOddInc Manual Y odd step
0x5709	OTP_DPC_SPD_8	0x07	RW	Bit[7:6]: Not used Bit[5:0]: GainLimit Gain threshold
0x570A	OTP_DPC_SPD_A	0x00	RW	Bit[7]: Not used Bit[6:0]: ExposureLimit Exposure threshold
0x570B	OTP_DPC_SPD_B	0x00	RW	Bit[7:0]: ExposureLimit Exposure threshold
0x570C	OTP_DPC_SPD_C	0x00	RW	Bit[7:0]: Manual X offset
0x570D	OTP_DPC_SPD_D	0x00	RW	Bit[7:0]: Manual X offset
0x570E	OTP_DPC_SPD_E	0x00	RW	Bit[7:0]: Manual Y offset
0x570F	OTP_DPC_SPD_F	0x00	RW	Bit[7:0]: Manual Y offset
0x5710	OTP_DPC_SPD_10	0x00	RW	Bit[7]: flip_mirror_man_en Bit[6]: flip_man Bit[5]: mirror_man Bit[4]: Cluster data bypass enable Bit[3]: Work mode manual enable Bit[2:0]: Work mode manual

table A-2 sensor control registers (sheet 174 of 255)

address	register name	default value	R/W	description
0x5711	OTP_DPC_SPD_11	0x00	RW	Bit[7]: Not used Bit[6]: dis_proc_gate Disable detect and remove blocks' clock gating option Bit[5]: dis_mem_rd_gate Disable get_cluster block's clock gating option Bit[4]: dis_start_gate Disable start frame process logic clock gating option Bit[3]: dis_buf3_gate Disable cluster_buf 3 of long exposure block's clock gating option Bit[2]: dis_buf2_gate Disable cluster_buf 2 of long exposure block's clock gating option Bit[1]: dis_buf1_gate Disable cluster_buf 1 of long exposure block's clock gating option Bit[0]: dis_buf0_gate Disable cluster_buf 0 of long exposure block's clock gating option
0x5712	OTP_DPC_SPD_12	0x00	RW	Bit[7]: y_bin_man_en Manual Y direction binning enable Bit[6]: y_bin4_man Manual Y direction bin4 enable, reserved Bit[5]: y_bin3_man Manual Y direction bin3 enable, reserved Bit[4]: y_bin2_man Manual Y direction bin2 enable Bit[3]: x_bin_man_en Manual X direction binning enable Bit[2]: x_bin4_man Manual X direction bin4 enable, reserved Bit[1]: x_bin3_man Manual X direction bin3 enable, reserved Bit[0]: x_bin2_man Manual X direction bin2 enable

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address	register name	default value	R/W	description
0x5713	OTP_DPC_SPD_13	0x00	RW	Bit[7]: Not used Bit[6]: OTP eFUSE debug mode enable Read out data of debug address in eFUSE Bit[5]: Manual size enable Bit[4]: bwbin2_man_en Bit[3]: y_bwbin2_man Manual Y direction BW binning enable Bit[2]: x_bwbin2_man Manual X direction BW binning enable Bit[1]: position_debug_en Replace detected defect pixel with its position in sensor array Bit[0]: Position counter select 0: H counter 1: V counter
0x5714	OTP_DPC_SPD_14	0x00	RW	Bit[7:0]: OTP eFUSE start address
0x5715	OTP_DPC_SPD_15	0x00	RW	Bit[7:0]: OTP eFUSE start address
0x5716	OTP_DPC_SPD_16	0xFF	RW	Bit[7:0]: OTP eFUSE end address
0x5717	OTP_DPC_SPD_17	0xFF	RW	Bit[7:0]: OTP eFUSE end address
0x5718	OTP_DPC_SPD_18	0x05	RW	Bit[7:0]: Manual X direction end in sensor array
0x5719	OTP_DPC_SPD_19	0x38	RW	Bit[7:0]: Manual X direction end in sensor array
0x571A	OTP_DPC_SPD_1A	0x00	RW	Bit[7:0]: OTP eFUSE debug address
0x571B	OTP_DPC_SPD_1B	0x00	RW	Bit[7:0]: OTP eFUSE debug address
0x571C	OTP_DPC_SPD_1C	0x00	RW	Bit[7:0]: Manual vsize
0x571D	OTP_DPC_SPD_1D	0x00	RW	Bit[7:0]: Manual vsize
0x571E	OTP_DPC_SPD_1E	0x00	RW	Bit[7:0]: Manual hsize
0x571F	OTP_DPC_SPD_1F	0x00	RW	Bit[7:0]: Manual hsize
0x5720	OTP_DPC_SPD_20	–	R	Bit[7:0]: Hsize[15:8]
0x5721	OTP_DPC_SPD_21	–	R	Bit[7:0]: Hsize[7:0]
0x5722	OTP_DPC_SPD_22	–	R	Bit[7:0]: Vsize[15:8]
0x5723	OTP_DPC_SPD_23	–	R	Bit[7:0]: Vsize[7:0]
0x5724	OTP_DPC_SPD_24	–	R	Bit[7:0]: X direction offset in sensor array
0x5725	OTP_DPC_SPD_25	–	R	Bit[7:0]: X direction offset in sensor array

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address	register name	default value	R/W	description
0x5726	OTP_DPC_SPD_26	–	R	Bit[7:0]: Y direction offset in sensor array
0x5727	OTP_DPC_SPD_27	–	R	Bit[7:0]: Y direction offset in sensor array
0x5729	OTP_DPC_SPD_29	–	R	Bit[7]: ro_y_bwbin2 Y direction BW binning Bit[6]: Y direction bin4 Bit[5]: Y direction bin3 Bit[4]: Y direction bin2 Bit[3]: ro_x_bwbin2 X direction BW binning Bit[2]: X direction bin4 Bit[1]: X direction bin3 Bit[0]: X direction bin2
0x572A	OTP_DPC_SPD_2A	–	R	Bit[7:0]: X direction end position in sensor array
0x572B	OTP_DPC_SPD_2B	–	R	Bit[7:0]: X direction end position in sensor array
0x572C	OTP_DPC_SPD_2C	–	R	Bit[7:5]: Not used Bit[4:0]: ro_x_even_inc X direction increase step of even points
0x572D	OTP_DPC_SPD_2D	–	R	Bit[7:5]: Not used Bit[4:0]: ro_x_odd_inc X direction increase step of odd points
0x572E	OTP_DPC_SPD_2E	–	R	Bit[7:5]: Not used Bit[4:0]: ro_y_even_inc Y direction increase step of even points
0x572F	OTP_DPC_SPD_2F	–	R	Bit[7:5]: Not used Bit[4:0]: ro_y_odd_inc Y direction increase step of odd points
0x5731	OTP_DPC_SPD_31	–	R	Bit[7:0]: ro_debug_data Data of debug address in OTP eFUSE
0x5732	OTP_DPC_SPD_32	–	R	Bit[7:0]: Software version
0x5733	OTP_DPC_SPD_33	–	R	Bit[7:0]: Hardware version

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address	register name	default value	R/W	description
0x5737	OTP_DPC_SPD_37	–	R	Bit[7:4]: Not used Bit[3:0]: work_mode 0000:for 1-expo 0001:for 2-expo 0010:for 3-expo Others:Not used
0x5800	PRE_RAWBIN_VS_0	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight0
0x5801	PRE_RAWBIN_VS_1	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight1
0x5802	PRE_RAWBIN_VS_2	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight2
0x5803	PRE_RAWBIN_VS_3	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight3
0x5804	PRE_RAWBIN_VS_4	0x00	RW	Bit[7:1]: Not used Bit[0]: blc_contr_en
0x5840	PRE_ISP_0_VS	0x0F	RW	Bit[7:6]: Not used Bit[5:4]: bar_style Bit[3]: isp_test Clear last four bits of image data to 0 Bit[2]: Transparent mode enable Combine test data and image data together Bit[1]: Rolling bar mode enable Bit[0]: Test pattern enable
0x5841	PRE_ISP_1_VS	0x00	RW	Bit[7:4]: Not used Bit[3]: Bayer constant test pattern enable Bit[2:0]: Test image select 0, color bar
0x5842	PRE_ISP_2_VS	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bayer_const_b
0x5843	PRE_ISP_3_VS	0x00	RW	Bit[7:0]: bayer_const_b Constant pixel value for B channel
0x5844	PRE_ISP_4_VS	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bayer_const_gb
0x5845	PRE_ISP_5_VS	0x00	RW	Bit[7:0]: bayer_const_gb Constant pixel value for Gb channel
0x5846	PRE_ISP_6_VS	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bayer_const_gr

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address	register name	default value	R/W	description
0x5847	PRE_ISP_7_VS	0x00	RW	Bit[7:0]: bayer_const_gr Constant pixel value for Gr channel
0x5848	PRE_ISP_8_VS	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bayer_const_r
0x5849	PRE_ISP_9_VS	0x00	RW	Bit[7:0]: bayer_const_r Constant pixel value for R channel
0x584A	PRE_ISP_A_VS	0x00	RW	Bit[7]: Not used Bit[6]: start_man_en Manual X direction start and Y direction start of sensor array enable 0: Disable 1: Enable Bit[5]: Offset manual enable 0: Disable 1: Enable Bit[4]: Flip option for Y offset Bit[3]: Mirror option for Y offset Bit[2]: end_man Manual X direction end and Y direction end of sensor array enable 0: Disable 1: Enable Bit[1]: Digital test row bypass enable Bit[0]: Window cut enable 0: Disable 1: Enable
0x584B	PRE_ISP_B_VS	0x00	RW	Bit[7:6]: Not used Bit[5:1]: X direction skip step manual enable 0: Disable 1: Enable Bit[0]: x_skip_man_en X direction skip step value
0x584C	PRE_ISP_C_VS	0x00	RW	Bit[7:6]: Not used Bit[5:1]: y_skip_man X direction skip step manual enable 0: Disable 1: Enable Bit[0]: y_skip_man_en X direction skip step value
0x584D	PRE_ISP_D_VS	0x00	RW	Bit[7:0]: ln_number

table A-2 sensor control registers (sheet 179 of 255)

address	register name	default value	R/W	description
0x584E	PRE_ISP_E_VS	0x00	RW	Bit[7:0]: Line number interrupt
0x584F	PRE_ISP_F_VS	0x00	RW	Bit[7:0]: man_x_offset
0x5850	PRE_ISP_1_VS0	0x00	RW	Bit[7:0]: Manual X direction offset in sensor array
0x5851	PRE_ISP_1_VS1	0x00	RW	Bit[7:0]: man_y_offset
0x5852	PRE_ISP_1_VS2	0x00	RW	Bit[7:0]: Manual Y direction offset in sensor array
0x5853	PRE_ISP_1_VS3	0x00	RW	Bit[7:0]: man_x_start
0x5854	PRE_ISP_1_VS4	0x00	RW	Bit[7:0]: Manual X start in sensor array
0x5855	PRE_ISP_1_VS5	0x00	RW	Bit[7:0]: man_y_start
0x5856	PRE_ISP_1_VS6	0x00	RW	Bit[7:0]: Manual Y start in sensor array
0x5857	PRE_ISP_1_VS7	0x00	RW	Bit[7:0]: man_x_end
0x5858	PRE_ISP_1_VS8	0x00	RW	Bit[7:0]: man_x_end Manual Y direction offset in sensor array
0x5859	PRE_ISP_1_VS9	0x00	RW	Bit[7:0]: man_y_end
0x585A	PRE_ISP_1_VSA	0x00	RW	Bit[7:0]: man_y_end Manual Y direction offset in sensor array
0x585B	PRE_ISP_1_VSB	0x0F	RW	Bit[7:0]: Ratio fraction part
0x585C	PRE_ISP_VS_ISP_CTRL_RO_0	–	R	Bit[7:5]: Not used Bit[4:0]: x_even_inc X direction increase step of even points
0x585D	PRE_ISP_VS_ISP_CTRL_RO_1	–	R	Bit[7:5]: Not used Bit[4:0]: x_odd_inc X direction increase step of odd points
0x585E	PRE_ISP_VS_ISP_CTRL_RO_2	–	R	Bit[7:5]: Not used Bit[4:0]: y_even_inc Y direction increase step of even points
0x585F	PRE_ISP_VS_ISP_CTRL_RO_3	–	R	Bit[7:5]: Not used Bit[4:0]: y_odd_inc Y direction increase step of odd points
0x5860	PRE_ISP_VS_ISP_CTRL_RO_4	–	R	Bit[7:0]: X direction offset in sensor array

table A-2 sensor control registers (sheet 180 of 255)

address	register name	default value	R/W	description
0x5861	PRE_ISP_VS_ISP_CTRL_RO_5	–	R	Bit[7:0]: x_offset X direction increase step of odd points
0x5862	PRE_ISP_VS_ISP_CTRL_RO_6	–	R	Bit[7:0]: Y direction offset in sensor array
0x5863	PRE_ISP_VS_ISP_CTRL_RO_7	–	R	Bit[7:0]: y_offset Y direction increase step of odd points
0x5864	PRE_ISP_VS_ISP_CTRL_RO_8	–	R	Bit[7:0]: Pixel counter
0x5865	PRE_ISP_VS_ISP_CTRL_RO_9	–	R	Bit[7:0]: Pixel counter
0x5866	PRE_ISP_VS_ISP_CTRL_RO_A	–	R	Bit[7:0]: Line counter
0x5867	PRE_ISP_VS_ISP_CTRL_RO_B	–	R	Bit[7:0]: Line counter
0x5868	PRE_ISP_VS_ISP_CTRL_RO_C	–	R	Bit[7:0]: Software version
0x5869	PRE_ISP_VS_ISP_CTRL_RO_D	–	R	Bit[7:0]: Hardware version
0x5880	AWB_GAIN_VS_0	0x04	RW	Bit[7:0]: Manual AWB gain[0]
0x5881	AWB_GAIN_VS_1	0x00	RW	Bit[7:0]: Manual AWB gain[0]
0x5882	AWB_GAIN_VS_2	0x04	RW	Bit[7:0]: Manual AWB gain[1]
0x5883	AWB_GAIN_VS_3	0x00	RW	Bit[7:0]: Manual AWB gain[1]
0x5884	AWB_GAIN_VS_4	0x04	RW	Bit[7:0]: Manual AWB gain[2]
0x5885	AWB_GAIN_VS_5	0x00	RW	Bit[7:0]: Manual AWB gain[2]
0x5886	AWB_GAIN_VS_6	0x04	RW	Bit[7:0]: Manual AWB gain[3]
0x5887	AWB_GAIN_VS_7	0x00	RW	Bit[7:0]: Manual AWB gain[3]
0x5888	AWB_GAIN_VS_8	0x00	RW	Bit[7:5]: Not used Bit[4]: gain_man_en Manual gain enable Bit[3]: blc_man_en Manual BLC enable Bit[2]: cfa_ptn_man_en Manual CFA pattern enable Bit[1:0]: cfa_ptn_man Manual CFA pattern

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address	register name	default value	R/W	description
0x5889	AWB_GAIN_VS_9	0x00	RW	Bit[7:2]: Not used Bit[1:0]: blc_man Manual BLC
0x588A	AWB_GAIN_VS_10	0x00	RW	Bit[7:0]: blc_man Manual BLC
0x5890	AWB_GAIN_VS_11	0x00	R	Bit[7:0]: Version
0x5891	AWB_GAIN_VS_12	0x00	R	Bit[7:0]: Version
0x58C0	DPC_VS_NUM_0	0x33	RW	Bit[7:6]: correct_opt Option to correct G/Br pixel Bit[5:4]: Edge filling option Bit[3]: manual_mode_en Enable manual mode Bit[2]: Enable cross cluster correction Bit[1]: Enable black pixel correction Bit[0]: Enable white pixel correction
0x58C1	DPC_VS_NUM_1	0x88	RW	Bit[7:4]: couplet_bgain_margin Black couplet defect pixel correction gain margin Bit[3:0]: couplet_wgain_margin White couplet defect pixel correction gain margin
0x58C2	DPC_VS_NUM_2	0x88	RW	Bit[7:4]: cluster_b_th Black couplet threshold ratio Bit[3:0]: cluster_w_th White couplet threshold ratio
0x58C3	DPC_VS_NUM_3	0x08	RW	Bit[7:0]: couplet_wgain_th White couplet defect pixel correction gain threshold
0x58C4	DPC_VS_NUM_4	0x08	RW	Bit[7:0]: couplet_bgain_th Black couplet defect pixel correction gain threshold
0x58C5	DPC_VS_NUM_5	0xFF	RW	Bit[7:0]: Saturation threshold
0x58C6	DPC_VS_0	0x00	RW	Bit[7:4]: dp_num_list0 Max allowed defect pixel list0 Bit[3:0]: dp_num_list1 Max allowed defect pixel list1
0x58C7	DPC_VS_1	0x12	RW	Bit[7:4]: dp_num_list2 Max allowed defect pixel list2 Bit[3:0]: dp_num_list3 Max allowed defect pixel list3
0x58C8	DPC_VS_2	0x04	RW	Bit[7:0]: w_th_list0 White pixel threshold list

table A-2 sensor control registers (sheet 182 of 255)

address	register name	default value	R/W	description
0x58C9	DPC_VS_3	0x04	RW	Bit[7:0]: w_th_list1 White pixel threshold list
0x58CA	DPC_VS_4	0x04	RW	Bit[7:0]: w_th_list2 White pixel threshold list
0x58CB	DPC_VS_5	0x04	RW	Bit[7:0]: w_th_list3 White pixel threshold list
0x58CC	DPC_VS_6	0x04	RW	Bit[7:0]: b_th_list0 Black pixel threshold list
0x58CD	DPC_VS_7	0x04	RW	Bit[7:0]: b_th_list1 Black pixel threshold list
0x58CE	DPC_VS_8	0x04	RW	Bit[7:0]: b_th_list2 Black pixel threshold list
0x58CF	DPC_VS_9	0x04	RW	Bit[7:0]: b_th_list3 Black pixel threshold list
0x58D0	DPC_VS_A	0x03	RW	Bit[7:0]: gain_list0 Gain control point
0x58D1	DPC_VS_B	0x08	RW	Bit[7:0]: gain_list1 Gain control point
0x58D2	DPC_VS_C	0x0C	RW	Bit[7:0]: gain_list2Gain control point
0x58D4	DPC_VS_14	0x00	RW	Bit[7:4]: Not used Bit[3:0]: roi_start_x ROI top left X location
0x58D5	DPC_VS_15	0x00	RW	Bit[7:0]: roi_start_x
0x58D6	DPC_VS_16	0x00	RW	Bit[7:4]: Not used Bit[3:0]: roi_start_y ROI top left Y location
0x58D7	DPC_VS_17	0x00	RW	Bit[7:0]: roi_start_y
0x58D8	DPC_VS_18	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI width
0x58D9	DPC_VS_19	0x0F	RW	Bit[7:0]: roi_width
0x58DA	DPC_VS_1A	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI height
0x58DB	DPC_VS_1B	0x0F	RW	Bit[7:0]: roi_height
0x58DC	DPC_VS_1C	0xFF	RW	Bit[7:0]: roi_dp_num Number of DP locations can be saved
0x58DD	DPC_VS_1D	0xFF	RW	Bit[7:0]: roi_dp_num

table A-2 sensor control registers (sheet 183 of 255)

address	register name	default value	R/W	description
0x58DE	DPC_VS_1E	0xFF	RW	Bit[7:0]: roi_dp_num
0x58E6	DPC_VS_26	–	R	Bit[7:0]: w_th
0x58E7	DPC_VS_27	–	R	Bit[7:0]: b_th
0x58E8	DPC_VS_28	–	R	Bit[7:4]: Not used Bit[3:0]: max_dp_num
0x58E9	DPC_VS_29	–	R	Bit[7:2]: Not used Bit[1]: couplet_w_en Bit[0]: couplet_b_en
0x58EA	DPC_VS_2A	–	R	Bit[7:0]: DPCount
0x58EB	DPC_VS_2B	–	R	Bit[7:0]: DPCount
0x58EC	DPC_VS_2C	–	R	Bit[7:0]: DPCount
0x58ED	DPC_VS_2D	–	R	Bit[7:0]: DPROICount
0x58EE	DPC_VS_2E	–	R	Bit[7:0]: DPROICount
0x58EF	DPC_VS_2F	–	R	Bit[7:0]: DPROICount
0x5900	OTP_DPC_VS_0	0x02	RW	Bit[7]: Mirror option Bit[6]: Flip option Bit[5]: Disable mirror and flip Bit[4]: Auto mode using gain enable Bit[3]: Auto mode using exposure enable Bit[2]: ThresEn Detection enable Bit[1]: Fixed pattern selection Bit[0]: Fixed pattern enable
0x5901	OTP_DPC_VS_1	0x10	RW	Bit[7:5]: Not used Bit[4]: GainSelect Gain-dependent OTPDPC cluster enable Bit[3]: EnableBWBin2 BW binning mode Bit[2]: Disable binning Bit[1]: Manual increase step enable Bit[0]: Manual offset enable
0x5902	OTP_DPC_VS_2	0x30	RW	Bit[7]: Reserved Bit[6:4]: Recovery method selection Bit[3:2]: Horizontal binning mode Bit[1:0]: Vertical binning mode
0x5903	OTP_DPC_VS_3	0x18	RW	Bit[7:4]: GainSelectThres Gain-dependent threshold Bit[3:0]: OTPThres Detection threshold

table A-2 sensor control registers (sheet 184 of 255)

address	register name	default value	R/W	description
0x5904	OTP_DPC_VS_4	0x01	RW	Bit[7:5]: Not used Bit[4:0]: ManualXEvenInc Manual X even step
0x5905	OTP_DPC_VS_5	0x01	RW	Bit[7:5]: Not used Bit[4:0]: ManualXOddInc Manual X odd step
0x5906	OTP_DPC_VS_6	0x01	RW	Bit[7:5]: Not used Bit[4:0]: ManualYEvenInc Manual Y even step
0x5907	OTP_DPC_VS_7	0x01	RW	Bit[7:5]: Not used Bit[4:0]: ManualYOddInc Manual Y odd step
0x5909	OTP_DPC_VS_8	0x07	RW	Bit[7:6]: Not used Bit[5:0]: GainLimit Gain threshold
0x590A	OTP_DPC_VS_A	0x00	RW	Bit[7]: Not used Bit[6:0]: ExposureLimit Exposure threshold
0x590B	OTP_DPC_VS_B	0x00	RW	Bit[7:0]: ExposureLimit Exposure threshold
0x590C	OTP_DPC_VS_C	0x00	RW	Bit[7:0]: Manual X offset
0x590D	OTP_DPC_VS_D	0x00	RW	Bit[7:0]: Manual X offset
0x590E	OTP_DPC_VS_E	0x00	RW	Bit[7:0]: Manual Y offset
0x590F	OTP_DPC_VS_F	0x00	RW	Bit[7:0]: Manual Y offset
0x5910	OTP_DPC_VS_10	0x00	RW	Bit[7]: flip_mirror_man_en Bit[6]: flip_man Bit[5]: mirror_man Bit[4]: Cluster data bypass enable Bit[3]: Work mode manual enable Bit[2:0]: Work mode manual

table A-2 sensor control registers (sheet 185 of 255)

address	register name	default value	R/W	description
0x5911	OTP_DPC_VS_11	0x00	RW	Bit[7]: Not used Bit[6]: dis_proc_gate Disable detect and remove blocks' clock gating option Bit[5]: dis_mem_rd_gate Disable get_cluster block's clock gating option Bit[4]: dis_start_gate Disable start frame process logic clock gating option Bit[3]: dis_buf3_gate Disable cluster_buf 3 of long exposure block's clock gating option Bit[2]: dis_buf2_gate Disable cluster_buf 2 of long exposure block's clock gating option Bit[1]: dis_buf1_gate Disable cluster_buf 1 of long exposure block's clock gating option Bit[0]: dis_buf0_gate Disable cluster_buf 0 of long exposure block's clock gating option
0x5912	OTP_DPC_VS_12	0x00	RW	Bit[7]: y_bin_man_en Manual Y direction binning enable Bit[6]: y_bin4_man Manual Y direction bin4 enable, reserved Bit[5]: y_bin3_man Manual Y direction bin3 enable, reserved Bit[4]: y_bin2_man Manual Y direction bin2 enable Bit[3]: x_bin_man_en Manual X direction binning enable Bit[2]: x_bin4_man Manual X direction bin4 enable, reserved Bit[1]: x_bin3_man Manual X direction bin3 enable, reserved Bit[0]: x_bin2_man Manual X direction bin2 enable

table A-2 sensor control registers (sheet 186 of 255)

address	register name	default value	R/W	description
0x5913	OTP_DPC_VS_13	0x00	RW	Bit[7]: Not used Bit[6]: OTP eFUSE debug mode enable Read out data of debug address in eFUSE Bit[5]: Manual size enable Bit[4]: bwbin2_man_en Bit[3]: y_bwbin2_man Manual Y direction BW binning enable Bit[2]: x_bwbin2_man Manual X direction BW binning enable Bit[1]: position_debug_en Replace detected defect pixel with its position in sensor array Bit[0]: Position counter select 0: H counter 1: V counter
0x5914	OTP_DPC_VS_14	0x00	RW	Bit[7:0]: OTP eFUSE start address
0x5915	OTP_DPC_VS_15	0x00	RW	Bit[7:0]: OTP eFUSE start address
0x5916	OTP_DPC_VS_16	0xFF	RW	Bit[7:0]: OTP eFUSE end address
0x5917	OTP_DPC_VS_17	0xFF	RW	Bit[7:0]: OTP eFUSE end address
0x5918	OTP_DPC_VS_18	0x05	RW	Bit[7:0]: Manual X direction end in sensor array
0x5919	OTP_DPC_VS_19	0x38	RW	Bit[7:0]: Manual X direction end in sensor array
0x591A	OTP_DPC_VS_1A	0x00	RW	Bit[7:0]: OTP eFUSE debug address
0x591B	OTP_DPC_VS_1B	0x00	RW	Bit[7:0]: OTP eFUSE debug address
0x591C	OTP_DPC_VS_1C	0x00	RW	Bit[7:0]: Manual vsize
0x591D	OTP_DPC_VS_1D	0x00	RW	Bit[7:0]: Manual vsize
0x591E	OTP_DPC_VS_1E	0x00	RW	Bit[7:0]: Manual hsize
0x591F	OTP_DPC_VS_1F	0x00	RW	Bit[7:0]: Manual hsize
0x5920	OTP_DPC_VS_20	–	R	Bit[7:0]: Hsize[15:8]
0x5921	OTP_DPC_VS_21	–	R	Bit[7:0]: Hsize[7:0]
0x5922	OTP_DPC_VS_22	–	R	Bit[7:0]: Vsize[15:8]
0x5923	OTP_DPC_VS_23	–	R	Bit[7:0]: Vsize[7:0]
0x5924	OTP_DPC_VS_24	–	R	Bit[7:0]: X direction offset in sensor array
0x5925	OTP_DPC_VS_25	–	R	Bit[7:0]: X direction offset in sensor array

table A-2 sensor control registers (sheet 187 of 255)

address	register name	default value	R/W	description
0x5926	OTP_DPC_VS_26	–	R	Bit[7:0]: Y direction offset in sensor array
0x5927	OTP_DPC_VS_27	–	R	Bit[7:0]: Y direction offset in sensor array
0x5929	OTP_DPC_VS_29	–	R	Bit[7]: ro_y_bwbin2 Y direction BW binning Bit[6]: Y direction bin4 Bit[5]: Y direction bin3 Bit[4]: Y direction bin2 Bit[3]: ro_x_bwbin2 X direction BW binning Bit[2]: X direction bin4 Bit[1]: X direction bin3 Bit[0]: X direction bin2
0x592A	OTP_DPC_VS_2A	–	R	Bit[7:0]: X direction end position in sensor array
0x592B	OTP_DPC_VS_2B	–	R	Bit[7:0]: X direction end position in sensor array
0x592C	OTP_DPC_VS_2C	–	R	Bit[7:5]: Not used Bit[4:0]: ro_x_even_inc X direction increase step of even points
0x592D	OTP_DPC_VS_2D	–	R	Bit[7:5]: Not used Bit[4:0]: ro_x_odd_inc X direction increase step of odd points
0x592E	OTP_DPC_VS_2E	–	R	Bit[7:5]: Not used Bit[4:0]: ro_y_even_inc Y direction increase step of even points
0x592F	OTP_DPC_VS_2F	–	R	Bit[7:5]: Not used Bit[4:0]: ro_y_odd_inc Y direction increase step of odd points
0x5931	OTP_DPC_VS_31	–	R	Bit[7:0]: ro_debug_data Data of debug address in OTP eFUSE
0x5932	OTP_DPC_VS_32	–	R	Bit[7:0]: Software version
0x5933	OTP_DPC_VS_33	–	R	Bit[7:0]: Hardware version

table A-2 sensor control registers (sheet 188 of 255)

address	register name	default value	R/W	description
0x5937	OTP_DPC_VS_37	–	R	Bit[7:4]: Not used Bit[3:0]: work_mode 0000:For 1-expo 0001:For 2-expo 0010:For 3-expo Others:Not used
0x5A00	LENC_0	0x05	RW	Bit[7:3]: Not used Bit[2]: less_1x_en Bit[1]: rand_bit_en Less than 1x gain process Bit[0]: auto_q_en Enable dithering function to avoid lost bit
0x5A01	LENC_1	0x18	RW	Bit[7]: Not used Bit[6:0]: minq_s MaxqfroS
0x5A02	LENC_2	0x40	RW	Bit[7]: Not used Bit[6:0]: maxq_s MinqfroS
0x5A03	LENC_3	0x00	RW	Bit[7:4]: Not used Bit[3:0]: MingainforS
0x5A04	LENC_4	0x20	RW	Bit[7:0]: MingainforS
0x5A05	LENC_5	0x00	RW	Bit[7:4]: Not used Bit[3:0]: MaxgainforS
0x5A06	LENC_6	0x60	RW	Bit[7:0]: MaxgainforS
0x5A07	LENC_7	0x00	RW	Bit[7:0]: br_hscale_man
0x5A08	LENC_8	0x00	RW	Bit[7:0]: br_hscale_man Scale H for Br channel
0x5A09	LENC_9	0x00	RW	Bit[7:0]: br_vscale_man Scale V for Br channel
0x5A0A	LENC_A	0x00	RW	Bit[7:0]: br_vscale_man Scale V for Br channel
0x5A0B	LENC_B	0x00	RW	Bit[7:0]: g_hscale_man Scale H for G channel
0x5A0C	LENC_C	0x00	RW	Bit[7:0]: g_hscale_man Scale H for G channel
0x5A0D	LENC_D	0x00	RW	Bit[7:0]: g_vscale_man Real gain for manual
0x5A0E	LENC_E	0x00	RW	Bit[7:0]: g_vscale_man

table A-2 sensor control registers (sheet 189 of 255)

address	register name	default value	R/W	description
0x5A0F	LENC_F	0x00	RW	Bit[7:4]: Not used Bit[3:0]: real_gain_s_man Scale V for G channel
0x5A10	LENC_10	0x00	RW	Bit[7:0]: real_gain_s_man Scale V for G channel
0x5A11	LENC_11	0x00	RW	Bit[7:4]: Not used Bit[3]: Realgainformanualenable Bit[2]: Scalemanualenable Bit[1]: Mnqmanualenable Bit[0]: Blcmanualenable
0x5A12	LENC_12	0x00	RW	Bit[7:2]: Not used Bit[1:0]: blc_s_man
0x5A13	LENC_13	0x00	RW	Bit[7:0]: blc_s_man Manualblc
0x5A14	LENC_14	0x00	RW	Bit[7]: Not used Bit[6]: Cfapatternmanualenable Bit[5]: Mirrormanualenable Bit[4]: Flipmanualenable Bit[3]: Skipmanualenable Bit[2]: Offsetmanualenable Bit[1]: mirror_man Manualmirror Bit[0]: flip_man Manualflip
0x5A15	LENC_15	0x00	RW	Bit[7:6]: Not used Bit[5:4]: cfa_pn_man Manual CFA pattern Bit[3:2]: x_skip_man Manual X skip Bit[1:0]: y_skip_man Manual Y skip
0x5A16	LENC_16	0x00	RW	Bit[7:4]: Not used Bit[3:0]: x_offset_man Manual X offset
0x5A17	LENC_17	0x00	RW	Bit[7:0]: x_offset_man Manual X offset
0x5A18	LENC_18	0x00	RW	Bit[7:4]: Not used Bit[3:0]: y_offset_man Manual Y offset
0x5A19	LENC_19	0x00	RW	Bit[7:0]: y_offset_man Manualyoffset

table A-2 sensor control registers (sheet 190 of 255)

address	register name	default value	R/W	description
0x5A1A	LENC_1A	0x40	RW	Bit[7]: Not used Bit[6:0]: m_nq_s_man manualm_nq
0x5A20	LENC_20	0x00	RW	Bit[7:0]: G00of8x8GcontrolpointarrayforS
0x5A21	LENC_21	0x00	RW	Bit[7:0]: G01of8x8GcontrolpointarrayforS
0x5A22	LENC_22	0x00	RW	Bit[7:0]: G02of8x8GcontrolpointarrayforS
0x5A23	LENC_23	0x00	RW	Bit[7:0]: G03of8x8GcontrolpointarrayforS
0x5A24	LENC_24	0x00	RW	Bit[7:0]: G04of8x8GcontrolpointarrayforS
0x5A25	LENC_25	0x00	RW	Bit[7:0]: G05of8x8GcontrolpointarrayforS
0x5A26	LENC_26	0x00	RW	Bit[7:0]: G06of8x8GcontrolpointarrayforS
0x5A27	LENC_27	0x00	RW	Bit[7:0]: G07of8x8GcontrolpointarrayforS
0x5A28	LENC_28	0x00	RW	Bit[7:0]: G10of8x8GcontrolpointarrayforS
0x5A29	LENC_29	0x00	RW	Bit[7:0]: G11of8x8GcontrolpointarrayforS
0x5A2A	LENC_2A	0x00	RW	Bit[7:0]: G12of8x8GcontrolpointarrayforS
0x5A2B	LENC_2B	0x00	RW	Bit[7:0]: G13of8x8GcontrolpointarrayforS
0x5A2C	LENC_2C	0x00	RW	Bit[7:0]: G14of8x8GcontrolpointarrayforS
0x5A2D	LENC_2D	0x00	RW	Bit[7:0]: G15of8x8GcontrolpointarrayforS
0x5A2E	LENC_2E	0x00	RW	Bit[7:0]: G16of8x8GcontrolpointarrayforS
0x5A2F	LENC_2F	0x00	RW	Bit[7:0]: G17of8x8GcontrolpointarrayforS
0x5A30	LENC_30	0x00	RW	Bit[7:0]: G20of8x8GcontrolpointarrayforS
0x5A31	LENC_31	0x00	RW	Bit[7:0]: G21of8x8GcontrolpointarrayforS
0x5A32	LENC_32	0x00	RW	Bit[7:0]: G22of8x8GcontrolpointarrayforS
0x5A33	LENC_33	0x00	RW	Bit[7:0]: G23of8x8GcontrolpointarrayforS
0x5A34	LENC_34	0x00	RW	Bit[7:0]: G24of8x8GcontrolpointarrayforS
0x5A35	LENC_35	0x00	RW	Bit[7:0]: G25of8x8GcontrolpointarrayforS
0x5A36	LENC_36	0x00	RW	Bit[7:0]: G26of8x8GcontrolpointarrayforS
0x5A37	LENC_37	0x00	RW	Bit[7:0]: G27of8x8GcontrolpointarrayforS
0x5A38	LENC_38	0x00	RW	Bit[7:0]: G30of8x8GcontrolpointarrayforS
0x5A39	LENC_39	0x00	RW	Bit[7:0]: G31of8x8GcontrolpointarrayforS
0x5A3A	LENC_3A	0x00	RW	Bit[7:0]: G32of8x8GcontrolpointarrayforS
0x5A3B	LENC_3B	0x00	RW	Bit[7:0]: G33of8x8GcontrolpointarrayforS

table A-2 sensor control registers (sheet 191 of 255)

address	register name	default value	R/W	description
0x5A3C	LENC_3C	0x00	RW	Bit[7:0]: G34of8x8GcontrolpointarrayforS
0x5A3D	LENC_3D	0x00	RW	Bit[7:0]: G35of8x8GcontrolpointarrayforS
0x5A3E	LENC_3E	0x00	RW	Bit[7:0]: G36of8x8GcontrolpointarrayforS
0x5A3F	LENC_3F	0x00	RW	Bit[7:0]: G37of8x8GcontrolpointarrayforS
0x5A40	LENC_40	0x00	RW	Bit[7:0]: G40of8x8GcontrolpointarrayforS
0x5A41	LENC_41	0x00	RW	Bit[7:0]: G41of8x8GcontrolpointarrayforS
0x5A42	LENC_42	0x00	RW	Bit[7:0]: G42of8x8GcontrolpointarrayforS
0x5A43	LENC_43	0x00	RW	Bit[7:0]: G43of8x8GcontrolpointarrayforS
0x5A44	LENC_44	0x00	RW	Bit[7:0]: G44of8x8GcontrolpointarrayforS
0x5A45	LENC_45	0x00	RW	Bit[7:0]: G45of8x8GcontrolpointarrayforS
0x5A46	LENC_46	0x00	RW	Bit[7:0]: G46of8x8GcontrolpointarrayforS
0x5A47	LENC_47	0x00	RW	Bit[7:0]: G47of8x8GcontrolpointarrayforS
0x5A48	LENC_48	0x00	RW	Bit[7:0]: G50of8x8GcontrolpointarrayforS
0x5A49	LENC_49	0x00	RW	Bit[7:0]: G51of8x8GcontrolpointarrayforS
0x5A4A	LENC_4A	0x00	RW	Bit[7:0]: G52of8x8GcontrolpointarrayforS
0x5A4B	LENC_4B	0x00	RW	Bit[7:0]: G53of8x8GcontrolpointarrayforS
0x5A4C	LENC_4C	0x00	RW	Bit[7:0]: G54of8x8GcontrolpointarrayforS
0x5A4D	LENC_4D	0x00	RW	Bit[7:0]: G55of8x8GcontrolpointarrayforS
0x5A4E	LENC_4E	0x00	RW	Bit[7:0]: G56of8x8GcontrolpointarrayforS
0x5A4F	LENC_4F	0x00	RW	Bit[7:0]: G57of8x8GcontrolpointarrayforS
0x5A50	LENC_50	0x00	RW	Bit[7:0]: G60of8x8GcontrolpointarrayforS
0x5A51	LENC_51	0x00	RW	Bit[7:0]: G61of8x8GcontrolpointarrayforS
0x5A52	LENC_52	0x00	RW	Bit[7:0]: G62of8x8GcontrolpointarrayforS
0x5A53	LENC_53	0x00	RW	Bit[7:0]: G63of8x8GcontrolpointarrayforS
0x5A54	LENC_54	0x00	RW	Bit[7:0]: G64of8x8GcontrolpointarrayforS
0x5A55	LENC_55	0x00	RW	Bit[7:0]: G65of8x8GcontrolpointarrayforS
0x5A56	LENC_56	0x00	RW	Bit[7:0]: G66of8x8GcontrolpointarrayforS
0x5A57	LENC_57	0x00	RW	Bit[7:0]: G67of8x8GcontrolpointarrayforS
0x5A58	LENC_58	0x00	RW	Bit[7:0]: G70of8x8GcontrolpointarrayforS
0x5A59	LENC_59	0x00	RW	Bit[7:0]: G71of8x8GcontrolpointarrayforS

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address	register name	default value	R/W	description
0x5A5A	LENC_5A	0x00	RW	Bit[7:0]: G72of8x8GcontrolpointarrayforS
0x5A5B	LENC_5B	0x00	RW	Bit[7:0]: G73of8x8GcontrolpointarrayforS
0x5A5C	LENC_5C	0x00	RW	Bit[7:0]: G74of8x8GcontrolpointarrayforS
0x5A5D	LENC_5D	0x00	RW	Bit[7:0]: G75of8x8GcontrolpointarrayforS
0x5A5E	LENC_5E	0x00	RW	Bit[7:0]: G76of8x8GcontrolpointarrayforS
0x5A5F	LENC_5F	0x00	RW	Bit[7:0]: G77of8x8GcontrolpointarrayforS
0x5A60	LENC_60	0x40	RW	Bit[7:0]: B00of8x8GcontrolpointarrayforS
0x5A61	LENC_61	0x40	RW	Bit[7:0]: B01of8x8GcontrolpointarrayforS
0x5A62	LENC_62	0x40	RW	Bit[7:0]: B02of8x8GcontrolpointarrayforS
0x5A63	LENC_63	0x40	RW	Bit[7:0]: B03of8x8GcontrolpointarrayforS
0x5A64	LENC_64	0x40	RW	Bit[7:0]: B04of8x8GcontrolpointarrayforS
0x5A65	LENC_65	0x40	RW	Bit[7:0]: B05of8x8GcontrolpointarrayforS
0x5A66	LENC_66	0x40	RW	Bit[7:0]: B06of8x8GcontrolpointarrayforS
0x5A67	LENC_67	0x40	RW	Bit[7:0]: B07of8x8GcontrolpointarrayforS
0x5A68	LENC_68	0x40	RW	Bit[7:0]: B10of8x8GcontrolpointarrayforS
0x5A69	LENC_69	0x40	RW	Bit[7:0]: B11of8x8GcontrolpointarrayforS
0x5A6A	LENC_6A	0x40	RW	Bit[7:0]: B12of8x8GcontrolpointarrayforS
0x5A6B	LENC_6B	0x40	RW	Bit[7:0]: B13of8x8GcontrolpointarrayforS
0x5A6C	LENC_6C	0x40	RW	Bit[7:0]: B14of8x8GcontrolpointarrayforS
0x5A6D	LENC_6D	0x40	RW	Bit[7:0]: B15of8x8GcontrolpointarrayforS
0x5A6E	LENC_6E	0x40	RW	Bit[7:0]: B16of8x8GcontrolpointarrayforS
0x5A6F	LENC_6F	0x40	RW	Bit[7:0]: B17of8x8GcontrolpointarrayforS
0x5A70	LENC_70	0x40	RW	Bit[7:0]: B20of8x8GcontrolpointarrayforS
0x5A71	LENC_71	0x40	RW	Bit[7:0]: B21of8x8GcontrolpointarrayforS
0x5A72	LENC_72	0x40	RW	Bit[7:0]: B22of8x8GcontrolpointarrayforS
0x5A73	LENC_73	0x40	RW	Bit[7:0]: B23of8x8GcontrolpointarrayforS
0x5A74	LENC_74	0x40	RW	Bit[7:0]: B24of8x8GcontrolpointarrayforS
0x5A75	LENC_75	0x40	RW	Bit[7:0]: B25of8x8GcontrolpointarrayforS
0x5A76	LENC_76	0x40	RW	Bit[7:0]: B26of8x8GcontrolpointarrayforS
0x5A77	LENC_77	0x40	RW	Bit[7:0]: B27of8x8GcontrolpointarrayforS

table A-2 sensor control registers (sheet 193 of 255)

address	register name	default value	R/W	description
0x5A78	LENC_78	0x40	RW	Bit[7:0]: B30of8x8GcontrolpointarrayforS
0x5A79	LENC_79	0x40	RW	Bit[7:0]: B31of8x8GcontrolpointarrayforS
0x5A7A	LENC_7A	0x40	RW	Bit[7:0]: B32of8x8GcontrolpointarrayforS
0x5A7B	LENC_7B	0x40	RW	Bit[7:0]: B33of8x8GcontrolpointarrayforS
0x5A7C	LENC_7C	0x40	RW	Bit[7:0]: B34of8x8GcontrolpointarrayforS
0x5A7D	LENC_7D	0x40	RW	Bit[7:0]: B35of8x8GcontrolpointarrayforS
0x5A7E	LENC_7E	0x40	RW	Bit[7:0]: B36of8x8GcontrolpointarrayforS
0x5A7F	LENC_7F	0x40	RW	Bit[7:0]: B37of8x8GcontrolpointarrayforS
0x5A80	LENC_80	0x40	RW	Bit[7:0]: B40of8x8GcontrolpointarrayforS
0x5A81	LENC_81	0x40	RW	Bit[7:0]: B41of8x8GcontrolpointarrayforS
0x5A82	LENC_82	0x40	RW	Bit[7:0]: B42of8x8GcontrolpointarrayforS
0x5A83	LENC_83	0x40	RW	Bit[7:0]: B43of8x8GcontrolpointarrayforS
0x5A84	LENC_84	0x40	RW	Bit[7:0]: B44of8x8GcontrolpointarrayforS
0x5A85	LENC_85	0x40	RW	Bit[7:0]: B45of8x8GcontrolpointarrayforS
0x5A86	LENC_86	0x40	RW	Bit[7:0]: B46of8x8GcontrolpointarrayforS
0x5A87	LENC_87	0x40	RW	Bit[7:0]: B47of8x8GcontrolpointarrayforS
0x5A88	LENC_88	0x40	RW	Bit[7:0]: B50of8x8GcontrolpointarrayforS
0x5A89	LENC_89	0x40	RW	Bit[7:0]: B51of8x8GcontrolpointarrayforS
0x5A8A	LENC_8A	0x40	RW	Bit[7:0]: B52of8x8GcontrolpointarrayforS
0x5A8B	LENC_8B	0x40	RW	Bit[7:0]: B53of8x8GcontrolpointarrayforS
0x5A8C	LENC_8C	0x40	RW	Bit[7:0]: B54of8x8GcontrolpointarrayforS
0x5A8D	LENC_8D	0x40	RW	Bit[7:0]: B55of8x8GcontrolpointarrayforS
0x5A8E	LENC_8E	0x40	RW	Bit[7:0]: B56of8x8GcontrolpointarrayforS
0x5A8F	LENC_8F	0x40	RW	Bit[7:0]: B57of8x8GcontrolpointarrayforS
0x5A90	LENC_90	0x40	RW	Bit[7:0]: B60of8x8GcontrolpointarrayforS
0x5A91	LENC_91	0x40	RW	Bit[7:0]: B61of8x8GcontrolpointarrayforS
0x5A92	LENC_92	0x40	RW	Bit[7:0]: B62of8x8GcontrolpointarrayforS
0x5A93	LENC_93	0x40	RW	Bit[7:0]: B63of8x8GcontrolpointarrayforS
0x5A94	LENC_94	0x40	RW	Bit[7:0]: B64of8x8GcontrolpointarrayforS
0x5A95	LENC_95	0x40	RW	Bit[7:0]: B65of8x8GcontrolpointarrayforS

table A-2 sensor control registers (sheet 194 of 255)

address	register name	default value	R/W	description
0x5A96	LENC_96	0x40	RW	Bit[7:0]: B66of8x8GcontrolpointarrayforS
0x5A97	LENC_97	0x40	RW	Bit[7:0]: B67of8x8GcontrolpointarrayforS
0x5A98	LENC_98	0x40	RW	Bit[7:0]: B70of8x8GcontrolpointarrayforS
0x5A99	LENC_99	0x40	RW	Bit[7:0]: B71of8x8GcontrolpointarrayforS
0x5A9A	LENC_9A	0x40	RW	Bit[7:0]: B72of8x8GcontrolpointarrayforS
0x5A9B	LENC_9B	0x40	RW	Bit[7:0]: B73of8x8GcontrolpointarrayforS
0x5A9C	LENC_9C	0x40	RW	Bit[7:0]: B74of8x8GcontrolpointarrayforS
0x5A9D	LENC_9D	0x40	RW	Bit[7:0]: B75of8x8GcontrolpointarrayforS
0x5A9E	LENC_9E	0x40	RW	Bit[7:0]: B76of8x8GcontrolpointarrayforS
0x5A9F	LENC_9F	0x40	RW	Bit[7:0]: B77of8x8GcontrolpointarrayforS
0x5AA0	LENC_A0	0x40	RW	Bit[7:0]: R00of8x8GcontrolpointarrayforS
0x5AA1	LENC_A1	0x40	RW	Bit[7:0]: R01of8x8GcontrolpointarrayforS
0x5AA2	LENC_A2	0x40	RW	Bit[7:0]: R02of8x8GcontrolpointarrayforS
0x5AA3	LENC_A3	0x40	RW	Bit[7:0]: R03of8x8GcontrolpointarrayforS
0x5AA4	LENC_A4	0x40	RW	Bit[7:0]: R04of8x8GcontrolpointarrayforS
0x5AA5	LENC_A5	0x40	RW	Bit[7:0]: R05of8x8GcontrolpointarrayforS
0x5AA6	LENC_A6	0x40	RW	Bit[7:0]: R06of8x8GcontrolpointarrayforS
0x5AA7	LENC_A7	0x40	RW	Bit[7:0]: R07of8x8GcontrolpointarrayforS
0x5AA8	LENC_A8	0x40	RW	Bit[7:0]: R10of8x8GcontrolpointarrayforS
0x5AA9	LENC_A9	0x40	RW	Bit[7:0]: R11of8x8GcontrolpointarrayforS
0x5AAA	LENC_AA	0x40	RW	Bit[7:0]: R12of8x8GcontrolpointarrayforS
0x5AAB	LENC_AB	0x40	RW	Bit[7:0]: R13of8x8GcontrolpointarrayforS
0x5AAC	LENC_AC	0x40	RW	Bit[7:0]: R14of8x8GcontrolpointarrayforS
0x5AAD	LENC_AD	0x40	RW	Bit[7:0]: R15of8x8GcontrolpointarrayforS
0x5AAE	LENC_AE	0x40	RW	Bit[7:0]: R16of8x8GcontrolpointarrayforS
0x5AAF	LENC_AF	0x40	RW	Bit[7:0]: R17of8x8GcontrolpointarrayforS
0x5AB0	LENC_B0	0x40	RW	Bit[7:0]: R20of8x8GcontrolpointarrayforS
0x5AB1	LENC_B1	0x40	RW	Bit[7:0]: R21of8x8GcontrolpointarrayforS
0x5AB2	LENC_B2	0x40	RW	Bit[7:0]: R22of8x8GcontrolpointarrayforS
0x5AB3	LENC_B3	0x40	RW	Bit[7:0]: R23of8x8GcontrolpointarrayforS

table A-2 sensor control registers (sheet 195 of 255)

address	register name	default value	R/W	description
0x5AB4	LENC_B4	0x40	RW	Bit[7:0]: R24of8x8GcontrolpointarrayforS
0x5AB5	LENC_B5	0x40	RW	Bit[7:0]: R25of8x8GcontrolpointarrayforS
0x5AB6	LENC_B6	0x40	RW	Bit[7:0]: R26of8x8GcontrolpointarrayforS
0x5AB7	LENC_B7	0x40	RW	Bit[7:0]: R27of8x8GcontrolpointarrayforS
0x5AB8	LENC_B8	0x40	RW	Bit[7:0]: R30of8x8GcontrolpointarrayforS
0x5AB9	LENC_B9	0x40	RW	Bit[7:0]: R31of8x8GcontrolpointarrayforS
0x5ABA	LENC_BA	0x40	RW	Bit[7:0]: R32of8x8GcontrolpointarrayforS
0x5ABB	LENC_BB	0x40	RW	Bit[7:0]: R33of8x8GcontrolpointarrayforS
0x5ABC	LENC_BC	0x40	RW	Bit[7:0]: R34of8x8GcontrolpointarrayforS
0x5ABD	LENC_BD	0x40	RW	Bit[7:0]: R35of8x8GcontrolpointarrayforS
0x5ABE	LENC_BE	0x40	RW	Bit[7:0]: R36of8x8GcontrolpointarrayforS
0x5ABF	LENC_BF	0x40	RW	Bit[7:0]: R37of8x8GcontrolpointarrayforS
0x5AC0	LENC_C0	0x40	RW	Bit[7:0]: R40of8x8GcontrolpointarrayforS
0x5AC1	LENC_C1	0x40	RW	Bit[7:0]: R41of8x8GcontrolpointarrayforS
0x5AC2	LENC_C2	0x40	RW	Bit[7:0]: R42of8x8GcontrolpointarrayforS
0x5AC3	LENC_C3	0x40	RW	Bit[7:0]: R43of8x8GcontrolpointarrayforS
0x5AC4	LENC_C4	0x40	RW	Bit[7:0]: R44of8x8GcontrolpointarrayforS
0x5AC5	LENC_C5	0x40	RW	Bit[7:0]: R45of8x8GcontrolpointarrayforS
0x5AC6	LENC_C6	0x40	RW	Bit[7:0]: R46of8x8GcontrolpointarrayforS
0x5AC7	LENC_C7	0x40	RW	Bit[7:0]: R47of8x8GcontrolpointarrayforS
0x5AC8	LENC_C8	0x40	RW	Bit[7:0]: R50of8x8GcontrolpointarrayforS
0x5AC9	LENC_C9	0x40	RW	Bit[7:0]: R51of8x8GcontrolpointarrayforS
0x5ACA	LENC_CA	0x40	RW	Bit[7:0]: R52of8x8GcontrolpointarrayforS
0x5ACB	LENC_CB	0x40	RW	Bit[7:0]: R53of8x8GcontrolpointarrayforS
0x5ACC	LENC_CC	0x40	RW	Bit[7:0]: R54of8x8GcontrolpointarrayforS
0x5ACD	LENC_CD	0x40	RW	Bit[7:0]: R55of8x8GcontrolpointarrayforS
0x5ACE	LENC_CE	0x40	RW	Bit[7:0]: R56of8x8GcontrolpointarrayforS
0x5ACF	LENC_CF	0x40	RW	Bit[7:0]: R57of8x8GcontrolpointarrayforS
0x5AD0	LENC_D0	0x40	RW	Bit[7:0]: R60of8x8GcontrolpointarrayforS
0x5AD1	LENC_D1	0x40	RW	Bit[7:0]: R61of8x8GcontrolpointarrayforS

table A-2 sensor control registers (sheet 196 of 255)

address	register name	default value	R/W	description
0x5AD2	LENC_D2	0x40	RW	Bit[7:0]: R62of8x8GcontrolpointarrayforS
0x5AD3	LENC_D3	0x40	RW	Bit[7:0]: R63of8x8GcontrolpointarrayforS
0x5AD4	LENC_D4	0x40	RW	Bit[7:0]: R64of8x8GcontrolpointarrayforS
0x5AD5	LENC_D5	0x40	RW	Bit[7:0]: R65of8x8GcontrolpointarrayforS
0x5AD6	LENC_D6	0x40	RW	Bit[7:0]: R66of8x8GcontrolpointarrayforS
0x5AD7	LENC_D7	0x40	RW	Bit[7:0]: R67of8x8GcontrolpointarrayforS
0x5AD8	LENC_D8	0x40	RW	Bit[7:0]: R70of8x8GcontrolpointarrayforS
0x5AD9	LENC_D9	0x40	RW	Bit[7:0]: R71of8x8GcontrolpointarrayforS
0x5ADA	LENC_DA	0x40	RW	Bit[7:0]: R72of8x8GcontrolpointarrayforS
0x5ADB	LENC_DB	0x40	RW	Bit[7:0]: R73of8x8GcontrolpointarrayforS
0x5ADC	LENC_DC	0x40	RW	Bit[7:0]: R74of8x8GcontrolpointarrayforS
0x5ADD	LENC_DD	0x40	RW	Bit[7:0]: R75of8x8GcontrolpointarrayforS
0x5ADE	LENC_DE	0x40	RW	Bit[7:0]: R76of8x8GcontrolpointarrayforS
0x5ADF	LENC_DF	0x40	RW	Bit[7:0]: R77of8x8GcontrolpointarrayforS
0x5AE0	LENC_E0	–	R	Bit[7:4]: Not used Bit[3:0]: pos_overflow_s_v0 H/V position overflow when calculating
0x5AE1	LENC_E1	–	R	Bit[7:4]: Not used Bit[3:0]: pos_overflow_s_v1 H/V position overflow when calculating
0x5AE2	LENC_E2	–	R	Bit[7]: Not used Bit[6:0]: m_nq_s m_nqformanual
0x5AE3	LENC_E3	–	R	Bit[7:0]: br_hscaleformannual
0x5AE4	LENC_E4	–	R	Bit[7:0]: br_hscaleformannual
0x5AE5	LENC_E5	–	R	Bit[7:0]: br_vscaleformannual
0x5AE6	LENC_E6	–	R	Bit[7:0]: br_vscaleformannual
0x5AE7	LENC_E7	–	R	Bit[7:0]: g_hscaleformannual
0x5AE8	LENC_E8	–	R	Bit[7:0]: g_hscaleformannual
0x5AE9	LENC_E9	–	R	Bit[7:0]: g_vscaleformannual
0x5AEA	LENC_EA	–	R	Bit[7:0]: g_vscaleformannual

table A-2 sensor control registers (sheet 197 of 255)

address	register name	default value	R/W	description
0x5B00	SIMPLECIP_0	0x04	RW	Bit[7:5]: Not used Bit[4:0]: BGRCoef0_0 BGR coefficient to calculate Y for L channel
0x5B01	SIMPLECIP_1	0x08	RW	Bit[7:5]: Not used Bit[4:0]: BGRCoef0_1 BGR coefficient to calculate Y for L channel
0x5B02	SIMPLECIP_2	0x04	RW	Bit[7:5]: Not used Bit[4:0]: BGRCoef0_2 BGR coefficient to calculate Y for L channel
0x5B03	SIMPLECIP_3	0x04	RW	Bit[7:5]: Not used Bit[4:0]: BGRCoef1_0 BGR coefficient to calculate Y for M channel
0x5B04	SIMPLECIP_4	0x08	RW	Bit[7:5]: Not used Bit[4:0]: BGRCoef1_1 BGR coefficient to calculate Y for M channel
0x5B05	SIMPLECIP_5	0x04	RW	Bit[7:5]: Not used Bit[4:0]: BGRCoef1_2 BGR coefficient to calculate Y for M channel
0x5B06	SIMPLECP_6	0x04	RW	Bit[7:5]: Not used Bit[4:0]: BGRCoef2_0 BGR coefficient to calculate Y for S channel
0x5B07	SIMPLECIP_7	0x08	RW	Bit[7:5]: Not used Bit[4:0]: BGRCoef2_1 BGR coefficient to calculate Y for S channel
0x5B08	SIMPLECIP_8	0x04	RW	Bit[7:5]: Not used Bit[4:0]: BGRCoef2_2 BGR coefficient to calculate Y for S channel
0x5B09	SIMPLECIP_9	0x04	RW	Bit[7:5]: Not used Bit[4:0]: BGRCoef3_0 BGR coefficient to calculate Y for V channel

table A-2 sensor control registers (sheet 198 of 255)

address	register name	default value	R/W	description
0x5B0A	SIMPLECIP_A	0x08	RW	Bit[7:5]: Not used Bit[4:0]: BGRCoef3_1 BGR coefficient to calculate Y for V channel
0x5B0B	SIMPLECIP_B	0x04	RW	Bit[7:5]: Not used Bit[4:0]: BGRCoef3_2 BGR coefficient to calculate Y for V channel
0x5B40	PMX_CTRL_00	0x01	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_D[0][0]
0x5B41	PMX_CTRL_01	0x44	RW	Bit[7:0]: m_nInvMLMS_D[0][0]
0x5B42	PMX_CTRL_02	0x03	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_D[0][1]
0x5B43	PMX_CTRL_03	0x91	RW	Bit[7:0]: m_nInvMLMS_D[0][1]
0x5B44	PMX_CTRL_04	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_D[0][2]
0x5B45	PMX_CTRL_05	0x2B	RW	Bit[7:0]: m_nInvMLMS_D[0][2]
0x5B46	PMX_CTRL_06	0x03	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_D[1][0]
0x5B47	PMX_CTRL_07	0xFF	RW	Bit[7:0]: m_nInvMLMS_D[1][0]
0x5B48	PMX_CTRL_08	0x01	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_D[1][1]
0x5B49	PMX_CTRL_09	0x04	RW	Bit[7:0]: m_nInvMLMS_D[1][1]
0x5B4A	PMX_CTRL_0A	0x03	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_D[1][2]
0x5B4B	PMX_CTRL_0B	0xFD	RW	Bit[7:0]: m_nInvMLMS_D[1][2]
0x5B4C	PMX_CTRL_0C	0x03	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_D[2][0]
0x5B4D	PMX_CTRL_0D	0xE0	RW	Bit[7:0]: m_nInvMLMS_D[2][0]
0x5B4E	PMX_CTRL_0E	0x03	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_D[2][1]
0x5B4F	PMX_CTRL_0F	0xAE	RW	Bit[7:0]: m_nInvMLMS_D[2][1]
0x5B50	PMX_CTRL_10	0x01	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_D[2][2]
0x5B51	PMX_CTRL_11	0x72	RW	Bit[7:0]: m_nInvMLMS_D[2][2]

table A-2 sensor control registers (sheet 199 of 255)

address	register name	default value	R/W	description
0x5B52	PMX_CTRL_12	0x01	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_C[0][0]
0x5B53	PMX_CTRL_13	0x00	RW	Bit[7:0]: m_nInvMLMS_C[0][0]
0x5B54	PMX_CTRL_14	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_C[0][1]
0x5B55	PMX_CTRL_15	0x00	RW	Bit[7:0]: m_nInvMLMS_C[0][1]
0x5B56	PMX_CTRL_16	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_C[0][2]
0x5B57	PMX_CTRL_17	0x00	RW	Bit[7:0]: m_nInvMLMS_C[0][2]
0x5B58	PMX_CTRL_18	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_C[1][0]
0x5B59	PMX_CTRL_19	0x00	RW	Bit[7:0]: m_nInvMLMS_C[1][0]
0x5B5A	PMX_CTRL_1A	0x01	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_C[1][1]
0x5B5B	PMX_CTRL_1B	0x00	RW	Bit[7:0]: m_nInvMLMS_C[1][1]
0x5B5C	PMX_CTRL_1C	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_C[1][2]
0x5B5D	PMX_CTRL_1D	0x00	RW	Bit[7:0]: m_nInvMLMS_C[1][2]
0x5B5E	PMX_CTRL_1E	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_C[2][0]
0x5B5F	PMX_CTRL_1F	0x00	RW	Bit[7:0]: m_nInvMLMS_C[2][0]
0x5B60	PMX_CTRL_20	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_C[2][1]
0x5B61	PMX_CTRL_21	0x00	RW	Bit[7:0]: m_nInvMLMS_C[2][1]
0x5B62	PMX_CTRL_22	0x01	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_C[2][2]
0x5B63	PMX_CTRL_23	0x00	RW	Bit[7:0]: m_nInvMLMS_C[2][2]
0x5B64	PMX_CTRL_24	0x01	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_A[0][0]
0x5B65	PMX_CTRL_25	0x00	RW	Bit[7:0]: m_nInvMLMS_A[0][0]
0x5B66	PMX_CTRL_26	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_A[0][1]
0x5B67	PMX_CTRL_27	0x00	RW	Bit[7:0]: m_nInvMLMS_A[0][1]
0x5B68	PMX_CTRL_28	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_A[0][2]

table A-2 sensor control registers (sheet 200 of 255)

address	register name	default value	R/W	description
0x5B69	PMX_CTRL_29	0x00	RW	Bit[7:0]: m_nInvMLMS_A[0][2]
0x5B6A	PMX_CTRL_2A	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_A[1][0]
0x5B6B	PMX_CTRL_2B	0x00	RW	Bit[7:0]: m_nInvMLMS_A[1][0]
0x5B6C	PMX_CTRL_2C	0x01	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_A[1][1]
0x5B6D	PMX_CTRL_2D	0x00	RW	Bit[7:0]: m_nInvMLMS_A[1][1]
0x5B6E	PMX_CTRL_2E	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_A[1][2]
0x5B6F	PMX_CTRL_2F	0x00	RW	Bit[7:0]: m_nInvMLMS_A[1][2]
0x5B70	PMX_CTRL_30	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_A[2][0]
0x5B71	PMX_CTRL_31	0x00	RW	Bit[7:0]: m_nInvMLMS_A[2][0]
0x5B72	PMX_CTRL_32	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_A[2][1]
0x5B73	PMX_CTRL_33	0x00	RW	Bit[7:0]: m_nInvMLMS_A[2][1]
0x5B74	PMX_CTRL_34	0x01	RW	Bit[7:4]: Not used Bit[3:0]: m_nInvMLMS_A[2][2]
0x5B75	PMX_CTRL_35	0x00	RW	Bit[7:0]: m_nInvMLMS_A[2][2]
0x5B76	PMX_CTRL_36	0x00	RW	Bit[7:5]: Not used Bit[4:0]: m_nManualCT
0x5B77	PMX_CTRL_37	0x98	RW	Bit[7:0]: m_nManualCT
0x5B78	PMX_CTRL_38	0x00	RW	Bit[7:5]: Not used Bit[4:0]: m_nCTList[0]
0x5B79	PMX_CTRL_39	0x98	RW	Bit[7:0]: m_nCTList[0]
0x5B7A	PMX_CTRL_3A	0x00	RW	Bit[7:5]: Not used Bit[4:0]: m_nCTList[1]
0x5B7B	PMX_CTRL_3B	0xAC	RW	Bit[7:0]: m_nCTList[1]
0x5B7C	PMX_CTRL_3C	0x01	RW	Bit[7:5]: Not used Bit[4:0]: m_nCTList[2]
0x5B7D	PMX_CTRL_3D	0x00	RW	Bit[7:0]: m_nCTList[2]
0x5B7E	PMX_CTRL_3E	0x03	RW	Bit[7:2]: Not used Bit[1]: m_bManualCTEnable Bit[0]: m_bAutoMatrixEnable

table A-2 sensor control registers (sheet 201 of 255)

address	register name	default value	R/W	description
0x5B7F	PMX_CTRL_3F	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nCustomMatrixSel
0x5B80	COMBINE_0_ISP_CTRL_00	0xE8	RW	Bit[7:6]: vs_output_option 00: Choose L output 01: choose M output 10: choose S output 11: choose VS output Bit[5]: m_bAutoErrorEnable Bit[4:3]: m_nCombineMethod Bit[2]: Not used Bit[1:0]: m_nCombineWorkMode
0x5B81	COMBINE_0_ISP_CTRL_01	0x0C	RW	Bit[7:6]: Not used Bit[5:0]: m_nStableHardThre
0x5B82	COMBINE_0_ISP_CTRL_02	0x00	RW	Bit[7:0]: m_nStableThre[0]
0x5B83	COMBINE_0_ISP_CTRL_03	0x04	RW	Bit[7:0]: m_nStableThre[0]
0x5B84	COMBINE_0_ISP_CTRL_04	0x02	RW	Bit[7:0]: m_nErrorThre[0]
0x5B85	COMBINE_0_ISP_CTRL_05	0xCC	RW	Bit[7:0]: m_nErrorThre[0]
0x5B86	COMBINE_0_ISP_CTRL_06	0x05	RW	Bit[7:5]: Not used Bit[4:0]: m_nErrorStep
0x5B87	COMBINE_0_ISP_CTRL_07	0x40	RW	Bit[7:0]: Maxiteration Reversed
0x5B88	COMBINE_0_ISP_CTRL_08	0xFF	RW	Bit[7:0]: m_nMaxExpoRatio&0xff
0x5B89	COMBINE_0_ISP_CTRL_09	0xFF	RW	Bit[7:0]: m_nMaxRealExpoRatio&0xff
0x5B8A	COMBINE_0_ISP_CTRL_0A	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][0]
0x5B8B	COMBINE_0_ISP_CTRL_0B	0x80	RW	Bit[7:0]: m_nNormCombineWeight[1][0]
0x5B8C	COMBINE_0_ISP_CTRL_ 0C	0x80	RW	Bit[7:0]: m_nNormCombineWeight[2][0]
0x5B8D	COMBINE_0_ISP_CTRL_ 0D	0x80	RW	Bit[7:0]: m_nNormCombineWeight[3][0]
0x5B8E	COMBINE_0_ISP_CTRL_0E	0x40	RW	Bit[7:0]: m_nNormCombineWeight[4][0]
0x5B8F	COMBINE_0_ISP_CTRL_0F	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][1]
0x5B90	COMBINE_0_ISP_CTRL_10	0x80	RW	Bit[7:0]: m_nNormCombineWeight[1][1]
0x5B91	COMBINE_0_ISP_CTRL_11	0x80	RW	Bit[7:0]: m_nNormCombineWeight[2][1]
0x5B92	COMBINE_0_ISP_CTRL_12	0x60	RW	Bit[7:0]: m_nNormCombineWeight[3][1]
0x5B93	COMBINE_0_ISP_CTRL_13	0x20	RW	Bit[7:0]: m_nNormCombineWeight[4][1]

table A-2 sensor control registers (sheet 202 of 255)

address	register name	default value	R/W	description
0x5B94	COMBINE_0_ISP_CTRL_14	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][2]
0x5B95	COMBINE_0_ISP_CTRL_15	0x80	RW	Bit[7:0]: m_nNormCombineWeight[1][2]
0x5B96	COMBINE_0_ISP_CTRL_16	0x80	RW	Bit[7:0]: m_nNormCombineWeight[2][2]
0x5B97	COMBINE_0_ISP_CTRL_17	0x40	RW	Bit[7:0]: m_nNormCombineWeight[3][2]
0x5B98	COMBINE_0_ISP_CTRL_18	0x00	RW	Bit[7:0]: m_nNormCombineWeight[4][2]
0x5B99	COMBINE_0_ISP_CTRL_19	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][3]
0x5B9A	COMBINE_0_ISP_CTRL_1A	0x80	RW	Bit[7:0]: m_nNormCombineWeight[1][3]
0x5B9B	COMBINE_0_ISP_CTRL_1B	0x80	RW	Bit[7:0]: m_nNormCombineWeight[2][3]
0x5B9C	COMBINE_0_ISP_CTRL_ 1C	0x20	RW	Bit[7:0]: m_nNormCombineWeight[3][3]
0x5B9D	COMBINE_0_ISP_CTRL_ 1D	0x00	RW	Bit[7:0]: m_nNormCombineWeight[4][3]
0x5B9E	COMBINE_0_ISP_CTRL_1E	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][4]
0x5B9F	COMBINE_0_ISP_CTRL_1F	0x80	RW	Bit[7:0]: m_nNormCombineWeight[1][4]
0x5BA0	COMBINE_0_ISP_CTRL_20	0x80	RW	Bit[7:0]: m_nNormCombineWeight[2][4]
0x5BA1	COMBINE_0_ISP_CTRL_21	0x10	RW	Bit[7:0]: m_nNormCombineWeight[3][4]
0x5BA2	COMBINE_0_ISP_CTRL_22	0x00	RW	Bit[7:0]: m_nNormCombineWeight[4][4]
0x5BA3	COMBINE_0_ISP_CTRL_23	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][5]
0x5BA4	COMBINE_0_ISP_CTRL_24	0x80	RW	Bit[7:0]: m_nNormCombineWeight[1][5]
0x5BA5	COMBINE_0_ISP_CTRL_25	0x80	RW	Bit[7:0]: m_nNormCombineWeight[2][5]
0x5BA6	COMBINE_0_ISP_CTRL_26	0x00	RW	Bit[7:0]: m_nNormCombineWeight[3][5]
0x5BA7	COMBINE_0_ISP_CTRL_27	0x00	RW	Bit[7:0]: m_nNormCombineWeight[4][5]
0x5BA8	COMBINE_0_ISP_CTRL_28	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreL[0]
0x5BA9	COMBINE_0_ISP_CTRL_29	0x00	RW	Bit[7:0]: m_nCombineThreL[0]
0x5BAA	COMBINE_0_ISP_CTRL_2A	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreL[1]
0x5BAB	COMBINE_0_ISP_CTRL_2B	0x76	RW	Bit[7:0]: m_nCombineThreL[1]
0x5BAC	COMBINE_0_ISP_CTRL_ 2C	0x03	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreL[2]
0x5BAD	COMBINE_0_ISP_CTRL_ 2D	0x08	RW	Bit[7:0]: m_nCombineThreL[2]

table A-2 sensor control registers (sheet 203 of 255)

address	register name	default value	R/W	description
0x5BAE	COMBINE_0_ISP_CTRL_2E	0x01	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreS[0]
0x5BAF	COMBINE_0_ISP_CTRL_2F	0x00	RW	Bit[7:0]: m_nCombineThreS[0]
0x5BB0	COMBINE_0_ISP_CTRL_30	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreS[1]
0x5BB1	COMBINE_0_ISP_CTRL_31	0x00	RW	Bit[7:0]: m_nCombineThreS[1]
0x5BB2	COMBINE_0_ISP_CTRL_32	0x03	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreS[2]
0x5BB3	COMBINE_0_ISP_CTRL_33	0x08	RW	Bit[7:0]: m_nCombineThreS[2]
0x5BB4	COMBINE_0_ISP_CTRL_34	0x05	RW	Bit[7:0]: m_nErrorThre[1]
0x5BB5	COMBINE_0_ISP_CTRL_35	0x33	RW	Bit[7:0]: m_nErrorThre[1]
0x5BB6	COMBINE_0_ISP_CTRL_36	0x00	RW	Bit[7:0]: m_nStableThre[1]
0x5BB7	COMBINE_0_ISP_CTRL_37	0x0C	RW	Bit[7:0]: m_nStableThre[1]
0x5BB8	COMBINE_0_ISP_CTRL_38	0x01	RW	Bit[7]: Not used Bit[6:0]: m_nWeightXThre
0x5BB9	COMBINE_0_ISP_CTRL_39	0x01	RW	Bit[7]: Not used Bit[6:0]: m_nWeightYThre
0x5BBA	COMBINE_0_ISP_CTRL_3A	0x01	RW	Bit[7:0]: m_nNumThre
0x5BBB	COMBINE_0_ISP_CTRL_3B	0x00	RW	Bit[7:0]: m_nNumThre
0x5BBC	COMBINE_0_ISP_CTRL_ 3C	0x04	RW	Bit[7:0]: manratio_err
0x5BBD	COMBINE_0_ISP_CTRL_ 3D	0x00	RW	Bit[7:0]: manratio_err
0x5BBE	COMBINE_0_ISP_CTRL_3E	0x12	RW	Bit[7:3]: combthre_shift Bit[2]: Not used Bit[1:0]: m_nCombineInputOption
0x5BBF	COMBINE_0_ISP_CTRL_3F	0x00	RW	Bit[7:2]: Not used Bit[1:0]: m_nThreSLow
0x5BC0	COMBINE_0_ISP_CTRL_40	0x04	RW	Bit[7:0]: m_nThreSLow
0x5BC1	COMBINE_0_ISP_CTRL_41	0x06	RW	Bit[7:3]: Not used Bit[2:0]: m_nThreSHigh
0x5BC2	COMBINE_0_ISP_CTRL_42	0xFF	RW	Bit[7:0]: m_nThreSHigh
0x5BC3	COMBINE_0_ISP_CTRL_43	0x00	RW	Bit[7:2]: Not used Bit[1:0]: m_nThreLLow
0x5BC4	COMBINE_0_ISP_CTRL_44	0x04	RW	Bit[7:0]: m_nThreLLow

table A-2 sensor control registers (sheet 204 of 255)

address	register name	default value	R/W	description
0x5BC5	COMBINE_0_ISP_CTRL_45	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nThreLHigh
0x5BC6	COMBINE_0_ISP_CTRL_46	0xB8	RW	Bit[7:0]: m_nThreLHigh
0x5BC7	COMBINE_0_ISP_CTRL_47	0x00	RW	Bit[7:3]: Not used Bit[2:0]: m_nLineNumThre
0x5BC8	COMBINE_0_ISP_CTRL_48	0x80	RW	Bit[7:0]: m_nLineNumThre
0x5BC9	COMBINE_0_ISP_CTRL_49	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[0][0]
0x5BCA	COMBINE_0_ISP_CTRL_4A	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[1][0]
0x5BCB	COMBINE_0_ISP_CTRL_4B	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[2][0]
0x5BCC	COMBINE_0_ISP_CTRL_4C	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[3][0]
0x5BCD	COMBINE_0_ISP_CTRL_4D	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[4][0]
0x5BCE	COMBINE_0_ISP_CTRL_4E	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[0][1]
0x5BCF	COMBINE_0_ISP_CTRL_4F	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[1][1]
0x5BD0	COMBINE_0_ISP_CTRL_50	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[2][1]
0x5BD1	COMBINE_0_ISP_CTRL_51	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[3][1]
0x5BD2	COMBINE_0_ISP_CTRL_52	0x60	RW	Bit[7:0]: m_nSPDCombineWeight[4][1]
0x5BD3	COMBINE_0_ISP_CTRL_53	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[0][2]
0x5BD4	COMBINE_0_ISP_CTRL_54	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[1][2]
0x5BD5	COMBINE_0_ISP_CTRL_55	0x60	RW	Bit[7:0]: m_nSPDCombineWeight[2][2]
0x5BD6	COMBINE_0_ISP_CTRL_56	0x40	RW	Bit[7:0]: m_nSPDCombineWeight[3][2]
0x5BD7	COMBINE_0_ISP_CTRL_57	0x40	RW	Bit[7:0]: m_nSPDCombineWeight[4][2]
0x5BD8	COMBINE_0_ISP_CTRL_58	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[0][3]
0x5BD9	COMBINE_0_ISP_CTRL_59	0x60	RW	Bit[7:0]: m_nSPDCombineWeight[1][3]
0x5BDA	COMBINE_0_ISP_CTRL_5A	0x40	RW	Bit[7:0]: m_nSPDCombineWeight[2][3]
0x5BDB	COMBINE_0_ISP_CTRL_5B	0x20	RW	Bit[7:0]: m_nSPDCombineWeight[3][3]
0x5BDC	COMBINE_0_ISP_CTRL_5C	0x20	RW	Bit[7:0]: m_nSPDCombineWeight[4][3]
0x5BDD	COMBINE_0_ISP_CTRL_5D	0x60	RW	Bit[7:0]: m_nSPDCombineWeight[0][4]
0x5BDE	COMBINE_0_ISP_CTRL_5E	0x40	RW	Bit[7:0]: m_nSPDCombineWeight[1][4]

table A-2 sensor control registers (sheet 205 of 255)

address	register name	default value	R/W	description
0x5BDF	COMBINE_0_ISP_CTRL_5F	0x20	RW	Bit[7:0]: m_nSPDCombineWeight[2][4]
0x5BE0	COMBINE_0_ISP_CTRL_60	0x20	RW	Bit[7:0]: m_nSPDCombineWeight[3][4]
0x5BE1	COMBINE_0_ISP_CTRL_61	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[4][4]
0x5BE2	COMBINE_0_ISP_CTRL_62	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[0][5]
0x5BE3	COMBINE_0_ISP_CTRL_63	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[1][5]
0x5BE4	COMBINE_0_ISP_CTRL_64	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[2][5]
0x5BE5	COMBINE_0_ISP_CTRL_65	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[3][5]
0x5BE6	COMBINE_0_ISP_CTRL_66	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[4][5]
0x5BE7	COMBINE_0_ISP_CTRL_67	0x06	RW	Bit[7]: m_bWeightSwitchEnable Bit[6]: m_bManualSPDFlagEnable Bit[5:4]: m_pManualSPDFlag Bit[3:0]: m_nMaxFrameShift
0x5BE8	COMBINE_0_ISP_CTRL_68	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_pSPDWeight
0x5BE9	COMBINE_0_ISP_CTRL_69	0x00	RW	Bit[7:0]: m_pSPDWeight
0x5BEA	COMBINE_0_ISP_RO_6A	–	R	Bit[7:0]: HDR max calculate in startframe for reverse AWB
0x5BEB	COMBINE_0_ISP_RO_6B	–	R	Bit[7:0]: HDR max calculate in startframe for reverse AWB
0x5BEC	COMBINE_0_ISP_RO_6C	–	R	Bit[7:0]: HDR max calculate in startframe for reverse AWB
0x5BED	COMBINE_0_ISP_RO_6D	–	R	Bit[7:2]: Not used Bit[1:0]: Real exposure ratio calculated in startframe
0x5BEE	COMBINE_0_ISP_RO_6E	–	R	Bit[7:0]: Real exposure ratio calculated in startframe
0x5BEF	COMBINE_0_ISP_RO_6F	–	R	Bit[7:0]: Real exposure ratio calculated in startframe
0x5BF0	COMBINE_0_ISP_RO_70	–	R	Bit[7:6]: Not used Bit[5:0]: Ratio for LFM
0x5BF1	COMBINE_0_ISP_RO_71	–	R	Bit[7:0]: Ratio for LFM

table A-2 sensor control registers (sheet 206 of 255)

address	register name	default value	R/W	description
0x5C00	COMBINE_1_ISP_CTRL_00	0xE8	RW	Bit[7:6]: vs_output_option 00: Choose L output 01: Choose M output 10: Choose S output 11: Choose VS output Bit[5]: m_bAutoErrorEnable Bit[4:3]: m_nCombineMethod Bit[2]: Not used Bit[1:0]: m_nCombineWorkMode
0x5C01	COMBINE_1_ISP_CTRL_01	0x0C	RW	Bit[7:6]: Not used Bit[5:0]: m_nStableHardThre
0x5C02	COMBINE_1_ISP_CTRL_02	0x00	RW	Bit[7:0]: m_nStableThre[0]
0x5C03	COMBINE_1_ISP_CTRL_03	0x04	RW	Bit[7:0]: m_nStableThre[0]
0x5C04	COMBINE_1_ISP_CTRL_04	0x02	RW	Bit[7:0]: m_nErrorThre[0]
0x5C05	COMBINE_1_ISP_CTRL_05	0xCC	RW	Bit[7:0]: m_nErrorThre[0]
0x5C06	COMBINE_1_ISP_CTRL_06	0x05	RW	Bit[7:5]: Not used Bit[4:0]: m_nErrorStep
0x5C07	COMBINE_1_ISP_CTRL_07	0x40	RW	Bit[7:0]: Maxiteration Reversed
0x5C08	COMBINE_1_ISP_CTRL_08	0xFF	RW	Bit[7:0]: m_nMaxExpoRatio&0xff
0x5C09	COMBINE_1_ISP_CTRL_09	0xFF	RW	Bit[7:0]: m_nMaxRealExpoRatio&0xff
0x5C0A	COMBINE_1_ISP_CTRL_0A	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][0]
0x5C0B	COMBINE_1_ISP_CTRL_0B	0x80	RW	Bit[7:0]: m_nNormCombineWeight[1][0]
0x5C0C	COMBINE_1_ISP_CTRL_ 0C	0x80	RW	Bit[7:0]: m_nNormCombineWeight[2][0]
0x5C0D	COMBINE_1_ISP_CTRL_ 0D	0x80	RW	Bit[7:0]: m_nNormCombineWeight[3][0]
0x5C0E	COMBINE_1_ISP_CTRL_0E	0x60	RW	Bit[7:0]: m_nNormCombineWeight[4][0]
0x5C0F	COMBINE_1_ISP_CTRL_0F	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][1]
0x5C10	COMBINE_1_ISP_CTRL_10	0x80	RW	Bit[7:0]: m_nNormCombineWeight[1][1]
0x5C11	COMBINE_1_ISP_CTRL_11	0x80	RW	Bit[7:0]: m_nNormCombineWeight[2][1]
0x5C12	COMBINE_1_ISP_CTRL_12	0x60	RW	Bit[7:0]: m_nNormCombineWeight[3][1]
0x5C13	COMBINE_1_ISP_CTRL_13	0x20	RW	Bit[7:0]: m_nNormCombineWeight[4][1]
0x5C14	COMBINE_1_ISP_CTRL_14	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][2]
0x5C15	COMBINE_1_ISP_CTRL_15	0x80	RW	Bit[7:0]: m_nNormCombineWeight[1][2]

table A-2 sensor control registers (sheet 207 of 255)

address	register name	default value	R/W	description
0x5C16	COMBINE_1_ISP_CTRL_16	0x80	RW	Bit[7:0]: m_nNormCombineWeight[2][2]
0x5C17	COMBINE_1_ISP_CTRL_17	0x20	RW	Bit[7:0]: m_nNormCombineWeight[3][2]
0x5C18	COMBINE_1_ISP_CTRL_18	0x00	RW	Bit[7:0]: m_nNormCombineWeight[4][2]
0x5C19	COMBINE_1_ISP_CTRL_19	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][3]
0x5C1A	COMBINE_1_ISP_CTRL_1A	0x40	RW	Bit[7:0]: m_nNormCombineWeight[1][3]
0x5C1B	COMBINE_1_ISP_CTRL_1B	0x20	RW	Bit[7:0]: m_nNormCombineWeight[2][3]
0x5C1C	COMBINE_1_ISP_CTRL_1C	0x00	RW	Bit[7:0]: m_nNormCombineWeight[3][3]
0x5C1D	COMBINE_1_ISP_CTRL_1D	0x00	RW	Bit[7:0]: m_nNormCombineWeight[4][3]
0x5C1E	COMBINE_1_ISP_CTRL_1E	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][4]
0x5C1F	COMBINE_1_ISP_CTRL_1F	0x00	RW	Bit[7:0]: m_nNormCombineWeight[1][4]
0x5C20	COMBINE_1_ISP_CTRL_20	0x00	RW	Bit[7:0]: m_nNormCombineWeight[2][4]
0x5C21	COMBINE_1_ISP_CTRL_21	0x00	RW	Bit[7:0]: m_nNormCombineWeight[3][4]
0x5C22	COMBINE_1_ISP_CTRL_22	0x00	RW	Bit[7:0]: m_nNormCombineWeight[4][4]
0x5C23	COMBINE_1_ISP_CTRL_23	0x00	RW	Bit[7:0]: m_nNormCombineWeight[0][5]
0x5C24	COMBINE_1_ISP_CTRL_24	0x00	RW	Bit[7:0]: m_nNormCombineWeight[1][5]
0x5C25	COMBINE_1_ISP_CTRL_25	0x00	RW	Bit[7:0]: m_nNormCombineWeight[2][5]
0x5C26	COMBINE_1_ISP_CTRL_26	0x00	RW	Bit[7:0]: m_nNormCombineWeight[3][5]
0x5C27	COMBINE_1_ISP_CTRL_27	0x00	RW	Bit[7:0]: m_nNormCombineWeight[4][5]
0x5C28	COMBINE_1_ISP_CTRL_28	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreL[0]
0x5C29	COMBINE_1_ISP_CTRL_29	0x00	RW	Bit[7:0]: m_nCombineThreL[0]
0x5C2A	COMBINE_1_ISP_CTRL_2A	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreL[1]
0x5C2B	COMBINE_1_ISP_CTRL_2B	0x76	RW	Bit[7:0]: m_nCombineThreL[1]
0x5C2C	COMBINE_1_ISP_CTRL_2C	0x03	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreL[2]
0x5C2D	COMBINE_1_ISP_CTRL_2D	0x08	RW	Bit[7:0]: m_nCombineThreL[2]
0x5C2E	COMBINE_1_ISP_CTRL_2E	0x00	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreS[0]
0x5C2F	COMBINE_1_ISP_CTRL_2F	0x80	RW	Bit[7:0]: m_nCombineThreS[0]

table A-2 sensor control registers (sheet 208 of 255)

address	register name	default value	R/W	description
0x5C30	COMBINE_1_ISP_CTRL_30	0x01	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreS[1]
0x5C31	COMBINE_1_ISP_CTRL_31	0x00	RW	Bit[7:0]: m_nCombineThreS[1]
0x5C32	COMBINE_1_ISP_CTRL_32	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreS[2]
0x5C33	COMBINE_1_ISP_CTRL_33	0x00	RW	Bit[7:0]: m_nCombineThreS[2]
0x5C34	COMBINE_1_ISP_CTRL_34	0x05	RW	Bit[7:0]: m_nErrorThre[1]
0x5C35	COMBINE_1_ISP_CTRL_35	0x33	RW	Bit[7:0]: m_nErrorThre[1]
0x5C36	COMBINE_1_ISP_CTRL_36	0x00	RW	Bit[7:0]: m_nStableThre[1]
0x5C37	COMBINE_1_ISP_CTRL_37	0x0C	RW	Bit[7:0]: m_nStableThre[1]
0x5C38	COMBINE_1_ISP_CTRL_38	0x01	RW	Bit[7]: Not used Bit[6:0]: m_nWeightXThre
0x5C39	COMBINE_1_ISP_CTRL_39	0x01	RW	Bit[7]: Not used Bit[6:0]: m_nWeightYThre
0x5C3A	COMBINE_1_ISP_CTRL_3A	0x01	RW	Bit[7:0]: m_nNumThre
0x5C3B	COMBINE_1_ISP_CTRL_3B	0x00	RW	Bit[7:0]: m_nNumThre
0x5C3C	COMBINE_1_ISP_CTRL_ 3C	0x04	RW	Bit[7:0]: manratio_err
0x5C3D	COMBINE_1_ISP_CTRL_ 3D	0x00	RW	Bit[7:0]: manratio_err
0x5C3E	COMBINE_1_ISP_CTRL_3E	0x12	RW	Bit[7:3]: combthre_shift Bit[2]: Not used Bit[1:0]: m_nCombineInputOption
0x5C3F	COMBINE_1_ISP_CTRL_3F	0x00	RW	Bit[7:2]: Not used Bit[1:0]: m_nThreSLow
0x5C40	COMBINE_1_ISP_CTRL_40	0x04	RW	Bit[7:0]: m_nThreSLow
0x5C41	COMBINE_1_ISP_CTRL_41	0x07	RW	Bit[7:3]: Not used Bit[2:0]: m_nThreSHigh
0x5C42	COMBINE_1_ISP_CTRL_42	0xFF	RW	Bit[7:0]: m_nThreSHigh
0x5C43	COMBINE_1_ISP_CTRL_43	0x00	RW	Bit[7:2]: Not used Bit[1:0]: m_nThreLLow
0x5C44	COMBINE_1_ISP_CTRL_44	0x04	RW	Bit[7:0]: m_nThreLLow
0x5C45	COMBINE_1_ISP_CTRL_45	0x03	RW	Bit[7:2]: Not used Bit[1:0]: m_nThreLHigh
0x5C46	COMBINE_1_ISP_CTRL_46	0xB8	RW	Bit[7:0]: m_nThreLHigh

table A-2 sensor control registers (sheet 209 of 255)

address	register name	default value	R/W	description
0x5C47	COMBINE_1_ISP_CTRL_47	0x00	RW	Bit[7:3]: Not used Bit[2:0]: m_nLineNumThre
0x5C48	COMBINE_1_ISP_CTRL_48	0x80	RW	Bit[7:0]: m_nLineNumThre
0x5C49	COMBINE_1_ISP_CTRL_49	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[0][0]
0x5C4A	COMBINE_1_ISP_CTRL_4A	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[1][0]
0x5C4B	COMBINE_1_ISP_CTRL_4B	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[2][0]
0x5C4C	COMBINE_1_ISP_CTRL_4C	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[3][0]
0x5C4D	COMBINE_1_ISP_CTRL_4D	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[4][0]
0x5C4E	COMBINE_1_ISP_CTRL_4E	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[0][1]
0x5C4F	COMBINE_1_ISP_CTRL_4F	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[1][1]
0x5C50	COMBINE_1_ISP_CTRL_50	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[2][1]
0x5C51	COMBINE_1_ISP_CTRL_51	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[3][1]
0x5C52	COMBINE_1_ISP_CTRL_52	0x60	RW	Bit[7:0]: m_nSPDCombineWeight[4][1]
0x5C53	COMBINE_1_ISP_CTRL_53	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[0][2]
0x5C54	COMBINE_1_ISP_CTRL_54	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[1][2]
0x5C55	COMBINE_1_ISP_CTRL_55	0x60	RW	Bit[7:0]: m_nSPDCombineWeight[2][2]
0x5C56	COMBINE_1_ISP_CTRL_56	0x40	RW	Bit[7:0]: m_nSPDCombineWeight[3][2]
0x5C57	COMBINE_1_ISP_CTRL_57	0x40	RW	Bit[7:0]: m_nSPDCombineWeight[4][2]
0x5C58	COMBINE_1_ISP_CTRL_58	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[0][3]
0x5C59	COMBINE_1_ISP_CTRL_59	0x60	RW	Bit[7:0]: m_nSPDCombineWeight[1][3]
0x5C5A	COMBINE_1_ISP_CTRL_5A	0x40	RW	Bit[7:0]: m_nSPDCombineWeight[2][3]
0x5C5B	COMBINE_1_ISP_CTRL_5B	0x20	RW	Bit[7:0]: m_nSPDCombineWeight[3][3]
0x5C5C	COMBINE_1_ISP_CTRL_5C	0x20	RW	Bit[7:0]: m_nSPDCombineWeight[4][3]
0x5C5D	COMBINE_1_ISP_CTRL_5D	0x60	RW	Bit[7:0]: m_nSPDCombineWeight[0][4]
0x5C5E	COMBINE_1_ISP_CTRL_5E	0x40	RW	Bit[7:0]: m_nSPDCombineWeight[1][4]
0x5C5F	COMBINE_1_ISP_CTRL_5F	0x20	RW	Bit[7:0]: m_nSPDCombineWeight[2][4]
0x5C60	COMBINE_1_ISP_CTRL_60	0x20	RW	Bit[7:0]: m_nSPDCombineWeight[3][4]
0x5C61	COMBINE_1_ISP_CTRL_61	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[4][4]

table A-2 sensor control registers (sheet 210 of 255)

address	register name	default value	R/W	description
0x5C62	COMBINE_1_ISP_CTRL_62	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[0][5]
0x5C63	COMBINE_1_ISP_CTRL_63	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[1][5]
0x5C64	COMBINE_1_ISP_CTRL_64	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[2][5]
0x5C65	COMBINE_1_ISP_CTRL_65	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[3][5]
0x5C66	COMBINE_1_ISP_CTRL_66	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[4][5]
0x5C67	COMBINE_1_ISP_CTRL_67	0x06	RW	Bit[7]: m_bWeightSwitchEnable Bit[6]: m_bManualSPDFlagEnable Bit[5:4]: m_pManualSPDFlag Bit[3:0]: m_nMaxFrameShift
0x5C68	COMBINE_1_ISP_CTRL_68	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_pSPDWeight
0x5C69	COMBINE_1_ISP_CTRL_69	0x00	RW	Bit[7:0]: m_pSPDWeight
0x5C6A	COMBINE_1_ISP_RO_6A	–	R	Bit[7:0]: HDR max calculate in startframe for reverse AWB
0x5C6B	COMBINE_1_ISP_RO_6B	–	R	Bit[7:0]: HDR max calculate in startframe for reverse AWB
0x5C6C	COMBINE_1_ISP_RO_6C	–	R	Bit[7:0]: HDR max calculate in startframe for reverse AWB
0x5C6D	COMBINE_1_ISP_RO_6D	–	R	Bit[7:2]: Not used Bit[1:0]: Real exposure ratio calculated in startframe
0x5C6E	COMBINE_1_ISP_RO_6E	–	R	Bit[7:0]: Real exposure ratio calculated in startframe
0x5C6F	COMBINE_1_ISP_RO_6F	–	R	Bit[7:0]: Real exposure ratio calculated in startframe
0x5C70	COMBINE_1_ISP_RO_70	–	R	Bit[7:6]: Not used Bit[5:0]: Ratio for LFM
0x5C71	COMBINE_1_ISP_RO_71	–	R	Bit[7:0]: Ratio for LFM
0x5C80	COMBINE_2_ISP_CTRL_00	0xE0	RW	Bit[7:6]: vs_output_option 00: Choose L output 01: Choose M output 10: Choose S output 11: Choose VS output Bit[5]: m_bAutoErrorEnable Bit[4:3]: m_nCombineMethod Bit[2]: Not used Bit[1:0]: m_nCombineWorkMode

table A-2 sensor control registers (sheet 211 of 255)

address	register name	default value	R/W	description
0x5C81	COMBINE_2_ISP_CTRL_01	0x0C	RW	Bit[7:6]: Not used Bit[5:0]: m_nStableHardThre
0x5C82	COMBINE_2_ISP_CTRL_02	0x00	RW	Bit[7:0]: m_nStableThre[0]
0x5C83	COMBINE_2_ISP_CTRL_03	0x04	RW	Bit[7:0]: m_nStableThre[0]
0x5C84	COMBINE_2_ISP_CTRL_04	0x02	RW	Bit[7:0]: m_nErrorThre[0]
0x5C85	COMBINE_2_ISP_CTRL_05	0xCC	RW	Bit[7:0]: m_nErrorThre[0]
0x5C86	COMBINE_2_ISP_CTRL_06	0x05	RW	Bit[7:5]: Not used Bit[4:0]: m_nErrorStep
0x5C87	COMBINE_2_ISP_CTRL_07	0x40	RW	Bit[7:0]: Maxiteration Reversed
0x5C88	COMBINE_2_ISP_CTRL_08	0xFF	RW	Bit[7:0]: m_nMaxExpoRatio&0xff
0x5C89	COMBINE_2_ISP_CTRL_09	0xFF	RW	Bit[7:0]: m_nMaxRealExpoRatio&0xff
0x5C8A	COMBINE_2_ISP_CTRL_0A	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][0]
0x5C8B	COMBINE_2_ISP_CTRL_0B	0x80	RW	Bit[7:0]: m_nNormCombineWeight[1][0]
0x5C8C	COMBINE_2_ISP_CTRL_ 0C	0x80	RW	Bit[7:0]: m_nNormCombineWeight[2][0]
0x5C8D	COMBINE_2_ISP_CTRL_ 0D	0x80	RW	Bit[7:0]: m_nNormCombineWeight[3][0]
0x5C8E	COMBINE_2_ISP_CTRL_0E	0x80	RW	Bit[7:0]: m_nNormCombineWeight[4][0]
0x5C8F	COMBINE_2_ISP_CTRL_0F	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][1]
0x5C90	COMBINE_2_ISP_CTRL_10	0x80	RW	Bit[7:0]: m_nNormCombineWeight[1][1]
0x5C91	COMBINE_2_ISP_CTRL_11	0x80	RW	Bit[7:0]: m_nNormCombineWeight[2][1]
0x5C92	COMBINE_2_ISP_CTRL_12	0x80	RW	Bit[7:0]: m_nNormCombineWeight[3][1]
0x5C93	COMBINE_2_ISP_CTRL_13	0x60	RW	Bit[7:0]: m_nNormCombineWeight[4][1]
0x5C94	COMBINE_2_ISP_CTRL_14	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][2]
0x5C95	COMBINE_2_ISP_CTRL_15	0x80	RW	Bit[7:0]: m_nNormCombineWeight[1][2]
0x5C96	COMBINE_2_ISP_CTRL_16	0x80	RW	Bit[7:0]: m_nNormCombineWeight[2][2]
0x5C97	COMBINE_2_ISP_CTRL_17	0x60	RW	Bit[7:0]: m_nNormCombineWeight[3][2]
0x5C98	COMBINE_2_ISP_CTRL_18	0x40	RW	Bit[7:0]: m_nNormCombineWeight[4][2]
0x5C99	COMBINE_2_ISP_CTRL_19	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][3]
0x5C9A	COMBINE_2_ISP_CTRL_1A	0x80	RW	Bit[7:0]: m_nNormCombineWeight[1][3]
0x5C9B	COMBINE_2_ISP_CTRL_1B	0x80	RW	Bit[7:0]: m_nNormCombineWeight[2][3]

table A-2 sensor control registers (sheet 212 of 255)

address	register name	default value	R/W	description
0x5C9C	COMBINE_2_ISP_CTRL_1C	0x40	RW	Bit[7:0]: m_nNormCombineWeight[3][3]
0x5C9D	COMBINE_2_ISP_CTRL_1D	0x20	RW	Bit[7:0]: m_nNormCombineWeight[4][3]
0x5C9E	COMBINE_2_ISP_CTRL_1E	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][4]
0x5C9F	COMBINE_2_ISP_CTRL_1F	0x80	RW	Bit[7:0]: m_nNormCombineWeight[1][4]
0x5CA0	COMBINE_2_ISP_CTRL_20	0x80	RW	Bit[7:0]: m_nNormCombineWeight[2][4]
0x5CA1	COMBINE_2_ISP_CTRL_21	0x20	RW	Bit[7:0]: m_nNormCombineWeight[3][4]
0x5CA2	COMBINE_2_ISP_CTRL_22	0x00	RW	Bit[7:0]: m_nNormCombineWeight[4][4]
0x5CA3	COMBINE_2_ISP_CTRL_23	0x80	RW	Bit[7:0]: m_nNormCombineWeight[0][5]
0x5CA4	COMBINE_2_ISP_CTRL_24	0x80	RW	Bit[7:0]: m_nNormCombineWeight[1][5]
0x5CA5	COMBINE_2_ISP_CTRL_25	0x80	RW	Bit[7:0]: m_nNormCombineWeight[2][5]
0x5CA6	COMBINE_2_ISP_CTRL_26	0x00	RW	Bit[7:0]: m_nNormCombineWeight[3][5]
0x5CA7	COMBINE_2_ISP_CTRL_27	0x00	RW	Bit[7:0]: m_nNormCombineWeight[4][5]
0x5CA8	COMBINE_2_ISP_CTRL_28	0x01	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreL[0]
0x5CA9	COMBINE_2_ISP_CTRL_29	0x00	RW	Bit[7:0]: m_nCombineThreL[0]
0x5CAA	COMBINE_2_ISP_CTRL_2A	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreL[1]
0x5CAB	COMBINE_2_ISP_CTRL_2B	0x00	RW	Bit[7:0]: m_nCombineThreL[1]
0x5CAC	COMBINE_2_ISP_CTRL_2C	0x03	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreL[2]
0x5CAD	COMBINE_2_ISP_CTRL_2D	0x08	RW	Bit[7:0]: m_nCombineThreL[2]
0x5CAE	COMBINE_2_ISP_CTRL_2E	0x01	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreS[0]
0x5CAF	COMBINE_2_ISP_CTRL_2F	0x00	RW	Bit[7:0]: m_nCombineThreS[0]
0x5CB0	COMBINE_2_ISP_CTRL_30	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreS[1]
0x5CB1	COMBINE_2_ISP_CTRL_31	0x00	RW	Bit[7:0]: m_nCombineThreS[1]
0x5CB2	COMBINE_2_ISP_CTRL_32	0x03	RW	Bit[7:2]: Not used Bit[1:0]: m_nCombineThreS[2]
0x5CB3	COMBINE_2_ISP_CTRL_33	0x08	RW	Bit[7:0]: m_nCombineThreS[2]

table A-2 sensor control registers (sheet 213 of 255)

address	register name	default value	R/W	description
0x5CB4	COMBINE_2_ISP_CTRL_34	0x05	RW	Bit[7:0]: m_nErrorThre[1]
0x5CB5	COMBINE_2_ISP_CTRL_35	0x33	RW	Bit[7:0]: m_nErrorThre[1]
0x5CB6	COMBINE_2_ISP_CTRL_36	0x00	RW	Bit[7:0]: m_nStableThre[1]
0x5CB7	COMBINE_2_ISP_CTRL_37	0x0C	RW	Bit[7:0]: m_nStableThre[1]
0x5CB8	COMBINE_2_ISP_CTRL_38	0x01	RW	Bit[7]: Not used Bit[6:0]: m_nWeightXThre
0x5CB9	COMBINE_2_ISP_CTRL_39	0x01	RW	Bit[7]: Not used Bit[6:0]: m_nWeightYThre
0x5CBA	COMBINE_2_ISP_CTRL_3A	0x01	RW	Bit[7:0]: m_nNumThre
0x5CBB	COMBINE_2_ISP_CTRL_3B	0x00	RW	Bit[7:0]: m_nNumThre
0x5CBC	COMBINE_2_ISP_CTRL_ 3C	0x04	RW	Bit[7:0]: manratio_err
0x5CBD	COMBINE_2_ISP_CTRL_ 3D	0x00	RW	Bit[7:0]: manratio_err
0x5CBE	COMBINE_2_ISP_CTRL_3E	0x12	RW	Bit[7:3]: combthre_shift Bit[2]: Not used Bit[1:0]: m_nCombineInputOption
0x5CBF	COMBINE_2_ISP_CTRL_3F	0x00	RW	Bit[7:2]: Not used Bit[1:0]: m_nThreSLow
0x5CC0	COMBINE_2_ISP_CTRL_40	0x20	RW	Bit[7:0]: m_nThreSLow
0x5CC1	COMBINE_2_ISP_CTRL_41	0x07	RW	Bit[7:3]: Not used Bit[2:0]: m_nThreSHigh
0x5CC2	COMBINE_2_ISP_CTRL_42	0xFF	RW	Bit[7:0]: m_nThreSHigh
0x5CC3	COMBINE_2_ISP_CTRL_43	0x00	RW	Bit[7:2]: Not used Bit[1:0]: m_nThreLLow
0x5CC4	COMBINE_2_ISP_CTRL_44	0x20	RW	Bit[7:0]: m_nThreLLow
0x5CC5	COMBINE_2_ISP_CTRL_45	0x03	RW	Bit[7:2]: Not used Bit[1:0]: m_nThreLHigh
0x5CC6	COMBINE_2_ISP_CTRL_46	0xB8	RW	Bit[7:0]: m_nThreLHigh
0x5CC7	COMBINE_2_ISP_CTRL_47	0x00	RW	Bit[7:3]: Not used Bit[2:0]: m_nLineNumThre
0x5CC8	COMBINE_2_ISP_CTRL_48	0x80	RW	Bit[7:0]: m_nLineNumThre
0x5CC9	COMBINE_2_ISP_CTRL_49	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[0][0]
0x5CCA	COMBINE_2_ISP_CTRL_4A	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[1][0]

table A-2 sensor control registers (sheet 214 of 255)

address	register name	default value	R/W	description
0x5CCB	COMBINE_2_ISP_CTRL_4B	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[2][0]
0x5CCC	COMBINE_2_ISP_CTRL_4C	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[3][0]
0x5CCD	COMBINE_2_ISP_CTRL_4D	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[4][0]
0x5CCE	COMBINE_2_ISP_CTRL_4E	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[0][1]
0x5CCF	COMBINE_2_ISP_CTRL_4F	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[1][1]
0x5CD0	COMBINE_2_ISP_CTRL_50	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[2][1]
0x5CD1	COMBINE_2_ISP_CTRL_51	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[3][1]
0x5CD2	COMBINE_2_ISP_CTRL_52	0x60	RW	Bit[7:0]: m_nSPDCombineWeight[4][1]
0x5CD3	COMBINE_2_ISP_CTRL_53	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[0][2]
0x5CD4	COMBINE_2_ISP_CTRL_54	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[1][2]
0x5CD5	COMBINE_2_ISP_CTRL_55	0x60	RW	Bit[7:0]: m_nSPDCombineWeight[2][2]
0x5CD6	COMBINE_2_ISP_CTRL_56	0x40	RW	Bit[7:0]: m_nSPDCombineWeight[3][2]
0x5CD7	COMBINE_2_ISP_CTRL_57	0x40	RW	Bit[7:0]: m_nSPDCombineWeight[4][2]
0x5CD8	COMBINE_2_ISP_CTRL_58	0x80	RW	Bit[7:0]: m_nSPDCombineWeight[0][3]
0x5CD9	COMBINE_2_ISP_CTRL_59	0x60	RW	Bit[7:0]: m_nSPDCombineWeight[1][3]
0x5CDA	COMBINE_2_ISP_CTRL_5A	0x40	RW	Bit[7:0]: m_nSPDCombineWeight[2][3]
0x5CDB	COMBINE_2_ISP_CTRL_5B	0x20	RW	Bit[7:0]: m_nSPDCombineWeight[3][3]
0x5CDC	COMBINE_2_ISP_CTRL_5C	0x20	RW	Bit[7:0]: m_nSPDCombineWeight[4][3]
0x5CDD	COMBINE_2_ISP_CTRL_5D	0x60	RW	Bit[7:0]: m_nSPDCombineWeight[0][4]
0x5CDE	COMBINE_2_ISP_CTRL_5E	0x40	RW	Bit[7:0]: m_nSPDCombineWeight[1][4]
0x5CDF	COMBINE_2_ISP_CTRL_5F	0x20	RW	Bit[7:0]: m_nSPDCombineWeight[2][4]
0x5CE0	COMBINE_2_ISP_CTRL_60	0x20	RW	Bit[7:0]: m_nSPDCombineWeight[3][4]
0x5CE1	COMBINE_2_ISP_CTRL_61	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[4][4]
0x5CE2	COMBINE_2_ISP_CTRL_62	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[0][5]
0x5CE3	COMBINE_2_ISP_CTRL_63	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[1][5]
0x5CE4	COMBINE_2_ISP_CTRL_64	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[2][5]
0x5CE5	COMBINE_2_ISP_CTRL_65	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[3][5]

table A-2 sensor control registers (sheet 215 of 255)

address	register name	default value	R/W	description
0x5CE6	COMBINE_2_ISP_CTRL_66	0x00	RW	Bit[7:0]: m_nSPDCombineWeight[4][5]
0x5CE7	COMBINE_2_ISP_CTRL_67	0x06	RW	Bit[7]: m_bWeightSwitchEnable Bit[6]: m_bManualSPDFlagEnable Bit[5:4]: m_pManualSPDFlag Bit[3:0]: m_nMaxFrameShift
0x5CE8	COMBINE_2_ISP_CTRL_68	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_pSPDWeight
0x5CE9	COMBINE_2_ISP_CTRL_69	0x00	RW	Bit[7:0]: m_pSPDWeight
0x5CEA	COMBINE_2_ISP_RO_6A	–	R	Bit[7:0]: HDR max calculate in startframe for reverse AWB
0x5CEB	COMBINE_2_ISP_RO_6B	–	R	Bit[7:0]: HDR max calculate in startframe for reverse AWB
0x5CEC	COMBINE_2_ISP_RO_6C	–	R	Bit[7:0]: HDR max calculate in startframe for reverse AWB
0x5CED	COMBINE_2_ISP_RO_6D	–	R	Bit[7:2]: Not used Bit[1:0]: Real exposure ratio calculated in startframe
0x5CEE	COMBINE_2_ISP_RO_6E	–	R	Bit[7:0]: Real exposure ratio calculated in startframe
0x5CEF	COMBINE_2_ISP_RO_6F	–	R	Bit[7:0]: Real exposure ratio calculated in startframe
0x5CF0	COMBINE_2_ISP_RO_70	–	R	Bit[7:6]: Not used Bit[5:0]: Ratio for LFM
0x5CF1	COMBINE_2_ISP_RO_71	–	R	Bit[7:0]: Ratio for LFM
0x5D00	LFM_CTRL_00	0x00	RW	Bit[7:1]: Not used Bit[0]: man_cal_en Manual start frame enable, hardware only register
0x5D01	LFM_CTRL_01	0x00	RW	Bit[7:1]: Not used Bit[0]: Manual ratio enable Hardware only register
0x5D02	LFM_CTRL_02	0x00	RW	Bit[7:1]: Not used Bit[0]: Manual SPD index enable Hardware only register
0x5D03	LFM_CTRL_03	0x00	RW	Bit[7:1]: Not used Bit[0]: bSPDShiftManual
0x5D04	LFM_CTRL_04	0x00	RW	Bit[7:0]: nSPDShiftCoef0
0x5D05	LFM_CTRL_05	0x00	RW	Bit[7:0]: nSPDShiftCoef1

table A-2 sensor control registers (sheet 216 of 255)

address	register name	default value	R/W	description
0x5D06	LFM_CTRL_06	0x00	RW	Bit[7:0]: nSPDShiftCoef2
0x5D07	LFM_CTRL_07	0x00	RW	Bit[7:0]: nSPDShiftCoef3
0x5D08	LFM_CTRL_08	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Kneepointvl2 Lower knee point for L/S exposure
0x5D09	LFM_CTRL_09	0x6B	RW	Bit[7:0]: Kneepointvl2 Lower knee point for L/S exposure
0x5D0A	LFM_CTRL_0A	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Kneepointl2 Lower knee point for S/VS Exposure
0x5D0B	LFM_CTRL_0B	0x6B	RW	Bit[7:0]: Kneepointl2 Lower knee point for S/VS Exposure
0x5D0D	LFM_CTRL_0D	0x0A	RW	Bit[7:6]: Not used Bit[5:0]: Diffthreshcoef1 Difference threshold for L/S
0x5D0E	LFM_CTRL_0E	0x0A	RW	Bit[7:6]: Not used Bit[5:0]: Diffthreshcoef2 Difference threshold for S/VS
0x5D0F	LFM_CTRL_0F	0x10	RW	Bit[7:6]: Not used Bit[5:0]: Diffthreshcoef3 Difference threshold for S/VS
0x5D11	LFM_CTRL_11	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Slopecoef1 Slope1 coefficient for L/S difference
0x5D12	LFM_CTRL_12	0x10	RW	Bit[7:6]: Not used Bit[5:0]: Slopecoef2 Slope1 coefficient for S/VS difference
0x5D13	LFM_CTRL_13	0x10	RW	Bit[7:6]: Not used Bit[5:0]: Slopecoef3 Slope1 coefficient for S/VS difference
0x5D15	LFM_CTRL_15	0x0C	RW	Bit[7:0]: Minthresh1 Minimum threshold for VL/SPD difference
0x5D16	LFM_CTRL_16	0x10	RW	Bit[7:0]: Minthresh2 Minimum threshold for L/SPD difference

table A-2 sensor control registers (sheet 217 of 255)

address	register name	default value	R/W	description
0x5D17	LFM_CTRL_17	0x0C	RW	Bit[7:0]: Minthresh3 Minimum threshold for VS/SPD difference
0x5D18	LFM_CTRL_18	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Kneepointvs2 Lower knee point for S/VS exposure
0x5D19	LFM_CTRL_19	0x6B	RW	Bit[7:0]: Kneepointvs2 Lower knee point for S/VS exposure
0x5D1A	LFM_CTRL_1A	0x04	RW	Bit[7:4]: Not used Bit[3:0]: VLSPDWeightCoef
0x5D1B	LFM_CTRL_1B	0x44	RW	Bit[7:4]: LSPDWeightCoef Bit[3:0]: VSSPDWeightCoef
0x5D1E	LFM_CTRL_1E	0x00	RW	Bit[7:0]: Lfmthr0 Low threshold for LFM bit
0x5D1F	LFM_CTRL_1F	0x81	RW	Bit[7:0]: Lfmthr1 High threshold for LFM bit
0x5D20	LFM_CTRL_20	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Manual input hsize Hardware only register
0x5D21	LFM_CTRL_21	0x80	RW	Bit[7:0]: Manual input hsize Hardware only register
0x5D22	LFM_CTRL_22	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Manual input vsize Hardware only register
0x5D23	LFM_CTRL_23	0xE0	RW	Bit[7:0]: Manual input vsize Hardware only register
0x5D24	LFM_CTRL_24	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual ratio1 Hardware only register
0x5D25	LFM_CTRL_25	0x00	RW	Bit[7:0]: Manual ratio1 Hardware only register
0x5D26	LFM_CTRL_26	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual ratio2 Hardware only register
0x5D27	LFM_CTRL_27	0x00	RW	Bit[7:0]: Manual ratio2 Hardware only register

table A-2 sensor control registers (sheet 218 of 255)

address	register name	default value	R/W	description
0x5D2A	LFM_CTRL_2A	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual ratio3 Hardware only register
0x5D2B	LFM_CTRL_2B	0x00	RW	Bit[7:0]: Manual ratio3 Hardware only register
0x5D2D	LFM_CTRL_2D	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Manual ratio SPD1 Hardware only register
0x5D2E	LFM_CTRL_2E	0x00	RW	Bit[7:0]: Manual ratio SPD1 Hardware only register
0x5D2F	LFM_CTRL_2F	0x00	RW	Bit[7:0]: Manual ratio SPD1 Hardware only register
0x5D31	LFM_CTRL_31	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Manual ratio SPD2 Hardware only register
0x5D32	LFM_CTRL_32	0x00	RW	Bit[7:0]: Manual ratio SPD2 Hardware only register
0x5D33	LFM_CTRL_33	0x00	RW	Bit[7:0]: Manual ratio SPD2 Hardware only register
0x5D35	LFM_CTRL_35	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Manual ratio SPD3 Hardware only register
0x5D36	LFM_CTRL_36	0x00	RW	Bit[7:0]: Manual ratio SPD3 Hardware only register
0x5D37	LFM_CTRL_37	0x00	RW	Bit[7:0]: Manual ratio SPD3 Hardware only register
0x5D38	LFM_CTRL_38	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual diffratio1 Hardware only register
0x5D39	LFM_CTRL_39	0x00	RW	Bit[7:0]: Manual diffratio1 Hardware only register
0x5D3A	LFM_CTRL_3A	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual diffratio2 Hardware only register
0x5D3B	LFM_CTRL_3B	0x00	RW	Bit[7:0]: Manual diffratio2 Hardware only register
0x5D3C	LFM_CTRL_3C	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual diffratio3 Hardware only register

table A-2 sensor control registers (sheet 219 of 255)

address	register name	default value	R/W	description
0x5D3D	LFM_CTRL_3D	0x00	RW	Bit[7:0]: Manual diffratio3 Hardware only register
0x5D3F	LFM_CTRL_3F	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual SPD index Hardware only register
0x5D40	LFM_CTRL_40	0x01	RW	Bit[7:2]: Not used Bit[1:0]: LFM diff coef auto mode
0x5D41	LFM_CTRL_41	0x01	RW	Bit[7:1]: Not used Bit[0]: LFM coef auto mode use long exp
0x5D42	LFM_CTRL_42	0x00	RW	Bit[7:0]: LFM diff coef exp low threshold
0x5D43	LFM_CTRL_43	0x64	RW	Bit[7:0]: LFM diff coef exp low threshold
0x5D44	LFM_CTRL_44	0x01	RW	Bit[7:0]: LFM diff coef exp high threshold
0x5D45	LFM_CTRL_45	0xF4	RW	Bit[7:0]: LFM diff coef exp high threshold
0x5D46	LFM_CTRL_46	0x00	RW	Bit[7:0]: LFM slope exp low threshold
0x5D47	LFM_CTRL_47	0x64	RW	Bit[7:0]: LFM slope exp low threshold
0x5D48	LFM_CTRL_48	0x01	RW	Bit[7:0]: LFM slope exp high threshold
0x5D49	LFM_CTRL_49	0xF4	RW	Bit[7:0]: LFM slope exp high threshold
0x5D4A	LFM_CTRL_4A	0x04	RW	Bit[7:0]: diffthrecoefvl_spdthrel0 LFM difference threshold low value for L vs SPD for SPD low threshold
0x5D4B	LFM_CTRL_4B	0x04	RW	Bit[7:0]: diffthrecoefvl_spdthrel1 LFM difference threshold low value for L vs SPD for SPD low threshold
0x5D4C	LFM_CTRL_4C	0x04	RW	Bit[7:0]: diffthrecoefl_spdthrel0 LFM difference threshold high value for L vs SPD for SPD low threshold
0x5D4D	LFM_CTRL_4D	0x04	RW	Bit[7:0]: diffthrecoefl_spdthrel1 LFM difference threshold high value for L vs SPD for SPD low threshold
0x5D4E	LFM_CTRL_4E	0x04	RW	Bit[7:0]: diffthrecoefvs_spdthrel0 LFM difference threshold low value for S vs SPD for SPD low threshold

table A-2 sensor control registers (sheet 220 of 255)

address	register name	default value	R/W	description
0x5D4F	LFM_CTRL_4F	0x04	RW	Bit[7:0]: diffthrecoefvs_spdthrel1 LFM difference threshold high value for L vs SPD for SPD low threshold
0x5D50	LFM_CTRL_50	0x04	RW	Bit[7:0]: diffthrecoefvl_spdthreh0 LFM difference threshold low value for L vs SPD for SPD high threshold
0x5D51	LFM_CTRL_51	0x04	RW	Bit[7:0]: diffthrecoefvl_spdthreh1 LFM difference threshold low value for L vs SPD for SPD high threshold
0x5D52	LFM_CTRL_52	0x04	RW	Bit[7:0]: diffthrecoefl_spdthreh0 LFM difference threshold high value for L vs SPD for SPD high threshold
0x5D53	LFM_CTRL_53	0x04	RW	Bit[7:0]: diffthrecoefl_spdthreh1 LFM difference threshold high value for L vs SPD for SPD high threshold
0x5D54	LFM_CTRL_54	0x04	RW	Bit[7:0]: diffthrecoefvs_spdthreh0 LFM difference threshold low value for S vs SPD for SPD high threshold
0x5D55	LFM_CTRL_55	0x04	RW	Bit[7:0]: diffthrecoefvs_spdthreh1 LFM difference threshold low value for S vs SPD for SPD high threshold
0x5D56	LFM_CTRL_56	0x00	RW	Bit[7:2]: Not used Bit[1:0]: diffthrecoef_spdthrel0 SPD low threshold for difference threshold coefficient (VL-SPD, L-SPD, VS-SPD)
0x5D57	LFM_CTRL_57	0x0C	RW	Bit[7:0]: diffthrecoef_spdthrel0 SPD low threshold for difference threshold coefficient (VL-SPD, L-SPD, VS-SPD)
0x5D58	LFM_CTRL_58	0x00	RW	Bit[7:2]: Not used Bit[1:0]: diffthrecoef_spdthrel1 SPD low threshold for difference threshold coefficient (VL-SPD, L-SPD, VS-SPD)

table A-2 sensor control registers (sheet 221 of 255)

address	register name	default value	R/W	description
0x5D59	LFM_CTRL_59	0x0C	RW	Bit[7:0]: diffthrecoef_spdthrel1 SPD low threshold for difference threshold coefficient (VL-SPD, L-SPD, VS-SPD)
0x5D5A	LFM_CTRL_5A	0x00	RW	Bit[7:2]: Not used Bit[1:0]: diffthrecoef_spdthrel2 SPD low threshold for difference threshold coefficient (VL-SPD, L-SPD, VS-SPD)
0x5D5B	LFM_CTRL_5B	0x0C	RW	Bit[7:0]: diffthrecoef_spdthrel2 SPD low threshold for difference threshold coefficient (VL-SPD, L-SPD, VS-SPD)
0x5D5C	LFM_CTRL_5C	0x00	RW	Bit[7:2]: Not used Bit[1:0]: diffthrecoef_spdthreh0 SPD low threshold for difference threshold coefficient (VL-SPD, L-SPD, VS-SPD)
0x5D5D	LFM_CTRL_5D	0x0C	RW	Bit[7:0]: diffthrecoef_spdthreh0 SPD low threshold for difference threshold coefficient (VL-SPD, L-SPD, VS-SPD)
0x5D5E	LFM_CTRL_5E	0x00	RW	Bit[7:2]: Not used Bit[1:0]: diffthrecoef_spdthreh1 SPD low threshold for difference threshold coefficient (VL-SPD, L-SPD, VS-SPD)
0x5D5F	LFM_CTRL_5F	0x0C	RW	Bit[7:0]: diffthrecoef_spdthreh1 SPD low threshold for difference threshold coefficient (VL-SPD, L-SPD, VS-SPD)
0x5D60	LFM_CTRL_60	0x00	RW	Bit[7:2]: Not used Bit[1:0]: diffthrecoef_spdthreh2 SPD low threshold for difference threshold coefficient (VL-SPD, L-SPD, VS-SPD)
0x5D61	LFM_CTRL_61	0x0C	RW	Bit[7:0]: diffthrecoef_spdthreh2 SPD low threshold for difference threshold coefficient (VL-SPD, L-SPD, VS-SPD)

table A-2 sensor control registers (sheet 222 of 255)

address	register name	default value	R/W	description
0x5D62	LFM_CTRL_62	0x03	RW	Bit[7:3]: Not used Bit[2]: diffthre_adjsel LFM defective adjust signal select between LPD and SPD Bit[1]: Difference threshold correction when SPD is darker enable Bit[0]: SPD adaptive LFM weight enable
0x5D63	LFM_CTRL_63	0x0C	RW	Bit[7:0]: spd_min_thre Minimum threshold for SPD before ratio
0x5D64	LFM_CTRL_64	0x01	RW	Bit[7:1]: Not used Bit[0]: min_thre_slope Slope of minimum threshold before ratio
0x5D65	LFM_CTRL_65	0x00	RW	Bit[7:0]: min_thre_slope Slope of minimum threshold before ratio
0x5D66	LFM_CTRL_66	0x00	RW	Bit[7:1]: Not used Bit[0]: Constant coefficient enable
0x5D67	LFM_CTRL_67	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Constant coefficient value 0
0x5D68	LFM_CTRL_68	0xA0	RW	Bit[7:0]: Constant coefficient value 0
0x5D69	LFM_CTRL_69	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Constant coefficient value 1
0x5D6A	LFM_CTRL_6A	0xA0	RW	Bit[7:0]: Constant coefficient value 1
0x5D6B	LFM_CTRL_6B	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Constant coefficient value 2
0x5D6C	LFM_CTRL_6C	0xA0	RW	Bit[7:0]: Constant coefficient value 2
0x5D6D	LFM_CTRL_6D	0x01	RW	Bit[7:1]: Not used Bit[0]: Max difference threshold enable
0x5D6E	LFM_CTRL_6E	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Max difference threshold 0
0x5D6F	LFM_CTRL_6F	0xB6	RW	Bit[7:0]: Max difference threshold 0
0x5D70	LFM_CTRL_70	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Max difference threshold 1
0x5D71	LFM_CTRL_71	0xB6	RW	Bit[7:0]: Max difference threshold 1
0x5D72	LFM_CTRL_72	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Max difference threshold 2

table A-2 sensor control registers (sheet 223 of 255)

address	register name	default value	R/W	description
0x5D73	LFM_CTRL_73	0xB6	RW	Bit[7:0]: Max difference threshold 2
0x5D74	LFM_CTRL_74	0x01	RW	Bit[7:1]: Not used Bit[0]: Use Absolute difference Enable
0x5D75	LFM_CTRL_75	0x00	RW	nSPDShiftMode Bit[7:4]: Not used Bit[3]: SPDShiftRight 0: Left 1: Right Bit[2]: SPDShiftDown 0: Up 1: Down Bit[1]: SPDShiftManual Bit[0]: SPDShiftEnable
0x5D80~ 0x5D90	RSVD	–	–	Reserved
0x5DA0	NON_RISC_0	0x00	RW	Bit[7:0]: Manual AWB inverse gain[0]
0x5DA1	NON_RISC_1	0x00	RW	Bit[7:0]: Manual AWB inverse gain[0]
0x5DA2	NON_RISC_2	0x00	RW	Bit[7:0]: Manual AWB inverse gain[1]
0x5DA3	NON_RISC_3	0x00	RW	Bit[7:0]: Manual AWB inverse gain[1]
0x5DA4	NON_RISC_4	0x00	RW	Bit[7:0]: Manual AWB inverse gain[2]
0x5DA5	NON_RISC_5	0x00	RW	Bit[7:0]: Manual AWB inverse gain[2]
0x5DA6	NON_RISC_6	0x00	RW	Bit[7:0]: Manual AWB inverse gain[3]
0x5DA7	NON_RISC_7	0x00	RW	Bit[7:0]: Manual AWB inverse gain[3]
0x5DA8	NON_RISC_8	0x00	RW	Bit[7:4]: Not used Bit[3]: nmax_man_en Manual NMAX value enable Bit[2]: blc_man_en Manual BLC enable Bit[1]: cfa_ptn_man_en Manual CFA pattern enable Bit[0]: awb_invgain_man_en Manual AWB inverse gain enable
0x5DA9	NON_RISC_9	0x00	RW	Bit[7:2]: Not used Bit[1:0]: cfa_ptn_man Manual CFA pattern
0x5DAA	NON_RISC_10	0x00	RW	Bit[7:4]: Not used Bit[3:0]: blc_man Manual BLC
0x5DAB	NON_RISC_11	0x00	RW	Bit[7:0]: blc_man Manual BLC

table A-2 sensor control registers (sheet 224 of 255)

address	register name	default value	R/W	description
0x5DAC	NON_RISC_12	0x00	RW	Bit[7:0]: nmax_man Manual NMAX
0x5DAD	NON_RISC_13	0x00	RW	Bit[7:0]: nmax_man Manual NMAX
0x5DB0	NON_RISC_14	0x00	RW	Bit[7:0]: nmax_man Manual NMAX
0x5DB2	NON_RISC_15	–	R	Bit[7:0]: Version
0x5DB3	NON_RISC_16	–	R	Bit[7:0]: Version
0x5DC0	POST_RAWBIN_0_RAWBIN_0	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight0
0x5DC1	POST_RAWBIN_0_RAWBIN_1	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight1
0x5DC2	POST_RAWBIN_0_RAWBIN_2	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight2
0x5DC3	POST_RAWBIN_0_RAWBIN_3	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight3
0x5DC4	POST_RAWBIN_0_RAWBIN_4	0x00	RW	Bit[7:1]: Not used Bit[0]: blc_contr_en
0x5DE0	POST_RAWBIN_1_RAWBIN_0	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight0
0x5DE1	POST_RAWBIN_1_RAWBIN_1	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight1
0x5DE2	POST_RAWBIN_1_RAWBIN_2	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight2
0x5DE3	POST_RAWBIN_1_RAWBIN_3	0x04	RW	Bit[7:5]: Not used Bit[4:0]: cfa_weight3
0x5DE4	POST_RAWBIN_1_RAWBIN_4	0x00	RW	Bit[7:1]: Not used Bit[0]: blc_contr_en
0x5E00	PWL0_0	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nMode 00: 24->12 bits 01: 24->14 bits 10: 24->16 bits 11: 24->20 bits
0x5E01	PWL0_0_1	0x08	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[0] X knee point difference

table A-2 sensor control registers (sheet 225 of 255)

address	register name	default value	R/W	description
0x5E02	PWL0_1	0x09	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[1]
0x5E03	PWL0_1_3	0x0A	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[2]
0x5E04	PWL0_1_4	0x0B	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[3]
0x5E05	PWL0_1_5	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[4]
0x5E06	PWL0_1_6	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[5]
0x5E07	PWL0_1_7	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[6]
0x5E08	PWL0_1_8	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[7]
0x5E09	PWL0_1_9	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[8]
0x5E0A	PWL0_1_A	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[9]
0x5E0B	PWL0_1_B	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[10]
0x5E0C	PWL0_1_C	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[11]
0x5E0D	PWL0_1_D	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[12]
0x5E0E	PWL0_1_E	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[13]
0x5E0F	PWL0_1_F	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[14]
0x5E10	PWL0_1_10	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[15]
0x5E11	PWL0_1_11	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[16]
0x5E12	PWL0_1_12	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[17]
0x5E13	PWL0_1_13	0x0F	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[18]
0x5E14	PWL0_1_14	0x0F	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[19]

table A-2 sensor control registers (sheet 226 of 255)

address	register name	default value	R/W	description
0x5E15	PWL0_1_15	0x10	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[20]
0x5E16	PWL0_1_16	0x11	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[21]
0x5E17	PWL0_1_17	0x11	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[22]
0x5E18	PWL0_1_18	0x12	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[23]
0x5E19	PWL0_1_19	0x12	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[24]
0x5E1A	PWL0_1_1A	0x13	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[25]
0x5E1B	PWL0_1_1B	0x13	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[26]
0x5E1C	PWL0_1_1C	0x14	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[27]
0x5E1D	PWL0_1_1D	0x14	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[28]
0x5E1E	PWL0_1_1E	0x16	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[29]
0x5E1F	PWL0_1_1F	0x16	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[30]
0x5E20	PWL0_1_20	0x16	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[31]
0x5E21	PWL0_1_21	0x08	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[32]
0x5E22	PWL0_1_22	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[0] Y knee point difference
0x5E23	PWL0_1_23	0x01	RW	Bit[7:0]: m_ndY_val[0]
0x5E24	PWL0_1_24	0x00	RW	Bit[7:0]: m_ndY_val[0]
0x5E25	PWL0_1_25	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[1]
0x5E26	PWL0_1_26	0x02	RW	Bit[7:0]: m_ndY_val[1]
0x5E27	PWL0_1_27	0x00	RW	Bit[7:0]: m_ndY_val[1]
0x5E28	PWL0_1_28	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[2]

table A-2 sensor control registers (sheet 227 of 255)

address	register name	default value	R/W	description
0x5E29	PWL0_1_29	0x02	RW	Bit[7:0]: m_ndY_val[2]
0x5E2A	PWL0_1_2A	0x00	RW	Bit[7:0]: m_ndY_val[2]
0x5E2B	PWL0_1_2B	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[3]
0x5E2C	PWL0_1_2C	0x02	RW	Bit[7:0]: m_ndY_val[3]
0x5E2D	PWL0_1_2D	0x00	RW	Bit[7:0]: m_ndY_val[3]
0x5E2E	PWL0_1_2E	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[4]
0x5E2F	PWL0_1_2F	0x02	RW	Bit[7:0]: m_ndY_val[4]
0x5E30	PWL0_1_30	0x00	RW	Bit[7:0]: m_ndY_val[4]
0x5E31	PWL0_1_31	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[5]
0x5E32	PWL0_1_32	0x02	RW	Bit[7:0]: m_ndY_val[5]
0x5E33	PWL0_1_33	0x00	RW	Bit[7:0]: m_ndY_val[5]
0x5E34	PWL0_1_34	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[6]
0x5E35	PWL0_1_35	0x02	RW	Bit[7:0]: m_ndY_val[6]
0x5E36	PWL0_1_36	0x00	RW	Bit[7:0]: m_ndY_val[6]
0x5E37	PWL0_1_37	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[7]
0x5E38	PWL0_1_38	0x02	RW	Bit[7:0]: m_ndY_val[7]
0x5E39	PWL0_1_39	0x00	RW	Bit[7:0]: m_ndY_val[7]
0x5E3A	PWL0_1_3A	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[8]
0x5E3B	PWL0_1_3B	0x02	RW	Bit[7:0]: m_ndY_val[8]
0x5E3C	PWL0_1_3C	0x00	RW	Bit[7:0]: m_ndY_val[8]
0x5E3D	PWL0_1_3D	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[9]
0x5E3E	PWL0_1_3E	0x02	RW	Bit[7:0]: m_ndY_val[9]
0x5E3F	PWL0_1_3F	0x00	RW	Bit[7:0]: m_ndY_val[9]
0x5E40	PWL0_1_40	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[10]
0x5E41	PWL0_1_41	0x02	RW	Bit[7:0]: m_ndY_val[10]]

table A-2 sensor control registers (sheet 228 of 255)

address	register name	default value	R/W	description
0x5E42	PWL0_1_42	0x00	RW	Bit[7:0]: m_ndY_val[10]
0x5E43	PWL0_1_43	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[11]
0x5E44	PWL0_1_44	0x02	RW	Bit[7:0]: m_ndY_val[11]
0x5E45	PWL0_1_45	0x00	RW	Bit[7:0]: m_ndY_val[11]
0x5E46	PWL0_1_46	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[12]
0x5E47	PWL0_1_47	0x04	RW	Bit[7:0]: m_ndY_val[12]
0x5E48	PWL0_1_48	0x00	RW	Bit[7:0]: m_ndY_val[12]
0x5E49	PWL0_1_49	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[13]
0x5E4A	PWL0_1_4A	0x04	RW	Bit[7:0]: m_ndY_val[13]
0x5E4B	PWL0_1_4B	0x00	RW	Bit[7:0]: m_ndY_val[13]
0x5E4C	PWL0_1_4C	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[14]
0x5E4D	PWL0_1_4D	0x04	RW	Bit[7:0]: m_ndY_val[14]
0x5E4E	PWL0_1_4E	0x00	RW	Bit[7:0]: m_ndY_val[14]
0x5E4F	PWL0_1_4F	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[15]
0x5E50	PWL0_1_50	0x04	RW	Bit[7:0]: m_ndY_val[15]
0x5E51	PWL0_1_51	0x00	RW	Bit[7:0]: m_ndY_val[15]
0x5E52	PWL0_1_52	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[16]
0x5E53	PWL0_1_53	0x04	RW	Bit[7:0]: m_ndY_val[16]
0x5E54	PWL0_1_54	0x00	RW	Bit[7:0]: m_ndY_val[16]
0x5E55	PWL0_1_55	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[17]
0x5E56	PWL0_1_56	0x04	RW	Bit[7:0]: m_ndY_val[17]
0x5E57	PWL0_1_57	0x00	RW	Bit[7:0]: m_ndY_val[17]
0x5E58	PWL0_1_58	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[18]
0x5E59	PWL0_1_59	0x04	RW	Bit[7:0]: m_ndY_val[18]
0x5E5A	PWL0_1_5A	0x00	RW	Bit[7:0]: m_ndY_val[18]

table A-2 sensor control registers (sheet 229 of 255)

address	register name	default value	R/W	description
0x5E5B	PWL0_1_5B	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[19]
0x5E5C	PWL0_1_5C	0x04	RW	Bit[7:0]: m_ndY_val[19]
0x5E5D	PWL0_1_5D	0x00	RW	Bit[7:0]: m_ndY_val[19]
0x5E5E	PWL0_1_5E	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[20]
0x5E5F	PWL0_1_5F	0x08	RW	Bit[7:0]: m_ndY_val[20]
0x5E60	PWL0_1_60	0x00	RW	Bit[7:0]: m_ndY_val[20]
0x5E61	PWL0_1_61	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[21]
0x5E62	PWL0_1_62	0x08	RW	Bit[7:0]: m_ndY_val[21]
0x5E63	PWL0_1_63	0x00	RW	Bit[7:0]: m_ndY_val[21]
0x5E64	PWL0_1_64	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[22]
0x5E65	PWL0_1_65	0x08	RW	Bit[7:0]: m_ndY_val[22]
0x5E66	PWL0_1_66	0x00	RW	Bit[7:0]: m_ndY_val[22]
0x5E67	PWL0_1_67	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[23]
0x5E68	PWL0_1_68	0x08	RW	Bit[7:0]: m_ndY_val[23]
0x5E69	PWL0_1_69	0x00	RW	Bit[7:0]: m_ndY_val[23]
0x5E6A	PWL0_1_6A	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[24]
0x5E6B	PWL0_1_6B	0x08	RW	Bit[7:0]: m_ndY_val[24]
0x5E6C	PWL0_1_6C	0x00	RW	Bit[7:0]: m_ndY_val[24]
0x5E6D	PWL0_1_6D	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[25]
0x5E6E	PWL0_1_6E	0x10	RW	Bit[7:0]: m_ndY_val[25]
0x5E6F	PWL0_1_6F	0x00	RW	Bit[7:0]: m_ndY_val[25]
0x5E70	PWL0_1_70	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[26]
0x5E71	PWL0_1_71	0x10	RW	Bit[7:0]: m_ndY_val[26]
0x5E72	PWL0_1_72	0x00	RW	Bit[7:0]: m_ndY_val[26]

table A-2 sensor control registers (sheet 230 of 255)

address	register name	default value	R/W	description
0x5E73	PWL0_1_73	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[27]
0x5E74	PWL0_1_74	0x10	RW	Bit[7:0]: m_ndY_val[27]
0x5E75	PWL0_1_75	0x00	RW	Bit[7:0]: m_ndY_val[27]
0x5E76	PWL0_1_76	0x00	RW	Bit[3:0]: m_ndY_val[28]
0x5E77	PWL0_1_77	0x10	RW	Bit[7:0]: m_ndY_val[28]
0x5E78	PWL0_1_78	0x00	RW	Bit[7:0]: m_ndY_val[28]
0x5E79	PWL0_1_79	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[29]
0x5E7A	PWL0_1_7A	0x20	RW	Bit[7:0]: m_ndY_val[29]
0x5E7B	PWL0_1_7B	0x00	RW	Bit[7:0]: m_ndY_val[29]
0x5E7C	PWL0_1_7C	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[30]
0x5E7D	PWL0_1_7D	0x20	RW	Bit[7:0]: m_ndY_val[30]
0x5E7E	PWL0_1_7E	0x00	RW	Bit[7:0]: m_ndY_val[30]
0x5E7F	PWL0_1_7F	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[31]
0x5E80	PWL0_1_80	0x20	RW	Bit[7:0]: m_ndY_val[31]
0x5E81	PWL0_1_81	0x00	RW	Bit[7:0]: m_ndY_val[31]
0x5E82	PWL0_1_82	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[32]
0x5E83	PWL0_1_83	0x00	RW	Bit[7:0]: m_ndY_val[32]
0x5E84	PWL0_1_84	0xFF	RW	Bit[7:0]: m_ndY_val[32]
0x5E85	PWL0_1_85	0x00	RW	Bit[7:3]: Not used Bit[2:0]: mode_man Manual mode 000: Default setting 001: Select PWL0 setting 010: Select PWL1 setting Others:Not used
0x5F00	PWL1_0	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nMode 00: 24->12 bits 01: 24->14 bits 10: 24->16 bits 11: 24->20 bits

table A-2 sensor control registers (sheet 231 of 255)

address	register name	default value	R/W	description
0x5F01	PWL1_0_1	0x08	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[0] X knee point difference
0x5F02	PWL1_1	0x09	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[1]
0x5F03	PWL1_1_3	0x0A	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[2]
0x5F04	PWL1_1_4	0x0B	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[3]
0x5F05	PWL1_1_5	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[4]
0x5F06	PWL1_1_6	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[5]
0x5F07	PWL1_1_7	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[6]
0x5F08	PWL1_1_8	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[7]
0x5F09	PWL1_1_9	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[8]
0x5F0A	PWL1_1_A	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[9]
0x5F0B	PWL1_1_B	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[10]
0x5F0C	PWL1_1_C	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[11]
0x5F0D	PWL1_1_D	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[12]
0x5F0E	PWL1_1_E	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[13]
0x5F0F	PWL1_1_F	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[14]
0x5F10	PWL1_1_10	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[15]
0x5F11	PWL1_1_11	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[16]
0x5F12	PWL1_1_12	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[17]

table A-2 sensor control registers (sheet 232 of 255)

address	register name	default value	R/W	description
0x5F13	PWL1_1_13	0x0F	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[18]
0x5F14	PWL1_1_14	0x0F	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[19]
0x5F15	PWL1_1_15	0x10	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[20]
0x5F16	PWL1_1_16	0x11	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[21]
0x5F17	PWL1_1_17	0x11	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[22]
0x5F18	PWL1_1_18	0x12	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[23]
0x5F19	PWL1_1_19	0x12	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[24]
0x5F1A	PWL1_1_1A	0x13	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[25]
0x5F1B	PWL1_1_1B	0x13	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[26]
0x5F1C	PWL1_1_1C	0x14	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[27]
0x5F1D	PWL1_1_1D	0x14	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[28]
0x5F1E	PWL1_1_1E	0x16	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[29]
0x5F1F	PWL1_1_1F	0x16	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[30]
0x5F20	PWL1_1_20	0x16	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[31]
0x5F21	PWL1_1_21	0x08	RW	Bit[7:5]: Not used Bit[4:0]: m_ndX_exp[32]
0x5F22	PWL1_1_22	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[0] Y knee point difference
0x5F23	PWL1_1_23	0x01	RW	Bit[7:0]: m_ndY_val[0]
0x5F24	PWL1_1_24	0x00	RW	Bit[7:0]: m_ndY_val[0]
0x5F25	PWL1_1_25	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[1]

table A-2 sensor control registers (sheet 233 of 255)

address	register name	default value	R/W	description
0x5F26	PWL1_1_26	0x02	RW	Bit[7:0]: m_ndY_val[1]
0x5F27	PWL1_1_27	0x00	RW	Bit[7:0]: m_ndY_val[1]
0x5F28	PWL1_1_28	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[2]
0x5F29	PWL1_1_29	0x02	RW	Bit[7:0]: m_ndY_val[2]
0x5F2A	PWL1_1_2A	0x00	RW	Bit[7:0]: m_ndY_val[2]
0x5F2B	PWL1_1_2B	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[3]
0x5F2C	PWL1_1_2C	0x02	RW	Bit[7:0]: m_ndY_val[3]
0x5F2D	PWL1_1_2D	0x00	RW	Bit[7:0]: m_ndY_val[3]
0x5F2E	PWL1_1_2E	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[4]
0x5F2F	PWL1_1_2F	0x02	RW	Bit[7:0]: m_ndY_val[4]
0x5F30	PWL1_1_30	0x00	RW	Bit[7:0]: m_ndY_val[4]
0x5F31	PWL1_1_31	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[5]
0x5F32	PWL1_1_32	0x02	RW	Bit[7:0]: m_ndY_val[5]
0x5F33	PWL1_1_33	0x00	RW	Bit[7:0]: m_ndY_val[5]
0x5F34	PWL1_1_34	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[6]
0x5F35	PWL1_1_35	0x02	RW	Bit[7:0]: m_ndY_val[6]
0x5F36	PWL1_1_36	0x00	RW	Bit[7:0]: m_ndY_val[6]
0x5F37	PWL1_1_37	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[7]
0x5F38	PWL1_1_38	0x02	RW	Bit[7:0]: m_ndY_val[7]
0x5F39	PWL1_1_39	0x00	RW	Bit[7:0]: m_ndY_val[7]
0x5F3A	PWL1_1_3A	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[8]
0x5F3B	PWL1_1_3B	0x02	RW	Bit[7:0]: m_ndY_val[8]
0x5F3C	PWL1_1_3C	0x00	RW	Bit[7:0]: m_ndY_val[8]
0x5F3D	PWL1_1_3D	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[9]
0x5F3E	PWL1_1_3E	0x02	RW	Bit[7:0]: m_ndY_val[9]

table A-2 sensor control registers (sheet 234 of 255)

address	register name	default value	R/W	description
0x5F3F	PWL1_1_3F	0x00	RW	Bit[7:0]: m_ndY_val[9]
0x5F40	PWL1_1_40	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[10]
0x5F41	PWL1_1_41	0x02	RW	Bit[7:0]: m_ndY_val[10]]
0x5F42	PWL1_1_42	0x00	RW	Bit[7:0]: m_ndY_val[10]
0x5F43	PWL1_1_43	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[11]
0x5F44	PWL1_1_44	0x02	RW	Bit[7:0]: m_ndY_val[11]
0x5F45	PWL1_1_45	0x00	RW	Bit[7:0]: m_ndY_val[11]
0x5F46	PWL1_1_46	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[12]
0x5F47	PWL1_1_47	0x04	RW	Bit[7:0]: m_ndY_val[12]
0x5F48	PWL1_1_48	0x00	RW	Bit[7:0]: m_ndY_val[12]
0x5F49	PWL1_1_49	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[13]
0x5F4A	PWL1_1_4A	0x04	RW	Bit[7:0]: m_ndY_val[13]
0x5F4B	PWL1_1_4B	0x00	RW	Bit[7:0]: m_ndY_val[13]
0x5F4C	PWL1_1_4C	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[14]
0x5F4D	PWL1_1_4D	0x04	RW	Bit[7:0]: m_ndY_val[14]
0x5F4E	PWL1_1_4E	0x00	RW	Bit[7:0]: m_ndY_val[14]
0x5F4F	PWL1_1_4F	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[15]
0x5F50	PWL1_1_50	0x04	RW	Bit[7:0]: m_ndY_val[15]
0x5F51	PWL1_1_51	0x00	RW	Bit[7:0]: m_ndY_val[15]
0x5F52	PWL1_1_52	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[16]
0x5F53	PWL1_1_53	0x04	RW	Bit[7:0]: m_ndY_val[16]
0x5F54	PWL1_1_54	0x00	RW	Bit[7:0]: m_ndY_val[16]
0x5F55	PWL1_1_55	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[17]
0x5F56	PWL1_1_56	0x04	RW	Bit[7:0]: m_ndY_val[17]
0x5F57	PWL1_1_57	0x00	RW	Bit[7:0]: m_ndY_val[17]

table A-2 sensor control registers (sheet 235 of 255)

address	register name	default value	R/W	description
0x5F58	PWL1_1_58	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[18]
0x5F59	PWL1_1_59	0x04	RW	Bit[7:0]: m_ndY_val[18]
0x5F5A	PWL1_1_5A	0x00	RW	Bit[7:0]: m_ndY_val[18]
0x5F5B	PWL1_1_5B	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[19]
0x5F5C	PWL1_1_5C	0x04	RW	Bit[7:0]: m_ndY_val[19]
0x5F5D	PWL1_1_5D	0x00	RW	Bit[7:0]: m_ndY_val[19]
0x5F5E	PWL1_1_5E	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[20]
0x5F5F	PWL1_1_5F	0x08	RW	Bit[7:0]: m_ndY_val[20]
0x5F60	PWL1_1_60	0x00	RW	Bit[7:0]: m_ndY_val[20]
0x5F61	PWL1_1_61	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[21]
0x5F62	PWL1_1_62	0x08	RW	Bit[7:0]: m_ndY_val[21]
0x5F63	PWL1_1_63	0x00	RW	Bit[7:0]: m_ndY_val[21]
0x5F64	PWL1_1_64	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[22]
0x5F65	PWL1_1_65	0x08	RW	Bit[7:0]: m_ndY_val[22]
0x5F66	PWL1_1_66	0x00	RW	Bit[7:0]: m_ndY_val[22]
0x5F67	PWL1_1_67	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[23]
0x5F68	PWL1_1_68	0x08	RW	Bit[7:0]: m_ndY_val[23]
0x5F69	PWL1_1_69	0x00	RW	Bit[7:0]: m_ndY_val[23]
0x5F6A	PWL1_1_6A	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[24]
0x5F6B	PWL1_1_6B	0x08	RW	Bit[7:0]: m_ndY_val[24]
0x5F6C	PWL1_1_6C	0x00	RW	Bit[7:0]: m_ndY_val[24]
0x5F6D	PWL1_1_6D	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[25]
0x5F6E	PWL1_1_6E	0x10	RW	Bit[7:0]: m_ndY_val[25]
0x5F6F	PWL1_1_6F	0x00	RW	Bit[7:0]: m_ndY_val[25]

table A-2 sensor control registers (sheet 236 of 255)

address	register name	default value	R/W	description
0x5F70	PWL1_1_70	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[26]
0x5F71	PWL1_1_71	0x10	RW	Bit[7:0]: m_ndY_val[26]
0x5F72	PWL1_1_72	0x00	RW	Bit[7:0]: m_ndY_val[26]
0x5F73	PWL1_1_73	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[27]
0x5F74	PWL1_1_74	0x10	RW	Bit[7:0]: m_ndY_val[27]
0x5F75	PWL1_1_75	0x00	RW	Bit[7:0]: m_ndY_val[27]
0x5F76	PWL1_1_76	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[28]
0x5F77	PWL1_1_77	0x10	RW	Bit[7:0]: m_ndY_val[28]
0x5F78	PWL1_1_78	0x00	RW	Bit[7:0]: m_ndY_val[28]
0x5F79	PWL1_1_79	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[29]
0x5F7A	PWL1_1_7A	0x20	RW	Bit[7:0]: m_ndY_val[29]
0x5F7B	PWL1_1_7B	0x00	RW	Bit[7:0]: m_ndY_val[29]
0x5F7C	PWL1_1_7C	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[30]
0x5F7D	PWL1_1_7D	0x20	RW	Bit[7:0]: m_ndY_val[30]
0x5F7E	PWL1_1_7E	0x00	RW	Bit[7:0]: m_ndY_val[30]
0x5F7F	PWL1_1_7F	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[31]
0x5F80	PWL1_1_80	0x20	RW	Bit[7:0]: m_ndY_val[31]
0x5F81	PWL1_1_81	0x00	RW	Bit[7:0]: m_ndY_val[31]
0x5F82	PWL1_1_82	0x00	RW	Bit[7:4]: Not used Bit[3:0]: m_ndY_val[32]
0x5F83	PWL1_1_83	0x00	RW	Bit[7:0]: m_ndY_val[32]
0x5F84	PWL1_1_84	0xFF	RW	Bit[7:0]: m_ndY_val[32]
0x5F85	PWL1_1_85	0x00	RW	Bit[7:3]: Not used Bit[2:0]: mode_man Manual mode 000: Default setting 001: Select PWL0 setting 010: Select PWL1 setting Others:Not used

table A-2 sensor control registers (sheet 237 of 255)

address	register name	default value	R/W	description
0x6000	STATIC_1015_D2V2_0_ STAT_CTRL_00	0x0F	RW	Bit[7:4]: Not used Bit[3:0]: Histogram Bayer mask
0x6001	STATIC_1015_D2V2_0_ STAT_CTRL_01	0x07	RW	Bit[7:5]: Not used Bit[4:0]: Histogram bin control point0, 4~10
0x6002	STATIC_1015_D2V2_0_ STAT_CTRL_02	0x08	RW	Bit[7:5]: Not used Bit[4:0]: Histogram bin control point1, 4~10
0x6003	STATIC_1015_D2V2_0_ STAT_CTRL_03	0x07	RW	Bit[7:3]: Not used Bit[2]: static_row Bit[1]: avg_en Enable average static Bit[0]: hist_en Enable histogram static
0x6004	STATIC_1015_D2V2_0_ STAT_CTRL_04	0x00	RW	Bit[7:1]: Not used Bit[0]: skip_col
0x6005	STATIC_1015_D2V2_0_ STAT_CTRL_05	0x00	RW	Bit[7:1]: Not used Bit[0]: skip_row
0x6006	STATIC_1015_D2V2_0_ STAT_CTRL_06	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI row start
0x6007	STATIC_1015_D2V2_0_ STAT_CTRL_07	0x3C	RW	Bit[7:0]: ROI row start
0x6008	STATIC_1015_D2V2_0_ STAT_CTRL_08	0x03	RW	Bit[7:4]: Not used Bit[3:0]: ROI row end
0x6009	STATIC_1015_D2V2_0_ STAT_CTRL_09	0x20	RW	Bit[7:0]: ROI row end
0x600A	STATIC_1015_D2V2_0_ STAT_CTRL_0A	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI col start
0x600B	STATIC_1015_D2V2_0_ STAT_CTRL_0B	0x3C	RW	Bit[7:0]: ROI col start
0x600C	STATIC_1015_D2V2_0_ STAT_CTRL_0C	0x03	RW	Bit[7:4]: Not used Bit[3:0]: ROI col end1
0x600D	STATIC_1015_D2V2_0_ STAT_CTRL_0D	0x20	RW	Bit[7:0]: ROI col end1
0x600E	STATIC_1015_D2V2_0_ STAT_CTRL_0E	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_row_start
0x600F	STATIC_1015_D2V2_0_ STAT_CTRL_0F	0x04	RW	Bit[7:4]: Not used Bit[3:0]: test_row_end
0x6010	STATIC_1015_D2V2_0_ STAT_CTRL_10	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_col_start

table A-2 sensor control registers (sheet 238 of 255)

address	register name	default value	R/W	description
0x6011	STATIC_1015_D2V2_0_ STAT_CTRL_11	0x00	RW	Bit[7:0]: test_col_start
0x6012	STATIC_1015_D2V2_0_ STAT_CTRL_12	0x02	RW	Bit[7:4]: Not used Bit[3:0]: test_col_end
0x6013	STATIC_1015_D2V2_0_ STAT_CTRL_13	0x80	RW	Bit[7:0]: test_col_end
0x6014	STATIC_1015_D2V2_0_ STAT_CTRL_14	0x07	RW	Bit[7:5]: Not used Bit[4:0]: test_pt_0
0x6015	STATIC_1015_D2V2_0_ STAT_CTRL_15	0x08	RW	Bit[7:5]: Not used Bit[4:0]: test_pt_1
0x6016	STATIC_1015_D2V2_0_ STAT_CTRL_16	0x00	RW	Bit[7:3]: Not used Bit[2:0]: norm_src_sel
0x6017	STATIC_1015_D2V2_0_ STAT_CTRL_17	0x00	RW	Bit[7:2]: Not used Bit[1]: test_skip_col Bit[0]: test_skip_row
0x601D	STATIC_1015_D2V2_0_ STAT_CTRL_1D	–	R	Bit[7:0]: static_ver
0x601E	STATIC_1015_D2V2_0_ STAT_CTRL_1E	–	R	Bit[7:0]: static_ver
0x6020	STATIC_1015_D2V2_1_ STAT_CTRL_00	0x0F	RW	Bit[7:4]: Not used Bit[3:0]: Histogram bayer mask
0x6021	STATIC_1015_D2V2_1_ STAT_CTRL_01	0x07	RW	Bit[7:5]: Not used Bit[4:0]: Histogram bin control point0, 4~10
0x6022	STATIC_1015_D2V2_1_ STAT_CTRL_02	0x08	RW	Bit[7:5]: Not used Bit[4:0]: Histogram bin control point1, 4~10
0x6023	STATIC_1015_D2V2_1_ STAT_CTRL_03	0x07	RW	Bit[7:3]: Not used Bit[2]: static_row Bit[1]: avg_en Enable average static Bit[0]: hist_en Enable histogram static
0x6024	STATIC_1015_D2V2_1_ STAT_CTRL_04	0x00	RW	Bit[7:1]: Not used Bit[0]: skip_col
0x6025	STATIC_1015_D2V2_1_ STAT_CTRL_05	0x00	RW	Bit[7:1]: Not used Bit[0]: skip_row
0x6026	STATIC_1015_D2V2_1_ STAT_CTRL_06	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI row start
0x6027	STATIC_1015_D2V2_1_ STAT_CTRL_07	0x3C	RW	Bit[7:0]: ROI row start

table A-2 sensor control registers (sheet 239 of 255)

address	register name	default value	R/W	description
0x6028	STATIC_1015_D2V2_1_ STAT_CTRL_08	0x03	RW	Bit[7:4]: Not used Bit[3:0]: ROI row end
0x6029	STATIC_1015_D2V2_1_ STAT_CTRL_09	0x20	RW	Bit[7:0]: ROI row end
0x602A	STATIC_1015_D2V2_1_ STAT_CTRL_0A	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI col start
0x602B	STATIC_1015_D2V2_1_ STAT_CTRL_0B	0x3C	RW	Bit[7:0]: ROI col start
0x602C	STATIC_1015_D2V2_1_ STAT_CTRL_0C	0x03	RW	Bit[7:4]: Not used Bit[3:0]: ROI col end1
0x602D	STATIC_1015_D2V2_1_ STAT_CTRL_0D	0x20	RW	Bit[7:0]: ROI col end1
0x602E	STATIC_1015_D2V2_1_ STAT_CTRL_0E	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_row_start
0x602F	STATIC_1015_D2V2_1_ STAT_CTRL_0F	0x04	RW	Bit[7:4]: Not used Bit[3:0]: test_row_end
0x6030	STATIC_1015_D2V2_1_ STAT_CTRL_10	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_col_start
0x6031	STATIC_1015_D2V2_1_ STAT_CTRL_11	0x00	RW	Bit[7:0]: test_col_start
0x6032	STATIC_1015_D2V2_1_ STAT_CTRL_12	0x02	RW	Bit[7:4]: Not used Bit[3:0]: test_col_end
0x6033	STATIC_1015_D2V2_1_ STAT_CTRL_13	0x80	RW	Bit[7:0]: test_col_end
0x6034	STATIC_1015_D2V2_1_ STAT_CTRL_14	0x07	RW	Bit[7:5]: Not used Bit[4:0]: test_pt_0
0x6035	STATIC_1015_D2V2_1_ STAT_CTRL_15	0x08	RW	Bit[7:5]: Not used Bit[4:0]: test_pt_1
0x6036	STATIC_1015_D2V2_1_ STAT_CTRL_16	0x01	RW	Bit[7:3]: Not used Bit[2:0]: norm_src_sel
0x6037	STATIC_1015_D2V2_1_ STAT_CTRL_17	0x00	RW	Bit[7:2]: Not used Bit[1]: test_skip_col Bit[0]: test_skip_row
0x603D	STATIC_1015_D2V2_1_ STAT_CTRL_1D	–	R	Bit[7:0]: static_ver
0x603E	STATIC_1015_D2V2_1_ STAT_CTRL_1E	–	R	Bit[7:0]: static_ver

table A-2 sensor control registers (sheet 240 of 255)

address	register name	default value	R/W	description
0x6040	STATIC_1015_D2V2_2_ STAT_CTRL_00	0x0F	RW	Bit[7:4]: Not used Bit[3:0]: Histogram bayer mask
0x6041	STATIC_1015_D2V2_2_ STAT_CTRL_01	0x07	RW	Bit[7:5]: Not used Bit[4:0]: Histogram bin control point0, 4~10
0x6042	STATIC_1015_D2V2_2_ STAT_CTRL_02	0x08	RW	Bit[7:5]: Not used Bit[4:0]: Histogram bin control point1, 4~10
0x6043	STATIC_1015_D2V2_2_ STAT_CTRL_03	0x07	RW	Bit[7:3]: Not used Bit[2]: static_row Bit[1]: avg_en Enable average static Bit[0]: hist_en Enable histogram static
0x6044	STATIC_1015_D2V2_2_ STAT_CTRL_04	0x00	RW	Bit[7:1]: Not used Bit[0]: skip_col
0x6045	STATIC_1015_D2V2_2_ STAT_CTRL_05	0x00	RW	Bit[7:1]: Not used Bit[0]: skip_row
0x6046	STATIC_1015_D2V2_2_ STAT_CTRL_06	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI row start
0x6047	STATIC_1015_D2V2_2_ STAT_CTRL_07	0x3C	RW	Bit[7:0]: ROI row start
0x6048	STATIC_1015_D2V2_2_ STAT_CTRL_08	0x03	RW	Bit[7:4]: Not used Bit[3:0]: ROI row end
0x6049	STATIC_1015_D2V2_2_ STAT_CTRL_09	0x20	RW	Bit[7:0]: ROI row end
0x604A	STATIC_1015_D2V2_2_ STAT_CTRL_0A	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI col start
0x604B	STATIC_1015_D2V2_2_ STAT_CTRL_0B	0x3C	RW	Bit[7:0]: ROI col start
0x604C	STATIC_1015_D2V2_2_ STAT_CTRL_0C	0x03	RW	Bit[7:4]: Not used Bit[3:0]: ROI col end1
0x604D	STATIC_1015_D2V2_2_ STAT_CTRL_0D	0x20	RW	Bit[7:0]: ROI col end1
0x604E	STATIC_1015_D2V2_2_ STAT_CTRL_0E	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_row_start
0x604F	STATIC_1015_D2V2_2_ STAT_CTRL_0F	0x04	RW	Bit[7:4]: Not used Bit[3:0]: test_row_end
0x6050	STATIC_1015_D2V2_2_ STAT_CTRL_10	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_col_start

table A-2 sensor control registers (sheet 241 of 255)

address	register name	default value	R/W	description
0x6051	STATIC_1015_D2V2_2_ STAT_CTRL_11	0x00	RW	Bit[7:0]: test_col_start
0x6052	STATIC_1015_D2V2_2_ STAT_CTRL_12	0x02	RW	Bit[7:4]: Not used Bit[3:0]: test_col_end
0x6053	STATIC_1015_D2V2_2_ STAT_CTRL_13	0x80	RW	Bit[7:0]: test_col_end
0x6054	STATIC_1015_D2V2_2_ STAT_CTRL_14	0x07	RW	Bit[7:5]: Not used Bit[4:0]: test_pt_0
0x6055	STATIC_1015_D2V2_2_ STAT_CTRL_15	0x08	RW	Bit[7:5]: Not used Bit[4:0]: test_pt_1
0x6056	STATIC_1015_D2V2_2_ STAT_CTRL_16	0x02	RW	Bit[7:3]: Not used Bit[2:0]: norm_src_sel
0x6057	STATIC_1015_D2V2_2_ STAT_CTRL_17	0x00	RW	Bit[7:2]: Not used Bit[1]: test_skip_col Bit[0]: test_skip_row
0x605D	STATIC_1015_D2V2_2_ STAT_CTRL_1D	–	R	Bit[7:0]: static_ver
0x605E	STATIC_1015_D2V2_2_ STAT_CTRL_1E	–	R	Bit[7:0]: static_ver
0x6060	STATIC_1015_D2V2_3_ STAT_CTRL_00	0x0F	RW	Bit[7:4]: Not used Bit[3:0]: Histogram Bayer mask
0x6061	STATIC_1015_D2V2_3_ STAT_CTRL_01	0x07	RW	Bit[7:5]: Not used Bit[4:0]: Histogram bin control point0, 4~10
0x6062	STATIC_1015_D2V2_3_ STAT_CTRL_02	0x08	RW	Bit[7:5]: Not used Bit[4:0]: Histogram bin control point1, 4~10
0x6063	STATIC_1015_D2V2_3_ STAT_CTRL_03	0x07	RW	Bit[7:3]: Not used Bit[2]: static_row Bit[1]: avg_en Enable average static Bit[0]: hist_en Enable histogram static
0x6064	STATIC_1015_D2V2_3_ STAT_CTRL_04	0x00	RW	Bit[7:1]: Not used Bit[0]: skip_col
0x6065	STATIC_1015_D2V2_3_ STAT_CTRL_05	0x00	RW	Bit[7:1]: Not used Bit[0]: skip_row
0x6066	STATIC_1015_D2V2_3_ STAT_CTRL_06	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI row start
0x6067	STATIC_1015_D2V2_3_ STAT_CTRL_07	0x3C	RW	Bit[7:0]: ROI row start

table A-2 sensor control registers (sheet 242 of 255)

address	register name	default value	R/W	description
0x6068	STATIC_1015_D2V2_3_ STAT_CTRL_08	0x03	RW	Bit[7:4]: Not used Bit[3:0]: ROI row end
0x6069	STATIC_1015_D2V2_3_ STAT_CTRL_09	0x20	RW	Bit[7:0]: ROI row end
0x606A	STATIC_1015_D2V2_3_ STAT_CTRL_0A	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI col start
0x606B	STATIC_1015_D2V2_3_ STAT_CTRL_0B	0x3C	RW	Bit[7:0]: ROI col start
0x606C	STATIC_1015_D2V2_3_ STAT_CTRL_0C	0x03	RW	Bit[7:4]: Not used Bit[3:0]: ROI col end1
0x606D	STATIC_1015_D2V2_3_ STAT_CTRL_0D	0x20	RW	Bit[7:0]: ROI col end1
0x606E	STATIC_1015_D2V2_3_ STAT_CTRL_0E	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_row_start
0x606F	STATIC_1015_D2V2_3_ STAT_CTRL_0F	0x04	RW	Bit[7:4]: Not used Bit[3:0]: test_row_end
0x6070	STATIC_1015_D2V2_3_ STAT_CTRL_10	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_col_start
0x6071	STATIC_1015_D2V2_3_ STAT_CTRL_11	0x00	RW	Bit[7:0]: test_col_start
0x6072	STATIC_1015_D2V2_3_ STAT_CTRL_12	0x02	RW	Bit[7:4]: Not used Bit[3:0]: test_col_end
0x6073	STATIC_1015_D2V2_3_ STAT_CTRL_13	0x80	RW	Bit[7:0]: test_col_end
0x6074	STATIC_1015_D2V2_3_ STAT_CTRL_14	0x07	RW	Bit[7:5]: Not used Bit[4:0]: test_pt_0
0x6075	STATIC_1015_D2V2_3_ STAT_CTRL_15	0x08	RW	Bit[7:5]: Not used Bit[4:0]: test_pt_1
0x6076	STATIC_1015_D2V2_3_ STAT_CTRL_16	0x03	RW	Bit[7:3]: Not used Bit[2:0]: norm_src_sel
0x6077	STATIC_1015_D2V2_3_ STAT_CTRL_17	0x00	RW	Bit[7:2]: Not used Bit[1]: test_skip_col Bit[0]: test_skip_row
0x607D	STATIC_1015_D2V2_3_ STAT_CTRL_1D	–	R	Bit[7:0]: static_ver
0x607E	STATIC_1015_D2V2_3_ STAT_CTRL_1E	–	R	Bit[7:0]: static_ver

table A-2 sensor control registers (sheet 243 of 255)

address	register name	default value	R/W	description
0x6080	STATIC_1015_D2V2_4_ STAT_CTRL_00	0x0F	RW	Bit[7:4]: Not used Bit[3:0]: Histogram bayer mask
0x6081	STATIC_1015_D2V2_4_ STAT_CTRL_01	0x07	RW	Bit[7:5]: Not used Bit[4:0]: Histogram bin control point0, 4~10
0x6082	STATIC_1015_D2V2_4_ STAT_CTRL_02	0x08	RW	Bit[7:5]: Not used Bit[4:0]: Histogram bin control point1, 4~10
0x6083	STATIC_1015_D2V2_4_ STAT_CTRL_03	0x07	RW	Bit[7:3]: Not used Bit[2]: static_row Bit[1]: avg_en Enable average static Bit[0]: hist_en Enable histogram static
0x6084	STATIC_1015_D2V2_4_ STAT_CTRL_04	0x00	RW	Bit[7:1]: Not used Bit[0]: skip_col
0x6085	STATIC_1015_D2V2_4_ STAT_CTRL_05	0x00	RW	Bit[7:1]: Not used Bit[0]: skip_row
0x6086	STATIC_1015_D2V2_4_ STAT_CTRL_06	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI row start
0x6087	STATIC_1015_D2V2_4_ STAT_CTRL_07	0x3C	RW	Bit[7:0]: ROI row start
0x6088	STATIC_1015_D2V2_4_ STAT_CTRL_08	0x03	RW	Bit[7:4]: Not used Bit[3:0]: ROI row end
0x6089	STATIC_1015_D2V2_4_ STAT_CTRL_09	0x20	RW	Bit[7:0]: ROI row end
0x608A	STATIC_1015_D2V2_4_ STAT_CTRL_0A	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ROI col start
0x608B	STATIC_1015_D2V2_4_ STAT_CTRL_0B	0x3C	RW	Bit[7:0]: ROI col start
0x608C	STATIC_1015_D2V2_4_ STAT_CTRL_0C	0x03	RW	Bit[7:4]: Not used Bit[3:0]: ROI col end1
0x608D	STATIC_1015_D2V2_4_ STAT_CTRL_0D	0x20	RW	Bit[7:0]: ROI col end1
0x608E	STATIC_1015_D2V2_4_ STAT_CTRL_0E	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_row_start
0x608F	STATIC_1015_D2V2_4_ STAT_CTRL_0F	0x04	RW	Bit[7:4]: Not used Bit[3:0]: test_row_end
0x6090	STATIC_1015_D2V2_4_ STAT_CTRL_10	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_col_start

table A-2 sensor control registers (sheet 244 of 255)

address	register name	default value	R/W	description
0x6091	STATIC_1015_D2V2_4_ STAT_CTRL_11	0x00	RW	Bit[7:0]: test_col_start
0x6092	STATIC_1015_D2V2_4_ STAT_CTRL_12	0x02	RW	Bit[7:4]: Not used Bit[3:0]: test_col_end
0x6093	STATIC_1015_D2V2_4_ STAT_CTRL_13	0x80	RW	Bit[7:0]: test_col_end
0x6094	STATIC_1015_D2V2_4_ STAT_CTRL_14	0x07	RW	Bit[7:5]: Not used Bit[4:0]: test_pt_0
0x6095	STATIC_1015_D2V2_4_ STAT_CTRL_15	0x08	RW	Bit[7:5]: Not used Bit[4:0]: test_pt_1
0x6096	STATIC_1015_D2V2_4_ STAT_CTRL_16	0x04	RW	Bit[7:3]: Not used Bit[2:0]: norm_src_sel
0x6097	STATIC_1015_D2V2_4_ STAT_CTRL_17	0x00	RW	Bit[7:2]: Not used Bit[1]: test_skip_col Bit[0]: test_skip_row
0x609D	STATIC_1015_D2V2_4_ STAT_CTRL_1D	–	R	Bit[7:0]: static_ver
0x609E	STATIC_1015_D2V2_4_ STAT_CTRL_1E	–	R	Bit[7:0]: static_ver
0x6102	XTC1_CTRL_2	0x0C	RW	Bit[7:6]: Not used Bit[5]: m_bOverCorrectLimit Limit over correction Bit[4]: Disable 1C CP out of range check Bit[3]: Enable dithering Bit[2]: step_one_mean Use mean value in step one Bit[1]: Enable step two Bit[0]: Enable step one
0x6103	XTC1_CTRL_3	0x06	RW	Bit[7:3]: Not used Bit[2]: Flip enable Bit[1]: Mirror enable Bit[0]: mirror_flip_man_en Using manual mirror and file enable
0x6104	XTC1_CTRL_4	0x00	RW	Bit[7:6]: Not used Bit[5:0]: x_offset Horizontal offset
0x6105	XTC1_CTRL_5	0x00	RW	Bit[7:0]: x_offset Horizontal offset

table A-2 sensor control registers (sheet 245 of 255)

address	register name	default value	R/W	description
0x6106	XTC1_CTRL_6	0x00	RW	Bit[7:5]: Not used Bit[4:0]: y_offset Vertical offset
0x6107	XTC1_CTRL_7	0x00	RW	Bit[7:0]: y_offset Vertical offset
0x610A	XTC1_CTRL_A	0x0F	RW	Bit[7:6]: Not used Bit[5:0]: Image calibration width
0x610B	XTC1_CTRL_B	0x20	RW	Bit[7:0]: Image calibration width
0x610C	XTC1_CTRL_C	0x08	RW	Bit[7:5]: Not used Bit[4:0]: Image calibration height
0x610D	XTC1_CTRL_D	0x80	RW	Bit[7:0]: Image calibration height
0x610E	XTC1_CTRL_E	0x78	RW	Bit[7:0]: Xtalk ratio upper limit
0x610F	XTC1_CTRL_F	0x88	RW	Bit[7:0]: Xtalk ratio lower limit
0x6112	XTC1_CTRL_12	0x75	RW	Bit[7:0]: Reserved
0x6113	XTC1_CTRL_13	0x00	RW	Bit[7:2]: Not used Bit[1]: img_size_man_en Using manual configuration for image size Bit[0]: offset_man_en Using manual configuration for offset
0x6120	XTC1_CTRL_20	0x00	RW	Bit[7:0]: cp_1c_00 XTalk CP 1C
0x6121	XTC1_CTRL_21	0x00	RW	Bit[7:0]: cp_1c_01 XTalk CP 1C
0x6122	XTC1_CTRL_22	0x00	RW	Bit[7:0]: cp_1c_02 XTalk CP 1C
0x6123	XTC1_CTRL_23	0x00	RW	Bit[7:0]: cp_1c_03 XTalk CP 1C
0x6124	XTC1_CTRL_24	0x00	RW	Bit[7:0]: cp_1c_04 XTalk CP 1C
0x6125	XTC1_CTRL_25	0x00	RW	Bit[7:0]: cp_1c_05 XTalk CP 1C
0x6126	XTC1_CTRL_26	0x00	RW	Bit[7:0]: cp_1c_10 XTalk CP 1C
0x6127	XTC1_CTRL_27	0x00	RW	Bit[7:0]: cp_1c_11 XTalk CP 1C

table A-2 sensor control registers (sheet 246 of 255)

address	register name	default value	R/W	description
0x6128	XTC1_CTRL_28	0x00	RW	Bit[7:0]: cp_1c_12 XTalk CP 1C
0x6129	XTC1_CTRL_29	0x00	RW	Bit[7:0]: cp_1c_13 XTalk CP 1C
0x612A	XTC1_CTRL_2A	0x00	RW	Bit[7:0]: cp_1c_14 XTalk CP 1C
0x612B	XTC1_CTRL_2B	0x00	RW	Bit[7:0]: cp_1c_15 XTalk CP 1C
0x612C	XTC1_CTRL_2C	0x00	RW	Bit[7:0]: cp_1c_20 XTalk CP 1C
0x612D	XTC1_CTRL_2D	0x00	RW	Bit[7:0]: cp_1c_21 XTalk CP 1C
0x612E	XTC1_CTRL_2E	0x00	RW	Bit[7:0]: cp_1c_22 XTalk CP 1C
0x612F	XTC1_CTRL_2F	0x00	RW	Bit[7:0]: cp_1c_23 XTalk CP 1C
0x6130	XTC1_CTRL_30	0x00	RW	Bit[7:0]: cp_1c_24 XTalk CP 1C
0x6131	XTC1_CTRL_31	0x00	RW	Bit[7:0]: cp_1c_25 XTalk CP 1C
0x6132	XTC1_CTRL_32	0x00	RW	Bit[7:0]: cp_1c_30 XTalk CP 1C
0x6133	XTC1_CTRL_33	0x00	RW	Bit[7:0]: cp_1c_31 XTalk CP 1C
0x6134	XTC1_CTRL_34	0x00	RW	Bit[7:0]: cp_1c_32 XTalk CP 1C
0x6135	XTC1_CTRL_35	0x00	RW	Bit[7:0]: cp_1c_33 XTalk CP 1C
0x6136	XTC1_CTRL_36	0x00	RW	Bit[7:0]: cp_1c_34 XTalk CP 1C
0x6137	XTC1_CTRL_37	0x00	RW	Bit[7:0]: cp_1c_35 XTalk CP 1C
0x6138	XTC1_CTRL_38	0x00	RW	Bit[7:0]: cp_1c_40 XTalk CP 1C
0x6139	XTC1_CTRL_39	0x00	RW	Bit[7:0]: cp_1c_41 XTalk CP 1C
0x613A	XTC1_CTRL_3A	0x00	RW	Bit[7:0]: cp_1c_42 XTalk CP 1C

table A-2 sensor control registers (sheet 247 of 255)

address	register name	default value	R/W	description
0x613B	XTC1_CTRL_3B	0x00	RW	Bit[7:0]: cp_1c_43 XTalk CP 1C
0x613C	XTC1_CTRL_3C	0x00	RW	Bit[7:0]: cp_1c_44 XTalk CP 1C
0x613D	XTC1_CTRL_3D	0x00	RW	Bit[7:0]: cp_1c_45 XTalk CP 1C
0x613E	XTC1_CTRL_3E	0x00	RW	Bit[7:0]: cp_1c_50 XTalk CP 1C
0x613F	XTC1_CTRL_3F	0x00	RW	Bit[7:0]: cp_1c_51 XTalk CP 1C
0x6140	XTC1_CTRL_40	0x00	RW	Bit[7:0]: cp_1c_52 XTalk CP 1C
0x6141	XTC1_CTRL_41	0x00	RW	Bit[7:0]: cp_1c_53 XTalk CP 1C
0x6142	XTC1_CTRL_42	0x00	RW	Bit[7:0]: cp_1c_54 XTalk CP 1C
0x6143	XTC1_CTRL_43	0x00	RW	Bit[7:0]: cp_1c_55 XTalk CP 1C
0x6144	XTC1_CTRL_44	0x00	RW	Bit[7:0]: cp_3c_b_00 XTalk CP 3C B
0x6145	XTC1_CTRL_45	0x00	RW	Bit[7:0]: cp_3c_b_01 XTalk CP 3C B
0x6146	XTC1_CTRL_46	0x00	RW	Bit[7:0]: cp_3c_b_02 XTalk CP 3C B
0x6147	XTC1_CTRL_47	0x00	RW	Bit[7:0]: cp_3c_b_03 XTalk CP 3C B
0x6148	XTC1_CTRL_48	0x00	RW	Bit[7:0]: cp_3c_b_04 XTalk CP 3C B
0x6149	XTC1_CTRL_49	0x00	RW	Bit[7:0]: cp_3c_b_05 XTalk CP 3C B
0x614A	XTC1_CTRL_4A	0x00	RW	Bit[7:0]: cp_3c_b_10 XTalk CP 3C B
0x614B	XTC1_CTRL_4B	0x00	RW	Bit[7:0]: cp_3c_b_11 XTalk CP 3C B
0x614C	XTC1_CTRL_4C	0x00	RW	Bit[7:0]: cp_3c_b_12 XTalk CP 3C B
0x614D	XTC1_CTRL_4D	0x00	RW	Bit[7:0]: cp_3c_b_13 XTalk CP 3C B

table A-2 sensor control registers (sheet 248 of 255)

address	register name	default value	R/W	description
0x614E	XTC1_CTRL_4E	0x00	RW	Bit[7:0]: cp_3c_b_14 XTalk CP 3C B
0x614F	XTC1_CTRL_4F	0x00	RW	Bit[7:0]: cp_3c_b_15 XTalk CP 3C B
0x6150	XTC1_CTRL_50	0x00	RW	Bit[7:0]: cp_3c_b_20 XTalk CP 3C B
0x6151	XTC1_CTRL_51	0x00	RW	Bit[7:0]: cp_3c_b_21 XTalk CP 3C B
0x6152	XTC1_CTRL_52	0x00	RW	Bit[7:0]: cp_3c_b_22 XTalk CP 3C B
0x6153	XTC1_CTRL_53	0x00	RW	Bit[7:0]: cp_3c_b_23 XTalk CP 3C B
0x6154	XTC1_CTRL_54	0x00	RW	Bit[7:0]: cp_3c_b_24 XTalk CP 3C B
0x6155	XTC1_CTRL_55	0x00	RW	Bit[7:0]: cp_3c_b_25 XTalk CP 3C B
0x6156	XTC1_CTRL_56	0x00	RW	Bit[7:0]: cp_3c_b_30 XTalk CP 3C B
0x6157	XTC1_CTRL_57	0x00	RW	Bit[7:0]: cp_3c_b_31 XTalk CP 3C B
0x6158	XTC1_CTRL_58	0x00	RW	Bit[7:0]: cp_3c_b_32 XTalk CP 3C B
0x6159	XTC1_CTRL_59	0x00	RW	Bit[7:0]: cp_3c_b_33 XTalk CP 3C B
0x615A	XTC1_CTRL_5A	0x00	RW	Bit[7:0]: cp_3c_b_34 XTalk CP 3C B
0x615B	XTC1_CTRL_5B	0x00	RW	Bit[7:0]: cp_3c_b_35 XTalk CP 3C B
0x615C	XTC1_CTRL_5C	0x00	RW	Bit[7:0]: cp_3c_b_40 XTalk CP 3C B
0x615D	XTC1_CTRL_5D	0x00	RW	Bit[7:0]: cp_3c_b_41 XTalk CP 3C B
0x615E	XTC1_CTRL_5E	0x00	RW	Bit[7:0]: cp_3c_b_42 XTalk CP 3C B
0x615F	XTC1_CTRL_5F	0x00	RW	Bit[7:0]: cp_3c_b_43 XTalk CP 3C B
0x6160	XTC1_CTRL_60	0x00	RW	Bit[7:0]: cp_3c_b_44 XTalk CP 3C B

table A-2 sensor control registers (sheet 249 of 255)

address	register name	default value	R/W	description
0x6161	XTC1_CTRL_61	0x00	RW	Bit[7:0]: cp_3c_b_45 XTalk CP 3C B
0x6162	XTC1_CTRL_62	0x00	RW	Bit[7:0]: cp_3c_b_50 XTalk CP 3C B
0x6163	XTC1_CTRL_63	0x00	RW	Bit[7:0]: cp_3c_b_51 XTalk CP 3C B
0x6164	XTC1_CTRL_64	0x00	RW	Bit[7:0]: cp_3c_b_52 XTalk CP 3C B
0x6165	XTC1_CTRL_65	0x00	RW	Bit[7:0]: cp_3c_b_53 XTalk CP 3C B
0x6166	XTC1_CTRL_66	0x00	RW	Bit[7:0]: cp_3c_b_54 XTalk CP 3C B
0x6167	XTC1_CTRL_67	0x00	RW	Bit[7:0]: cp_3c_b_55 XTalk CP 3C B
0x6168	XTC1_CTRL_68	0x00	RW	Bit[7:0]: cp_3c_g_00 XTalk CP 3C G
0x6169	XTC1_CTRL_69	0x00	RW	Bit[7:0]: cp_3c_g_01 XTalk CP 3C G
0x616A	XTC1_CTRL_6A	0x00	RW	Bit[7:0]: cp_3c_g_02 XTalk CP 3C G
0x616B	XTC1_CTRL_6B	0x00	RW	Bit[7:0]: cp_3c_g_03 XTalk CP 3C G
0x616C	XTC1_CTRL_6C	0x00	RW	Bit[7:0]: cp_3c_g_04 XTalk CP 3C G
0x616D	XTC1_CTRL_6D	0x00	RW	Bit[7:0]: cp_3c_g_05 XTalk CP 3C G
0x616E	XTC1_CTRL_6E	0x00	RW	Bit[7:0]: cp_3c_g_10 XTalk CP 3C G
0x616F	XTC1_CTRL_6F	0x00	RW	Bit[7:0]: cp_3c_g_11 XTalk CP 3C G
0x6170	XTC1_CTRL_70	0x00	RW	Bit[7:0]: cp_3c_g_12 XTalk CP 3C G
0x6171	XTC1_CTRL_71	0x00	RW	Bit[7:0]: cp_3c_g_13 XTalk CP 3C G
0x6172	XTC1_CTRL_72	0x00	RW	Bit[7:0]: cp_3c_g_14 XTalk CP 3C G
0x6173	XTC1_CTRL_73	0x00	RW	Bit[7:0]: cp_3c_g_15 XTalk CP 3C G

table A-2 sensor control registers (sheet 250 of 255)

address	register name	default value	R/W	description
0x6174	XTC1_CTRL_74	0x00	RW	Bit[7:0]: cp_3c_g_20 XTalk CP 3C G
0x6175	XTC1_CTRL_75	0x00	RW	Bit[7:0]: cp_3c_g_21 XTalk CP 3C G
0x6176	XTC1_CTRL_76	0x00	RW	Bit[7:0]: cp_3c_g_22 XTalk CP 3C G
0x6177	XTC1_CTRL_77	0x00	RW	Bit[7:0]: cp_3c_g_23 XTalk CP 3C G
0x6178	XTC1_CTRL_78	0x00	RW	Bit[7:0]: cp_3c_g_24 XTalk CP 3C G
0x6179	XTC1_CTRL_79	0x00	RW	Bit[7:0]: cp_3c_g_25 XTalk CP 3C G
0x617A	XTC1_CTRL_7A	0x00	RW	Bit[7:0]: cp_3c_g_30 XTalk CP 3C G
0x617B	XTC1_CTRL_7B	0x00	RW	Bit[7:0]: cp_3c_g_31 XTalk CP 3C G
0x617C	XTC1_CTRL_7C	0x00	RW	Bit[7:0]: cp_3c_g_32 XTalk CP 3C G
0x617D	XTC1_CTRL_7D	0x00	RW	Bit[7:0]: cp_3c_g_33 XTalk CP 3C G
0x617E	XTC1_CTRL_7E	0x00	RW	Bit[7:0]: cp_3c_g_34 XTalk CP 3C G
0x617F	XTC1_CTRL_7F	0x00	RW	Bit[7:0]: cp_3c_g_35 XTalk CP 3C G
0x6180	XTC1_CTRL_80	0x00	RW	Bit[7:0]: cp_3c_g_40 XTalk CP 3C G
0x6181	XTC1_CTRL_81	0x00	RW	Bit[7:0]: cp_3c_g_41 XTalk CP 3C G
0x6182	XTC1_CTRL_82	0x00	RW	Bit[7:0]: cp_3c_g_42 XTalk CP 3C G
0x6183	XTC1_CTRL_83	0x00	RW	Bit[7:0]: cp_3c_g_43 XTalk CP 3C G
0x6184	XTC1_CTRL_84	0x00	RW	Bit[7:0]: cp_3c_g_44 XTalk CP 3C G
0x6185	XTC1_CTRL_85	0x00	RW	Bit[7:0]: cp_3c_g_45 XTalk CP 3C G
0x6186	XTC1_CTRL_86	0x00	RW	Bit[7:0]: cp_3c_g_50 XTalk CP 3C G

table A-2 sensor control registers (sheet 251 of 255)

address	register name	default value	R/W	description
0x6187	XTC1_CTRL_87	0x00	RW	Bit[7:0]: cp_3c_g_51 XTalk CP 3C G
0x6188	XTC1_CTRL_88	0x00	RW	Bit[7:0]: cp_3c_g_52 XTalk CP 3C G
0x6189	XTC1_CTRL_89	0x00	RW	Bit[7:0]: cp_3c_g_53 XTalk CP 3C G
0x618A	XTC1_CTRL_8A	0x00	RW	Bit[7:0]: cp_3c_g_54 XTalk CP 3C G
0x618B	XTC1_CTRL_8B	0x00	RW	Bit[7:0]: cp_3c_g_55 XTalk CP 3C G
0x618C	XTC1_CTRL_8C	0x00	RW	Bit[7:0]: cp_3c_r_00 XTalk CP 3C R
0x618D	XTC1_CTRL_8D	0x00	RW	Bit[7:0]: cp_3c_r_01 XTalk CP 3C R
0x618E	XTC1_CTRL_8E	0x00	RW	Bit[7:0]: cp_3c_r_02 XTalk CP 3C R
0x618F	XTC1_CTRL_8F	0x00	RW	Bit[7:0]: cp_3c_r_03 XTalk CP 3C R
0x6190	XTC1_CTRL_90	0x00	RW	Bit[7:0]: cp_3c_r_04 XTalk CP 3C R
0x6191	XTC1_CTRL_91	0x00	RW	Bit[7:0]: cp_3c_r_05 XTalk CP 3C R
0x6192	XTC1_CTRL_92	0x00	RW	Bit[7:0]: cp_3c_r_10 XTalk CP 3C R
0x6193	XTC1_CTRL_93	0x00	RW	Bit[7:0]: cp_3c_r_11 XTalk CP 3C R
0x6194	XTC1_CTRL_94	0x00	RW	Bit[7:0]: cp_3c_r_12 XTalk CP 3C R
0x6195	XTC1_CTRL_95	0x00	RW	Bit[7:0]: cp_3c_r_13 XTalk CP 3C R
0x6196	XTC1_CTRL_96	0x00	RW	Bit[7:0]: cp_3c_r_14 XTalk CP 3C R
0x6197	XTC1_CTRL_97	0x00	RW	Bit[7:0]: cp_3c_r_15 XTalk CP 3C R
0x6198	XTC1_CTRL_98	0x00	RW	Bit[7:0]: cp_3c_r_20 XTalk CP 3C R
0x6199	XTC1_CTRL_99	0x00	RW	Bit[7:0]: cp_3c_r_21 XTalk CP 3C R

table A-2 sensor control registers (sheet 252 of 255)

address	register name	default value	R/W	description
0x619A	XTC1_CTRL_9A	0x00	RW	Bit[7:0]: cp_3c_r_22 XTalk CP 3C R
0x619B	XTC1_CTRL_9B	0x00	RW	Bit[7:0]: cp_3c_r_23 XTalk CP 3C R
0x619C	XTC1_CTRL_9C	0x00	RW	Bit[7:0]: cp_3c_r_24 XTalk CP 3C R
0x619D	XTC1_CTRL_9D	0x00	RW	Bit[7:0]: cp_3c_r_25 XTalk CP 3C R
0x619E	XTC1_CTRL_9E	0x00	RW	Bit[7:0]: cp_3c_r_30 XTalk CP 3C R
0x619F	XTC1_CTRL_9F	0x00	RW	Bit[7:0]: cp_3c_r_31 XTalk CP 3C R
0x61A0	XTC1_CTRL_A0	0x00	RW	Bit[7:0]: cp_3c_r_32 XTalk CP 3C R
0x61A1	XTC1_CTRL_A1	0x00	RW	Bit[7:0]: cp_3c_r_33 XTalk CP 3C R
0x61A2	XTC1_CTRL_A2	0x00	RW	Bit[7:0]: cp_3c_r_34 XTalk CP 3C R
0x61A3	XTC1_CTRL_A3	0x00	RW	Bit[7:0]: cp_3c_r_35 XTalk CP 3C R
0x61A4	XTC1_CTRL_A4	0x00	RW	Bit[7:0]: cp_3c_r_40 XTalk CP 3C R
0x61A5	XTC1_CTRL_A5	0x00	RW	Bit[7:0]: cp_3c_r_41 XTalk CP 3C R
0x61A6	XTC1_CTRL_A6	0x00	RW	Bit[7:0]: cp_3c_r_42 XTalk CP 3C R
0x61A7	XTC1_CTRL_A7	0x00	RW	Bit[7:0]: cp_3c_r_43 XTalk CP 3C R
0x61A8	XTC1_CTRL_A8	0x00	RW	Bit[7:0]: cp_3c_r_44 XTalk CP 3C R
0x61A9	XTC1_CTRL_A9	0x00	RW	Bit[7:0]: cp_3c_r_45 XTalk CP 3C R
0x61AA	XTC1_CTRL_AA	0x00	RW	Bit[7:0]: cp_3c_r_50 XTalk CP 3C R
0x61AB	XTC1_CTRL_AB	0x00	RW	Bit[7:0]: cp_3c_r_51 XTalk CP 3C R
0x61AC	XTC1_CTRL_AC	0x00	RW	Bit[7:0]: cp_3c_r_52 XTalk CP 3C R

table A-2 sensor control registers (sheet 253 of 255)

address	register name	default value	R/W	description
0x61AD	XTC1_CTRL_AD	0x00	RW	Bit[7:0]: cp_3c_r_53 XTalk CP 3C R
0x61AE	XTC1_CTRL_AE	0x00	RW	Bit[7:0]: cp_3c_r_54 XTalk CP 3C R
0x61AF	XTC1_CTRL_AF	0x00	RW	Bit[7:0]: cp_3c_r_55 XTalk CP 3C R
0x61B2	ISP_STAT_16	–	R	Bit[7:0]: Version
0x61B3	ISP_STAT_17	–	R	Bit[7:0]: Version
0x6A00	REG_WIN_00	0x00	RW	Bit[7:5]: Not used Bit[4:0]: size0b_x_offset
0x6A01	REG_WIN_01	0x20	RW	Bit[7:0]: size0b_x_offset
0x6A02	REG_WIN_02	0x00	RW	Bit[7:5]: Not used Bit[4:0]: size0b_y_offset
0x6A03	REG_WIN_03	0x20	RW	Bit[7:0]: size0b_y_offset
0x6A04	REG_WIN_04	0x02	RW	Bit[7:5]: Not used Bit[4:0]: size0b_x_output_size
0x6A05	REG_WIN_05	0x80	RW	Bit[7:0]: size0b_x_output_size
0x6A06	REG_WIN_06	0x01	RW	Bit[7:5]: Not used Bit[4:0]: size0b_y_output_size
0x6A07	REG_WIN_07	0xE0	RW	Bit[7:0]: size0b_y_output_size
0x6A08	REG_WIN_08	0xCF	RW	Bit[7]: sof_sel Bit[6]: win_en Bit[5]: blk_out_en Bit[4]: ab_l_href_sync_eco eco_sl0b: bz407 Bit[3]: flip_keep_view_en Bit[2]: mirror_keep_view_en Bit[1]: hwin_en Bit[0]: vwin_en
0x6A09	REG_WIN_09	0x01	RW	Bit[7:4]: emb_end_pos Bit[3]: dummy_mask_eco eco_sl0b: bz361 masked special flags in dummy Bit[2]: ab_s_href_sync_eco eco_sl0b: bz407 Bit[1]: flip_auto_cut_en Bit[0]: mirror_auto_cut_en

table A-2 sensor control registers (sheet 254 of 255)

address	register name	default value	R/W	description
0x6A0A	REG_WIN_0A	0x40	RW	Bit[7]: single_dummy_seof_en Generate only 1 SOF and EOF for dummy in one stream session Bit[6]: vblk_req_dummy_seof_en Bit[5:4]: dummy_seof_sel Bit[3:0]: dummy_pos
0x6A10	REG_WIN_10	–	R	Bit[7:3]: Not used Bit[2:0]: l_px_cnt
0x6A11	REG_WIN_11	–	R	Bit[7:0]: l_px_cnt
0x6A12	REG_WIN_12	–	R	Bit[7:3]: Not used Bit[2:0]: l_ln_cnt
0x6A13	REG_WIN_13	–	R	Bit[7:0]: l_ln_cnt
0x6A14	REG_WIN_14	–	R	Bit[7:3]: Not used Bit[2:0]: s_px_cnt
0x6A15	REG_WIN_15	–	R	Bit[7:0]: s_px_cnt
0x6A16	REG_WIN_16	–	R	Bit[7:3]: Not used Bit[2:0]: s_ln_cnt
0x6A17	REG_WIN_17	–	R	Bit[7:0]: s_ln_cnt
0x6A18	REG_WIN_18	–	R	Bit[7:3]: Not used Bit[2:0]: m_px_cnt
0x6A19	REG_WIN_19	–	R	Bit[7:0]: m_px_cnt
0x6A1A	REG_WIN_1A	–	R	Bit[7:3]: Not used Bit[2:0]: m_ln_cnt
0x6A1B	REG_WIN_1B	–	R	Bit[7:0]: m_ln_cnt
0x6A1C	REG_WIN_1C	–	R	Bit[7:3]: Not used Bit[2:0]: vs_px_cnt
0x6A1D	REG_WIN_1D	–	R	Bit[7:0]: vs_px_cnt
0x6A1E	REG_WIN_1E	–	R	Bit[7:3]: Not used Bit[2:0]: vs_ln_cnt
0x6A1F	REG_WIN_1F	–	R	Bit[7:0]: vs_ln_cnt
0x6A20	REG_WIN_20	0x00	RW	Bit[7:5]: Not used Bit[4:0]: size1_x_offset
0x6A21	REG_WIN_21	0x02	RW	Bit[7:0]: size1_x_offset
0x6A22	REG_WIN_22	0x00	RW	Bit[7:5]: Not used Bit[4:0]: size1_y_offset
0x6A23	REG_WIN_23	0x00	RW	Bit[7:0]: size1_y_offset

table A-2 sensor control registers (sheet 255 of 255)

address	register name	default value	R/W	description
0x6A24	REG_WIN_24	0x00	RW	Bit[7:5]: Not used Bit[4:0]: size1_x_output_size
0x6A25	REG_WIN_25	0x00	RW	Bit[7:0]: size1_x_output_size
0x6A26	REG_WIN_26	0x00	RW	Bit[7:5]: Not used Bit[4:0]: size1_y_output_size
0x6A27	REG_WIN_27	0x00	RW	Bit[7:0]: size1_y_output_size
0x6A28	REG_WIN_28	0x00	RW	Bit[7:4]: Not used Bit[3]: l_size_select Bit[2]: m_size_select Bit[1]: s_size_select Bit[0]: vs_size_select
0x6A29	REG_WIN_29	0x01	RW	Bit[7:2]: Not used Bit[1]: dummy_mis_align_enable Bit[0]: register_frame_sync_en
0x6A2A	REG_WIN_2A	0x11	RW	Bit[7:0]: mtest_bus Connections inside ISP, don't care[1:0], TEST1, RME, RM[3:0]
0x6A2B	REG_WIN_2B	0x30	RW	Bit[7:0]: mtest_bus Connections inside ISP, RA[1:0], WA[2:0], WPULSE[2:0]
0x6A2C	REG_WIN_2C	–	R	Bit[7:1]: Not used Bit[0]: mtest_result
0x7000~ 0x73FF	OTP BUFFER	–	–	1024B SRAM for OTP data

revision history

version 1.0 06.29.2020

- initial release

version 1.01 10.14.2020

- in ordering information, changed ordering part number to "OX03C10-E66Y-001B-Z ..."

version 1.1 11.04.2020

- in key specifications, changed max S/N ratio specification to 41.6 dB
- in table 1-5, changed table footnote b to "t2 (ms) = 144 / XVCLK (MHz)" and changed table footnote d to "t3 (ms) = 16.4 / XVCLK (MHz)"
- in figure, 2-1, removed signal PWDNB
- in figure 3-3, removed "SPD" from sample HCG, LCG, SPD
- in section 3.2, changed first sentence of first paragraph to "...from 20 to 1296 in steps of two..."
- in figure 3-5, changed "ISP_X_WIN_INT" to "ISP_X_WIN_TRUNC" and "ISP_Y_WIN_INT" to "ISP_Y_WIN_TRUNC"
- in section 3.4, removed second sentence of third paragraph
- in section 3.7.1, changed second sentence of section description to "The VCO range is from 1250 MHz to 2500 MHz."
- in figure 3-10, changed register bits for mipi_divider block to "0x0306[2:0]"
- in section 3.7.2, changed second sentence of section description to "The VCO range is from 1250 MHz to 2500 MHz"
- in figure 3-11, changed register bits for tc_divider block to "0x032B[3:0]"
- in table 4-1, changed default value for register 0x5002 to 0x3F
- in section 4.2, changed first sentence of third paragraph to "...disabled by register bits 0x5004[1] ~ 0x5007[1]..."
- in section 4.4, removed sixth sentence of first paragraph, removed figure 4-7, removed bullets 3~7, removed table 4-5, removed paragraphs 2~6, and removed figure 4-8
- in section 5.2, removed second and third sentence from third paragraph and removed table 5-2 and figure 5-3
- in table 5-2 (previously table 5-3), changed default value for register 0x5002 to 0x3F
- in section 5.5, changed end of seventh sentence in third paragraph to "...embedded data (see section 5.6)."
- in section 5.5.3.1, changed end of first paragraph to "...register 0x3211 to 0." and changed first line of code in setting example to "6C 3211 00;..."
- in section 5.5.3.2, changed first line of code in setting example to "6C 3211 00;..."
- in section 5.5.3.3, changed second sentence of section description to "...is controlled by the register 0x3211,... ", changed seventh sentence of section description to "Frame numbers 0x320A, 0x320B, 0x320C, and 0x320D...", changed first line of code of setting example to "6C 3211 11;",

changed second line of code of setting example to "6C 320A 04;...", and changed third line of code of setting example to "6C 3208 01;..."

- in section 5.5.3.4, changed first line of code of setting example to "6C 3211 11;...", changed second line of code of setting example to "6C 320A 04;...", and changed third line of code of setting example to "6C 3208 01;..."
- in section 5.5.3.5, changed first sentence of first paragraph to "... by register bit 0x3211[5].", changed second sentence of first paragraph to "Frame numbers 0x320A, 0x320B, 0x320C, and 0x320D...", changed first line of code in setting example to "6C 320A 02;...", changed second line of code in setting example to "6C 320B 03;...", changed third line of code in setting example to "6C 320C 00;...", changed fourth line of code in setting example to "6C 320D 08;...", and changed fifth line of code in setting example to "6C 3211 30;..."
- in table 5-7, changed register name, default value, R/W, and description for registers 0x320E~0x320F to "RSVD", "–", "–", and "Reserved", respectively and changed register name, default value, R/W, and description for registers 0x322A~0x322C to "RSVD", "–", "–", and "Reserved", respectively
- in table 5-10 (previously table 5-11), changed default value for register 0x5002 to 0x3F
- in chapter 6, changed second sentence of first paragraph to "SCCB is fully compatible with I2C standard mode, fast mode, and fast mode plus (when the sensor input clock is 12 MHz or higher)."
- in table 9-3, changed typ value for supply symbol I_{AVDD} to 66 mA, changed typ value for supply symbol I_{DVDD} to 141 mA, and changed typ value for supply symbol I_{DOVDD} to 0.21 mA
- in appendix A, added section A.2

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