Data File Overview

File Type	Time Domain Differential
Waveform File	E:\Project\5 SAK4\PCIE CLOCK\clock jitter test\U.2 1.wfm
Waveform File Creation Date	2019-11-15 11:05:32 GMT+08:00
Edge Filtering	On
Clock Frequency	99.768 MHz
SSC Frequency	31.250 kHz
Number of Edges	38,306
Sample Interval	40.000 ps
Selected Threshold Voltage	-129.856 mV (via auto-threshold search)
Warning	Data file should contain 160,000 or more edges

Filter Compliance Summary

Class	Data Rate	Architecture	Specs	Max HF RMS	Max HLF RMS	Max Pk-Pk	Compliance Summary
GEN3	8 Gb/s	Common Clock	3.1 4.0	912.11 fs	517.79 fs	2.97 ps	All PASS

Jitter Summary

#	Class	Data Rate	Arch (1)	Specs	PLL1 BW	PLL1 Peak	PLL2 BW	PLL2 Peak	CDR BW	CDR Peak	Specification			Analysis Result			Compliance Result
											HF RMS	LF RMS	Pk-Pk	HF RMS	LF RMS	Pk-Pk	
1	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz	0.01 dB	2 MHz	0.01 dB	10 MHz	0 dB	1 ps			382.68 fs	68.24 fs	967.64 fs	PASS
2	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 2 MHz (H')	0.01 dB (H) 1 dB (H')	2 MHz (H) 2 MHz (H')	1 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			595.81 fs (H)	489.24 fs (H)	1.89 ps (H)	PASS
3	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 2 MHz (H')	0.01 dB (H) 2 dB (H')	2 MHz (H) 2 MHz (H')	2 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			597.38 fs (H)	506.52 fs (H)	2.08 ps (H)	PASS
4	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 4 MHz (H')	0.01 dB (H) 0.01 dB (H')	4 MHz (H) 2 MHz (H')	0.01 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			715.83 fs (H)	296.34 fs (H)	2.20 ps (H)	PASS
5	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 4 MHz (H')	0.01 dB (H) 2 dB (H')	4 MHz (H) 2 MHz (H')	2 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			713.90 fs (H)	517.79 fs (H)	2.65 ps (H)	PASS
6	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 5 MHz (H')	0.01 dB (H) 0.01 dB (H')	5 MHz (H) 2 MHz (H')	0.01 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			861.68 fs (H)	342.76 fs (H)	2.62 ps (H)	PASS
7	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 5 MHz (H')	0.01 dB (H) 1 dB (H')	5 MHz (H) 2 MHz (H')	1 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			861.95 fs (H)	513.46 fs (H)	2.97 ps (H)	PASS
8	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz	1 dB	2 MHz	1 dB	10 MHz	0 dB	1 ps			327.56 fs	69.53 fs	829.33 fs	PASS
9	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 2 MHz (H')	1 dB (H) 2 dB (H')	2 MHz (H) 2 MHz (H')	2 dB (H) 1 dB (H')	10 MHz	0 dB	1 ps			323.91 fs (H')	111.80 fs (H)	1.01 ps (H')	PASS
10	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 4 MHz (H')	1 dB (H) 0.01 dB (H')	4 MHz (H) 2 MHz (H')	0.01 dB (H) 1 dB (H')	10 MHz	0 dB	1 ps			686.25 fs (H)	283.90 fs (H')	2.12 ps (H)	PASS
11	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 4 MHz (H')	1 dB (H) 2 dB (H')	4 MHz (H) 2 MHz (H')	2 dB (H) 1 dB (H')	10 MHz	0 dB	1 ps			538.27 fs (H)	205.06 fs (H)	2.00 ps (H)	PASS
12	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 5 MHz (H')	1 dB (H) 0.01 dB (H')	5 MHz (H) 2 MHz (H')	0.01 dB (H) 1 dB (H')	10 MHz	0 dB	1 ps			817.68 fs (H)	248.24 fs (H')	2.52 ps (H)	PASS
13	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 5 MHz (H')	1 dB (H) 1 dB (H')	5 MHz (H) 2 MHz (H')	1 dB (H) 1 dB (H')	10 MHz	0 dB	1 ps			729.81 fs (H)	196.19 fs (H)	2.40 ps (H)	PASS
14	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz	2 dB	2 MHz	2 dB	10 MHz	0 dB	1 ps			275.87 fs	70.39 fs	727.61 fs	PASS
15	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 4 MHz (H')	2 dB (H) 0.01 dB (H')	4 MHz (H) 2 MHz (H')	0.01 dB (H) 2 dB (H')	10 MHz	0 dB	1 ps			701.62 fs (H)	300.77 fs (H')	2.32 ps (H)	PASS
16	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 4 MHz (H')	2 dB (H) 2 dB (H')	4 MHz (H) 2 MHz (H')	2 dB (H) 2 dB (H')	10 MHz	0 dB	1 ps			548.89 fs (H)	194.73 fs (H)	2.19 ps (H)	PASS
17	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 5 MHz (H')	2 dB (H) 0.01 dB (H')	5 MHz (H) 2 MHz (H')	0.01 dB (H) 2 dB (H')	10 MHz	0 dB	1 ps			831.41 fs (H)	265.04 fs (H')	2.71 ps (H)	PASS
18	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 5 MHz (H')	2 dB (H) 1 dB (H')	5 MHz (H) 2 MHz (H')	1 dB (H) 2 dB (H')	10 MHz	0 dB	1 ps			742.90 fs (H)	189.21 fs (H)	2.57 ps (H)	PASS
19	GEN3	8 Gb/s	CC	3.1 4.0	4 MHz	0.01 dB	4 MHz	0.01 dB	10 MHz	0 dB	1 ps			740.19 fs	68.73 fs	1.85 ps	PASS
20	GEN3	8 Gb/s	CC	3.1 4.0	4 MHz (H) 4 MHz (H')	0.01 dB (H) 2 dB (H')	4 MHz (H) 4 MHz (H')	2 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			736.92 fs (H')	290.71 fs (H)	2.11 ps (H)	PASS

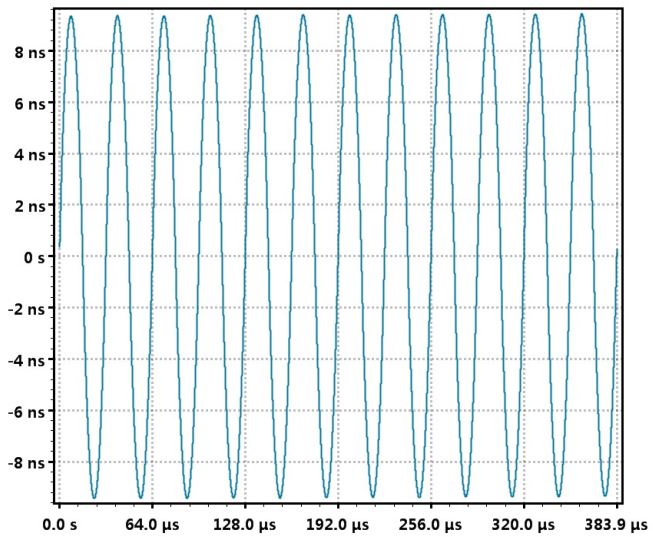
#	Class	Data Rate	Arch (1)	Specs	PLL1 BW	PLL1 Peak	PLL2 BW	PLL2 Peak	CDR BW	CDR Peak	Specification			Analysis Result			Compliance Result
											HF RMS	LF RMS	Pk-Pk	HF RMS	LF RMS	Pk-Pk	
21	GEN3	8 Gb/s	CC	3.1 4.0	4 MHz (H) 5 MHz (H')	0.01 dB (H) 0.01 dB (H')	5 MHz (H) 4 MHz (H')	0.01 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			863.21 fs (H)	115.20 fs (H)	2.19 ps (H)	PASS
22	GEN3	8 Gb/s	CC	3.1 4.0	4 MHz (H) 5 MHz (H')	0.01 dB (H) 1 dB (H')	5 MHz (H) 4 MHz (H')	1 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			804.30 fs (H)	286.06 fs (H)	2.29 ps (H)	PASS
23	GEN3	8 Gb/s	CC	3.1 4.0	4 MHz	2 dB	4 MHz	2 dB	10 MHz	0 dB	1 ps			537.90 fs	70.23 fs	1.40 ps	PASS
24	GEN3	8 Gb/s	CC	3.1 4.0	4 MHz (H) 5 MHz (H')	2 dB (H) 0.01 dB (H')	5 MHz (H) 4 MHz (H')	0.01 dB (H) 2 dB (H')	10 MHz	0 dB	1 ps			860.84 fs (H)	245.19 fs (H')	2.40 ps (H)	PASS
25	GEN3	8 Gb/s	CC	3.1 4.0	4 MHz (H) 5 MHz (H')	2 dB (H) 1 dB (H')	5 MHz (H) 4 MHz (H')	1 dB (H) 2 dB (H')	10 MHz	0 dB	1 ps			740.92 fs (H)	73.97 fs (H')	2.07 ps (H)	PASS
26	GEN3	8 Gb/s	CC	3.1 4.0	5 MHz	0.01 dB	5 MHz	0.01 dB	10 MHz	0 dB	1 ps			912.11 fs	68.80 fs	2.27 ps	PASS
27	GEN3	8 Gb/s	CC	3.1 4.0	5 MHz (H) 5 MHz (H')	0.01 dB (H) 1 dB (H')	5 MHz (H) 5 MHz (H')	1 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			900.90 fs (H')	240.19 fs (H)	2.33 ps (H')	PASS
28	GEN3	8 Gb/s	CC	3.1 4.0	5 MHz	1 dB	5 MHz	1 dB	10 MHz	0 dB	1 ps			788.49 fs	69.68 fs	1.99 ps	PASS

(1) CC: Common Clock; DC: Data Clock; SRNS: Separate Clock SRNS; SRIS: Separate Clock SRIS

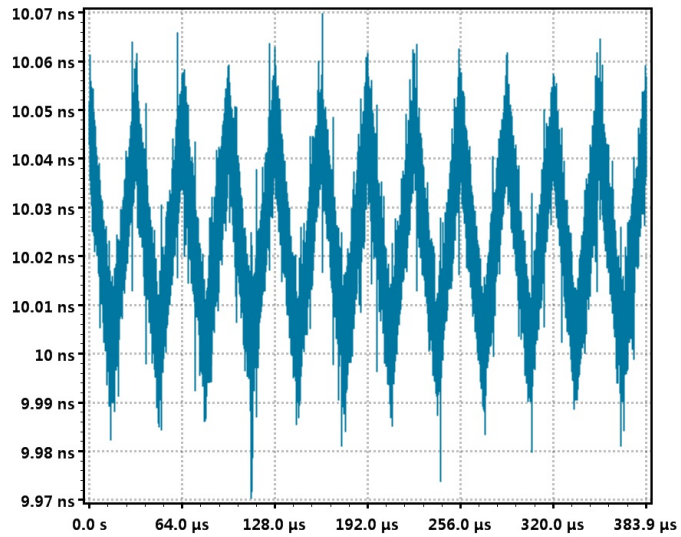
(2) Spread Spectrum Clocking (SSC) separation is intended to remove the energy associated with the spread spectrum (30KHz-33KHz) in the low frequency range (0.01-1.5MHz) specified by the PCI-Express Base Specification in order to define separate low frequency Rj and Dj components.

Waveform Analysis

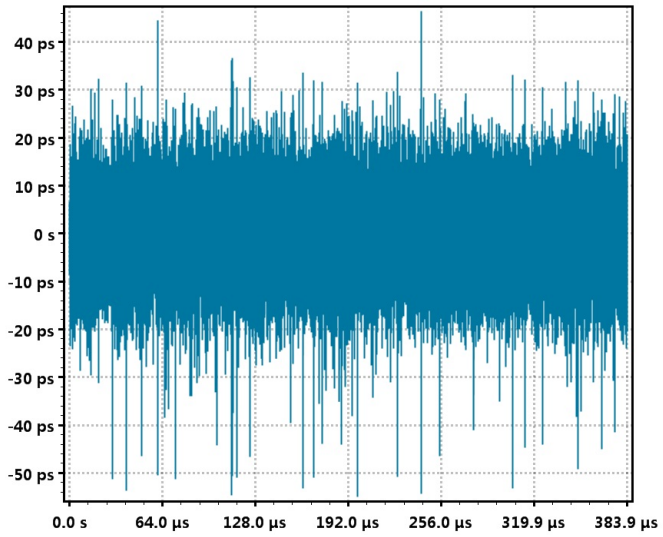
Time Interval Error



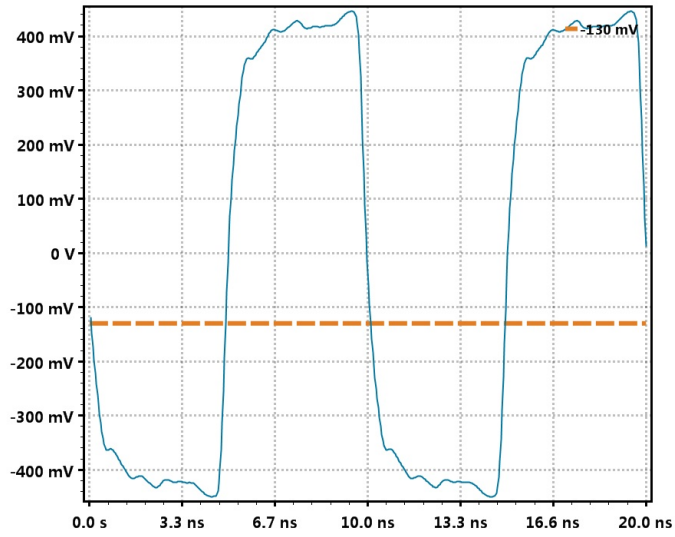
Period



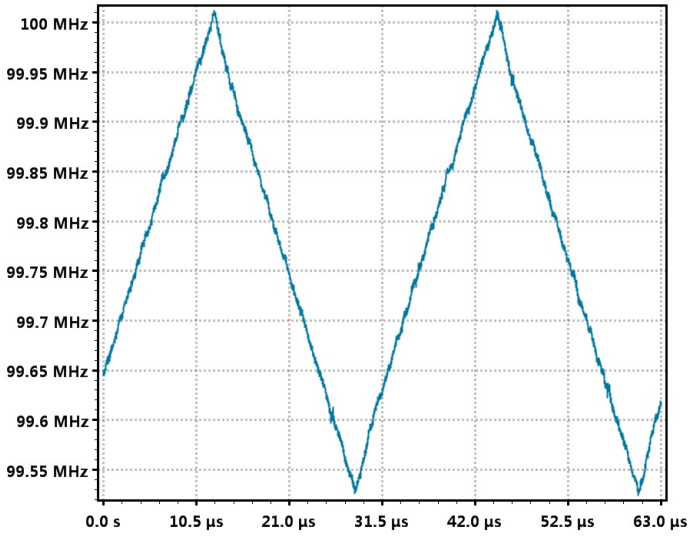
Cycle-to-Cycle



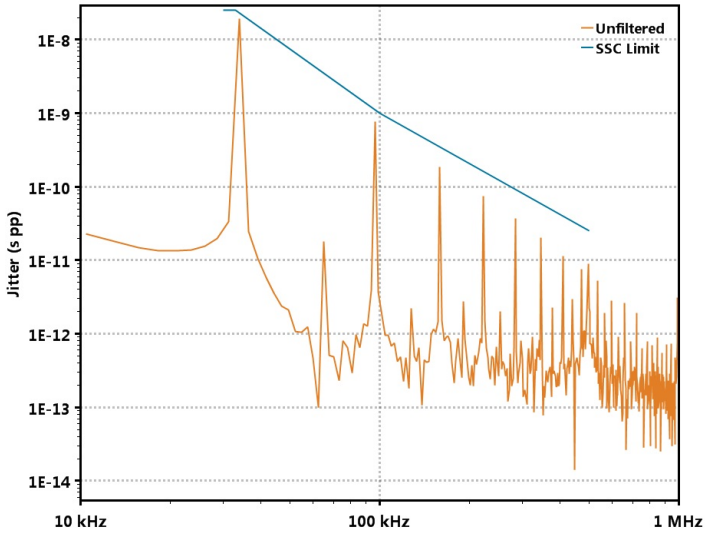
Differential Clock Signal



Spread-Spectrum Clocking Profile



Spread Spectrum Phase Jitter



Reference Clock AC Specifications

Symbol	Parameter	Specification		Analysis Result			Compliance Result
		Min	Max	Min	Max	Avg	
Rising Edge Rate	Rising Edge Rate	0.6 V/ns	4 V/ns	1.30 V/ns	1.61 V/ns	1.44 V/ns	PASS
Falling Edge Rate	Falling Edge Rate	0.6 V/ns	4 V/ns	0.64 V/ns	0.84 V/ns	0.72 V/ns	PASS
V_{IH}	Differential Input High Voltage	150 mV		408.19 mV	448.27 mV	428.56 mV	PASS
V_{IL}	Differential Input Low Voltage		-150 mV	-456.14 mV	-404.89 mV	-431.20 mV	PASS
V_{RB}	Ring-Back Voltage		200 mV	N/A	895.22 mV	473.25 mV	FAIL
V_{OVS}	Overshoot Voltage relative to V_{IH}		300 mV	-1.195 mV	38.187 mV	17.173 mV	PASS
V_{UDS}	Undershoot Voltage relative to V_{IL}		300 mV	-4.294 mV	46.098 mV	18.330 mV	PASS
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300 ppm	2,800 ppm	N/A	N/A	2,317 ppm	PASS
$T_{PERIOD\ ABS}$	Absolute Period (including Jitter and Spread Spectrum modulation)	9.847 ns	10.203 ns	9.970 ns	10.070 ns	10.023 ns	PASS
$T_{CCJITTER}$	Cycle to Cycle Jitter		150 ps	0.00 s	54.93 ps	6.91 ps	PASS
Duty Cycle	Duty Cycle	40 %	60 %	51.4 %	52.4 %	51.9 %	PASS
SSC Parameters							
F_{REFCLK}	Refclk Frequency		100.03 MHz	N/A	N/A	100.01 MHz	PASS
F_{SSC}	SSC frequency range	30 kHz	33 kHz	N/A	N/A	31.25 kHz	PASS
$T_{SSC-FREQ-DEVIATION}$	SSC deviation	-0.5 %	0 %	N/A	N/A	-0.49 %	PASS
$T_{SSC-MAX-FREQ-SLEW}$	Max SSC df/dt		1,250 ppm/us	N/A	N/A	541 ppm/us	PASS

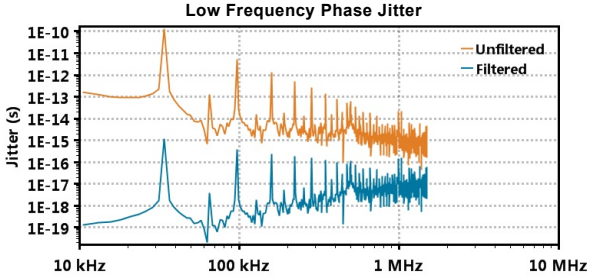
Detailed Jitter Reports

In the pages that follow, jitter response is analyzed for each selected standard, architecture and filter parameter combination.

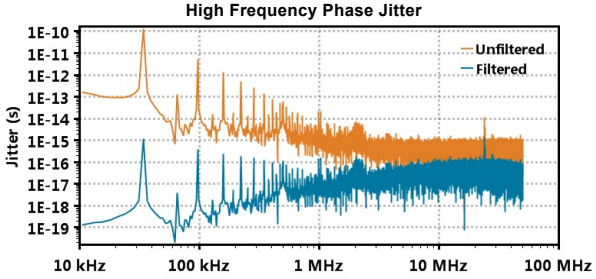
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
1	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz	0.01 dB	2 MHz	0.01 dB	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	382.685 fs	PASS
Refclk LF RMS Jitter		68.235 fs	N/A
Pk-pk Phase Jitter		967.644 fs	N/A

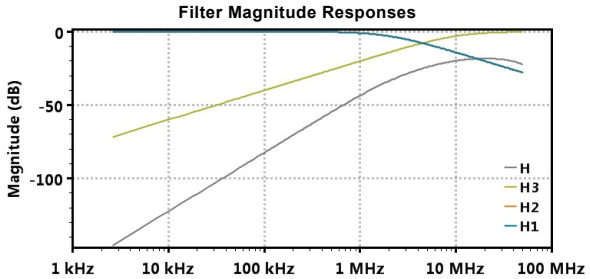
Low Frequency Phase Jitter



High Frequency Phase Jitter



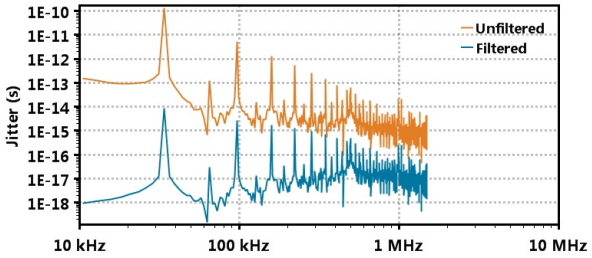
Filter Magnitude Responses



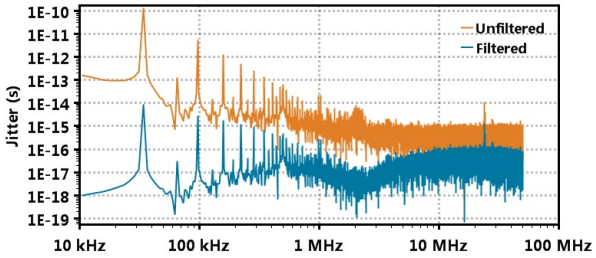
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
2	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 2 MHz (H')	0.01 dB (H) 1 dB (H')	2 MHz (H) 2 MHz (H')	1 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	595.807 fs (H)	PASS
Refclk LF RMS Jitter		489.237 fs (H)	N/A
Pk-pk Phase Jitter		1.892 ps (H)	N/A

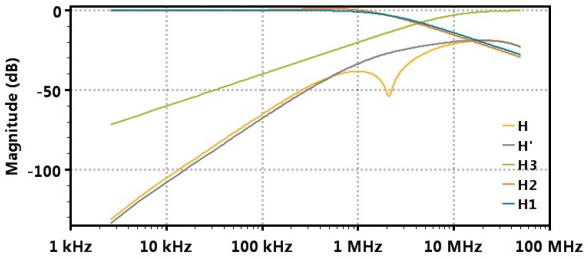
Low Frequency Phase Jitter



High Frequency Phase Jitter



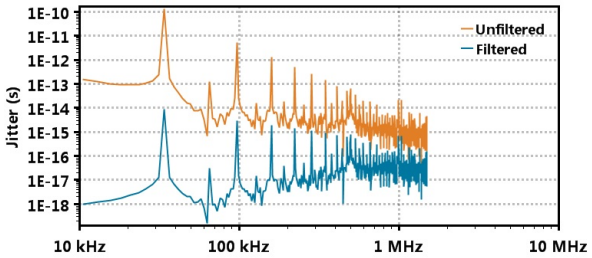
Filter Magnitude Responses



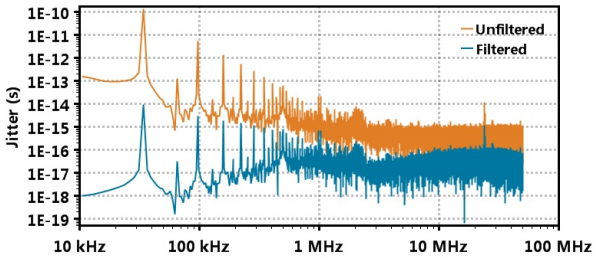
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
3	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 2 MHz (H')	0.01 dB (H) 2 dB (H')	2 MHz (H) 2 MHz (H')	2 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	597.382 fs (H)	PASS
Refclk LF RMS Jitter		506.517 fs (H)	N/A
Pk-pk Phase Jitter		2.080 ps (H)	N/A

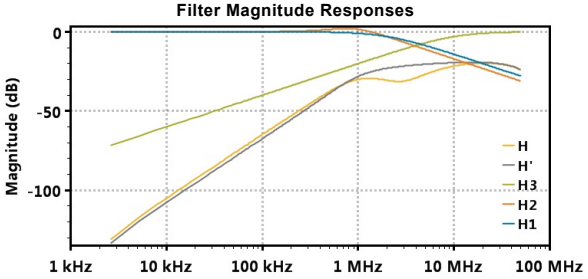
Low Frequency Phase Jitter



High Frequency Phase Jitter



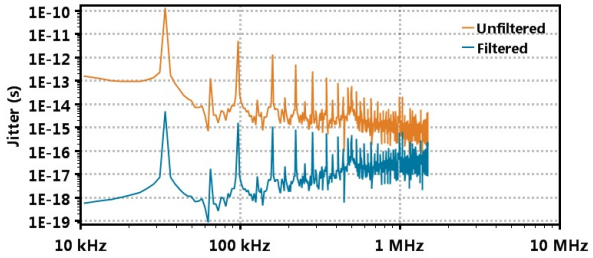
Filter Magnitude Responses



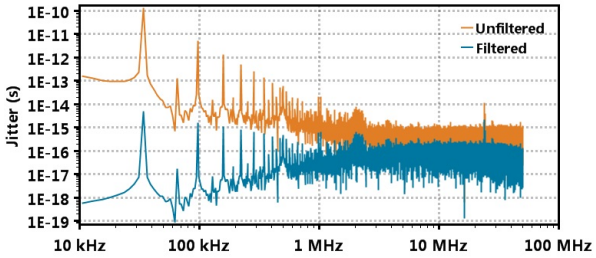
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
4	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 4 MHz (H')	0.01 dB (H) 0.01 dB (H')	4 MHz (H) 2 MHz (H')	0.01 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	715.831 fs (H)	PASS
Refclk LF RMS Jitter		296.335 fs (H)	N/A
Pk-pk Phase Jitter		2.203 ps (H)	N/A

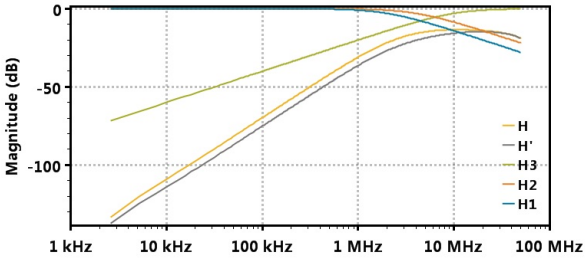
Low Frequency Phase Jitter



High Frequency Phase Jitter



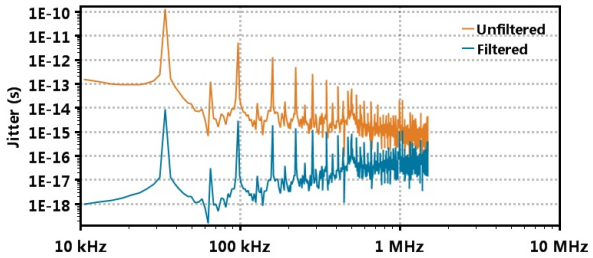
Filter Magnitude Responses



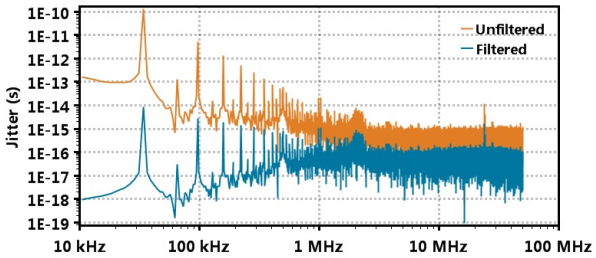
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
5	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 4 MHz (H')	0.01 dB (H) 2 dB (H')	4 MHz (H) 2 MHz (H')	2 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	713.900 fs (H)	PASS
Refclk LF RMS Jitter		517.789 fs (H)	N/A
Pk-pk Phase Jitter		2.651 ps (H)	N/A

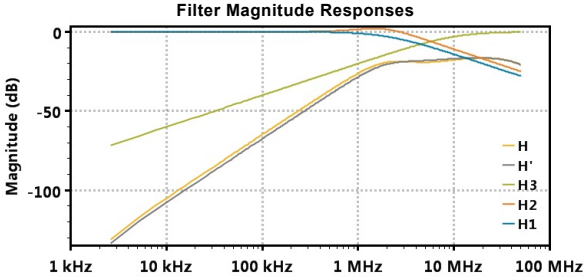
Low Frequency Phase Jitter



High Frequency Phase Jitter



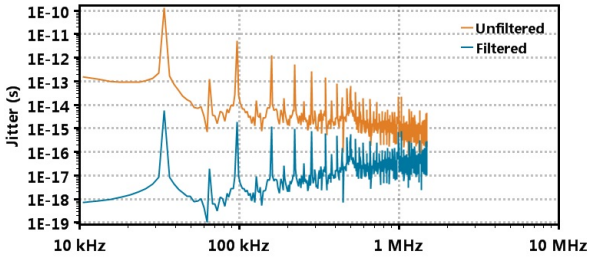
Filter Magnitude Responses



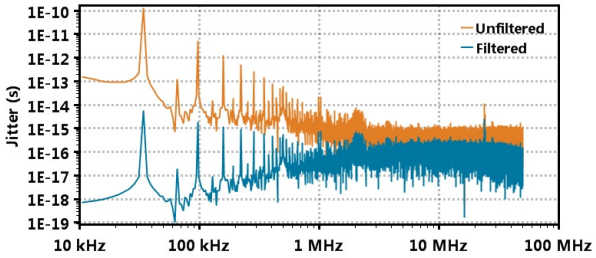
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
6	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 5 MHz (H')	0.01 dB (H) 0.01 dB (H')	5 MHz (H) 2 MHz (H')	0.01 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	861.678 fs (H)	PASS
Refclk LF RMS Jitter		342.761 fs (H)	N/A
Pk-pk Phase Jitter		2.622 ps (H)	N/A

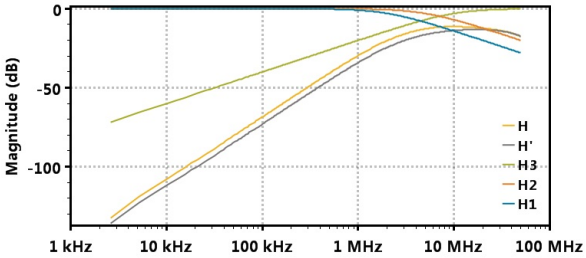
Low Frequency Phase Jitter



High Frequency Phase Jitter



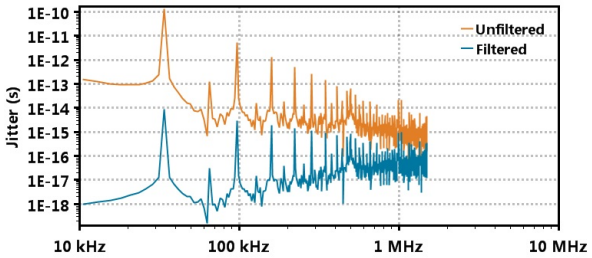
Filter Magnitude Responses



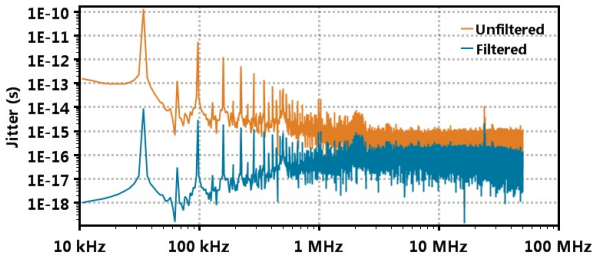
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
7	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 5 MHz (H')	0.01 dB (H) 1 dB (H')	5 MHz (H) 2 MHz (H')	1 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	861.946 fs (H)	PASS
Refclk LF RMS Jitter		513.463 fs (H)	N/A
Pk-pk Phase Jitter		2.967 ps (H)	N/A

Low Frequency Phase Jitter



High Frequency Phase Jitter



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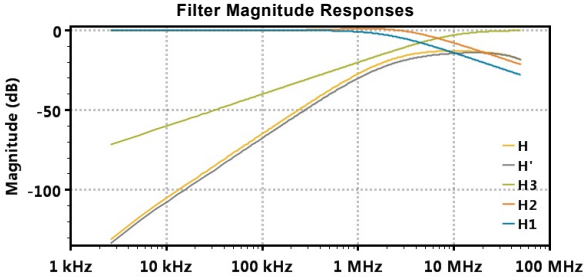
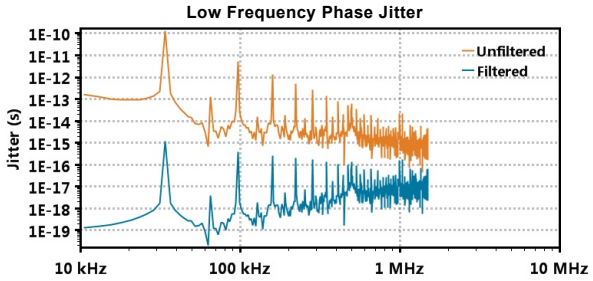
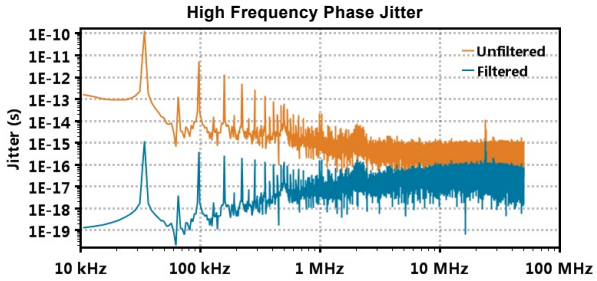
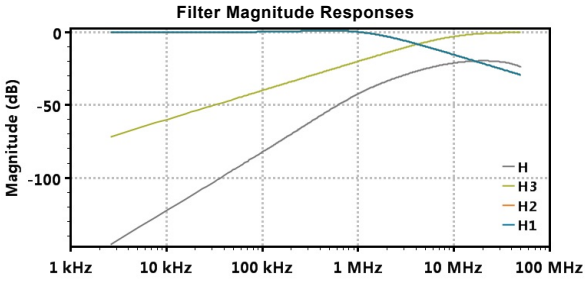


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
8	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz	1 dB	2 MHz	1 dB	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	327.556 fs	PASS
Refclk LF RMS Jitter		69.531 fs	N/A
Pk-pk Phase Jitter		829.333 fs	N/A

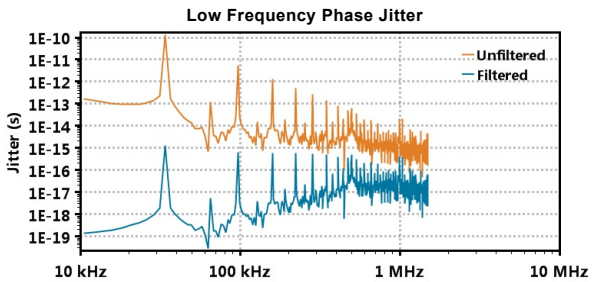


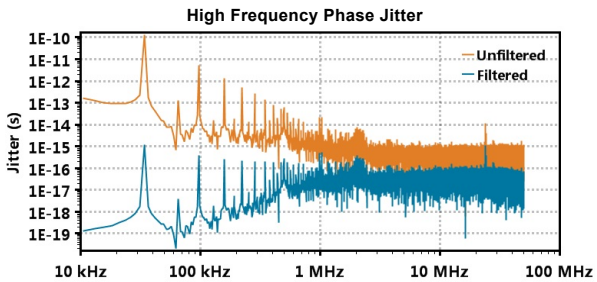


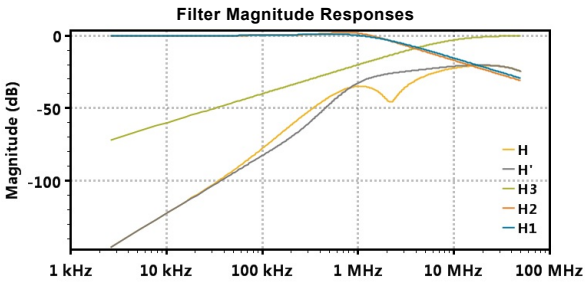


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
9	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 2 MHz (H')	1 dB (H) 2 dB (H')	2 MHz (H) 2 MHz (H')	2 dB (H) 1 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	323.911 fs (H')	PASS
Refclk LF RMS Jitter		111.798 fs (H)	N/A
Pk-pk Phase Jitter		1.008 ps (H')	N/A

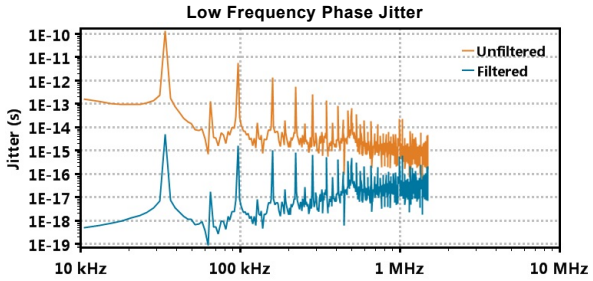


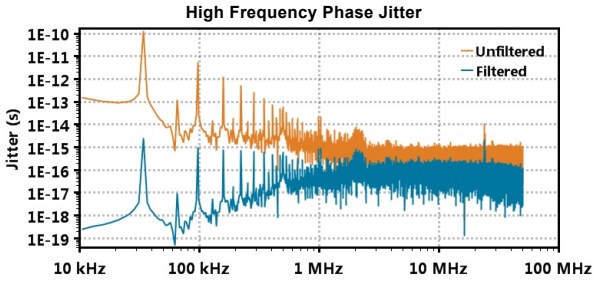


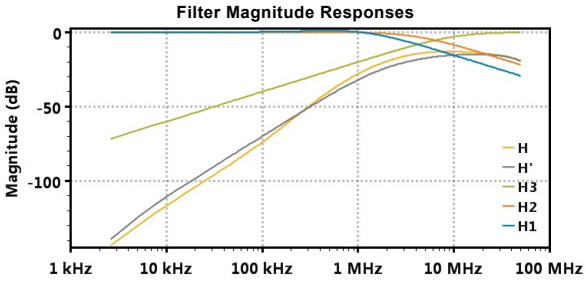


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
10	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 4 MHz (H')	1 dB (H) 0.01 dB (H')	4 MHz (H) 2 MHz (H')	0.01 dB (H) 1 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	686.253 fs (H)	PASS
Refclk LF RMS Jitter		283.897 fs (H')	N/A
Pk-pk Phase Jitter		2.120 ps (H)	N/A

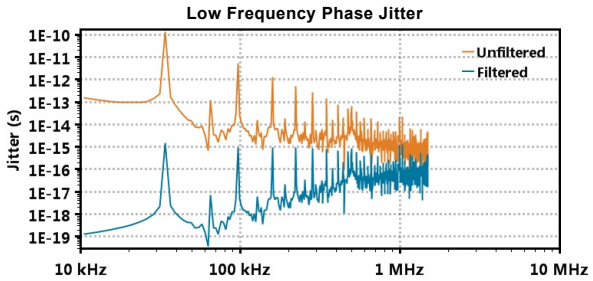


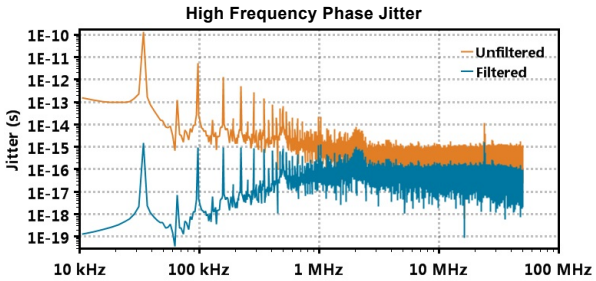


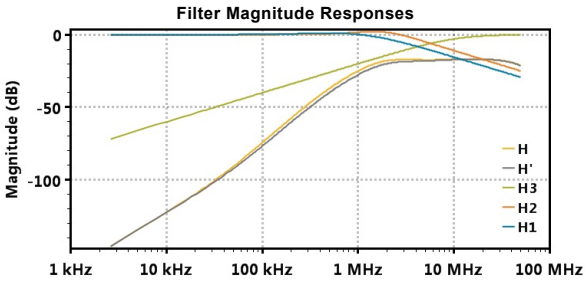


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
11	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 4 MHz (H')	1 dB (H) 2 dB (H')	4 MHz (H) 2 MHz (H')	2 dB (H) 1 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	538.269 fs (H)	PASS
Refclk LF RMS Jitter		205.061 fs (H)	N/A
Pk-pk Phase Jitter		1.999 ps (H)	N/A



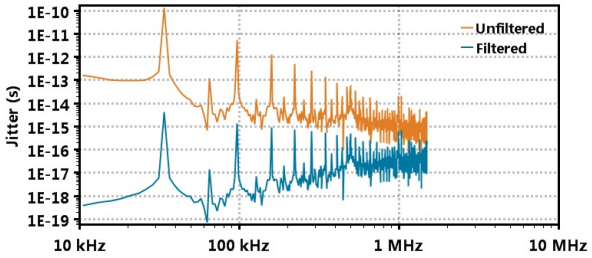




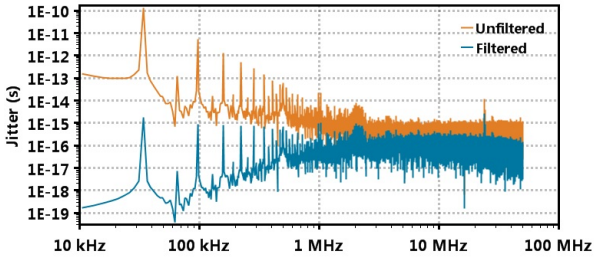
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
12	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 5 MHz (H')	1 dB (H) 0.01 dB (H')	5 MHz (H) 2 MHz (H')	0.01 dB (H) 1 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	817.681 fs (H)	PASS
Refclk LF RMS Jitter		248.243 fs (H')	N/A
Pk-pk Phase Jitter		2.515 ps (H)	N/A

Low Frequency Phase Jitter



High Frequency Phase Jitter



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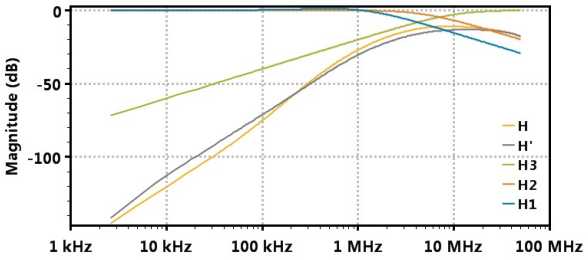
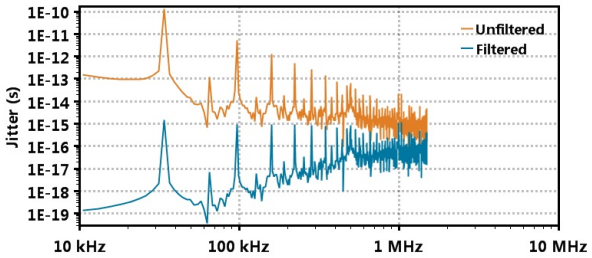


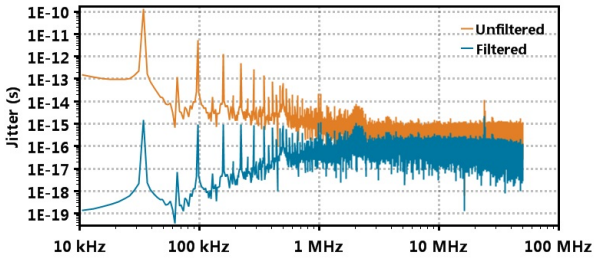
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
13	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 5 MHz (H')	1 dB (H) 1 dB (H')	5 MHz (H) 2 MHz (H')	1 dB (H) 1 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	729.810 fs (H)	PASS
Refclk LF RMS Jitter		196.188 fs (H)	N/A
Pk-pk Phase Jitter		2.400 ps (H)	N/A

Low Frequency Phase Jitter



High Frequency Phase Jitter



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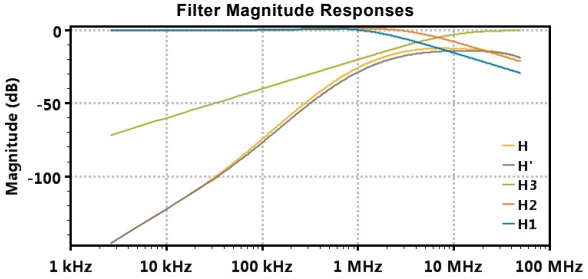
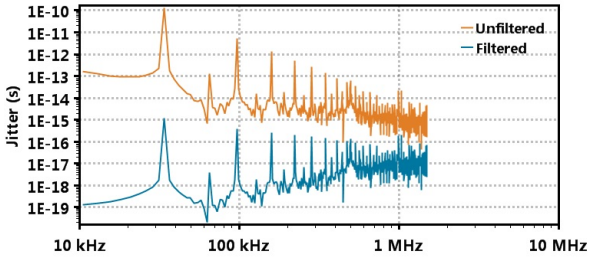


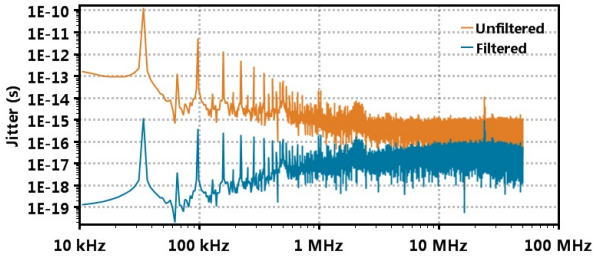
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
14	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz	2 dB	2 MHz	2 dB	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	275.875 fs	PASS
Refclk LF RMS Jitter		70.387 fs	N/A
Pk-pk Phase Jitter		727.611 fs	N/A

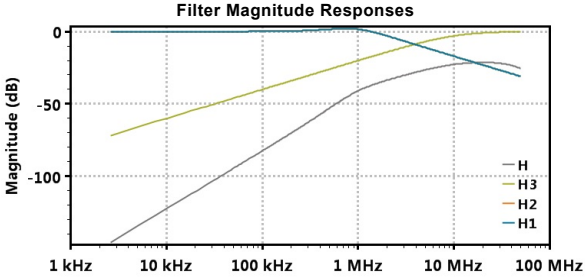
Low Frequency Phase Jitter



High Frequency Phase Jitter



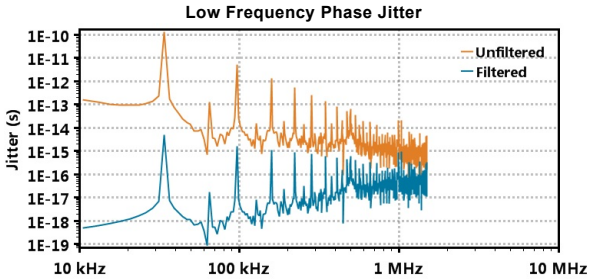
Filter Magnitude Responses



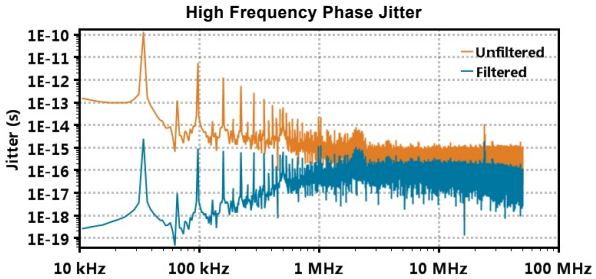
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
15	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 4 MHz (H')	2 dB (H) 0.01 dB (H')	4 MHz (H) 2 MHz (H')	0.01 dB (H) 2 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	701.616 fs (H)	PASS
Refclk LF RMS Jitter		300.770 fs (H')	N/A
Pk-pk Phase Jitter		2.320 ps (H)	N/A

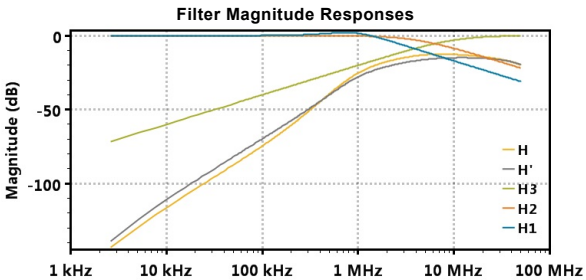
Low Frequency Phase Jitter



High Frequency Phase Jitter



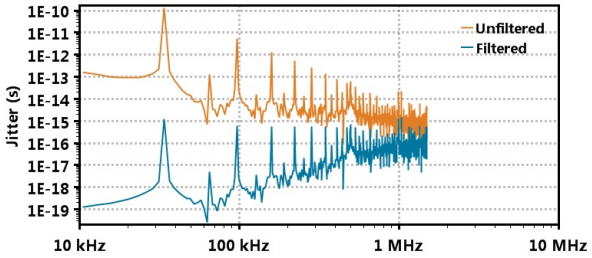
Filter Magnitude Responses



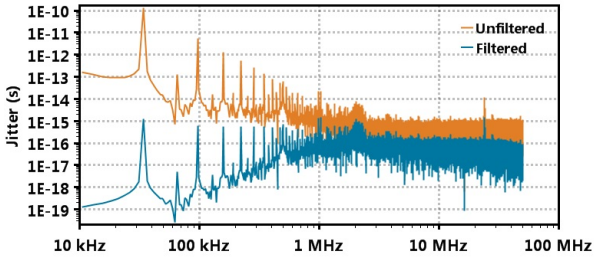
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
16	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 4 MHz (H')	2 dB (H) 2 dB (H')	4 MHz (H) 2 MHz (H')	2 dB (H) 2 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	548.885 fs (H)	PASS
Refclk LF RMS Jitter		194.734 fs (H)	N/A
Pk-pk Phase Jitter		2.193 ps (H)	N/A

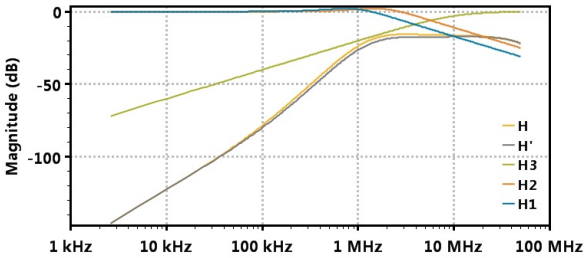
Low Frequency Phase Jitter



High Frequency Phase Jitter



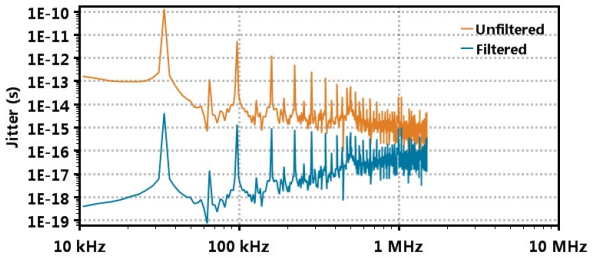
Filter Magnitude Responses



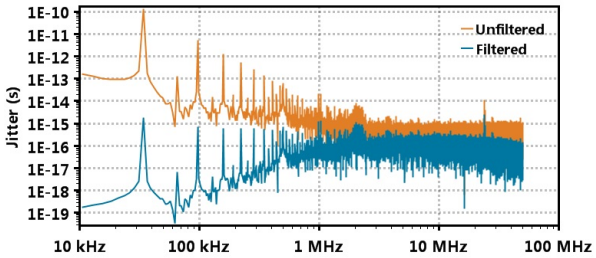
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
17	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 5 MHz (H')	2 dB (H) 0.01 dB (H')	5 MHz (H) 2 MHz (H')	0.01 dB (H) 2 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	831.406 fs (H)	PASS
Refclk LF RMS Jitter		265.042 fs (H')	N/A
Pk-pk Phase Jitter		2.711 ps (H)	N/A

Low Frequency Phase Jitter



High Frequency Phase Jitter



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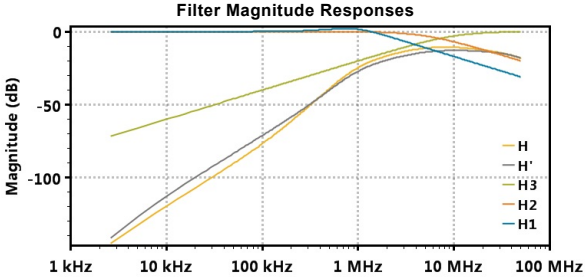
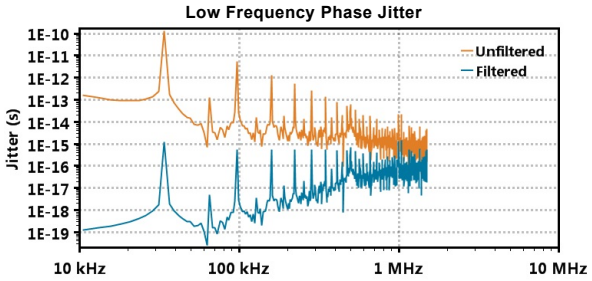
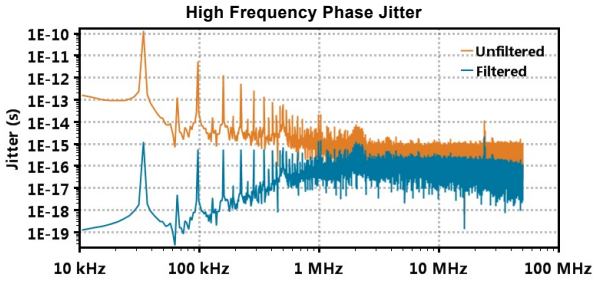
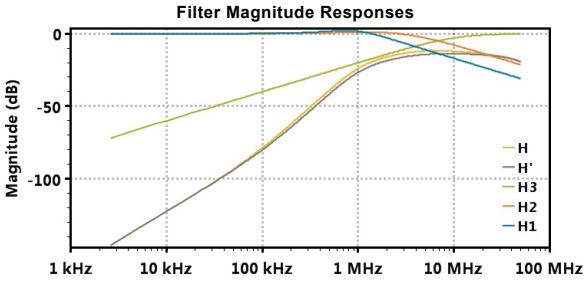


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
18	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 5 MHz (H')	2 dB (H) 1 dB (H')	5 MHz (H) 2 MHz (H')	1 dB (H) 2 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	742.901 fs (H)	PASS
Refclk LF RMS Jitter		189.212 fs (H)	N/A
Pk-pk Phase Jitter		2.574 ps (H)	N/A

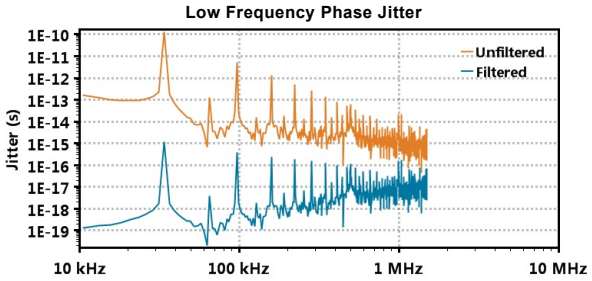


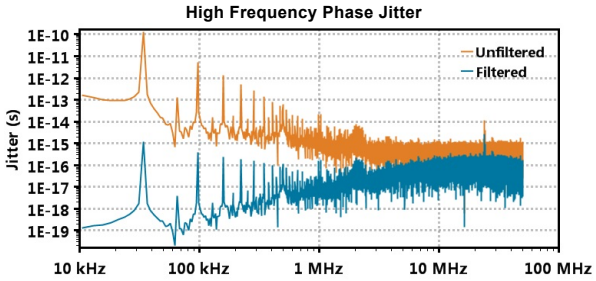


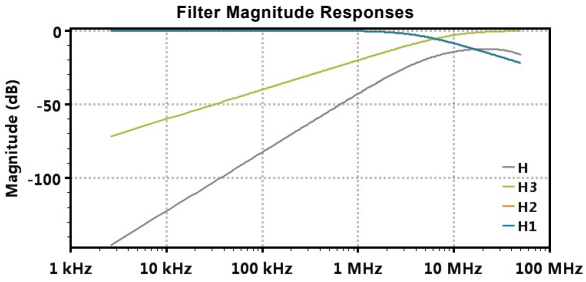


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
19	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	4 MHz	0.01 dB	4 MHz	0.01 dB	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	740.190 fs	PASS
Refclk LF RMS Jitter		68.725 fs	N/A
Pk-pk Phase Jitter		1.852 ps	N/A

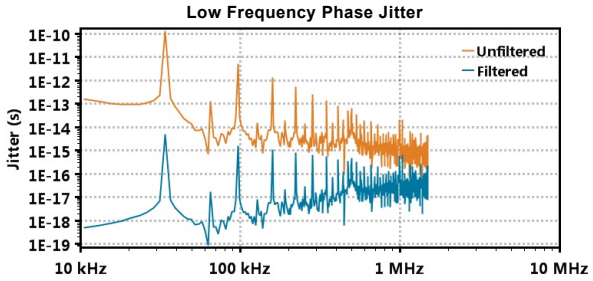


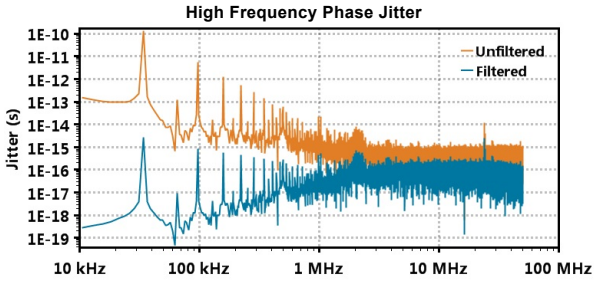


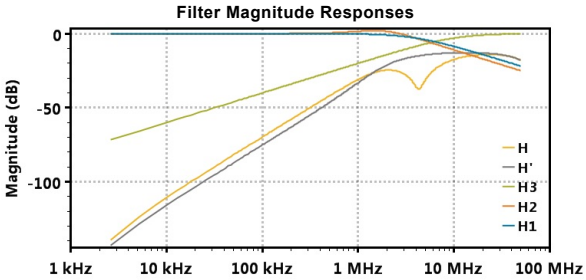


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
20	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	4 MHz (H) 4 MHz (H')	0.01 dB (H) 2 dB (H')	4 MHz (H) 4 MHz (H')	2 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	736.918 fs (H')	PASS
Refclk LF RMS Jitter		290.713 fs (H)	N/A
Pk-pk Phase Jitter		2.111 ps (H)	N/A

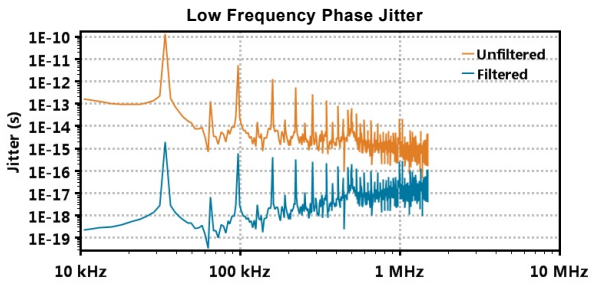


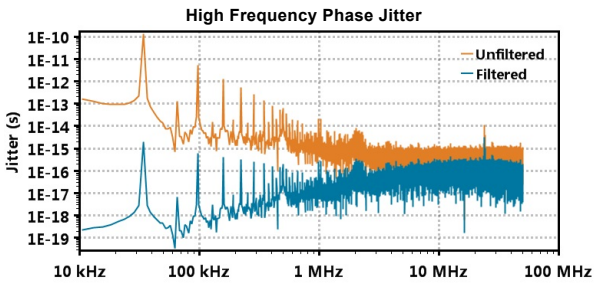


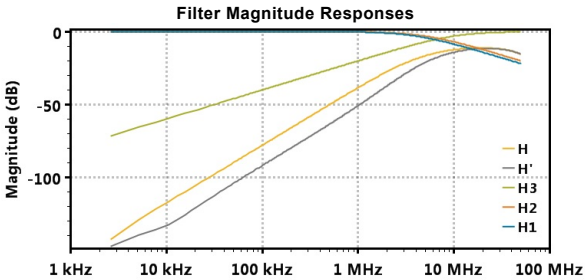


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
21	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	4 MHz (H) 5 MHz (H')	0.01 dB (H) 0.01 dB (H')	5 MHz (H) 4 MHz (H')	0.01 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	863.210 fs (H)	PASS
Refclk LF RMS Jitter		115.204 fs (H)	N/A
Pk-pk Phase Jitter		2.193 ps (H)	N/A



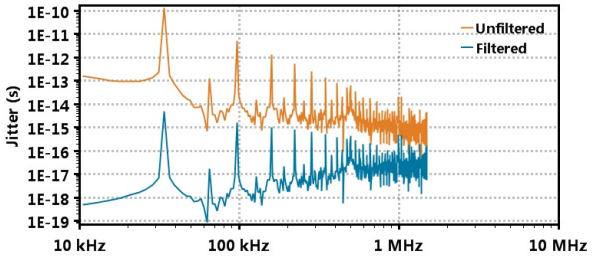




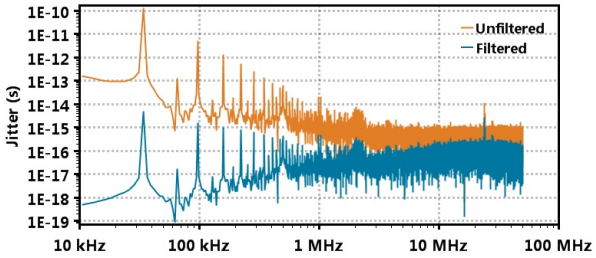
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
22	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	4 MHz (H) 5 MHz (H')	0.01 dB (H) 1 dB (H')	5 MHz (H) 4 MHz (H')	1 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	804.300 fs (H)	PASS
Refclk LF RMS Jitter		286.059 fs (H)	N/A
Pk-pk Phase Jitter		2.288 ps (H)	N/A

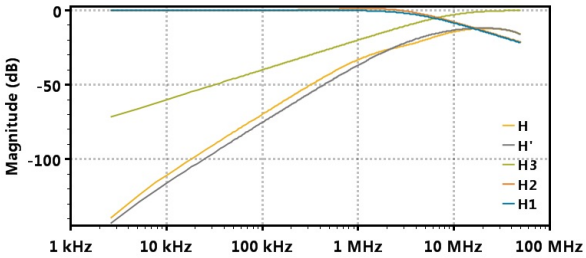
Low Frequency Phase Jitter



High Frequency Phase Jitter



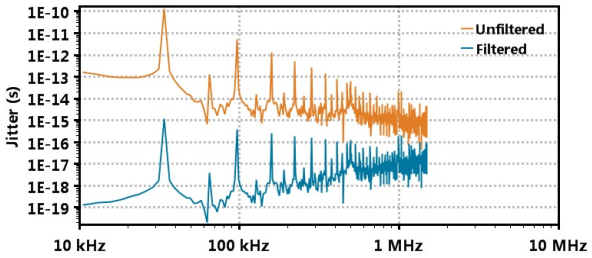
Filter Magnitude Responses



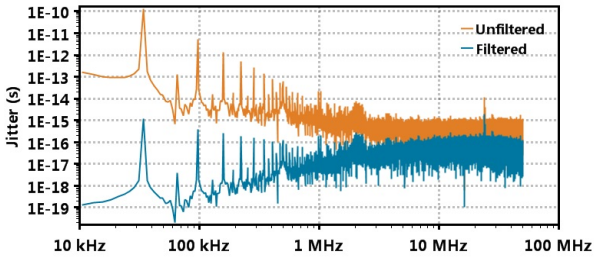
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
23	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	4 MHz	2 dB	4 MHz	2 dB	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	537.895 fs	PASS
Refclk LF RMS Jitter		70.233 fs	N/A
Pk-pk Phase Jitter		1.405 ps	N/A

Low Frequency Phase Jitter



High Frequency Phase Jitter



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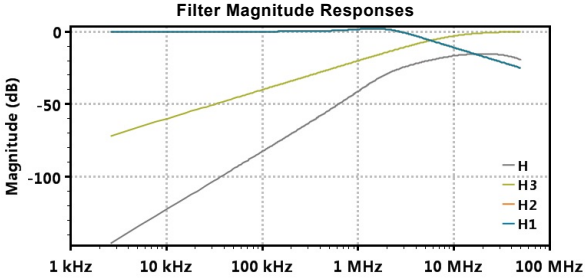
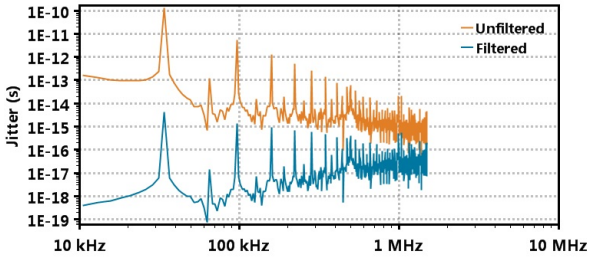


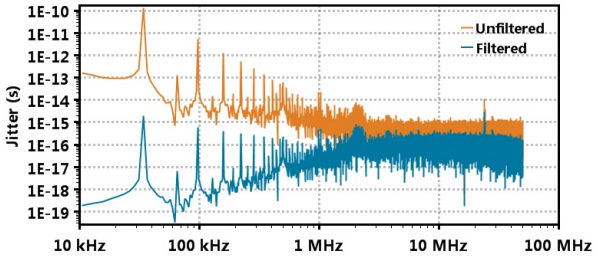
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
24	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	4 MHz (H) 5 MHz (H')	2 dB (H) 0.01 dB (H')	5 MHz (H) 4 MHz (H')	0.01 dB (H) 2 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	860.844 fs (H)	PASS
Refclk LF RMS Jitter		245.191 fs (H')	N/A
Pk-pk Phase Jitter		2.397 ps (H)	N/A

Low Frequency Phase Jitter



High Frequency Phase Jitter



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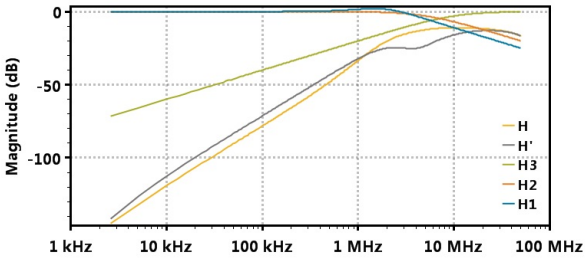
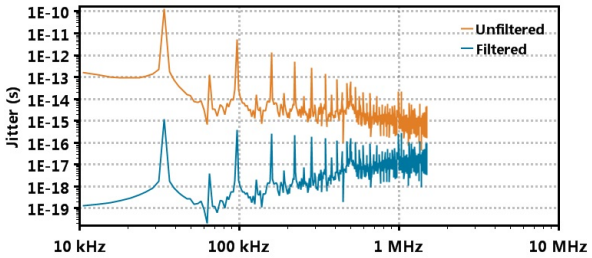


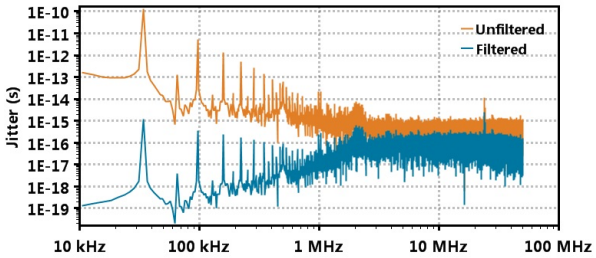
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
25	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	4 MHz (H) 5 MHz (H')	2 dB (H) 1 dB (H')	5 MHz (H) 4 MHz (H')	1 dB (H) 2 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	740.922 fs (H)	PASS
Refclk LF RMS Jitter		73.970 fs (H')	N/A
Pk-pk Phase Jitter		2.066 ps (H)	N/A

Low Frequency Phase Jitter



High Frequency Phase Jitter



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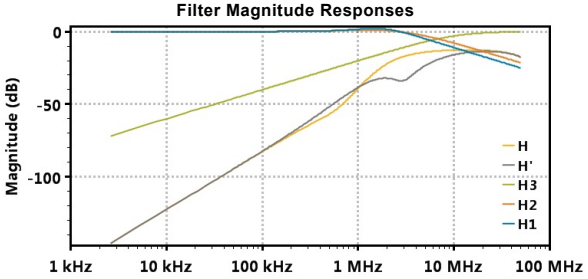
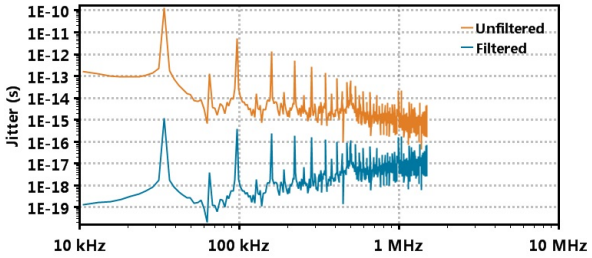


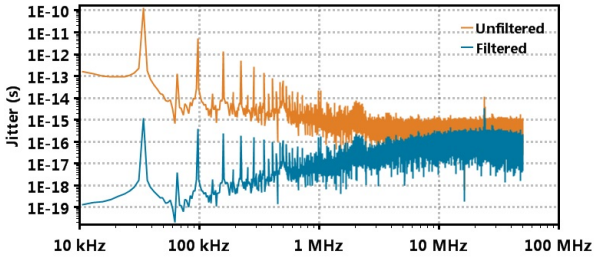
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
26	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	5 MHz	0.01 dB	5 MHz	0.01 dB	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	912.112 fs	PASS
Refclk LF RMS Jitter		68.797 fs	N/A
Pk-pk Phase Jitter		2.266 ps	N/A

Low Frequency Phase Jitter



High Frequency Phase Jitter



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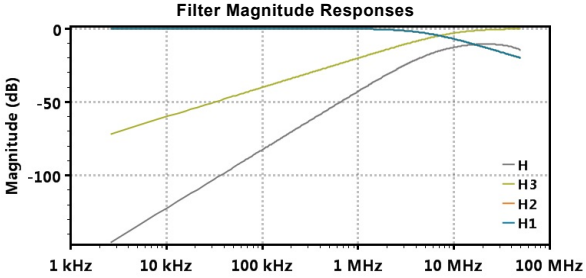
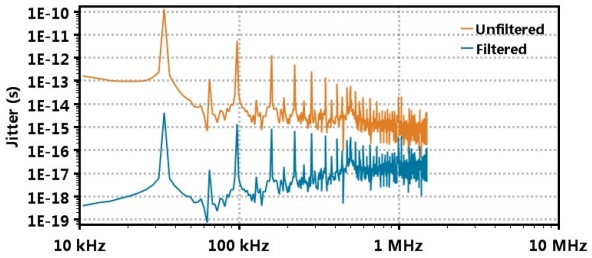


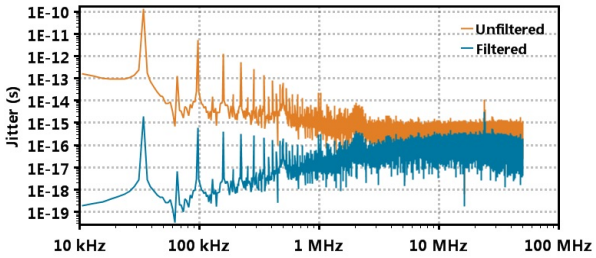
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
27	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	5 MHz (H) 5 MHz (H')	0.01 dB (H) 1 dB (H')	5 MHz (H) 5 MHz (H')	1 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	900.904 fs (H')	PASS
Refclk LF RMS Jitter		240.186 fs (H)	N/A
Pk-pk Phase Jitter		2.329 ps (H')	N/A

Low Frequency Phase Jitter



High Frequency Phase Jitter



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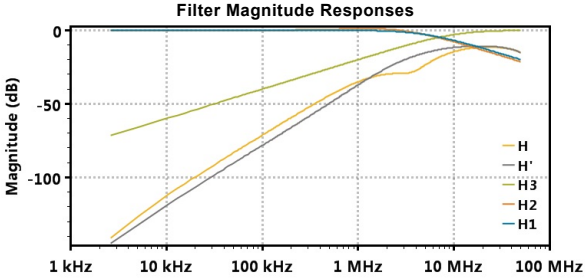
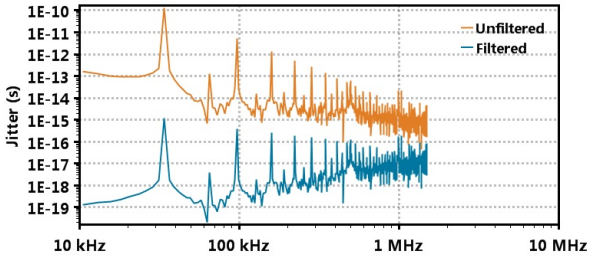


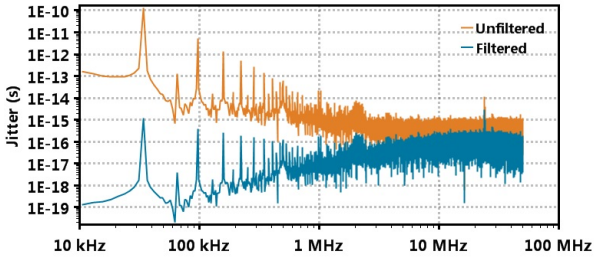
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
28	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	5 MHz	1 dB	5 MHz	1 dB	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	788.493 fs	PASS
Refclk LF RMS Jitter		69.684 fs	N/A
Pk-pk Phase Jitter		1.992 ps	N/A

Low Frequency Phase Jitter



High Frequency Phase Jitter



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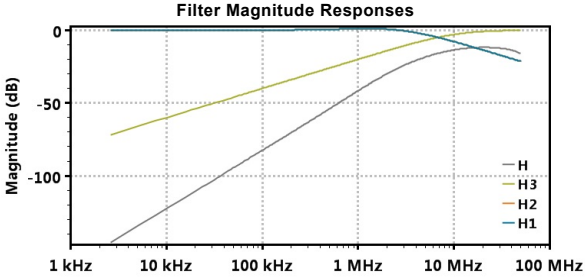

Transfer Function Constants

#	Class	Architecture	Specs	H1 BW	H1 Peaking	H1 Omega	H1 Zeta	H2 BW	H2 Peaking	H2 Omega	H2 Zeta	H3 BW	H3 Peaking	H3 Omega	H3 Zeta	Delay
1	GEN3	Common Clock	3.1 4.0	2 MHz	0.01 dB	4.48227E+5	1.40000E+1	2 MHz	0.01 dB	4.48227E+5	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
2	GEN3	Common Clock	3.1 4.0	2 MHz	0.01 dB	4.48227E+5	1.40000E+1	2 MHz	1 dB	4.61180E+6	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns
3	GEN3	Common Clock	3.1 4.0	2 MHz	0.01 dB	4.48227E+5	1.40000E+1	2 MHz	2 dB	6.01757E+6	7.30000E-1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
4	GEN3	Common Clock	3.1 4.0	2 MHz	0.01 dB	4.48227E+5	1.40000E+1	4 MHz	0.01 dB	8.96454E+5	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
5	GEN3	Common Clock	3.1 4.0	2 MHz	0.01 dB	4.48227E+5	1.40000E+1	4 MHz	2 dB	1.20351E+7	7.30000E-1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
6	GEN3	Common Clock	3.1 4.0	2 MHz	0.01 dB	4.48227E+5	1.40000E+1	5 MHz	0.01 dB	1.12057E+6	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
7	GEN3	Common Clock	3.1 4.0	2 MHz	0.01 dB	4.48227E+5	1.40000E+1	5 MHz	1 dB	1.15295E+7	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns
8	GEN3	Common Clock	3.1 4.0	2 MHz	1 dB	4.61180E+6	1.15000E+0	2 MHz	1 dB	4.61180E+6	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns
9	GEN3	Common Clock	3.1 4.0	2 MHz	1 dB	4.61180E+6	1.15000E+0	2 MHz	2 dB	6.01757E+6	7.30000E-1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
10	GEN3	Common Clock	3.1 4.0	2 MHz	1 dB	4.61180E+6	1.15000E+0	4 MHz	0.01 dB	8.96454E+5	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
11	GEN3	Common Clock	3.1 4.0	2 MHz	1 dB	4.61180E+6	1.15000E+0	4 MHz	2 dB	1.20351E+7	7.30000E-1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
12	GEN3	Common Clock	3.1 4.0	2 MHz	1 dB	4.61180E+6	1.15000E+0	5 MHz	0.01 dB	1.12057E+6	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
13	GEN3	Common Clock	3.1 4.0	2 MHz	1 dB	4.61180E+6	1.15000E+0	5 MHz	1 dB	1.15295E+7	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns
14	GEN3	Common Clock	3.1 4.0	2 MHz	2 dB	6.01757E+6	7.30000E-1	2 MHz	2 dB	6.01757E+6	7.30000E-1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
15	GEN3	Common Clock	3.1 4.0	2 MHz	2 dB	6.01757E+6	7.30000E-1	4 MHz	0.01 dB	8.96454E+5	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
16	GEN3	Common Clock	3.1 4.0	2 MHz	2 dB	6.01757E+6	7.30000E-1	4 MHz	2 dB	1.20351E+7	7.30000E-1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
17	GEN3	Common Clock	3.1 4.0	2 MHz	2 dB	6.01757E+6	7.30000E-1	5 MHz	0.01 dB	1.12057E+6	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
18	GEN3	Common Clock	3.1 4.0	2 MHz	2 dB	6.01757E+6	7.30000E-1	5 MHz	1 dB	1.15295E+7	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns
19	GEN3	Common Clock	3.1 4.0	4 MHz	0.01 dB	8.96454E+5	1.40000E+1	4 MHz	0.01 dB	8.96454E+5	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
20	GEN3	Common Clock	3.1 4.0	4 MHz	0.01 dB	8.96454E+5	1.40000E+1	4 MHz	2 dB	1.20351E+7	7.30000E-1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
21	GEN3	Common Clock	3.1 4.0	4 MHz	0.01 dB	8.96454E+5	1.40000E+1	5 MHz	0.01 dB	1.12057E+6	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
22	GEN3	Common Clock	3.1 4.0	4 MHz	0.01 dB	8.96454E+5	1.40000E+1	5 MHz	1 dB	1.15295E+7	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns
23	GEN3	Common Clock	3.1 4.0	4 MHz	2 dB	1.20351E+7	7.30000E-1	4 MHz	2 dB	1.20351E+7	7.30000E-1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
24	GEN3	Common Clock	3.1 4.0	4 MHz	2 dB	1.20351E+7	7.30000E-1	5 MHz	0.01 dB	1.12057E+6	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
25	GEN3	Common Clock	3.1 4.0	4 MHz	2 dB	1.20351E+7	7.30000E-1	5 MHz	1 dB	1.15295E+7	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns
26	GEN3	Common Clock	3.1 4.0	5 MHz	0.01 dB	1.12057E+6	1.40000E+1	5 MHz	0.01 dB	1.12057E+6	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
27	GEN3	Common Clock	3.1 4.0	5 MHz	0.01 dB	1.12057E+6	1.40000E+1	5 MHz	1 dB	1.15295E+7	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns
28	GEN3	Common Clock	3.1 4.0	5 MHz	1 dB	1.15295E+7	1.15000E+0	5 MHz	1 dB	1.15295E+7	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns