Data File Overview

File Type	Time Domain Differential
Waveform File	E:\Project\5 SAK4\PCIE CLOCK\clock jitter test\U.2 2.wfm
Waveform File Creation Date	2019-11-15 13:38:21 GMT+08:00
Edge Filtering	On
Clock Frequency	99.768 MHz
SSC Frequency	31.246 kHz
Number of Edges	19,150
Sample Interval	40.000 ps
Selected Threshold Voltage	-140.936 mV (via auto-threshold search)
Warning	Data file should contain 160,000 or more edges

Filter Compliance Summary

Class	Data Rate	Architecture	Specs	Max HF RMS	Max HLF RMS	Max Pk-Pk	Compliance Summary
GEN3	8 Gb/s	Common Clock	3.1 4.0	750.45 fs	583.57 fs	2.44 ps	All PASS

Jitter Summary

#	Class	Data Rate	Arch (1)	Specs	PLL1 BW	PLL1 Peak	PLL2 BW	PLL2 Peak	CDR BW	CDR Peak	Specification			Analysis Result			Compliance Result
											HF RMS	LF RMS	Pk-Pk	HF RMS	LF RMS	Pk-Pk	
1	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz	0.01 dB	2 MHz	0.01 dB	10 MHz	0 dB	1 ps			267.55 fs	76.81 fs	627.43 fs	PASS
2	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 2 MHz (H')	0.01 dB (H) 1 dB (H')	2 MHz (H) 2 MHz (H')	1 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			603.89 fs (H)	557.93 fs (H)	1.74 ps (H)	PASS
3	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 2 MHz (H')	0.01 dB (H) 2 dB (H')	2 MHz (H) 2 MHz (H')	2 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			613.34 fs (H)	574.01 fs (H)	1.89 ps (H)	PASS
4	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 4 MHz (H')	0.01 dB (H) 0.01 dB (H')	4 MHz (H) 2 MHz (H')	0.01 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			557.12 fs (H)	333.61 fs (H)	1.63 ps (H)	PASS
5	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 4 MHz (H')	0.01 dB (H) 2 dB (H')	4 MHz (H) 2 MHz (H')	2 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			676.27 fs (H)	583.57 fs (H)	2.31 ps (H)	PASS
6	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 5 MHz (H')	0.01 dB (H) 0.01 dB (H')	5 MHz (H) 2 MHz (H')	0.01 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			664.41 fs (H)	385.75 fs (H)	1.93 ps (H)	PASS
7	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 5 MHz (H')	0.01 dB (H) 1 dB (H')	5 MHz (H) 2 MHz (H')	1 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			750.45 fs (H)	579.97 fs (H)	2.44 ps (H)	PASS
8	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz	1 dB	2 MHz	1 dB	10 MHz	0 dB	1 ps			231.51 fs	77.97 fs	554.77 fs	PASS
9	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 2 MHz (H')	1 dB (H) 2 dB (H')	2 MHz (H) 2 MHz (H')	2 dB (H) 1 dB (H')	10 MHz	0 dB	1 ps			233.96 fs (H')	119.31 fs (H)	711.54 fs (H)	PASS
10	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 4 MHz (H')	1 dB (H) 0.01 dB (H')	4 MHz (H) 2 MHz (H')	0.01 dB (H) 1 dB (H')	10 MHz	0 dB	1 ps			504.09 fs (H')	320.47 fs (H')	1.51 ps (H)	PASS
11	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 4 MHz (H')	1 dB (H) 2 dB (H')	4 MHz (H) 2 MHz (H')	2 dB (H) 1 dB (H')	10 MHz	0 dB	1 ps			405.56 fs (H)	207.35 fs (H)	1.50 ps (H)	PASS
12	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 5 MHz (H')	1 dB (H) 0.01 dB (H')	5 MHz (H) 2 MHz (H')	0.01 dB (H) 1 dB (H')	10 MHz	0 dB	1 ps			578.48 fs (H)	277.58 fs (H')	1.62 ps (H)	PASS
13	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 5 MHz (H')	1 dB (H) 1 dB (H')	5 MHz (H) 2 MHz (H')	1 dB (H) 1 dB (H')	10 MHz	0 dB	1 ps			525.16 fs (H)	199.23 fs (H)	1.66 ps (H)	PASS
14	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz	2 dB	2 MHz	2 dB	10 MHz	0 dB	1 ps			198.08 fs	78.60 fs	487.03 fs	PASS
15	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 4 MHz (H')	2 dB (H) 0.01 dB (H')	4 MHz (H) 2 MHz (H')	0.01 dB (H) 2 dB (H')	10 MHz	0 dB	1 ps			517.36 fs (H')	335.34 fs (H')	1.67 ps (H')	PASS
16	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 4 MHz (H')	2 dB (H) 2 dB (H')	4 MHz (H) 2 MHz (H')	2 dB (H) 2 dB (H')	10 MHz	0 dB	1 ps			410.41 fs (H)	191.58 fs (H)	1.44 ps (H)	PASS
17	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 5 MHz (H')	2 dB (H) 0.01 dB (H')	5 MHz (H) 2 MHz (H')	0.01 dB (H) 2 dB (H')	10 MHz	0 dB	1 ps			591.62 fs (H)	292.03 fs (H')	1.70 ps (H')	PASS
18	GEN3	8 Gb/s	CC	3.1 4.0	2 MHz (H) 5 MHz (H')	2 dB (H) 1 dB (H')	5 MHz (H) 2 MHz (H')	1 dB (H) 2 dB (H')	10 MHz	0 dB	1 ps			533.36 fs (H)	186.39 fs (H)	1.62 ps (H)	PASS
19	GEN3	8 Gb/s	CC	3.1 4.0	4 MHz	0.01 dB	4 MHz	0.01 dB	10 MHz	0 dB	1 ps			507.09 fs	77.22 fs	1.19 ps	PASS
20	GEN3	8 Gb/s	CC	3.1 4.0	4 MHz (H) 4 MHz (H')	0.01 dB (H) 2 dB (H')	4 MHz (H) 4 MHz (H')	2 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			525.00 fs (H)	327.71 fs (H)	1.49 ps (H)	PASS

Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

#	Class	Data Rate	Arch (1)	Specs	PLL1 BW	PLL1 Peak	PLL2 BW	PLL2 Peak	CDR BW	CDR Peak	Specification			Analysis Result			Compliance Result
											HF RMS	LF RMS	Pk-Pk	HF RMS	LF RMS	Pk-Pk	
21	GEN3	8 Gb/s	CC	3.1 4.0	4 MHz (H) 5 MHz (H')	0.01 dB (H) 0.01 dB (H')	5 MHz (H) 4 MHz (H')	0.01 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			596.16 fs (H)	129.40 fs (H)	1.39 ps (H)	PASS
22	GEN3	8 Gb/s	CC	3.1 4.0	4 MHz (H) 5 MHz (H')	0.01 dB (H) 1 dB (H')	5 MHz (H) 4 MHz (H')	1 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			605.72 fs (H)	323.83 fs (H)	1.64 ps (H)	PASS
23	GEN3	8 Gb/s	CC	3.1 4.0	4 MHz	2 dB	4 MHz	2 dB	10 MHz	0 dB	1 ps			371.60 fs	78.43 fs	851.33 fs	PASS
24	GEN3	8 Gb/s	CC	3.1 4.0	4 MHz (H) 5 MHz (H')	2 dB (H) 0.01 dB (H')	5 MHz (H) 4 MHz (H')	0.01 dB (H) 2 dB (H')	10 MHz	0 dB	1 ps			598.04 fs (H)	276.33 fs (H')	1.43 ps (H')	PASS
25	GEN3	8 Gb/s	CC	3.1 4.0	4 MHz (H) 5 MHz (H')	2 dB (H) 1 dB (H')	5 MHz (H) 4 MHz (H')	1 dB (H) 2 dB (H')	10 MHz	0 dB	1 ps			510.47 fs (H)	81.61 fs (H')	1.11 ps (H)	PASS
26	GEN3	8 Gb/s	CC	3.1 4.0	5 MHz	0.01 dB	5 MHz	0.01 dB	10 MHz	0 dB	1 ps			623.23 fs	77.28 fs	1.46 ps	PASS
27	GEN3	8 Gb/s	CC	3.1 4.0	5 MHz (H) 5 MHz (H')	0.01 dB (H) 1 dB (H')	5 MHz (H) 5 MHz (H')	1 dB (H) 0.01 dB (H')	10 MHz	0 dB	1 ps			621.17 fs (H')	272.17 fs (H)	1.61 ps (H)	PASS
28	GEN3	8 Gb/s	CC	3.1 4.0	5 MHz	1 dB	5 MHz	1 dB	10 MHz	0 dB	1 ps			539.84 fs	77.99 fs	1.26 ps	PASS

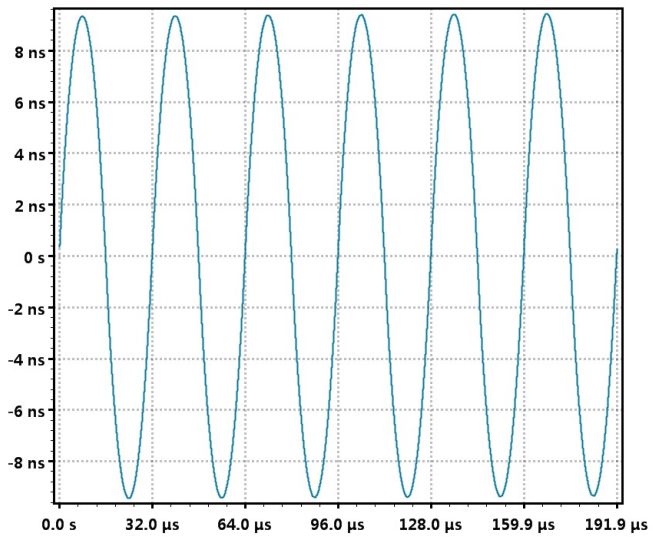
(1) CC: Common Clock; DC: Data Clock; SRNS: Separate Clock SRNS; SRIS: Separate Clock SRIS

(2) Spread Spectrum Clocking (SSC) separation is intended to remove the energy associated with the spread spectrum (30KHz-33KHz) in the low frequency range (0.01-1.5MHz) specified by the PCI-Express Base Specification in order to define separate low frequency Rj and Dj components.

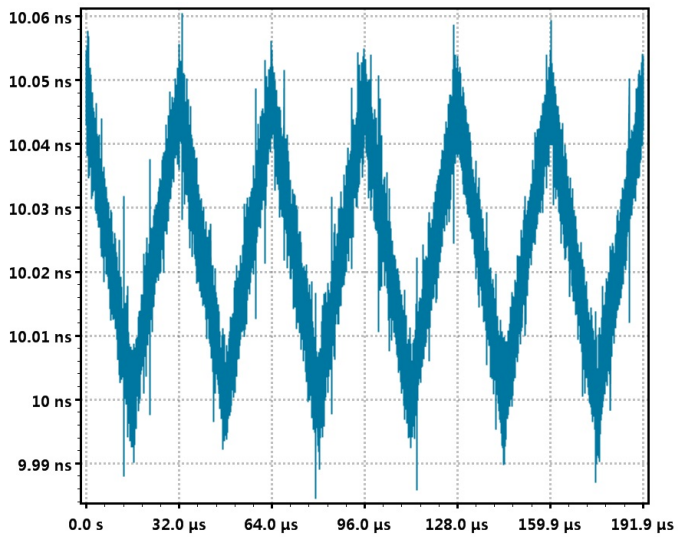
Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

Waveform Analysis

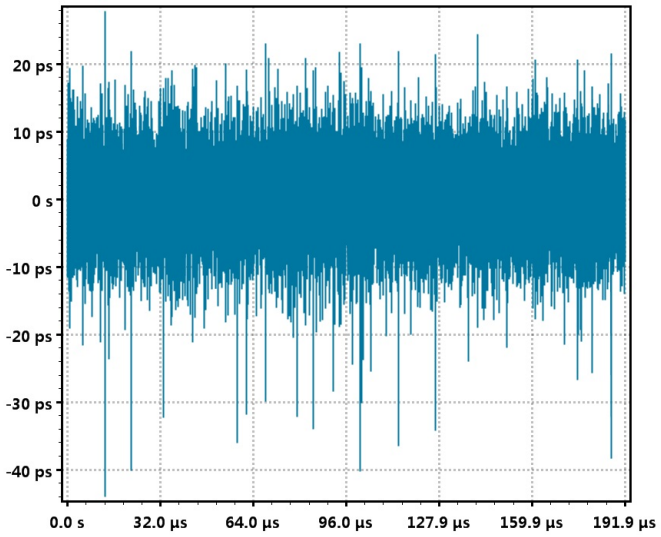
Time Interval Error



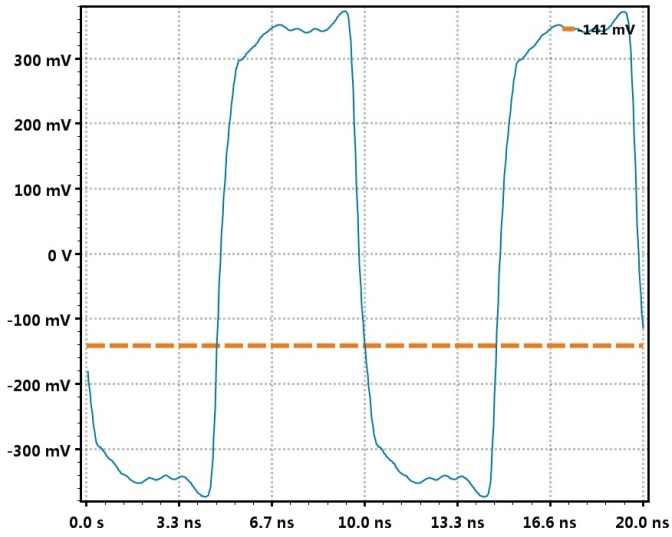
Period



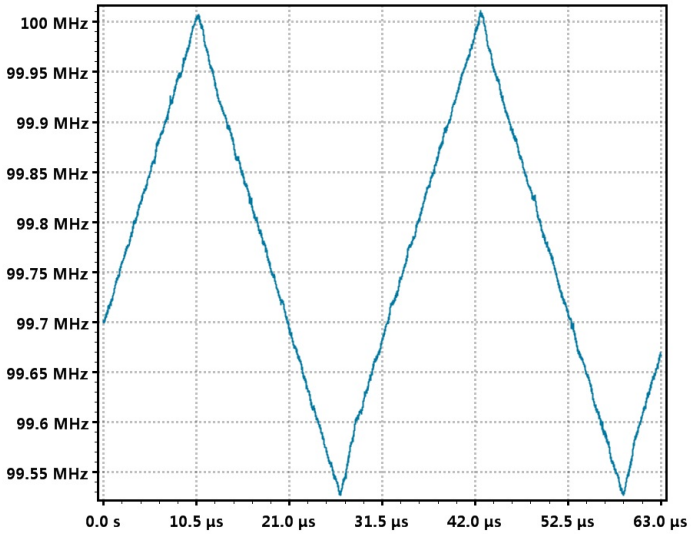
Cycle-to-Cycle



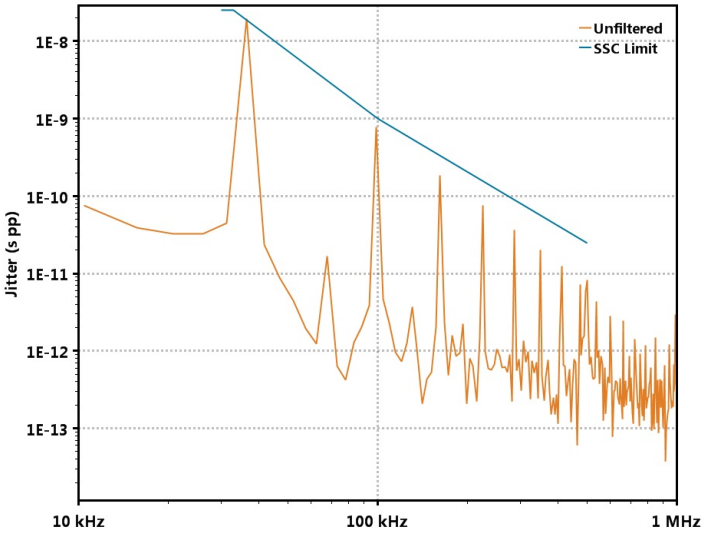
Differential Clock Signal



Spread-Spectrum Clocking Profile



Spread Spectrum Phase Jitter



Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

Reference Clock AC Specifications

Symbol	Parameter	Specification		Analysis Result			Compliance Result
		Min	Max	Min	Max	Avg	
Rising Edge Rate	Rising Edge Rate	0.6 V/ns	4 V/ns	0.00 V/ns	1.14 V/ns	0.00 V/ns	FAIL
Falling Edge Rate	Falling Edge Rate	0.6 V/ns	4 V/ns	0.00 V/ns	0.51 V/ns	0.00 V/ns	FAIL
V_{IH}	Differential Input High Voltage	150 mV		331.07 mV	355.29 mV	343.47 mV	PASS
V_{IL}	Differential Input Low Voltage		-150 mV	-356.47 mV	-332.05 mV	-344.81 mV	PASS
V_{RB}	Ring-Back Voltage		200 mV	N/A	730.37 mV	716.76 mV	FAIL
V_{OVS}	Overshoot Voltage relative to V_{IH}		300 mV	17.614 mV	42.408 mV	29.060 mV	PASS
V_{UDS}	Undershoot Voltage relative to V_{IL}		300 mV	16.738 mV	42.288 mV	28.294 mV	PASS
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300 ppm	2,800 ppm	N/A	N/A	2,316 ppm	PASS
$T_{PERIOD\ ABS}$	Absolute Period (including Jitter and Spread Spectrum modulation)	9.847 ns	10.203 ns	9.984 ns	10.060 ns	10.023 ns	PASS
$T_{CCJITTER}$	Cycle to Cycle Jitter		150 ps	0.00 s	43.97 ps	4.59 ps	PASS
Duty Cycle	Duty Cycle	40 %	60 %	52.4 %	53.4 %	52.9 %	PASS
SSC Parameters							
F_{REFCLK}	Refclk Frequency		100.03 MHz	N/A	N/A	100.01 MHz	PASS
F_{SSC}	SSC frequency range	30 kHz	33 kHz	N/A	N/A	31.25 kHz	PASS
$T_{SSC-FREQ-DEVIATION}$	SSC deviation	-0.5 %	0 %	N/A	N/A	-0.48 %	PASS
$T_{SSC-MAX-FREQ-SLEW}$	Max SSC df/dt		1,250 ppm/us	N/A	N/A	536 ppm/us	PASS

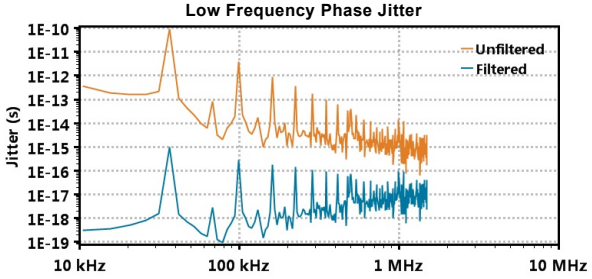
Detailed Jitter Reports

In the pages that follow, jitter response is analyzed for each selected standard, architecture and filter parameter combination.

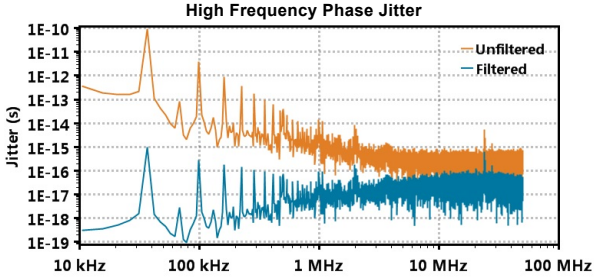
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
1	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz	0.01 dB	2 MHz	0.01 dB	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	267.552 fs	PASS
Refclk LF RMS Jitter		76.814 fs	N/A
Pk-pk Phase Jitter		627.429 fs	N/A

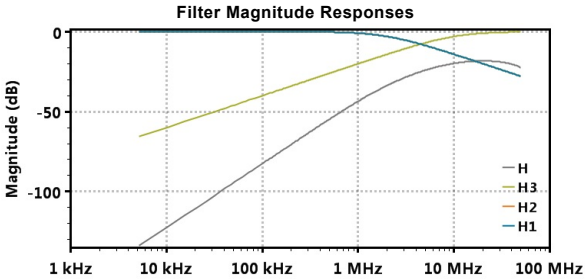
Low Frequency Phase Jitter



High Frequency Phase Jitter



Filter Magnitude Responses

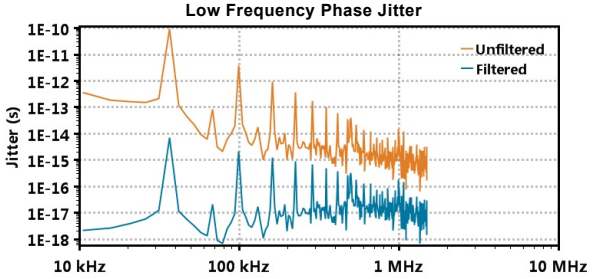


Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

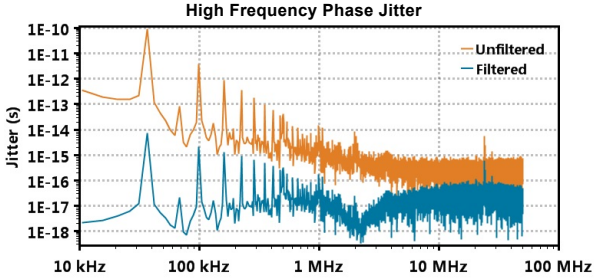
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
2	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 2 MHz (H')	0.01 dB (H) 1 dB (H')	2 MHz (H) 2 MHz (H')	1 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	603.887 fs (H)	PASS
Refclk LF RMS Jitter		557.928 fs (H)	N/A
Pk-pk Phase Jitter		1.738 ps (H)	N/A

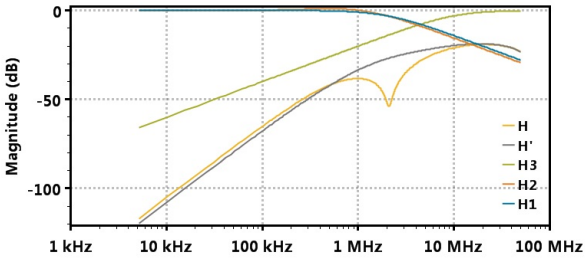
Low Frequency Phase Jitter



High Frequency Phase Jitter



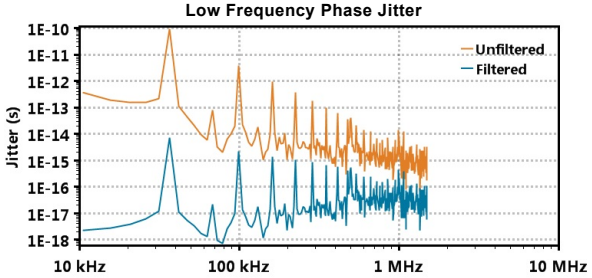
Filter Magnitude Responses



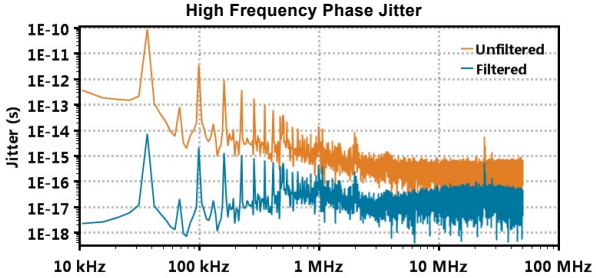
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
3	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 2 MHz (H')	0.01 dB (H) 2 dB (H')	2 MHz (H) 2 MHz (H')	2 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	613.337 fs (H)	PASS
Refclk LF RMS Jitter		574.010 fs (H)	N/A
Pk-pk Phase Jitter		1.892 ps (H)	N/A

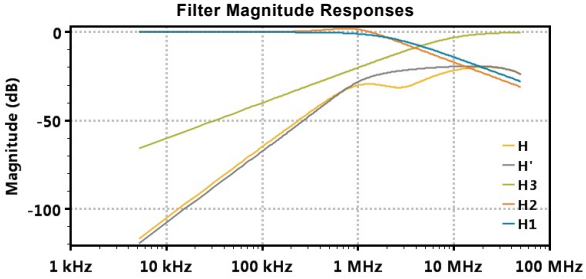
Low Frequency Phase Jitter



High Frequency Phase Jitter



Filter Magnitude Responses

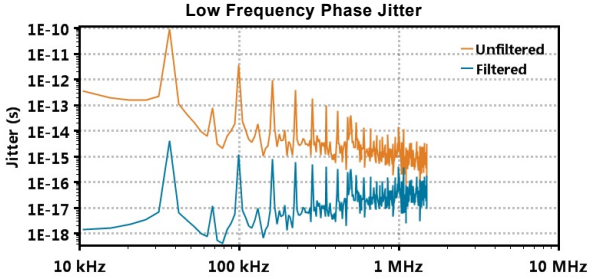


Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

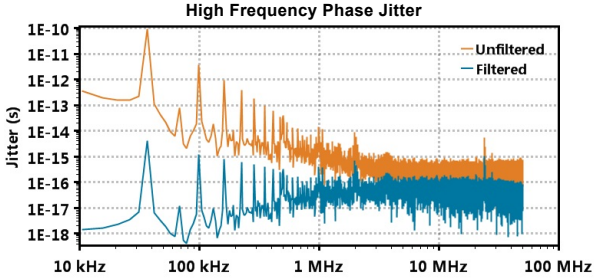
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
4	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 4 MHz (H')	0.01 dB (H) 0.01 dB (H')	4 MHz (H) 2 MHz (H')	0.01 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	557.124 fs (H)	PASS
Refclk LF RMS Jitter		333.611 fs (H)	N/A
Pk-pk Phase Jitter		1.631 ps (H)	N/A

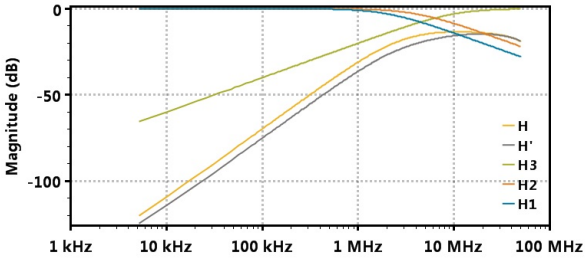
Low Frequency Phase Jitter



High Frequency Phase Jitter



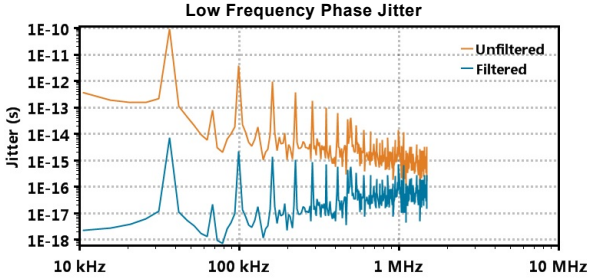
Filter Magnitude Responses



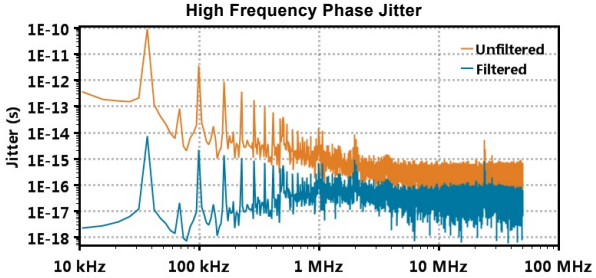
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
5	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 4 MHz (H')	0.01 dB (H) 2 dB (H')	4 MHz (H) 2 MHz (H')	2 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	676.275 fs (H)	PASS
Refclk LF RMS Jitter		583.574 fs (H)	N/A
Pk-pk Phase Jitter		2.308 ps (H)	N/A

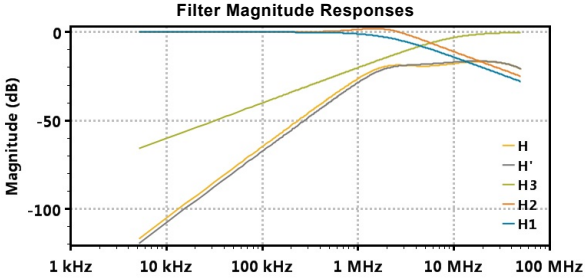
Low Frequency Phase Jitter



High Frequency Phase Jitter



Filter Magnitude Responses

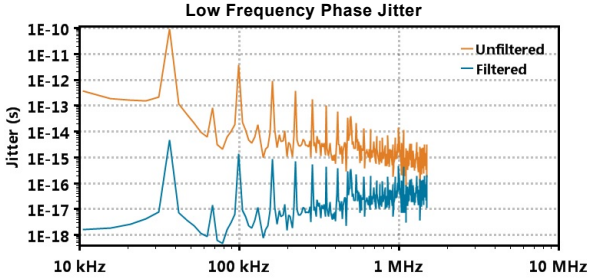


Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

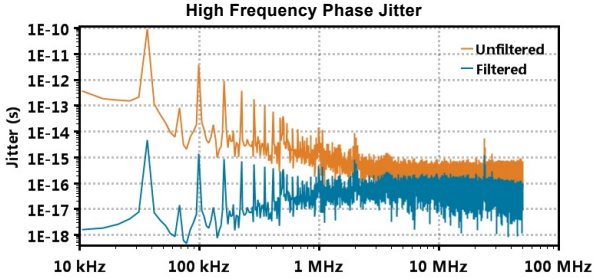
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
6	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 5 MHz (H')	0.01 dB (H) 0.01 dB (H')	5 MHz (H) 2 MHz (H')	0.01 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	664.415 fs (H)	PASS
Refclk LF RMS Jitter		385.749 fs (H)	N/A
Pk-pk Phase Jitter		1.928 ps (H)	N/A

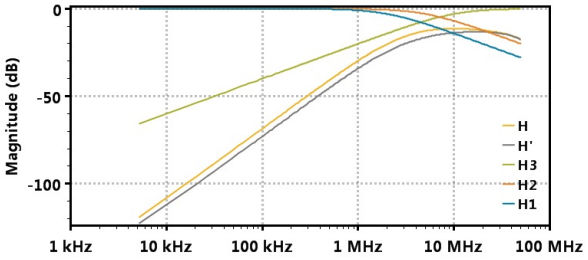
Low Frequency Phase Jitter



High Frequency Phase Jitter



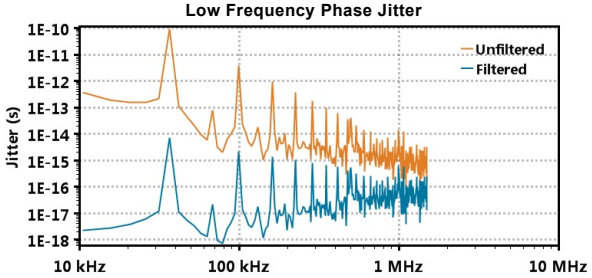
Filter Magnitude Responses



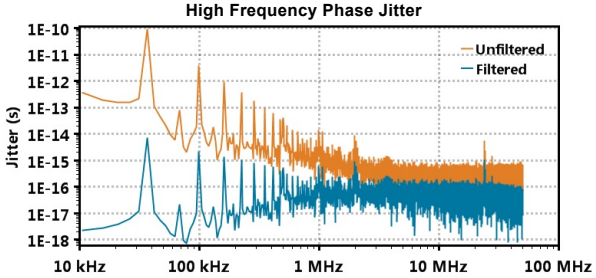
#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
7	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 5 MHz (H')	0.01 dB (H) 1 dB (H')	5 MHz (H) 2 MHz (H')	1 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	750.445 fs (H)	PASS
Refclk LF RMS Jitter		579.968 fs (H)	N/A
Pk-pk Phase Jitter		2.438 ps (H)	N/A

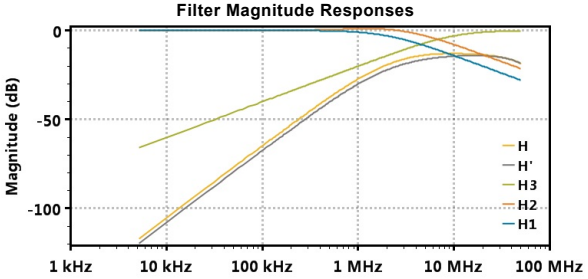
Low Frequency Phase Jitter



High Frequency Phase Jitter



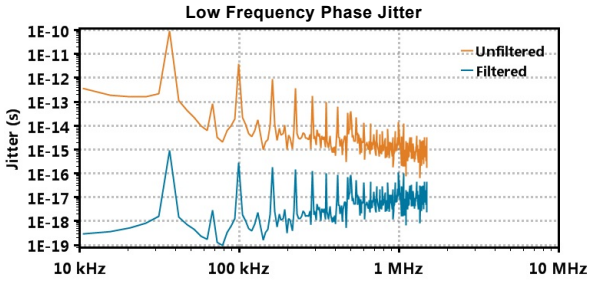
Filter Magnitude Responses

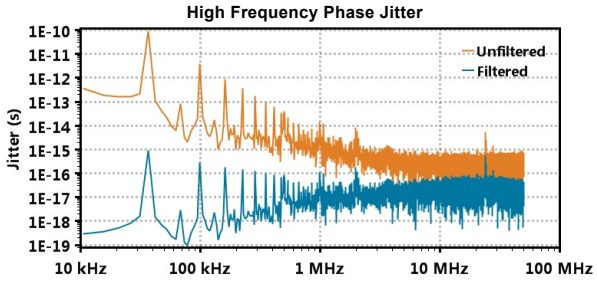


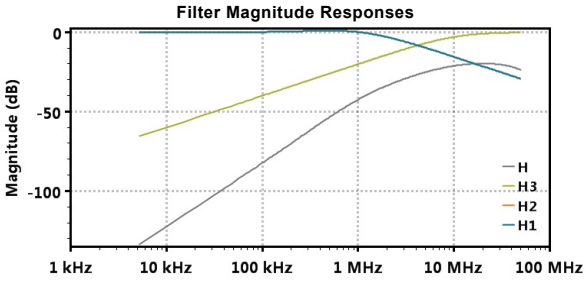
Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
8	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz	1 dB	2 MHz	1 dB	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	231.513 fs	PASS
Refclk LF RMS Jitter		77.972 fs	N/A
Pk-pk Phase Jitter		554.766 fs	N/A

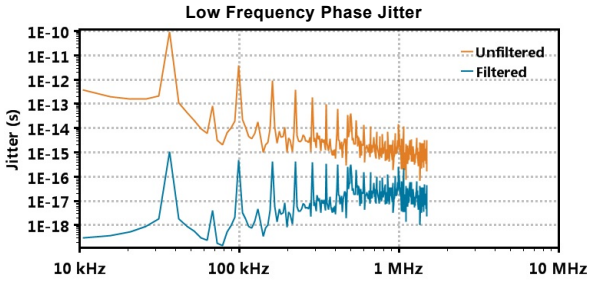


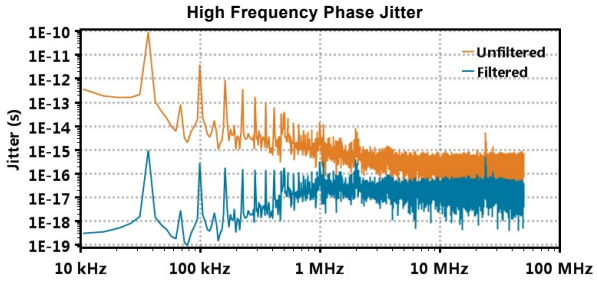


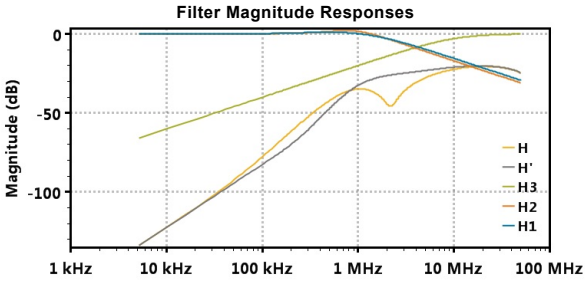


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
9	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 2 MHz (H')	1 dB (H) 2 dB (H')	2 MHz (H) 2 MHz (H')	2 dB (H) 1 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	233.956 fs (H')	PASS
Refclk LF RMS Jitter		119.308 fs (H)	N/A
Pk-pk Phase Jitter		711.537 fs (H)	N/A



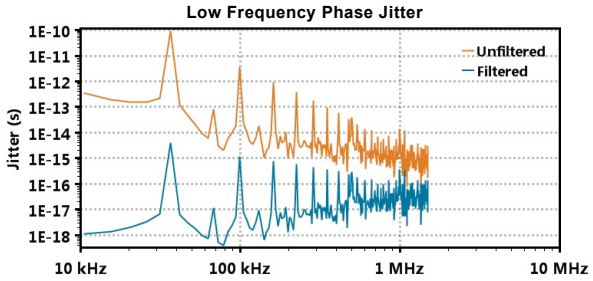


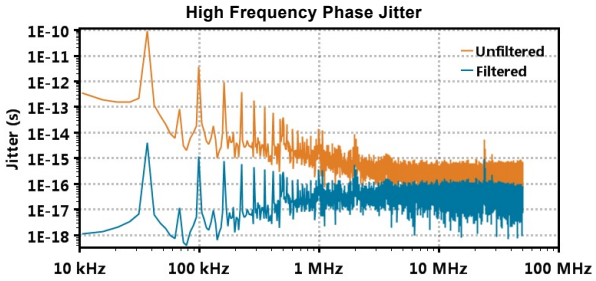


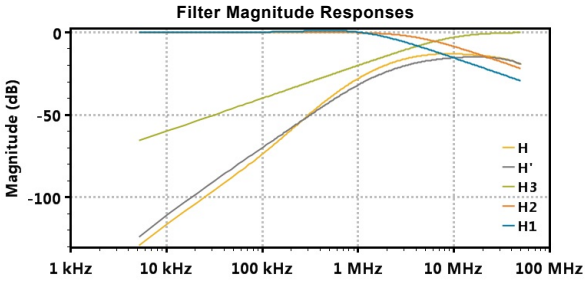
Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
10	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 4 MHz (H')	1 dB (H) 0.01 dB (H')	4 MHz (H) 2 MHz (H')	0.01 dB (H) 1 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	504.089 fs (H')	PASS
Refclk LF RMS Jitter		320.475 fs (H')	N/A
Pk-pk Phase Jitter		1.512 ps (H)	N/A

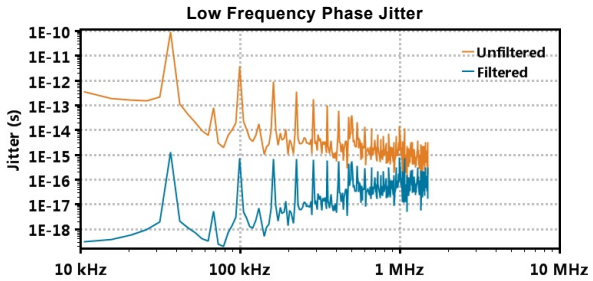


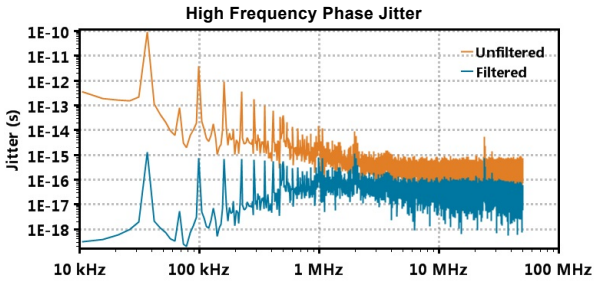


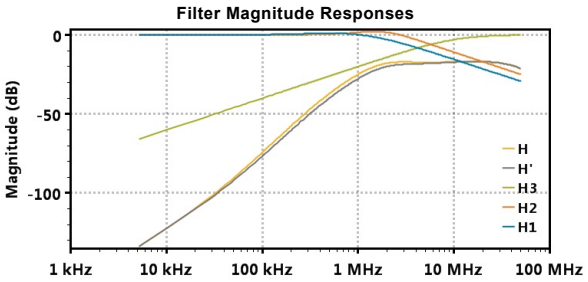


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
11	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 4 MHz (H')	1 dB (H) 2 dB (H')	4 MHz (H) 2 MHz (H')	2 dB (H) 1 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	405.557 fs (H)	PASS
Refclk LF RMS Jitter		207.352 fs (H)	N/A
Pk-pk Phase Jitter		1.499 ps (H)	N/A



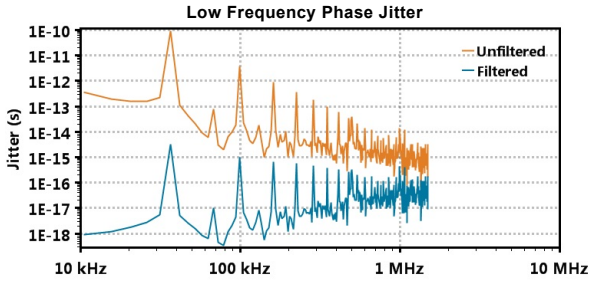


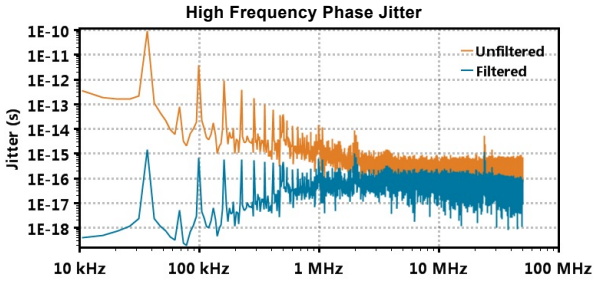


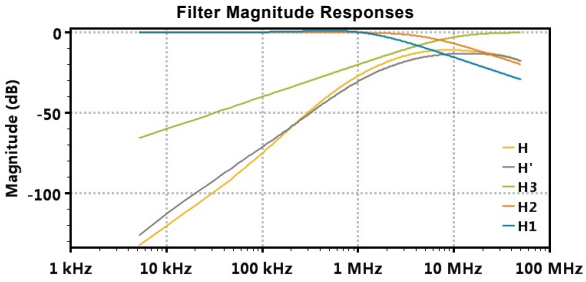
Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
12	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 5 MHz (H')	1 dB (H) 0.01 dB (H')	5 MHz (H) 2 MHz (H')	0.01 dB (H) 1 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	578.478 fs (H)	PASS
Refclk LF RMS Jitter		277.583 fs (H')	N/A
Pk-pk Phase Jitter		1.617 ps (H)	N/A

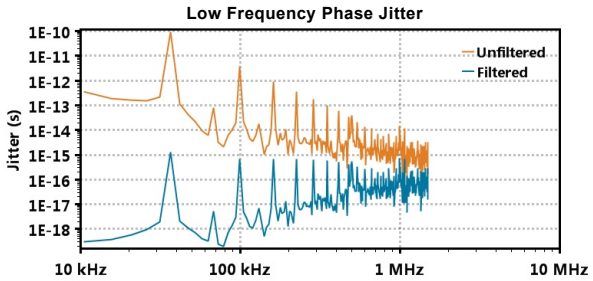


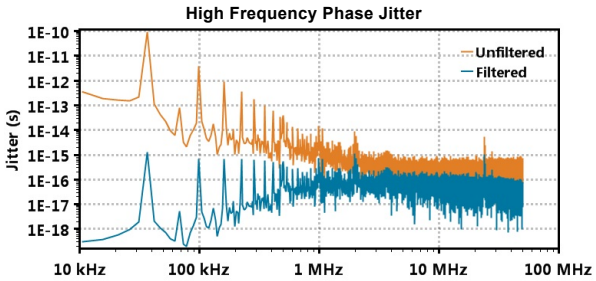


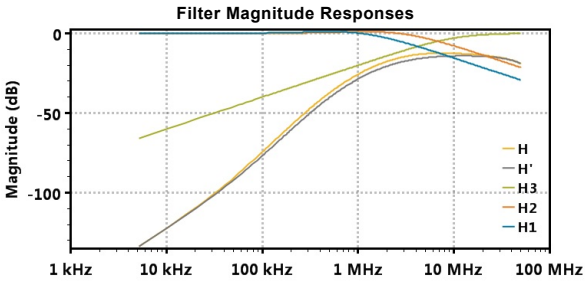


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
13	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 5 MHz (H')	1 dB (H) 1 dB (H')	5 MHz (H) 2 MHz (H')	1 dB (H) 1 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	525.157 fs (H)	PASS
Refclk LF RMS Jitter		199.231 fs (H)	N/A
Pk-pk Phase Jitter		1.659 ps (H)	N/A



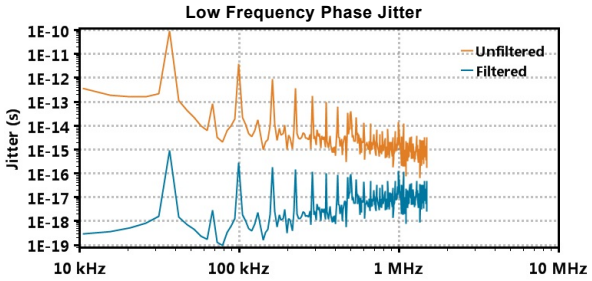


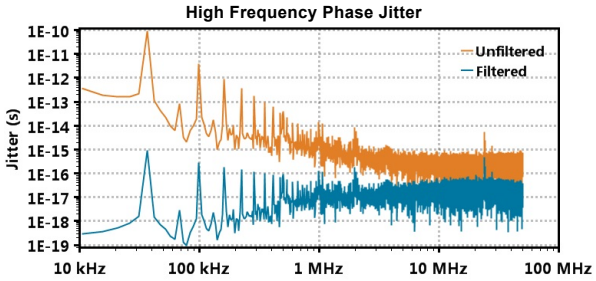


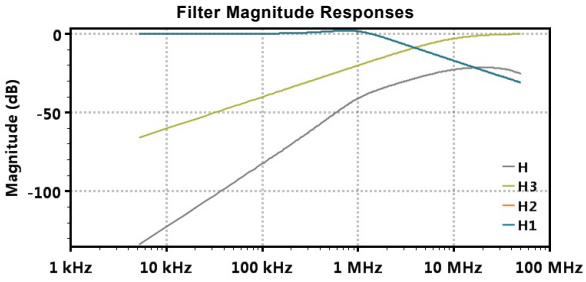
Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
14	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz	2 dB	2 MHz	2 dB	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	198.085 fs	PASS
Refclk LF RMS Jitter		78.604 fs	N/A
Pk-pk Phase Jitter		487.031 fs	N/A

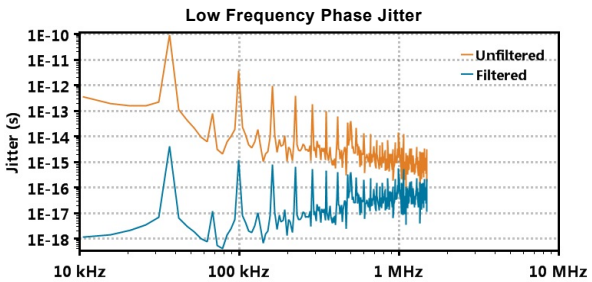


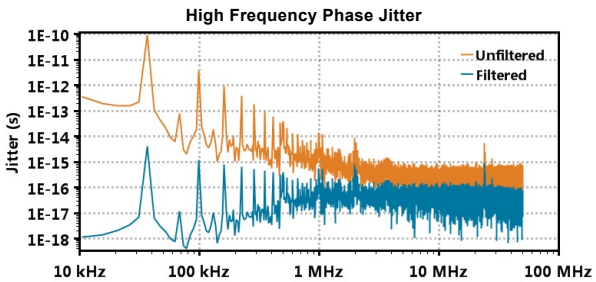


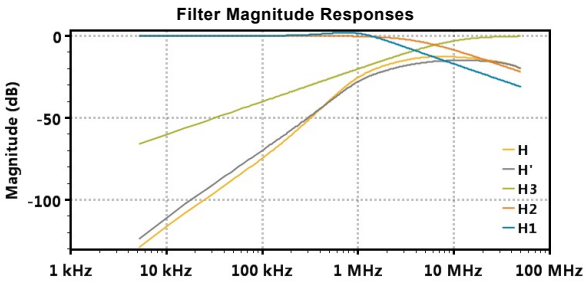


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
15	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 4 MHz (H')	2 dB (H) 0.01 dB (H')	4 MHz (H) 2 MHz (H')	0.01 dB (H) 2 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	517.358 fs (H')	PASS
Refclk LF RMS Jitter		335.336 fs (H')	N/A
Pk-pk Phase Jitter		1.666 ps (H')	N/A



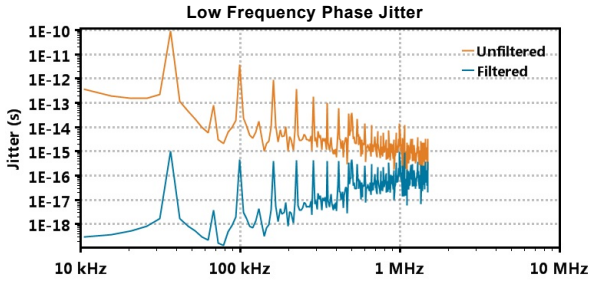


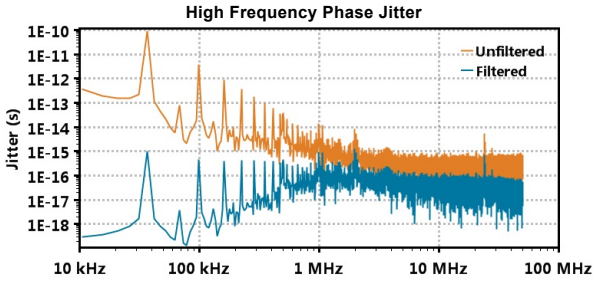


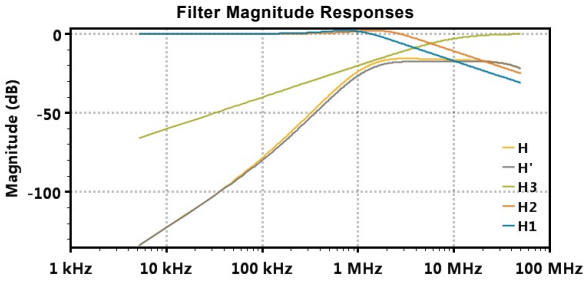
Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
16	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 4 MHz (H')	2 dB (H) 2 dB (H')	4 MHz (H) 2 MHz (H')	2 dB (H) 2 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	410.406 fs (H)	PASS
Refclk LF RMS Jitter		191.582 fs (H)	N/A
Pk-pk Phase Jitter		1.444 ps (H)	N/A

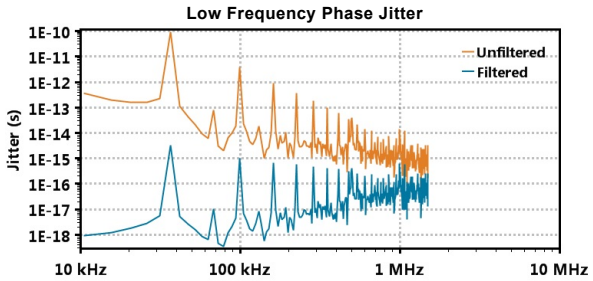


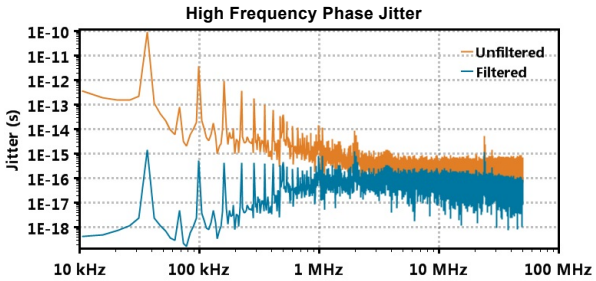


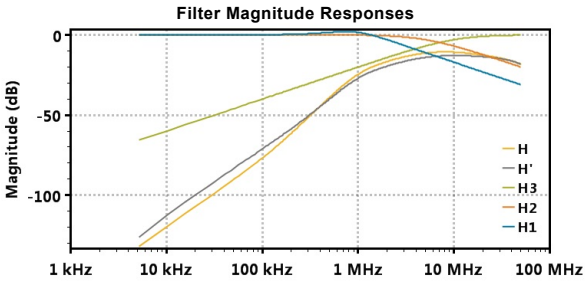


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
17	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 5 MHz (H')	2 dB (H) 0.01 dB (H')	5 MHz (H) 2 MHz (H')	0.01 dB (H) 2 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	591.624 fs (H)	PASS
Refclk LF RMS Jitter		292.029 fs (H')	N/A
Pk-pk Phase Jitter		1.700 ps (H')	N/A



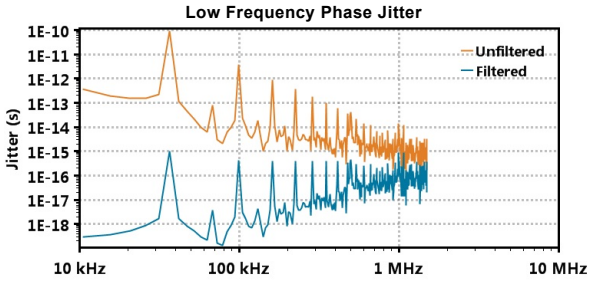


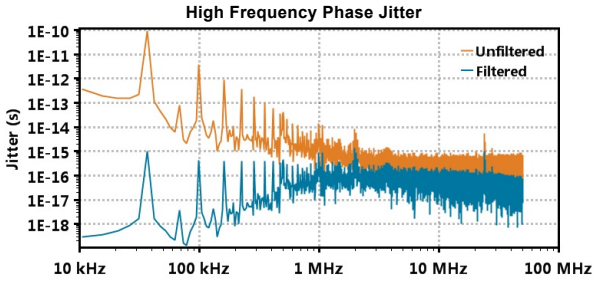


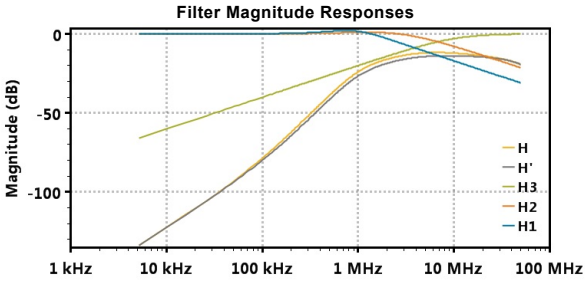
Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
18	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	2 MHz (H) 5 MHz (H')	2 dB (H) 1 dB (H')	5 MHz (H) 2 MHz (H')	1 dB (H) 2 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	533.356 fs (H)	PASS
Refclk LF RMS Jitter		186.391 fs (H)	N/A
Pk-pk Phase Jitter		1.618 ps (H)	N/A

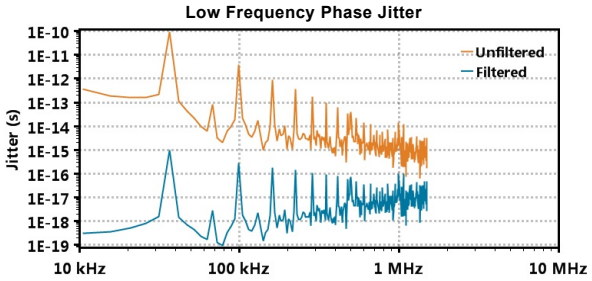


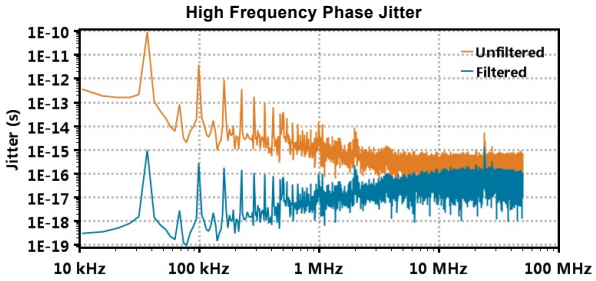


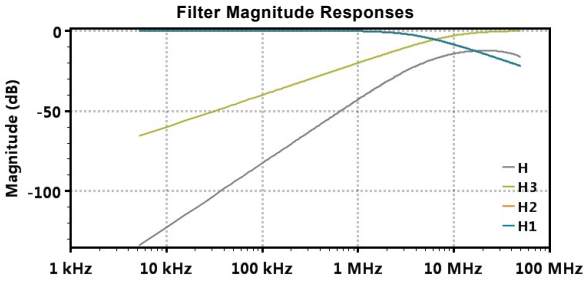


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
19	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	4 MHz	0.01 dB	4 MHz	0.01 dB	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	507.086 fs	PASS
Refclk LF RMS Jitter		77.217 fs	N/A
Pk-pk Phase Jitter		1.190 ps	N/A



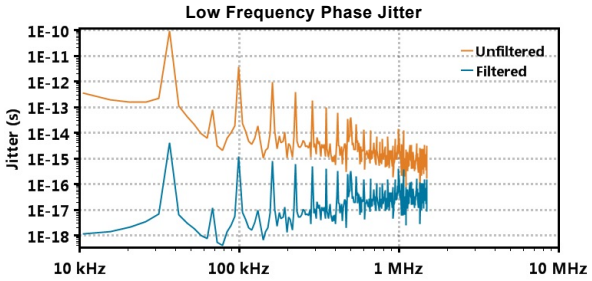


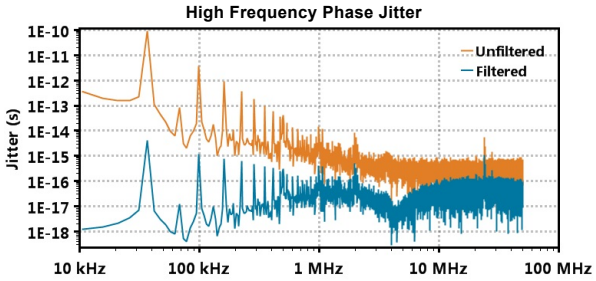


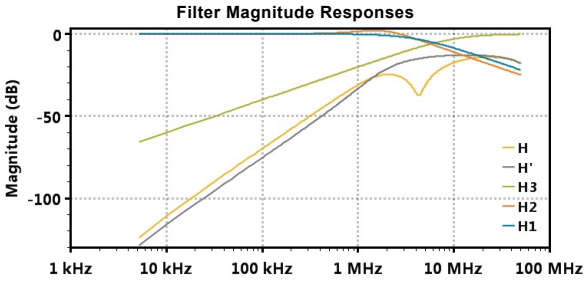
Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
20	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	4 MHz (H) 4 MHz (H')	0.01 dB (H) 2 dB (H')	4 MHz (H) 4 MHz (H')	2 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	525.001 fs (H)	PASS
Refclk LF RMS Jitter		327.708 fs (H)	N/A
Pk-pk Phase Jitter		1.491 ps (H)	N/A

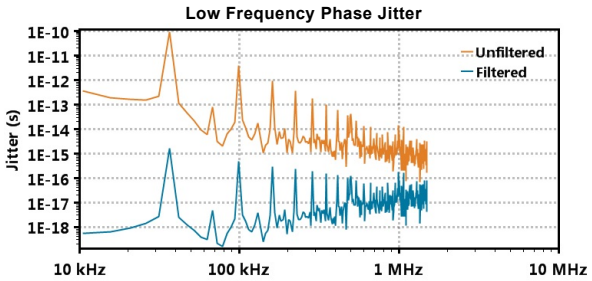


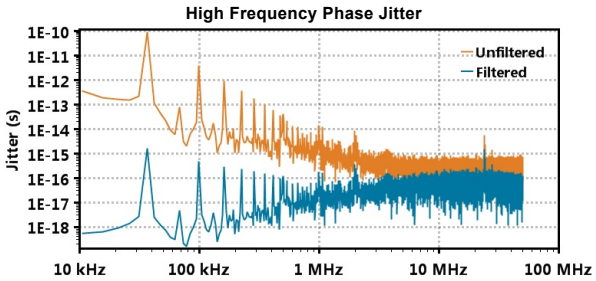


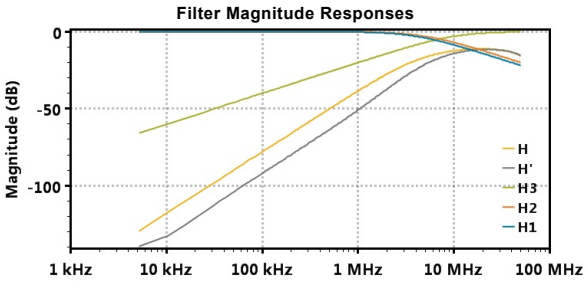


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
21	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	4 MHz (H) 5 MHz (H')	0.01 dB (H) 0.01 dB (H')	5 MHz (H) 4 MHz (H')	0.01 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	596.163 fs (H)	PASS
Refclk LF RMS Jitter		129.400 fs (H)	N/A
Pk-pk Phase Jitter		1.388 ps (H)	N/A



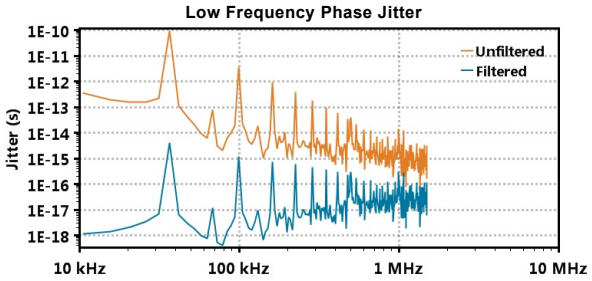


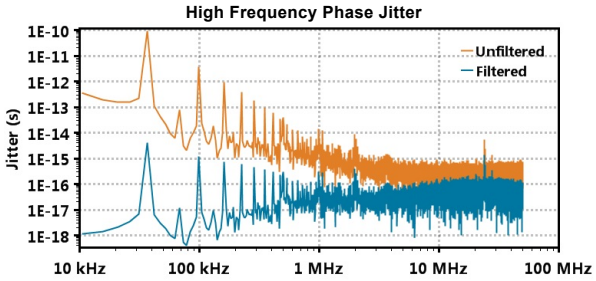


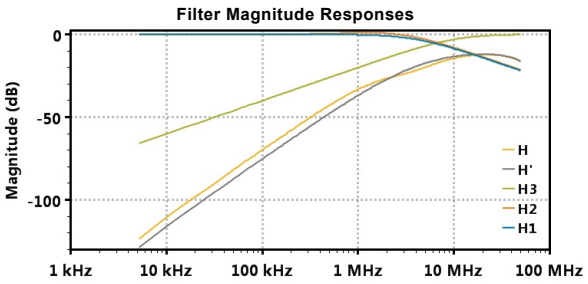
Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
22	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	4 MHz (H) 5 MHz (H')	0.01 dB (H) 1 dB (H')	5 MHz (H) 4 MHz (H')	1 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	605.725 fs (H)	PASS
Refclk LF RMS Jitter		323.833 fs (H)	N/A
Pk-pk Phase Jitter		1.644 ps (H)	N/A

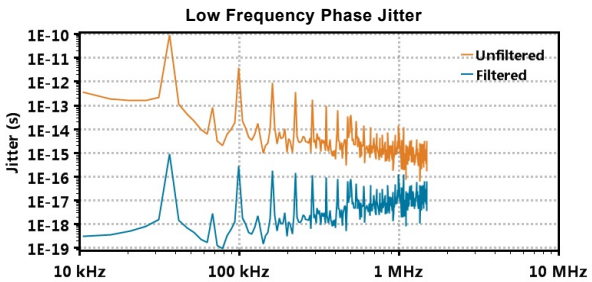


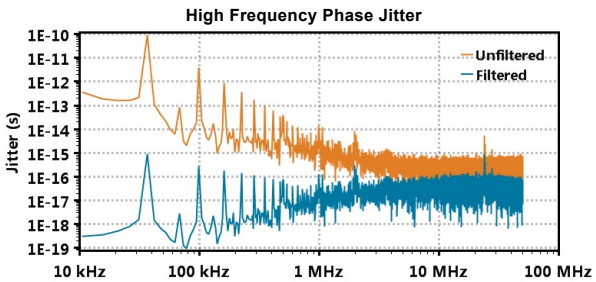


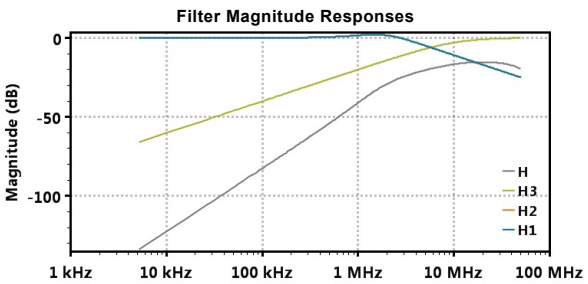


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
23	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	4 MHz	2 dB	4 MHz	2 dB	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	371.597 fs	PASS
Refclk LF RMS Jitter		78.432 fs	N/A
Pk-pk Phase Jitter		851.330 fs	N/A



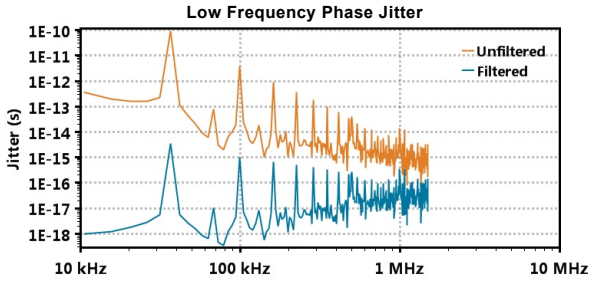


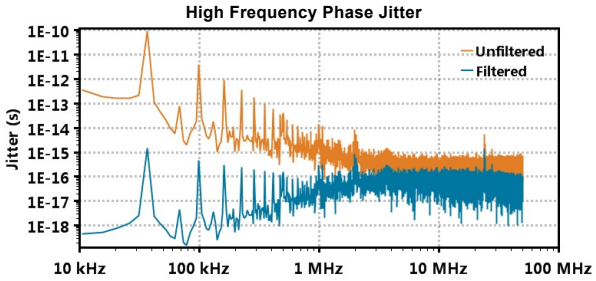


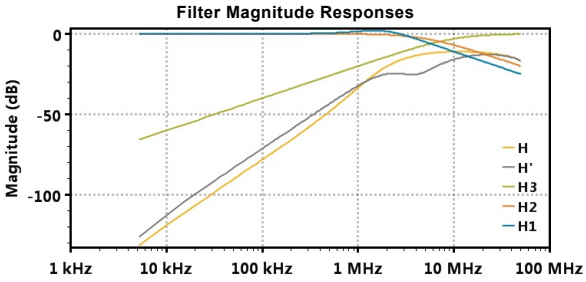
Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
24	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	4 MHz (H) 5 MHz (H')	2 dB (H) 0.01 dB (H')	5 MHz (H) 4 MHz (H')	0.01 dB (H) 2 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	598.040 fs (H)	PASS
Refclk LF RMS Jitter		276.328 fs (H')	N/A
Pk-pk Phase Jitter		1.430 ps (H')	N/A

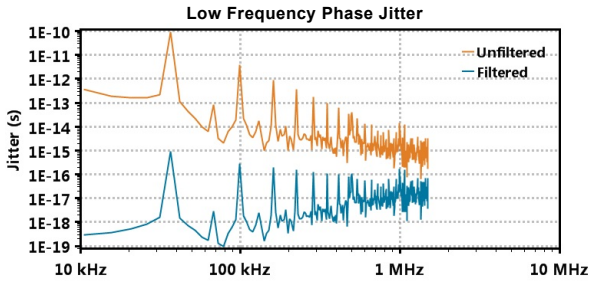


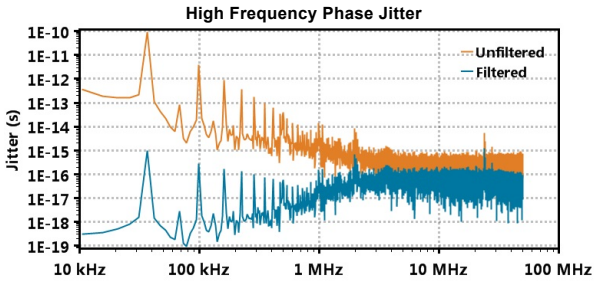


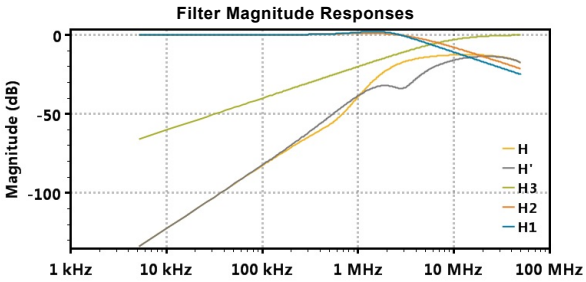


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
25	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	4 MHz (H) 5 MHz (H')	2 dB (H) 1 dB (H')	5 MHz (H) 4 MHz (H')	1 dB (H) 2 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	510.470 fs (H)	PASS
Refclk LF RMS Jitter		81.611 fs (H')	N/A
Pk-pk Phase Jitter		1.107 ps (H)	N/A



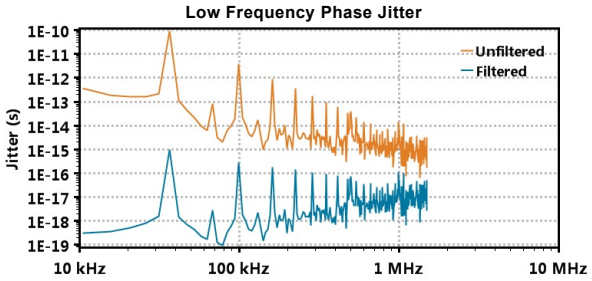


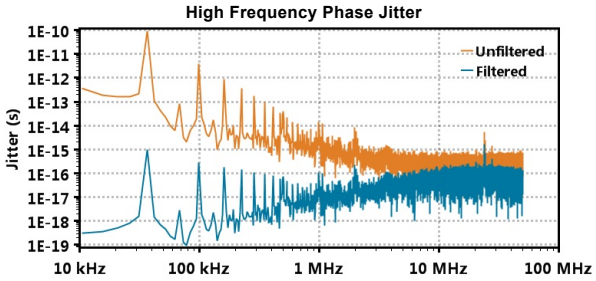


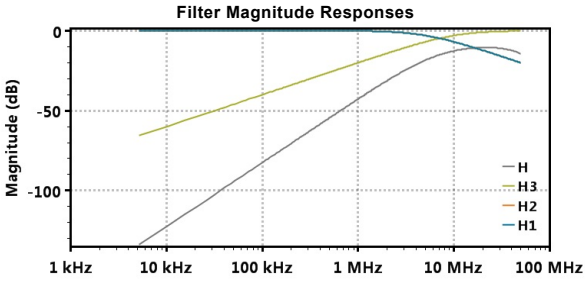
Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
26	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	5 MHz	0.01 dB	5 MHz	0.01 dB	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	623.231 fs	PASS
Refclk LF RMS Jitter		77.276 fs	N/A
Pk-pk Phase Jitter		1.463 ps	N/A

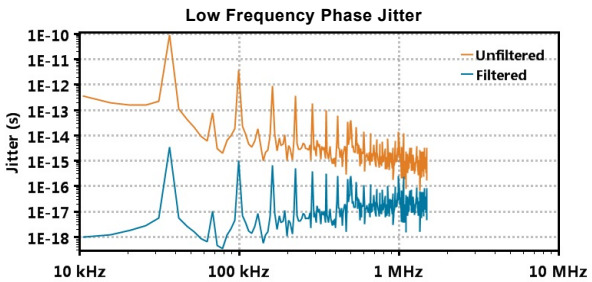


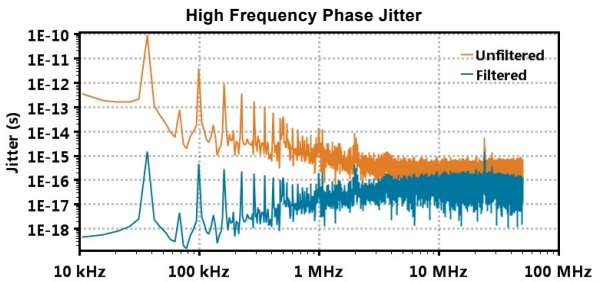


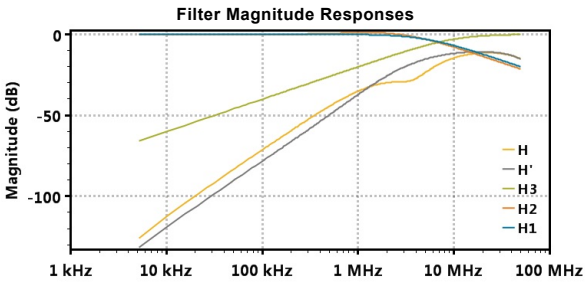


#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
27	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	5 MHz (H) 5 MHz (H')	0.01 dB (H) 1 dB (H')	5 MHz (H) 5 MHz (H')	1 dB (H) 0.01 dB (H')	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	621.169 fs (H')	PASS
Refclk LF RMS Jitter		272.166 fs (H)	N/A
Pk-pk Phase Jitter		1.614 ps (H)	N/A



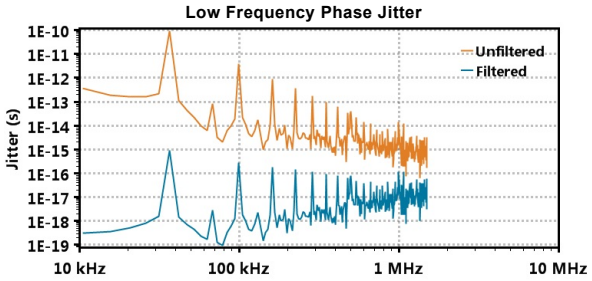


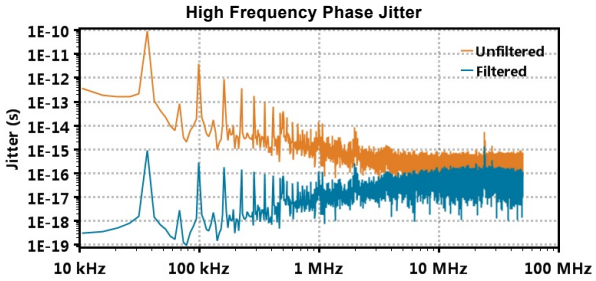


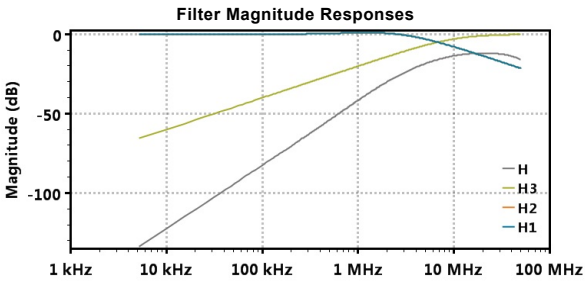
Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
28	GEN3	8 Gb/s	Common Clock	3.1 · 4.0	5 MHz	1 dB	5 MHz	1 dB	10 MHz	0 dB	12 ns	On (2)

Parameter	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	539.835 fs	PASS
Refclk LF RMS Jitter		77.987 fs	N/A
Pk-pk Phase Jitter		1.257 ps	N/A







Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

Transfer Function Constants

#	Class	Architecture	Specs	H1 BW	H1 Peaking	H1 Omega	H1 Zeta	H2 BW	H2 Peaking	H2 Omega	H2 Zeta	H3 BW	H3 Peaking	H3 Omega	H3 Zeta	Delay
1	GEN3	Common Clock	3.1 4.0	2 MHz	0.01 dB	4.48227E+5	1.40000E+1	2 MHz	0.01 dB	4.48227E+5	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
2	GEN3	Common Clock	3.1 4.0	2 MHz	0.01 dB	4.48227E+5	1.40000E+1	2 MHz	1 dB	4.61180E+6	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns
3	GEN3	Common Clock	3.1 4.0	2 MHz	0.01 dB	4.48227E+5	1.40000E+1	2 MHz	2 dB	6.01757E+6	7.30000E-1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
4	GEN3	Common Clock	3.1 4.0	2 MHz	0.01 dB	4.48227E+5	1.40000E+1	4 MHz	0.01 dB	8.96454E+5	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
5	GEN3	Common Clock	3.1 4.0	2 MHz	0.01 dB	4.48227E+5	1.40000E+1	4 MHz	2 dB	1.20351E+7	7.30000E-1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
6	GEN3	Common Clock	3.1 4.0	2 MHz	0.01 dB	4.48227E+5	1.40000E+1	5 MHz	0.01 dB	1.12057E+6	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
7	GEN3	Common Clock	3.1 4.0	2 MHz	0.01 dB	4.48227E+5	1.40000E+1	5 MHz	1 dB	1.15295E+7	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns
8	GEN3	Common Clock	3.1 4.0	2 MHz	1 dB	4.61180E+6	1.15000E+0	2 MHz	1 dB	4.61180E+6	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns
9	GEN3	Common Clock	3.1 4.0	2 MHz	1 dB	4.61180E+6	1.15000E+0	2 MHz	2 dB	6.01757E+6	7.30000E-1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
10	GEN3	Common Clock	3.1 4.0	2 MHz	1 dB	4.61180E+6	1.15000E+0	4 MHz	0.01 dB	8.96454E+5	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
11	GEN3	Common Clock	3.1 4.0	2 MHz	1 dB	4.61180E+6	1.15000E+0	4 MHz	2 dB	1.20351E+7	7.30000E-1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
12	GEN3	Common Clock	3.1 4.0	2 MHz	1 dB	4.61180E+6	1.15000E+0	5 MHz	0.01 dB	1.12057E+6	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
13	GEN3	Common Clock	3.1 4.0	2 MHz	1 dB	4.61180E+6	1.15000E+0	5 MHz	1 dB	1.15295E+7	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns
14	GEN3	Common Clock	3.1 4.0	2 MHz	2 dB	6.01757E+6	7.30000E-1	2 MHz	2 dB	6.01757E+6	7.30000E-1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
15	GEN3	Common Clock	3.1 4.0	2 MHz	2 dB	6.01757E+6	7.30000E-1	4 MHz	0.01 dB	8.96454E+5	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
16	GEN3	Common Clock	3.1 4.0	2 MHz	2 dB	6.01757E+6	7.30000E-1	4 MHz	2 dB	1.20351E+7	7.30000E-1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
17	GEN3	Common Clock	3.1 4.0	2 MHz	2 dB	6.01757E+6	7.30000E-1	5 MHz	0.01 dB	1.12057E+6	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
18	GEN3	Common Clock	3.1 4.0	2 MHz	2 dB	6.01757E+6	7.30000E-1	5 MHz	1 dB	1.15295E+7	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns
19	GEN3	Common Clock	3.1 4.0	4 MHz	0.01 dB	8.96454E+5	1.40000E+1	4 MHz	0.01 dB	8.96454E+5	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
20	GEN3	Common Clock	3.1 4.0	4 MHz	0.01 dB	8.96454E+5	1.40000E+1	4 MHz	2 dB	1.20351E+7	7.30000E-1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
21	GEN3	Common Clock	3.1 4.0	4 MHz	0.01 dB	8.96454E+5	1.40000E+1	5 MHz	0.01 dB	1.12057E+6	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
22	GEN3	Common Clock	3.1 4.0	4 MHz	0.01 dB	8.96454E+5	1.40000E+1	5 MHz	1 dB	1.15295E+7	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns
23	GEN3	Common Clock	3.1 4.0	4 MHz	2 dB	1.20351E+7	7.30000E-1	4 MHz	2 dB	1.20351E+7	7.30000E-1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
24	GEN3	Common Clock	3.1 4.0	4 MHz	2 dB	1.20351E+7	7.30000E-1	5 MHz	0.01 dB	1.12057E+6	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
25	GEN3	Common Clock	3.1 4.0	4 MHz	2 dB	1.20351E+7	7.30000E-1	5 MHz	1 dB	1.15295E+7	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns
26	GEN3	Common Clock	3.1 4.0	5 MHz	0.01 dB	1.12057E+6	1.40000E+1	5 MHz	0.01 dB	1.12057E+6	1.40000E+1	10 MHz	0 dB	6.28319E+7	NaN	12 ns
27	GEN3	Common Clock	3.1 4.0	5 MHz	0.01 dB	1.12057E+6	1.40000E+1	5 MHz	1 dB	1.15295E+7	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns
28	GEN3	Common Clock	3.1 4.0	5 MHz	1 dB	1.15295E+7	1.15000E+0	5 MHz	1 dB	1.15295E+7	1.15000E+0	10 MHz	0 dB	6.28319E+7	NaN	12 ns

Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.