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48 1 1 OE

47 1 1A1

46 1 1A2

45 GND

44 🛮 1A3

43 1 1A4

42 V_{CC}

41 1 1A5

40 1 1A6

39 | GND

38 L 1A7

37 L 1A8

36 2A1

35 2A2

34 | GND

33 🛮 2A3

32 2A4

31 V_{CC}

30 L 2A5

29 **1** 2A6

28 GND 27 2A7

26 L 2A8

25 20E

DGG OR DL PACKAGE

(TOP VIEW)

1DIR L

GND 4

1B1 📙 2

1B2 🛮 3

1B3 🛮 5

1B4 **6**

1B5 📙 8

GND 10

1B8 L 12

2B1 13

2B2 🛮 14

GND I 15

2B3 16

2B4 17

2B5 | 19

2B6 🛭 20

GND | 21

2B7 🛮 22

2B8 | 23

2DIR 🛭 24

V_{CC} 4 18

 V_{CC}

1B6 4 9

1B7 11

- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- Member of the Texas Instruments Widebus™ Family
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

The SN74ALVC16245 16-bit (dual-octal) noninverting bus transceiver is designed for 2.3-V to 3.6-V V $_{\rm CC}$ operation; it is tested at 2.5-V, 2.7-V, and 3.3-V V $_{\rm CC}$.

The SN74ALVC16245 is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data

transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16245 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 8-bit section)

INP	UTS				
OE	DIR	OPERATION			
L	L	B data to A bus			
L	Н	A data to B bus			
Н	X	Isolation			

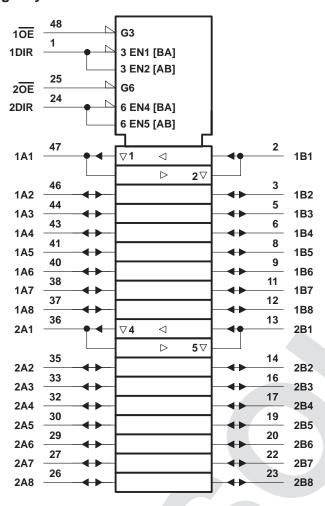


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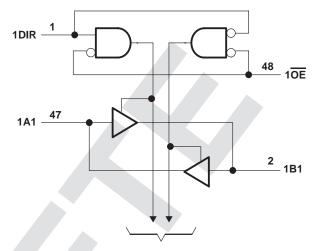
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logic symbol†

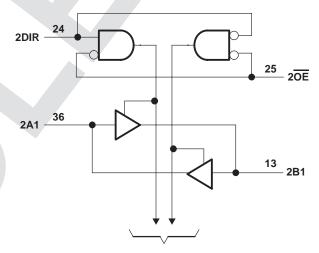


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	
Output voltage range, V _O (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range, T _{sta}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vсс	Supply voltage		2.3	3.6	V
.,	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.7		.,
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
.,	Law law Line day law a	V _{CC} = 2.3 V to 2.7 V		0.7	.,
V_{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		8.0	V
VI	Input voltage		0	VCC	V
VO	Output voltage		0	VCC	V
		V _{CC} = 2.3 V		-12	
lOH	High-level output current	V _{CC} = 2.7 V	-12 m		mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
	V _{CC} = 3 V			24	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEST COMPLETIONS		+	$T_A = -40^{\circ}C$ to $85^{\circ}C$				
PARAMETER		TEST CONDITIONS		v _{cc} †	MIN	TYP [‡]	MAX	UNIT	
		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0	.2			
		$I_{OH} = -6 \text{ mA},$ $V_{IH} = 1.7 \text{ V}$		2.3 V	2.0				
,,			V _{IH} = 1.7 V	2.3 V	1.7			V	
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2				
			V _{IH} = 2 V	3 V	2.4				
		$I_{OH} = -24 \text{ mA},$	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2		
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4	V	
VOL		104	V _{IL} = 0.7 V	2.3 V			0.7		
		I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4		
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55		
lį		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ	
		V _I = 0.7 V		227	45				
		V _I = 1.7 V		2.3 V	-45				
Ihold		V _I = 0.8 V			75			μΑ	
		V _I = 2 V		3 V	-75			[
IOZ§		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ	
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ	
ΔI _{CC}		V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND	One input at V _{CC} – 0.6 V,				750	μΑ	
Ci	Control inputs	$V_I = V_{CC}$ or GND		3.3 V		4		pF	
Cio	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		9		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM	TO	V _{CC} = 2.5 ± 0.2 V	V	V _{CC} = 2.7	7 V	0.3 VCC = 3	3.3 V ± V	UNIT
	(INPUT)	(OUTPUT)	MIN MA	AX	MIN N	ΙΑΧ	MIN	MAX	
t _{pd}	A or B	B or A	1	5		4	1	3.6	ns
t _{en}	ŌE	B or A	1 6	6.8		6	1	5	ns
^t dis	ŌĒ	B or A	1	6		5.2	1	5	ns

operating characteristics, T_A = 25° C

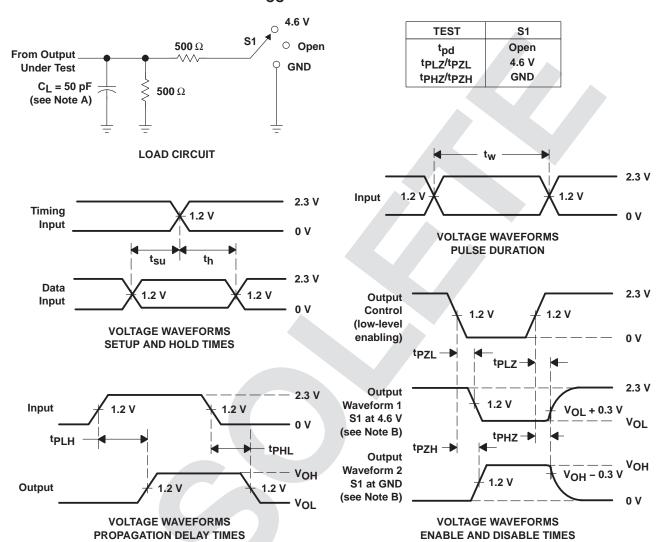
PARAMETER			TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP		
C		Outputs enabled	C ₁ = 50 pF. f = 10 MHz	22	29	pF
C _{pd}	Power dissipation capacitance	Outputs disabled	$C_L = 50 \text{ pF}, \qquad f = 10 \text{ MHz}$	4	5	рг



[‡] All typical values are at $V_{CC} = 3.3 \text{ V}$.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

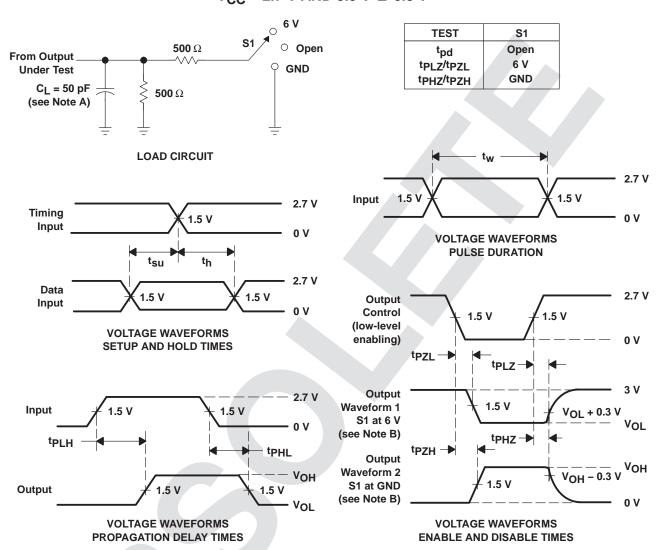


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



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