Application Report

Exploring the Int Test Pattern Generation Feature of FPD-Link III IVI Devices

Winston Wong, Ryan Bailey

ABSTRACT

This application report describes the pattern generator feature of the FPD-Link III Infotainment devices (DS90Ux92x-Q1 and DS90Ux94x-Q1), including the relevant control registers. It also provides several examples for accessing these control registers to meet custom display application requirements.

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1 Introduction

The Texas Instruments' FPD-Link III family of products (Table 1-1) offers an internal test pattern generator. This feature provides a user-friendly method for quickly debugging and testing both integrated displays, as well as the link between the serializer and deserializer. This app note focuses specifically on FPD Link III IVI (In Vehicle Infotainment) devices for display applications (94x and 92x).

Table 1-1. FPD-Link III IVI Devices

Serializers	Deserializers
DS90UH925Q-Q1/DS90UB925Q-Q1	DS90UH926Q-Q1/DS90UB926Q-Q1
DS90UB921-Q1	DS90UB924-Q1
DS90UH927Q-Q1/DS90UH927Q-Q1	DS90UH928Q-Q1/DS90UB928Q-Q1
DS90UH947-Q1/DS90UH947-Q1	DS90UH948-Q1/DS90UB948-Q1
DS90UH929-Q1/DS90UB929-Q1	DS90UH940-Q1/DS90UB940-Q1
DS90UH949-Q1/DS90UB949-Q1	DS90UH940N-Q1/DS90UB940N-Q1
DS90UH949A-Q1/DS90UB949A-Q1	
DS90UH941AS-Q1/DS90UB941AS-Q1	

2 Overview of Internal Test Pattern Generation

The internal test patterns are simple and repetitive in order to allow quick visual verification of system and display panel operation. As long as the device is not in power down mode, a test pattern can be generated, even if the device is not linked to a source. If no clock is received, the test pattern can be configured to use an internally generated programmable pixel clock.

Video timing may be based on external control signals (HS, VS, DE) provided at the serializer inputs, or they may be generated internally by either the serializer or the deserializer (Figure 2-1).

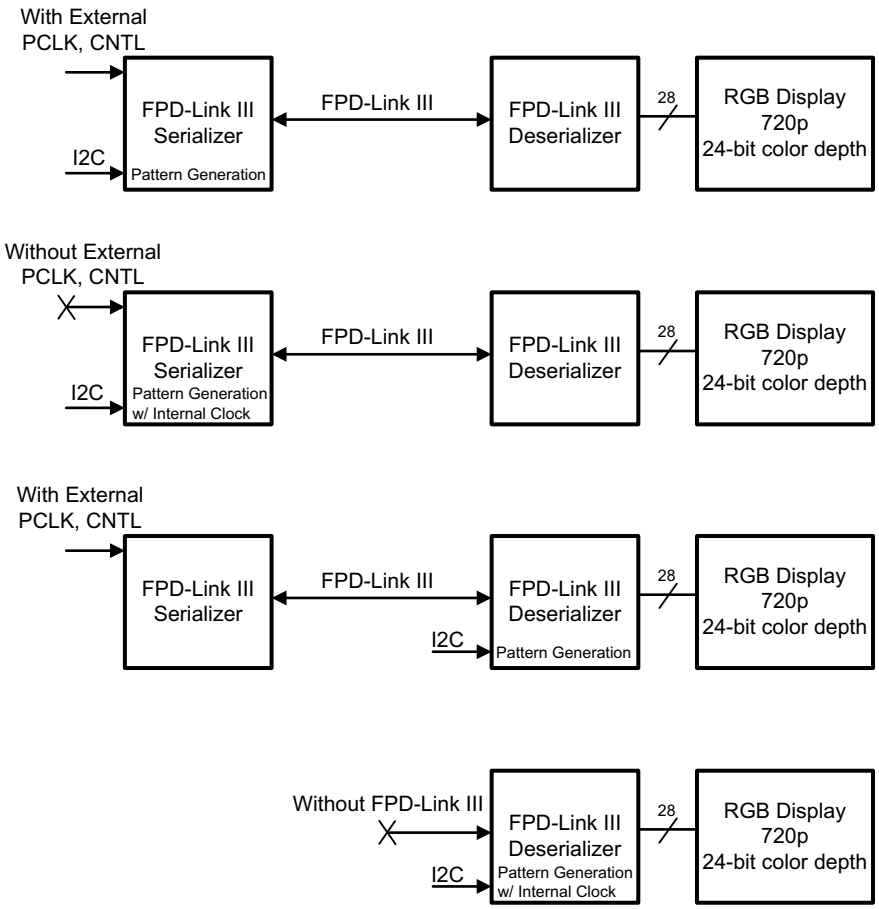

Figure 2-1. Configuration Options

No pin configuration is required to enable or control the pattern generation feature. All aspects of pattern generation are controlled through the device control registers, accessible locally through the device I2C interface, or remotely via the FPD-Link III bidirectional control channel. The test pattern generation feature is able to handle a wide range of display timings and test image options:

- Five pre-configured solid color outputs
- One user-configurable solid color output
- Horizontal ramp over full dynamic range of red, green, blue, or white
- Vertical ramp over full dynamic range of red, green, blue, or white
- Automatic scaling of brightness ramps based on frame size
- VCOM, Checkerboard, and Color Bars patterns (For all devices listed in Table 1-1 except DS90UB921-Q1, DS90Ux925Q-Q1, and DS90Ux926Q-Q1)
- Optional color inversion
- Flexible Auto-scrolling mechanism that rotates through a user-defined list of patterns
- Fully programmable internal video clock and timing generation
- Optional 18-bit color mode

2.1 Color Mode

By default, the pattern generator operates in 24-bit color mode (RGB888), where all 8 bits of the Red, Green, and Blue sub-pixels are active. 18-bit color mode (RGB666) may be enabled from the control registers (Table 3-1). In 18-bit mode, the 6 MSBs (bits 7-2) of the Red, Green, and Blue sub-pixels are enabled; the two least significant bits idle low.

2.2 Video Timing Modes

The pattern generator offers two video timing modes: external and internal. In external timing mode (default), the pattern generator detects the video frame timing present on the DE and VS inputs. If Vertical Sync signaling is not present on VS, the pattern generator determines Vertical Blank by detecting when the number of inactive pixel clocks (DE = 0) exceeds twice the detected active line length. In internal timing mode, the pattern generator generates custom video timing as determined by the control registers.

2.3 Clock Generation

The FPD Link devices listed in Table 1-1 include an internal oscillator which can be used as a reference to generate video with internal timing. Table 2-1 describes the nominal oscillator frequencies for each device. The examples in this document assume the default 200MHz nominal oscillator frequency is used unless otherwise noted.

Table 2-1. Internal Oscillator Frequencies

Device	Nominal Internal Oscillator Frequency
DS90UH925Q-Q1/DS90UB925Q-Q1	200 MHz
DS90UB921-Q1	200 MHz
DS90UH927Q-Q1/DS90UH927Q-Q1	200 MHz
DS90UH947-Q1/DS90UH947-Q1	200 MHz or 800 MHz by selection
DS90UH929-Q1/DS90UB929-Q1	200 MHz or 800 MHz by selection
DS90UH949-Q1/DS90UB949-Q1	200 MHz or 800 MHz by selection
DS90UH949A-Q1/DS90UB949A-Q1	200 MHz or 800 MHz by selection
DS90UH941AS-Q1/DS90UB941AS-Q1	200 MHz or 800 MHz by selection
DS90UH926Q-Q1/DS90UB926Q-Q1	200 MHz
DS90UB924-Q1	160 MHz
DS90UH928Q-Q1/DS90UB928Q-Q1	160 MHz
DS90UH948-Q1/DS90UB948-Q1	140 MHz
DS90UH940-Q1/DS90UB940-Q1	140 MHz
DS90UH940N-Q1/DS90UB940N-Q1	140 MHz

The pattern generator can be configured to use an internal oscillator source to generate the pixel clock and timing signals necessary to drive a wide variety of display configurations using an M/N divider. For all devices besides the DS90Ux941AS-Q1, DS90Ux949-Q1, DS90Ux949A-Q1, DS90Ux929-Q1, and DS90Ux947-Q1, the M value is assumed to be 1 and the valid range of values for N is 2 to 63. For DS90Ux941AS-Q1, DS90Ux949-Q1, DS90Ux949A-Q1, DS90Ux929-Q1, and DS90Ux947-Q1, the M and N values can both be varied as an 800-MHz oscillator option is available. The internal reference oscillator is multiplied by the M/N ratio to generate the target pixel clock (PCLK = M/N*(Oscillator Frequency)). Table 2-2 shows example video modes, divider values, and refresh rates.

Table 2-2. Sample Video Modes and Refresh Rates (200MHz Oscillator)

Active Resolution		Total Resolution		Total Pixels	Divider Ratio (4)	Minimum Refresh (Hz)	Typical Refresh (Hz)(1)	Maximum Refresh (Hz)
Horizontal	Vertical	Horizontal	Vertical					
400	240	480	288	138240	24	48.2	60.3	72.3
960	160	1152	192	221184	15	48.2	60.3	72.3
640	480	800	525	420000	8	47.6	59.5	71.4
800	480	840	485	407400	8	49.1	61.4	73.6
1280	480	1320	485	640200	5	50.0	62.5	75.0
800	600	1056	628	663168	5	48.3	60.3	72.4
1024	768	1344	806	1083264	3	49.2	61.5	73.9
1280	768	1440	798	1149120	3	46.4	58.0	69.6
1280	800	1450	844	1223800	3	43.6	54.5	65.4
1360	768	1792	795	1424640	3	37.4	46.8	56.2

Table 2-2. Sample Video Modes and Refresh Rates (200MHz Oscillator) (continued)

Active Resolution		Total Resolution		Total Pixels	Divider Ratio (4)	Minimum Refresh (Hz)	Typical Refresh (Hz)(1)	Maximum Refresh (Hz)
Horizontal	Vertical	Horizontal	Vertical					
1920(2)	1080(2)	2047	1125	2302875	3	23.2	28.9	34.7
1920(3)	1080(3)	2200	1125	2302875	2	30.4	43.4	56.5

(1) The minimum, typical, and maximum refresh rates are related to the device internal oscillator reference frequency variation of 140 MHz (min), 200 MHz (typ), and 260 (max) MHz respectively.
(2) 1080p30 target resolution
(3) 1080p60 target resolution - only supported on 94x dual link devices
(4) The divider ratios in this table assume the M value for the M/N divider is 1

Note

The DS90Ux928Q-Q1 and DS90UB924-Q1 deserializers require extra configuration to use the internally generated pixel clock. Refer to Table 3-3 for additional details.

2.4 Pattern Selection

The pattern generator offers 14 (DS90Ux925Q-Q1/DS90Ux926Q-Q1/DS90UB921-Q1) or 17 (All other aforementioned devices) built-in color patterns:

1. Full-screen White
2. Full-screen Black
3. Full-screen Red
4. Full-screen Green
5. Full-screen Blue
6. Horizontally scaled Black to White
7. Horizontally scaled Black to Red
8. Horizontally scaled Black to Green
9. Horizontally scaled Black to Blue
10. Vertically scaled Black to White
11. Vertically scaled Black to Red
12. Vertically scaled Black to Green
13. Vertically scaled Black to Blue
14. Full-screen User-Configurable Color
15. VCOM **(Not available for 921/925Q/926Q)**
16. Black & White (or User-configurable Color) Checkerboard **(Not available for 921/925Q/926Q)**
17. Vertical Color Bars **(Not available for 921/925Q/926Q)**

Note

The Color Bars Pattern is not available for use in Auto-Scrolling Mode.

2.5 Pattern Inversion

The pattern generator also incorporates a global inversion control that performs a bitwise inversion of the output pattern when activated. For example, the full-screen red pattern becomes full-screen cyan, and the vertically scaled black to green pattern becomes vertically scaled white to magenta.

2.6 Auto-Scrolling

The pattern generator supports an auto-scrolling mode, in which the output pattern cycles through a list of enabled pattern types. A sequence of up to 14 patterns (925Q/921/926Q) or up to 16 patterns (all other aforementioned devices) may be defined in the registers. The patterns may appear in any order in the sequence and may also appear more than once.

This feature is accessed through the device control registers described in Table 3-1.

3 Serial Control Bus Registers for Internal Test Pattern Generation

The Internal Test Pattern generator is configured and enabled from the internal control registers, accessible locally through the I2C control interface, or remotely via the FPD-Link III Bidirectional Control Channel. The Pattern Generator control registers consist of both a Direct Register Map, as well as an Indirect Register Map, the latter of which is accessible through an indirect address pointer/data mechanism.

3.1 Direct Register Map

The Direct Register Map is used to control and enable basic features of the Internal Test Pattern Generator, including the selected pattern, clocking, and timing sources. The Direct Registers are also used to access the Indirect Register Map space.

3.1.1 Control and Configuration

The PGCTL and PGCFG registers are used to enable and configure the general behavior of the pattern generator.

Table 3-1. Pattern Generator Direct Registers

ADD(hex)	Register Name	Bit	Access	Default (hex)	Function	Description
0x64	Pattern Generator Control (PGCTL)	7:4	RW	0x10	Pattern Generator Select	Fixed Pattern Select This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. Table 3-4 shows the color selections in non-inverted followed by inverted color mode 0000: **(Not available for 921/925Q/926Q)** Checkerboard 0001: White/Black 0010: Black/White 0011: Red/Cyan 0100: Green/Magenta 0101: Blue/Yellow 0110: Horizontally Scaled Black to White/White to Black 0111: Horizontally Scaled Black to Red/Cyan to White 1000: Horizontally Scaled Black to Green/Magenta to White 1001: Horizontally Scaled Black to Blue/Yellow to White 1010: Vertically Scaled Black to White/White to Black 1011: Vertically Scaled Black to Red/Cyan to White 1100: Vertically Scaled Black to Green/Magenta to White 1101: Vertically Scaled Black to Blue/Yellow to White 1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers 1111: **(927Q/928Q only)** VCOM
		3				***Reserved***
		2	RW		Color Bars Pattern	**(Not available for 921/925Q/926Q)** Enable Color Bars Pattern 0: Color Bars Disabled (default) 1: Color Bars Enabled Overrides the selection from bits [7:4]
		1	RW		VCOM Pattern Reverse	**(Not available for 921/925Q/926Q)** Reverse Order of Color Bands in VCOM Pattern 0: Color sequence from top left is (YCBR) (default) 1: Color sequence from top left is (RBCY)
		0	RW		Pattern Generator Enable	Pattern Generator Enable 1: Enable Pattern Generator (1) 0: Disable Pattern Generator

Table 3-1. Pattern Generator Direct Registers (continued)

ADD(hex)	Register Name	Bit	Access	Default (hex)	Function	Description
0x65	Pattern Generator Configuration (PGCFG)	7		0x00		***Reserved***
		6	RW		Checkerboard Scale	**(Not available for 921/925Q/926Q)** Scale Checkerboard Patterns 0: Normal operation (each square is 1x1 pixel) (default) 1: Scale Checkerboard Patterns (VCOM and Checkerboard) by 8 (each square is 8x8 pixels) Setting this bit gives better visibility of the checkerboard patterns
		5	RW		Custom Checkerboard	**(Not available for 921/925Q/926Q)** Use Custom Color in Checkerboard Pattern 0: Use white and black Checkerboard pattern (default) 1: Use the Customer Color and Black in the Checkerboard Pattern
		4	RW		Pattern Generator 18 Bits	18-bit Mode Select 1: Enable 18-bit color pattern generation. Scaled patterns have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness.
		3	RW		Pattern Generator External Clock	Select External Clock Source 1: Selects the external pixel clock when using internal timing. 0: Selects the internal divided clock when using internal timing This bit has no effect in external timing mode (PATGEN_TSEL = 0).
		2	RW		Pattern Generator Timing Select	Timing Select Control 1: The pattern generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size. Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: The pattern generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals.
		1	RW		Pattern Generator Color Invert	Enable Inverted Color Patterns 1: Invert the color output. 0: Do not invert the color output.
		0	RW		Pattern Generator Auto- Scroll Enable	Auto-Scroll Enable: 1: The pattern generator automatically moves to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time Register (PGFT). 0: The pattern generator retains the current pattern.

Table 3-1. Pattern Generator Direct Registers (continued)

ADD(hex)	Register Name	Bit	Access	Default (hex)	Function	Description
0x68	Pattern Generator Debug (PGDBG) **948 and 940/940N only**	7:4	RW	0x00	PATGEN Debug Select	Test Mux Select: This field selects the signals to be monitored in the PGTSTDAT register. These signals can be monitored while the serializer is in PATGEN mode, or during normal operation as well. Bit 3 of this register must be set high to enable the test mux. 0000: Video Active Height LSB [5:0] 0001: Video Active Height MSB [11:6] 0010: Video Active Width LSB [5:0] 0011: Video Active Width MSB [11:6]
		3	RW		PATGEN BIST Enable	Pattern Generator BIST Enable: Enables Pattern Generator in BIST mode. Pattern Generator will compare received video data with local generated pattern. Upstream device must be programmed to the same pattern. PATGEN enable in register 0x64 should not be set prior to enabling this bit.
		2	RW		RESERVED	
		1	RW		RESERVED	
		0	RW		PATGEN Debug Sample	Triggers a sampling of the data for the selected test mux. This bit must be set before reading back the test data from PGTSTDAT. This bit is self clearing
0x69	Pattern Generator Test Data (PGTSTDAT) **948 and 940/940N only**	7	R	0x00	Pattern Generator BIST Error	Pattern Generator BIST Error Flag During Pattern Generator BIST mode, this bit indicates if the BIST engine has detected errors. If the BIST Error Count (available in the Pattern Generator indirect registers) is non-zero, this flag will be set.
		6	R		RESERVED	
		5:0	R		Pattern Generator Test Data	Test Data: This field contains data output based on the selection of the test mux in PGDBG. The PATGEN debug sample bit in PGDBG must be set high to trigger an update to this data.

(1) PATGEN at the deserializer side should only be enabled via local I2C, not via remote control from the serializer. Enabling PATGEN remotely from the serializer side will cause a loss of I2C communication over the bidirectional control channel.

3.1.2 Indirect Access Address and Data

The PGIA and PGID registers are used to indirectly access the detailed configuration registers for the Internal Test Pattern Generator. To use these registers to access the indirect register space, perform the following steps:

- Set PGIA to the indirect register address to be read/written.
- To READ indirect register: Read from PGID.
- To WRITE indirect register: Write indirect register data to PGID.

Table 3-2. Pattern Generator Indirect Registers

ADD(hex)	Register Name	Bit	Access	Default (hex)	Function	Description
0x66	Pattern Generator Indirect Address (PGIA)	7:0	RW	0x00	Indirect Address	This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data Register (PGID).
0x67	Pattern Generator Indirect Data (PGID)	7:0	RW	0x00	Indirect Data	When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the read back value.

3.1.3 DS90Ux928Q-Q1/DS90UB924-Q1 Internal Clock Source

The DS90Ux928Q-Q1 and DS90UB924-Q1 deserializers require an extra configuration step to use their internal clock source. Note that this step is unnecessary if the pixel clock is derived externally (that is received from the serializer). Before enabling the Internal Test Pattern Generator with an internal pixel clock source, configure the register shown below:

Table 3-3. DS90Ux928Q-Q1/DS90UB924-Q1 Pattern Generator Internal Clock Enable

ADD(hex)	Register Name	Bit	Access	Default (hex)	Function	Description
0x39	PG Internal Clock Enable	7:2		0x00		Reserved
		1	RW		PG INT CLK	Enable Pattern Generator Internal Clock This bit must be used to set the Pattern Generator Internal Clock Generation 0: Pattern Generator with external PCLK 1: Pattern Generator with internal PCLK
		0				Reserved

3.2 Indirect Register Map

Additional Pattern Generator features are accessed through the Indirect Address register space. These registers are read/written through the indirect access address (PGIA) and data (PGID) control registers.

Note

Indirect Registers may only be modified while the Pattern Generator is disabled.

Table 3-4. Pattern Generator Indirect Address

ADD (hex)	Access	Tag (Name)	Description
General Control Registers			
0x00	RW	PGRS	Pattern Generator Red Sub-Pixel
0x01	RW	PGGS	Pattern Generator Green Sub-Pixel
0x02	RW	PGBS	Pattern Generator Blue Sub-Pixel
Internal Timing Control Registers			
0x03	RW	PGCDC	Pattern Generator Clock Divider Control
0x04	RW	PGTFS1	Pattern Generator Total Frame Size 1
0x05	RW	PGTFS2	Pattern Generator Total Frame Size 2
0x06	RW	PGTFS3	Pattern Generator Total Frame Size 3
0x07	RW	PGAFS1	Pattern Generator Active Frame Size 1
0x08	RW	PGAFS2	Pattern Generator Active Frame Size 2
0x09	RW	PGAFS3	Pattern Generator Active Frame Size 3
0x0A	RW	PGHSW	Pattern Generator Horizontal Sync Width
0x0B	RW	PGVSW	Pattern Generator Vertical Sync Width
0x0C	RW	PGHBP	Pattern Generator Horizontal Back Porch
0x0D	RW	PGVBP	Pattern Generator Vertical Back Porch
0x0E	RW	PGSC	Pattern Generator Sync Configuration
Auto-Scrolling Control Registers			
0x0F	RW	PGFT	Pattern Generator Frame Time
0x10	RW	PGTSC	Pattern Generator Time Slot Configuration
0x11	RW	PGTSO1	Pattern Generator Time Slot Order 1
0x12	RW	PGTSO2	Pattern Generator Time Slot Order 2
0x13	RW	PGTSO3	Pattern Generator Time Slot Order 3
0x14	RW	PGTSO4	Pattern Generator Time Slot Order 4
0x15	RW	PGTSO5	Pattern Generator Time Slot Order 5
0x16	RW	PGTSO6	Pattern Generator Time Slot Order 6
0x17	RW	PGTSO7	Pattern Generator Time Slot Order 7
0x18	RW	PGTSO8	Pattern Generator Time Slot Order 8 **(Not available for 921/925Q/926Q)**
0x19	R	PGBE	Pattern Generator BIST Errors **(Only available on DS90Ux948-Q1 or DS90Ux940-Q1/DS90Ux940N-Q1)**

Table 3-4. Pattern Generator Indirect Address (continued)

ADD (hex)	Access	Tag (Name)	Description
0x1A	RW	PGCDC2	Pattern Generator Clock Divider M Configuration **(Only available on DS90Ux941AS-Q1, DS90Ux949-Q1, DS90Ux949A-Q1, DS90Ux929-Q1, and DS90Ux947-Q1)**

3.2.1 General Control

Pattern Generator Red Sub-Pixel (PGRS), address 0x00 in Table 3-4.

This register controls the Red sub-pixel when the custom color is selected.

Table 3-5. Pattern Generator Red Sub-Pixel (PGRS)

Bit	Access	Field	Default (bin)	Description
7:0	RW	PATGEN_RSP	00000000	Red Sub-Pixel: This field is the 8-bit Red sub-pixel for the custom color.

Pattern Generator Green Sub-Pixel (PGGS), address 0x01 in Table 3-4.

This register controls the Green sub-pixel when the custom color is selected.

Table 3-6. Pattern Generator Green Sub-Pixel (PGGS)

Bit	Access	Field	Default (bin)	Description
7:0	RW	PATGEN_GSP	00000000	Green Sub-Pixel: This field is the 8-bit Green sub-pixel for the custom color.

Pattern Generator Blue Sub-Pixel (PGBS), address 0x02 in Table 3-4.

This register controls the Blue sub-pixel when the custom color is selected.

Table 3-7. Pattern Generator Blue Sub-Pixel (PGBS)

Bit	Access	Field	Default (bin)	Description
7:0	RW	PATGEN_BSP	00000000	Blue Sub-Pixel: This field is the 8-bit Blue sub-pixel for the custom color.

3.2.2 Internal Timing Control

The Internal Timing Control registers configure the generated pixel clock frequency and video frame parameters for internal timing mode. The default values are configured for 800x480 resolution at 61.4Hz as shown in the following Table 3-8.

Table 3-8. Internal Timing Default Values

Parameter	Default	Units
Clock Divider	8	-
Refresh Rate	61.4	Hz
Total Horizontal Width	840	Pixels
Total Vertical Width	485	Lines
Active Horizontal Width	800	Pixels
Active Vertical Width	480	Lines
Horizontal Sync Width	10	Pixels
Vertical Sync Width	2	Lines
Horizontal Back Porch	10	Pixels
Vertical Back Porch	2	Lines
Horizontal Sync Polarity	Negative	N/A
Vertical Sync Polarity	Negative	N/A

Pattern Generator Clock Divider N Configuration (PGCDC1), address 0x03 in Table 3-4.

This register controls the N divider for the internal clock when the internal pixel clock is selected. For all devices besides DS90Ux941AS-Q1, DS90Ux949-Q1, DS90Ux949A-Q1, DS90Ux929-Q1, and DS90Ux947-Q1, the M clock divider value is assumed to be 1.

Table 3-9. Pattern Generator Clock Divider N Configuration (PGCDC1)

Bit	Access	Field	Default (bin)	Description
7:6		Reserved	00	***Reserved.*** Reads return 0, writes are ignored.
5:0	RW	PATGEN_CDIV_N	001000	Clock Divider: This field configures the "N" clock divider for the internal 200 MHz clock when the pattern generator uses internal timing. Valid values are 2 through 63; values 0 and 1 are reserved and must not be used.

Pattern Generator Total Frame Size 1 (PGTFS1), address 0x04 in Table 3-4.

This register, along with the Total Frame Size 2 register, configures the Total Horizontal Width of the frame. The value in this register is used when internal video timing is enabled.

Table 3-10. Pattern Generator Total Frame Size 1 (PGTFS1)

Bit	Access	Field	Default (bin)	Description
7:0	RW	PATGEN_THW	01001000	Total Horizontal Width: This field is the 8 least significant bits of the 12-bit Total Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

Pattern Generator Total Frame Size 2 (PGTFS2), address 0x05 in Table 3-4.

This register, along with the Total Frame Size 1 register, configures the Total Horizontal Width of the frame. In addition, along with the Total Frame Size 3 register, this register configures the Total Vertical Width of the frame. The values in this register are used when internal video timing is enabled.

Table 3-11. Pattern Generator Total Frame Size 2 (PGTFS2)

Bit	Access	Field	Default (bin)	Description
7:4	RW	PATGEN_TVW	0101	Total Vertical Width: This field is the 4 least significant bits of the 12-bit Total Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.
3:0	RW	PATGEN_THW	0011	Total Horizontal Width: This field is the 4 most significant bits of the 12-bit Total Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

Pattern Generator Total Frame Size 3 (PGTFS3), address 0x06 in Table 3-4.

This register, along with the Total Frame Size 2 register, configures the Total Vertical Width of the frame. The values in this register are used when internal video timing is enabled.

Table 3-12. Pattern Generator Total Frame Size 3 (PGTFS3)

Bit	Access	Field	Default (bin)	Description
7:0	RW	PATGEN_TVW	00011110	Total Vertical Width: This field is the 8 most significant bits of the 12-bit Total Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.

Pattern Generator Active Frame Size 1 (PGAFS1), address 0x07 in Table 3-4.

This register, along with the Active Frame Size 2 register, configures the Active Horizontal Width of the frame. The value in this register is used when internal video timing is enabled.

Table 3-13. Pattern Generator Active Frame Size 1 (PGAFS1)

Bit	Access	Field	Default (bin)	Description
7:0	RW	PATGEN_AHW	00100000	Active Horizontal Width: This field is the 8 least significant bits of the 12-bit Active Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

Pattern Generator Active Frame Size 2 (PGAFS2), address 0x08 in Table 3-4.

This register, along with the Active Frame Size 1 register, configures the Active Horizontal Width of the frame. In addition, along with the Active Frame Size 3 register, this register configures the Active Vertical Width of the frame. The values in this register are used when internal video timing is enabled.

Table 3-14. Pattern Generator Active Frame Size 2 (PGAFS2)

Bit	Access	Field	Default (bin)	Description
7:4	RW	PATGEN_AVW	0000	Active Vertical Width: This field is the 4 least significant bits of the 12-bit Active Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.
3:0	RW	PATGEN_AHW	0011	Active Horizontal Width: This field is the 4 most significant bits of the 12-bit Active Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

Pattern Generator Active Frame Size 3 (PGAFS3), address 0x09 in Table 3-4.

This register, along with the Active Frame Size 2 register, configures the Active Vertical Width of the frame. The value in this register is used when internal video timing is enabled.

Table 3-15. Pattern Generator Active Frame Size 3 (PGAFS3)

Bit	Access	Field	Default (bin)	Description
7:0	RW	PATGEN_AVW	00011110	Active Vertical Width: This field is the 8 most significant bits of the 12-bit Active Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.

Pattern Generator Horizontal Sync Width (PGHSW), address 0x0A in Table 3-4.

This register configures the Horizontal Sync Width of the frame. The value in this register is used when internal video timing is enabled.

Table 3-16. Pattern Generator Horizontal Sync Width (PGHSW)

Bit	Access	Field	Default (bin)	Description
7:0	RW	PATGEN_HSW	00001010	Horizontal Sync Width: This field controls the width of the Horizontal Sync pulse, in units of pixels. Valid values are 1-255. This field should only be written when the pattern generator is disabled.

Pattern Generator Vertical Sync Width (PGVSW), address 0x0B in Table 3-4.

This register configures the Vertical Sync Width of the frame. The value in this register is used when internal video timing is enabled.

Table 3-17. Pattern Generator Vertical Sync Width (PGVSW)

Bit	Access	Field	Default (bin)	Description
7:0	RW	PATGEN_VSW	00000010	Vertical Sync Width: This field controls the width of the Vertical Sync pulse, in units of lines. Valid values are 1-255. This field should only be written when the pattern generator is disabled.

Pattern Generator Horizontal Back Porch (PGHBP), address 0x0C in Table 3-4.

This register configures the width of the Horizontal Back Porch of the frame. The value in this register is used when internal video timing is enabled.

Table 3-18. Pattern Generator Horizontal Back Porch (PGHBP)

Bit	Access	Field	Default (bin)	Description
7:0	RW	PATGEN_HBP	00001010	Horizontal Back Porch Width: This field controls the width of the Horizontal Back Porch, in units of pixels. Valid values are 1-255. This field should only be written when the pattern generator is disabled.

Pattern Generator Vertical Back Porch (PGVBP), address 0x0D in Table 3-4.

This register configures the width of the Horizontal Back Porch of the frame. The value in this register is used when internal video timing is enabled.

Table 3-19. Pattern Generator Vertical Back Porch (PGVBP)

Bit	Access	Field	Default (bin)	Description
7:0	RW	PATGEN_VBP	00000010	Vertical Back Porch Width: This field controls the width of the Vertical Back Porch, in units of lines. Valid values are 1-255. This field should only be written when the pattern generator is disabled.

Pattern Generator Sync Configuration (PGSC), address 0x0E in Table 3-4.

This register configures the generator of Horizontal and Vertical Sync signaling.

Table 3-20. Pattern Generator Sync Configuration (PGSC)

Bit	Access	Field	Default (bin)	Description
7:4		Reserved	0000	Reserved: Reads return 0, writes are ignored.
3	RW	PATGEN_VS_DIS	0	Vertical Sync Disable: Disable Vertical Sync signaling when the pattern generator is in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled.
2	RW	PATGEN_HS_DIS	0	Horizontal Sync Disable: Disable Horizontal Sync signaling when the pattern generator is in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled.
1	RW	PATGEN_VS_POL	1	Vertical Sync Polarity: When 1, the pattern generator will invert the Vertical Sync signal when in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled.
0	RW	PATGEN_HS_POL	1	Horizontal Sync Polarity: When 1, the pattern generator will invert the Horizontal Sync signal when in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled.

3.2.3 Auto-Scrolling Control

Pattern Generator Frame Time (PGFT), Offset 0x0F in Table 3-4.

This register configures the number of frames to display each pattern when Auto-Scrolling is enabled.

Table 3-21. Pattern Generator Frame Time (PGFT)

Bit	Access	Field	Default (bin)	Description
7:0	RW	PATGEN_FTIME	00011110	Frame Time: When Auto-Scrolling is enabled, this field controls the number of frames to display each pattern, in increments of two frames. Valid register values are 1-255, giving a programmable range of the even numbers between 2 and 510, inclusive.

Pattern Generator Time Slot Configuration (PGTSC), Offset 0X10 in Table 3-4.

This register configures the number of time slots enabled for Auto-Scrolling.

Table 3-22. Pattern Generator Time Slot Configuration (PGTSC)

Bit	Access	Field	Default (bin)	Description
7:4		Reserved	0000	Reserved: Reads return 0, writes are ignored.
3:0	RW	PATGEN_TSLOT	1110	Time Slots: This field configures the number of enabled time slots for Auto-Scrolling. Valid values are 1-14 (925Q/921/926Q) or 1-16 (All other aforementioned devices).

Pattern Generator Time Slot Order 1 (PGTSO1), Offset 0X11 in Table 3-4.

This register configures patterns for Time Slots 1 and 2.

Table 3-23. Pattern Generator Time Slot Order 1 (PGTSO1)

Bit	Access	Field	Default (bin)	Description
7:4	RW	PATGEN_TS2	0010	Time Slot 2 Pattern: This field configures the pattern enabled in Time Slot 2. Valid values are 1-14 (925Q/921/926Q) or 0-15 (All other aforementioned devices).
3:0	RW	PATGEN_TS1	0001	Time Slot 1 Pattern: This field configures the pattern enabled in Time Slot 1. Valid values are 1-14 (925Q/921/926Q) or 0-15 (All other aforementioned devices).

Pattern Generator Time Slot Order 2 (PGTSO2), Offset 0X12 in Table 3-4.

This register configures patterns for Time Slots 3 and 4.

Table 3-24. Pattern Generator Time Slot Order 2 (PGTSO2)

Bit	Access	Field	Default (bin)	Description
7:4	RW	PATGEN_TS4	0100	Time Slot 4 Pattern: This field configures the pattern enabled in Time Slot 4. Valid values are 1-14 (925Q/921/926Q) or 0-15 (All other aforementioned devices).
3:0	RW	PATGEN_TS3	0011	Time Slot 3 Pattern: This field configures the pattern enabled in Time Slot 3. Valid values are 1-14 (925Q/921/926Q) or 0-15 (All other aforementioned devices).

Pattern Generator Time Slot Order 3 (PGTSO3), Offset 0X13 in Table 3-4.

This register configures patterns for Time Slots 5 and 6.

Table 3-25. Pattern Generator Time Slot Order 3 (PGTSO3)

Bit	Access	Field	Default (bin)	Description
7:4	RW	PATGEN_TS6	0110	Time Slot 6 Pattern: This field configures the pattern enabled in Time Slot 6. Valid values are 1-14 (925Q/921/926Q) or 0-15 (All other aforementioned devices).

Table 3-25. Pattern Generator Time Slot Order 3 (PGTSO3) (continued)

Bit	Access	Field	Default (bin)	Description
3:0	RW	PATGEN_TS5	0101	Time Slot 5 Pattern: This field configures the pattern enabled in Time Slot 5. Valid values are 1-14 (925Q/921/926Q) or 0-15 (All other aforementioned devices).

Pattern Generator Time Slot Order 4 (PGTSO4), Offset 0X14 in Table 3-4.

This register configures patterns for Time Slots 7 and 8.

Table 3-26. Pattern Generator Time Slot Order 4 (PGTSO4)

Bit	Access	Field	Default (bin)	Description
7:4	RW	PATGEN_TS8	1000	Time Slot 8 Pattern: This field configures the pattern enabled in Time Slot 8. Valid values are 1-14 (925Q/921/926Q) or 0-15 (All other aforementioned devices).
3:0	RW	PATGEN_TS7	0111	Time Slot 7 Pattern: This field configures the pattern enabled in Time Slot 7. Valid values are 1-14 (925Q/921/926Q) or 0-15 (All other aforementioned devices).

Pattern Generator Time Slot Order 5 (PGTSO5), Offset 0X15 in Table 3-4.

This register configures patterns for Time Slots 9 and 10.

Table 3-27. Pattern Generator Time Slot Order 5 (PGTSO5)

Bit	Access	Field	Default (bin)	Description
7:4	RW	PATGEN_TS10	1010	Time Slot 10 Pattern: This field configures the pattern enabled in Time Slot 10. Valid values are 1-14 (925Q/921/926Q) or 0-15 (All other aforementioned devices).
3:0	RW	PATGEN_TS9	1001	Time Slot 9 Pattern: This field configures the pattern enabled in Time Slot 9. Valid values are 1-14 (925Q/921/926Q) or 0-15 (All other aforementioned devices).

Pattern Generator Time Slot Order 6 (PGTSO6), Offset 0X16 in Table 3-4.

This register configures patterns for Time Slots 11 and 12.

Table 3-28. Pattern Generator Time Slot Order 6 (PGTSO6)

Bit	Access	Field	Default (bin)	Description
7:4	RW	PATGEN_TS12	1100	Time Slot 12 Pattern: This field configures the pattern enabled in Time Slot 12. Valid values are 1-14 (925Q/921/926Q) or 0-15 (All other aforementioned devices).
3:0	RW	PATGEN_TS11	1011	Time Slot 11 Pattern: This field configures the pattern enabled in Time Slot 11. Valid values are 1-14 (925Q/921/926Q) or 0-15 (All other aforementioned devices).

Pattern Generator Time Slot Order 7 (PGTSO7), Offset 0X17 in Table 3-4.

This register configures patterns for Time Slots 13 and 14.

Table 3-29. Pattern Generator Time Slot Order 7 (PGTSO7)

Bit	Access	Field	Default (bin)	Description
7:4	RW	PATGEN_TS14	1110	Time Slot 14 Pattern: This field configures the pattern enabled in Time Slot 14. Valid values are 1-14 (925Q/921/926Q) or 0-15 (All other aforementioned devices).

Table 3-29. Pattern Generator Time Slot Order 7 (PGTSO7) (continued)

Bit	Access	Field	Default (bin)	Description
3:0	RW	PATGEN_TS13	1101	Time Slot 13 Pattern: This field configures the pattern enabled in Time Slot 13. Valid values are 1-14 (925Q/921/926Q) or 0-15 (All other aforementioned devices).

Pattern Generator Time Slot Order 8 (PGTSO8), Offset 0X18 in Table 3-4.

This register configures patterns for Time Slots 15 and 16.

Table 3-30. Pattern Generator Time Slot Order 8 (PGTSO8, Not available on 925Q/921/926Q)

Bit	Access	Field	Default (bin)	Description
7:4	RW	PATGEN_TS16	0000	Time Slot 16 Pattern: This field configures the pattern enabled in Time Slot 16. Valid values are 0-15.
3:0	RW	PATGEN_TS15	1111	Time Slot 15 Pattern: This field configures the pattern enabled in Time Slot 15. Valid values are 0-15.

Pattern Generator BIST Errors (PGBE, Only Available on DS90Ux948-Q1 and DS90Ux940-Q1/ DS90Ux940N-Q1), Offset 0X19 in Table 3-4.

This register is used for reading back error counts from PATGEN BIST (Built in Self Test).

Table 3-31. Pattern Generator BIST Errors (PGBE, Only Available on DS90Ux948-Q1 and DS90Ux940-Q1/ DS90Ux940N-Q1)

Bit	Access	Field	Default (bin)	Description
7:0	R	PATGEN_BIST_ERRS	00000000	PATGEN BIST error count - Clear on read

Pattern Generator Clock Divider M Configuration (PGCDC2, Only Available on DS90Ux941AS-Q1, DS90Ux949-Q1, DS90Ux949A-Q1, DS90Ux929-Q1, and DS90Ux947-Q1), Offset 0X1A in Table 3-4.

This register configures the M divider value for the 941AS/949/949A/929/947 device. Adjusting this value can enable usage of the 800MHz nominal clock instead of the 200MHz nominal clock. When using 800MHz clock PATGEN, it is recommended to force the FPD-Link single/dual mode to prevent the device from falsely detecting the single/dual operational mode. See the DUAL_CTL1 register in the corresponding serializer for settings to force either single or dual FPD-Link.

Table 3-32. Pattern Generator Clock Divider M Configuration (PGCDC2, Only Available on DS90Ux941AS-Q1, DS90Ux949-Q1, DS90Ux949A-Q1, DS90Ux929-Q1, and DS90Ux947-Q1)

Bit	Access	Field	Default (bin)	Description
7:5	R	RESERVED	0000	
4:0	RW	PATGEN_CDIV_M	0001	Clock Divider: This field configures the "M" clock divider for the internally generated pixel clock on the 941AS/949/949A/ 929/947. If PGCDC2:PGEN_CDIV_M is 1, the internal pixel clock frequency is nominally (200/N) MHz. If PGCDC2:PGEN_CDIV_M is greater than 1, the internal pixel clock frequency is nominally (800*M/N) MHz.

4 Configuration Examples

4.1 Auto-Scrolling Configuration

This example configures the Pattern Generator to scroll through a sequence of Red, Green, Blue, with each pattern displayed for 60 video frames, using external timing:

1. Write 0x1E to the PGFT register (Table 3-21). This sets the frame timer to 60.
2. Write 0x03 to the PGTSC register (Table 3-22). This sets the number of active patterns to 3.
3. Write 0x43 to the PGTSO1 register (Table 3-23). This sets Pattern 1 to Red (3) and Pattern 2 to Green (4).
4. Write 0x05 to the PGTSO2 register (Table 3-24). This sets Pattern 3 to Blue (5); Pattern 4 is ignored.

5. Write 0x01 to the PGCFG register (Table 3-1) to enable Auto-Scrolling with external timing.
6. Write 0x01 to the PGCTL register (Table 3-1) to enable the pattern generator.

4.2 Internal Default Timing Configuration

This example configures the Pattern Generator internal default timing values as shown in Table 3-8:

1. Write 0x03 to address 0x65 PGCFG (Table 3-1) to enable 24-bit with internal Clock.
2. **(DS90Ux928Q-Q1 and DS90UB924-Q1 only)** Write 0x02 to address 0x39 (PG INT CLK) to enable Pattern Generator Internal Clock
3. Write 0x11 to address 0x64 PGCTL (Table 3-1) enable pattern generator with White/Black pattern or 1 of 14 patterns that provided.

4.3 Custom Display Configuration

This example configures the pattern generator for a custom resolution with the pixel clock and all timing signals generated internally:

Table 4-1. Custom Display Example

Parameter	Value	Units
Pixel Clock	37.007	MHz
Total Horizontal Width	1176	pixels
Total Vertical Height	525	pixels
Active Horizontal Width	800	pixels
Active Vertical Height	480	pixels
Horizontal Sync Width	10	pixels
Vertical Sync Width	2	pixels
Horizontal Back Porch	216	pixels
Vertical Back Porch	35	pixels
Horizontal Sync Polarity	Negative	-
Vertical Sync Polarity	Negative	-

Configuration Sequence

1. Set Pixel Clock and Active Frame Size. **Active H Width:** 800 (dec) = 0011 0010 0000 (bin), **Active V Height:** 480 (dec) -> 0001 1110 0000 (bin)
   a. Write 0x03 (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGCDC1, then write 0x06 (Table 3-9) to address 0x67 PGID (Table 3-2) to set the clock divider to be 6 (200/33.3).
   b. Write 0x07 (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGAFS1, then write 0x20 (Table 3-13) to address 0x67 PGID (Table 3-2) to set desired Active Horizontal Width.
   c. Write 0x08 (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGAFS2, then write 0x03 (Table 3-14) to address 0x67 PGID (Table 3-2) to set desired Active Vertical and Horizontal Widths.
   d. Write 0x09 (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGAFS3, then write 0x1E (Table 3-15) to address 0x67 PGID (Table 3-2) to set desired Active Vertical Width.

Note

33.3 MHz (200/6) is the closest available frequency to the desired 37.007 MHz. 200 MHz clock can be anywhere from 140 MHz to 260 MHz, so the generated pixel clock can be between 23.3 MHz and 43.3 MHz, with a nominal value of 33.3 MHz. Therefore, the internal timing with an external, more accurate pixel clock is allowed by setting 0x65 bit 3 (Table 3-1).

2. Set Total Frame Size. **Total H Width:** 1176 (dec) -> 0100 1001 1000 (bin), **Total V Width:** 525 (dec) -> 0010 0000 1101 (bin)
   a. Write 0x04 (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGTFS1, then write 0x98 (Table 3-10) to 0x67 PGID (Table 3-2) to set desired Total Horizontal Width.

b. Write 0x05 (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGTFS2, then write 0xD4 (Table 3-14) to address 0x67 PGID (Table 3-2) to set desired Total Vertical and Horizontal Widths.
c. Write 0x06 (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGTFS3, then write 0x20 (Table 3-12) to address 0x67 PGID (Table 3-2) to set desired Total Vertical Width.

3. Set Back Porch. **H Back Porch:** 216 (dec) CLK (effective from 217th CLK -> 1101 1000 (bin), **V Back Porch:** 35 (dec) lines (effective from 36th line -> 0010 0011 (bin)
   a. Write 0x0C (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGHBP, then write 0xD8 (Table 3-18) to address 0x67 PGID (Table 3-2) to set desired Horizontal Back Porch Width.
   b. Write 0x0D (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGVBP, then write 0x23 (Table 3-19) to address 0x67 PGID (Table 3-2) to set desired Vertical Back Porch Width.
4. Set Sync Widths. **H Sync Width:** 10 (dec) pixels 1010 (bin), **V Sync Width:** 2 (dec) lines 0010 (bin)
   a. Write 0x0A (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGHSW, then write 0x0A (Table 3-18) to address 0x67 PGID (Table 3-2) to set desired Horizontal Sync Width.
   b. Write 0x0B (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGVSW, then write 0x02 (Table 3-19) to address 0x67 PGID (Table 3-2) to set desired Vertical Sync Width.
5. Set Sync Polarities.
   a. Write 0x0E (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PBSC, then write 0x03 (Table 3-18) to address 0x67 PGID (Table 3-2) to set desired horizontal and vertical sync widths to "Negative".
6. Enable Pattern Generation
   a. Write 0x03 to address 0x65 PGCFG (Table 3-2) to enable 24-bit with internal Clock.
   b. **(DS90Ux928Q-Q1 and DS90UB924-Q1 only)** Write 0x02 to address 0x39 (PG INT CLK) to enable Pattern Generator Internal Clock
   c. Write 0x11 to address 0x64 PGCTL (Table 3-2) enable Pattern Generator with White pattern or 1 of 14 patterns that provided.

4.4 1080p60 with External Clock Example Configuration

This example configures the pattern generator for a 1920x1080 60Hz output using an external PCLK reference frequency applied at the serializer input. This example can only be used with 94x devices in dual FPD Link mode:

Table 4-2. 1080p60 with External Clock Example

Parameter	Value	Units
Pixel Clock (Applied Externally)	148.5	MHz
Total Horizontal Width	2200	pixels
Total Vertical Height	1125	pixels
Active Horizontal Width	1920	pixels
Active Vertical Height	1080	pixels
Horizontal Sync Width	44	pixels
Vertical Sync Width	5	pixels
Horizontal Back Porch	148	pixels
Vertical Back Porch	36	pixels
Horizontal Sync Polarity	Positive	-
Vertical Sync Polarity	Positive	-

Configuration Sequence

1. Set Pixel Clock and Active Frame Size. **Active H Width:** 1920 (dec) = 0111 1000 0000 (bin), **Active V Height:** 1080 (dec) -> 0100 0011 1000 (bin)
   a. Write 0x07 (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGAFS1, then write 0x80 (Table 3-13) to address 0x67 PGID (Table 3-2) to set desired Active Horizontal Width.
   b. Write 0x08 (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGAFS2, then write 0x87 (Table 3-14) to address 0x67 PGID (Table 3-2) to set desired Active Vertical and Horizontal Widths.

c. Write 0x09 (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGAFS3, then write 0x43 (Table 3-15) to address 0x67 PGID (Table 3-2) to set desired Active Vertical Width.

2. Set Total Frame Size. **Total H Width:** 2200 (dec) -> 1000 1001 1000 (bin), **Total V Width:** 1125 (dec) -> 0100 0110 0101 (bin)
   a. Write 0x04 (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGTFS1, then write 0x98 (Table 3-10) to 0x67 PGID (Table 3-2) to set desired Total Horizontal Width.
   b. Write 0x05 (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGTFS2, then write 0x58 (Table 3-14) to address 0x67 PGID (Table 3-2) to set desired Total Vertical and Horizontal Widths.
   c. Write 0x06 (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGTFS3, then write 0x46 (Table 3-12) to address 0x67 PGID (Table 3-2) to set desired Total Vertical Width.
3. Set Back Porch. **H Back Porch:** 148 (dec) 1001 0100 (bin), **V Back Porch:** 36 (dec) lines 0010 0100 (bin)
   a. Write 0x0C (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGHBP, then write 0x94 (Table 3-18) to address 0x67 PGID (Table 3-2) to set desired Horizontal Back Porch Width.
   b. Write 0x0D (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGVBP, then write 0x24 (Table 3-19) to address 0x67 PGID (Table 3-2) to set desired Vertical Back Porch Width.
4. Set Sync Width. **H Sync Width:** 44 (dec) pixels 0010 1100 (bin), **V Sync Width:** 5 (dec) lines 0101 (bin)
   a. Write 0x0A (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGHSW, then write 0x2C (Table 3-18) to address 0x67 PGID (Table 3-2) to set desired Horizontal Sync Width.
   b. Write 0x0B (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PGVSW, then write 0x05 (Table 3-19) to address 0x67 PGID (Table 3-2) to set desired Vertical Sync Width.
5. Set Sync Polarities.
   a. Write 0x0E (Table 3-2) to address 0x66 PGIA (Table 3-2) to enable PBSC, then write 0x00 (Table 3-18) to address 0x67 PGID (Table 3-2) to set desired horizontal and vertical sync polarities to "Positive".
6. Enable Pattern Generation
   a. Write 0x0C to address 0x65 PGCFG (Table 3-2) to set external clock and internal PATGEN timing.
   b. Write 0x05 to address 0x64 PGCTL (Table 3-2) to enable PATGEN with color bars.

4.5 Resolution Readback Example

This example configures the DS90Ux947-Q1 serializer to allow for measuring the detected active video dimensions at the DS90Ux948-Q1 deserializer during operation. This feature can be used to detect a video transmission error by comparing the expected active resolution against the detected resolution. Note that this feature should only be used during system statup, and should not be left permenantly enabled during normal operation. Enabling this feature will disable the use of the LOCK pin as a link indicator, and will cause one white pixel to appear randomly in the video output for one frame at the time of enabling/disabling. For this reason it is best to enable this readback feature during system startup before the display backlight has been enabled, to avoid visual disruption.

Configuration Sequence

1. Check the recovered active horizontal and vertical frame dimensions.
   a. Write 0x09 to address 0x68 PGDBG (Table 3-2) to select active horizontal LSB and trigger an update of the test mux data.
   b. Read 0x69 PGTSTDAT (Table 3-2) and record bits [5:0] as "AHL".
   c. Write 0x19 to address 0x68 PGDBG (Table 3-2) to select active horizontal MSB and trigger an update of the test mux data.
   d. Read 0x69 PGTSTDAT (Table 3-2) and record bits [5:0] as "AHM".
   e. Write 0x29 to address 0x68 PGDBG (Table 3-2) to select active vertical LSB and trigger an update of the test mux data.
   f. Read 0x69 PGTSTDAT (Table 3-2) and record bits [5:0] as "AVL".
   g. Write 0x39 to address 0x68 PGDBG (Table 3-2) to select active horizontal MSB and trigger an update of the test mux data.
   h. Read 0x69 PGTSTDAT (Table 3-2) and record bits [5:0] as "AVM".
   i. Calculate active horizontal pixels [11:0] = [AHM:AHL] (Table 3-2) (for example, AHM = 011110b, AHL = 000000b, Active horizontal pixels = 011110000000b = 0x780 = 1920 pixels).

j. Calculate active vertical pixels [11:0] = [AVM:AVL] (Table 3-2) (for example AVM = 010000b, AVL = 111000b, Active horizontal pixels = 010000111000b = 0x438 = 1080 pixels).

2. Compare measured active horizontal and vertical pixel dimensions to expected values for the external video source attached to the serializer side.
3. Disable readback features

a. Write 0x00 to address 0x68

5 Conclusion

This application report gives several usage examples for the Internal Test Pattern Generator of the FPD Link III IVI devices, as well as detailed descriptions of the control registers used to control this feature.

6 References

- Texas Instruments, *DS90UB925Q-Q1 5 - 85 MHz 24-Bit Color FPD-Link III Serializer With Bidirectional Control Channel Datasheet* (SNLS407)
- Texas Instruments, *DS90UH925Q-Q1 720p 24-Bit Color FPD-Link III Serializer With HDCP Datasheet* (SNLS336)
- Texas Instruments, *DS90UB921-Q1 5 - 96 MHz 24-bit Color FPD-Link III Serializer with Bidirectional Control Channel Datasheet* (SNLS488)
- Texas Instruments, *DS90UB926Q-Q1 5 - 85 MHz 24-Bit Color FPD-Link III Deserializer With Bidirectional Control Channel Datasheet* (SNLS422)
- Texas Instruments, *DS90UH926Q-Q1 720p 24-Bit Color FPD-Link III Deserializer With HDCP Datasheet* (SNLS337)
- Texas Instruments, *DS90UB927Q-Q1 5MHz - 85MHz 24-Bit Color FPD-Link III Serializer With Bidirectional Control Channel Datasheet* (SNLS416)
- Texas Instruments, *DS90UH927Q-Q1 5MHz - 85MHz 24-Bit Color FPD-Link III Serializer With HDCP Datasheet* (SNLS433)
- Texas Instruments, *DS90UB928Q-Q1 FPD-Link III Deserializer With Bidirectional Control Channel Datasheet* (SNLS417)
- Texas Instruments, *DS90UH928Q-Q1 5MHz - 85MHz 24-Bit Color FPD-Link III Deserializer With HDCP Datasheet* (SNLS440)
- Texas Instruments, *DS90UB924-Q1 5-MHz to 96-MHz 24-bit Color FPD-Link III to OpenLDI Deserializer With Bidirectional Control Channel Datasheet* (SNLS512)
- Texas Instruments, *DS90UH948-Q1 2K FPD-Link III to OpenLDI Deserializer With HDCP Datasheet* (SNLS473)
- Texas Instruments, *DS90UB948-Q1 2K FPD-Link III to OpenLDI Deserializer Datasheet* (SNLS477)
- Texas Instruments, *DS90UH947-Q1 1080p OpenLDI to FPD-Link III Serializer with HDCP Datasheet* (SNLS455)
- Texas Instruments, *DS90UB947-Q1 1080p OpenLDI to FPD-Link III Serializer Datasheet* (SNLS454)
- Texas Instruments, *DS90UH949-Q1 1080p HDMI to FPD-Link III Bridge Serializer with HDCP Datasheet* (SNLS453)
- Texas Instruments, *DS90UB949-Q1 1080p HDMI to FPD-Link III Bridge Serializer Datasheet* (SNLS452)
- Texas Instruments, *DS90UH949A-Q1 2K HDMI-to-FPD-Link III Bridge Serializer With HDCP Datasheet* (SNLS543)
- Texas Instruments, *DS90UB949A-Q1 2K HDMI-to-FPD-Link III Bridge Serializer Datasheet* (SNLS650)
- Texas Instruments, *DS90UH941AS-Q1 2K DSI to FPD-Link III Bridge Serializer with Video Splitting and HDCP Datasheet* (SNLS633)
- Texas Instruments, *DS90UB941AS-Q1 2K DSI to FPD-Link III Bridge Serializer with Video Splitting Datasheet* (SNLS640)
- Texas Instruments, *DS90UH940N-Q1 1080p FPD-Link III to CSI-2 Deserializer With HDCP Datasheet* (SNLS613)
- Texas Instruments, *DS90UB940N-Q1 1080p FPD-Link III to CSI-2 Deserializer Datasheet* (SNLS641)

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (October 2020) to Revision G (November 2020)	Page
• Fixed typos in the supported devices for PGCDC2 register	15
• Added recommendation to force single/dual FPD-Link mode when utilizing 800MHz internal base clock on DS90Ux941AS-Q1, DS90Ux949-Q1, DS90Ux949A-Q1, DS90Ux929-Q1, and DS90Ux947-Q1	15
• Renamed PATGEN BIST Example to Resolution Readback Example and simplified steps	21

Changes from Revision E (February 2020) to Revision F (October 2020)	Page
• Added 800MHz base clock option for DS90Ux949-Q1, DS90Ux949A-Q1, DS90Ux929-Q1, and DS90Ux947-Q1	5
• Added DS90Ux949-Q1, DS90Ux949A-Q1, DS90Ux929-Q1, and DS90Ux947-Q1 to the supported list for PGCDC2	11
• Clarified supported devices which can adjust the M clock divider	12

Changes from Revision D (June 2019) to Revision E (February 2020)	Page
• Changed text to remove typos	3

Changes from Revision C (June 2013) to Revision D (June 2019)	Page
• Added 94x devices	3
• Added 921/924	3
• Edited application report for clarity	3
• Clarified supported features differences between 92x devices and between 92x vs. 94x	3
• Added 1080p60 target resolution to the Internal Oscillator Frequencies table	5
• Clarified clock generation 94x has more capability and also added 800 MHz info for 941AS	5
• Added PATGEN Bist Register	7
• Added 941AS “M” divider register	15
• Clarified target clock frequencies between devices.	15
• Added missing example code in the custom display example for setting sync polarities and widths	19
• Added 94x example code for 1080p with external PCLK	20
• Added PATGEN BIST Example section	21

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265