Application Report

DP83TC811, DP83TG720 Rollover Document

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ABSTRACT

Texas Instruments 100Base-T1 (DP83TC811) and 1000Base-T1 (DP83TG720) Automotive Ethernet PHYs have been designed such that same PCB board can be used for both of them. This application note acts as a reference guide to help design a single system that can support these devices with minor component changes.

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Trademarks

1 Introduction

Texas Instruments Automotive Ethernet PHY portfolio consists of 100Base-T1 (DP83TC811) and 1000Base-T1 (DP83TG720) devices. Automotive system qualification cycles are time consuming and any significant change in system can lead to increase in development costs. To reduce the complexity of automotive Ethernet system design, TI PHYs were design such that they can be implemented on a single system. This avoids a complete redesign of the system when going from one speed to the other based on the application requirement. To help achieve this both the devices have the same package footprint of 36 pin QFN, 6mm x 6mm.

Apart from the cable side communication speed,MAC interface selection can also affect PCB design. DP83TC811 supports MII, RMII, RGMII, and SGMII MAC interfaces. DP83TG720 supports RGMII and SGMII MAC interfaces. MII and RMII standards were defined only for 10 and 100Mbps only, so DP83TG720 does not support these options. This application report assumes that DP83TC811 will also be operated in RGMII or SGMII mode.

2 Device Comparison

2.1 Feature Comparison

Table 2-1. Device Comparison Table

Device	Speed	MAC Interface	TC-10
DP83TC811	100BASE-T1	MII, RMII,RGMII,SGMII	No
DP83TG720	1000BASE-T1	RGMII, SGMII	Yes[1]

1. DP83TG720 supports a proprietary sleep mode with both local and remote wake-up features.

2.2 Pin Map Comparison

The Pin Comparison Table shows pin comparison between DP83TC811 and DP83TG720.

Table 2-2. Pin Comparison Table

Pin No.	DP83TC811	DP83TG720
1	MDC	MDC
2	INT_N	INT_N
3	RESET_N	RESET_N
4	XO	XO
5	XI	XI
6	LED_1	LED_1
7 [1]	**EN**	**VSLEEP**
8 [2] [3]	**WAKE**	**WAKE**
9	**DNC** [4]	**VDD1P0** [6]
10 [5]	**INH**	**INH**
11	VDDA[6]	VDDA[6]
12	TRD_P	TRD_P
13	TRD_M	TRD_M
14	RX_ER	STRP1
15	RX_DV	RX_CTRL
16	CLKOUT	CLKOUT
17	**TCK**	**DNC** [4]
18	**TDO**	**DNC** [4]
19	**TMS**	**DNC** [4]
20	**TCK**	**DNC** [4]
21	**DNC** [4]	**VDD1P0** [6]
22	VDDIO[6]	VDDIO[6]
23	RX_D3[7]	RX_D3
24	RX_D2[7]	RX_D2
25	RX_D1[7]	RX_D1
26	RX_D0[7]	RX_D0
27	RX_CLK[7]	RX_CLK
28	TXCLK[7]	TXCLK
29	TX_EN[7]	TX_CTRL
30	TX_D3[7]	TX_D3
31	TX_D2[7]	TX_D2
32	TX_D1[7]	TX_D1
33	TX_D0[7]	TX_D0
34	**TX_ER**	**VDDIO** [6]
35	LED_0	LED_0

Table 2-2. Pin Comparison Table (continued)

Pin No.	DP83TC811	DP83TG720
36	MDIO	MDIO

1. Pin 7's functionality in DP83TC811 is of an input pin to put the phy in the disabled state (when low) and works on VDDIO supply domain. Whereas Pin 7 of DP83TG720 is a supply pin which must be connected to 3.3V supply (supply should be on for both functional and sleep mode).
2. Wake pin of DP83TC811 should be on VDDIO supply domain and should be asserted high for wake-up feature. Whereas Wake pin of DP83TG720 should be on VSLEEP supply domain and sending high pulse for defined duration is sufficient for wake-up feature.
3. DP83TC811 does not require turning off of any external supply for PHY to go into sleep mode. DP83TG720's supplies must be powered down for PHY to go into sleep mode. Refer to data sheet of DP83TG720 for application diagram for its sleep mode.
4. Do Not Connect : These pins must be left floating. Test structures connected to these pins and should be kept floating to avoid damage or wrong mode entry of PHY
5. DP83TC811 has INH pin on VDDIO domain and is high (Vddio level) when PHY is in sleep mode. Whereas DP83TG720 has INH pin on VSLEEP domain (3.3V) and is low when PHY is in sleep mode.
6. Refer to respective data sheets and reference schematic in this document for the power supply network requirements.
7. For Rgmii use case, layout constraint for 1Gbps Rgmii signals should be followed to facilitate reuse of MAC routes for both DP83TG720 and DP83TC811.

2.3 Strap Comparison

To maintain pin compatibility, the features associated with each strap pins are the same for both devices.

The differences between DP83TG720 and DP83TC811 straps are that some of the pins strap resistor values will be different.

2.3.1 PHY Address Straps

Table 2-3 shows the PHY address strap comparison between DP83TC811 and DP83TG720.

DP83TC811 can support 16 PHY addresses from 0x00 to 0x0F. DP83TG720 can support 9 PHY addresses: 0x00, 0x04, 0x05, 0x08, 0x0A, 0x0C, 0x0D, 0x0D, 0x0E, 0x0F. By provisioning for a pull up and pull down resistor on pin 14 and 15 of the PHY, both devices can be supported by simply changing the resistor combination.

Table 2-3. PHY Address Strap Comparison Table

Pin No.	Pin Name	DP83TC811			DP83TG720		
		STRAP MODE Table 2-4	STRAP		STRAP MODE Table 2-5	STRAP	
15	RX_DV/ RX_CTRL RX_CTRL (DP83TG720)		PHYADD[0]	PHYADD[2]		PHYADD[0]	PHYADD[2]
		Mode 1	0	0	Mode 1	0	0
		Mode 2	0	1	Mode 2	0	1
		Mode 3	1	0	NA	NA	NA
		Mode 4	1	1	Mode 3	1	1
14	RXER STRP1 (DP83TG720)		PHYADD[1]	PHYADD[3]		PHYADD[1]	PHYADD[3]
		Mode 1	0	0	Mode 1	0	0
		Mode 2	0	1	Mode 2	0	1
		Mode 3	1	0	NA	NA	NA
		Mode 4	1	1	Mode 3	1	1

Table 2-4 shows strap resistor values for DP83TC811's phy address and Table 2-5 show the recommended strap resistor values for DP83TG720's phy address. RH are pull-up resistors and RL are pull down resistors.

Table 2-4. Recommended 4-level Strap Resistor Ratios For DP83TC811

MODE	IDEAL RH (kΩ)[1] for VDDIO = 3.3 V/2.5V/1.8V	IDEAL RL (kΩ)[1] for VDDIO = 3.3 V/2.5V/1.8V
1	OPEN	OPEN
2	10	2.49
3	5.76	2.49
4	2.49	OPEN

1. 1% resistor accuracy

Table 2-5. Recommended 3-level Strap Resistor Ratios for DP83TG720

MODE	IDEAL RH (kΩ) [1] for VDDIO = 3.3 V	IDEAL RH (kΩ) [2] for VDDIO = 2.5 V	IDEAL RH (kΩ)[1] for VDDIO = 1.8V
1	OPEN	OPEN	OPEN
2	13	12	4
3	4.5	2	0.8

1. 10% resistor accuracy
2. 1% resistor accuracy

2.3.2 MAC Interface, Master/Slave, Autonomous Strap

Strap features on RX_D0, RX_D1, RX_D2, LED_0, and LED_1 are same for all four devices. They can be used by keeping the strap resistors open or by using a pull up resistor. Test Mode straps are not not supported on DP83TG720. This allows those strap pins to be used as two level straps. The two PHYs can be configured in Test Modes via register access.

When strap resistors are not used, the PHY's internal pull down resistors will configure the PHY in Mode 1 by default. However, for LED pins it is recommended to use pull down resistor in parallel with the an LED when using Mode 1.

Table 2-6. MAC Interface, Master/Slave, Autonomous Strap Comparison Table

PIN NO.	PIN NAME	DP83TC811			DP83TG720		
		STRAP MODE Table 2-7	STRAP		STRAP MODE Table 2-8	STRAP	
26	RX_D0		MAC[0]	TEST[0]		MAC[0]	NA
		Mode 1	0	0	Mode 1	0	
		Mode 2	0	1	NA	NA	
		Mode 3	1	0	NA	NA	
		Mode 4	1	1	Mode 2	1	
25	RX_D1		MAC[1]	TEST[1]		MAC[1]	NA
		Mode 1	0	0	Mode 1	0	
		Mode 2	0	1	NA	NA	
		Mode 3	1	0	NA	NA	
		Mode 4	1	1	Mode 2	1	
24	RX_D2		MAC[1]	TEST[2]		MAC[2]	NA
		Mode 1	0	0	Mode 1	0	
		Mode 2	0	1	NA	NA	
		Mode 3	1	0	NA	NA	
		Mode 4	1	1	Mode 2	1	
35	LED_0		MS	RESERVED		MS	NA
		Mode 1	0		Mode 1	0	
		Mode 2	RESERVED	RESERVED	NA	NA	
		Mode 3	RESERVED	RESERVED	NA	NA	
		Mode 4	1		Mode 2	1	
6	LED_1		RESERVED		RESERVED		
		Mode 1	0		Mode 1	0	
		Mode 2	RESERVED	RESERVED	NA	NA	
		Mode 3	RESERVED	RESERVED	NA	NA	
		Mode 4	1		Mode 2	1	

Required strap resistor values for MAC, Master/Slave and Autonomous mode configurations are in Table 2-7 for DP83TC811 and in Table 2-8 for DP83TG720.

Table 2-7. Recommended Resistor Ratios For DP83TC811's MAC, Master/Slave and Autonomous mode configurations: 4-level straps

MODE	IDEAL RH (kΩ)	IDEAL RL (kΩ)
1	OPEN	OPEN
2	10	2.49
3	5.76	2.49
4	2.49	OPEN

Table 2-8. Recommended Resistor Ratios For DP83TG720's MAC, Master/Slave and Autonomous mode configurations: 2-level straps

MODE	IDEAL RH (kΩ)
1	OPEN
2	2.49

2.4 Power-Supply Comparison

DP83TC811 has two power supply rails, VDDA and VDDIO. VDDA support 3.3 V operation while VDDIO supports 1.8 V, 2.5 V, and 3.3 V. Each pin is recommended to have 4 decoupling capacitors (10µF, 1µF, 0.1µF, 100nF) with optional series ferrite beads. Additionally EN pin can be connected to VDDIO. Refer to DP83TC811's data sheet's *Power Supply Recommendation* section.

DP83TG720 has four supply rails VDDA, VDDIO, VDDA1P0, VSLEEP. VSLEEP should be stable even when the PHY is in the sleep mode. Supply pins 22,21,9 and 11 are recommended to have 3 decoupling capacitors (2.2µF, 0.1µF, 100nF) close to the pins. For supply pin 34, 2 decoupling capacitors (0.1uF and 100nF) should be sufficient. VSLEEP (for sleep mode application) should come from a 3.3 V LDO which is active during sleep mode also. For applications not using sleep mode, pin 7 can be connected to pin 11. VDDA, VDDIO, VDD1P0 also need series ferrite bead. Refer to DP83TG720's data sheet's *Power Supply Recommendation* section for full component and connection details.

Note

- TP784105-Q1 (TPS784105QWDRBRQ1) has been optimized at 1.05V to be DP83TG720's dedicated companion LDO for vdd1p0 supply. Tuning of the LDO to 1.05V takes care of the votlage drop due to ferrite bead's DC impedance and switching current of PHY, insuring that DP83TG720 gets required voltage level at the pin .
- TPS7B81-Q1 is the recommended LDO for DP83TG720's VSleep. Ultra-low quiescent current of TPS7B81-Q1 makes it the right choice for sleep mode application.

2.5 MDI Comparison

LPF

DP83TC811 data sheet recommends optional LPF to pass OA EMC emission tests. DP83TG720 all have integrated LPF to improve EMC performance. On-board LPF components should not be used while using DP83TG720.

CMC

CMC for 100Base-T1 devices and 1000Base-T1 devices are different. When changing PHYs between100Base-T1 and 1000Base-T1, CMC needs to be changed accordingly. CMC recommendations are included in device data sheets.

3 Reference Schematics

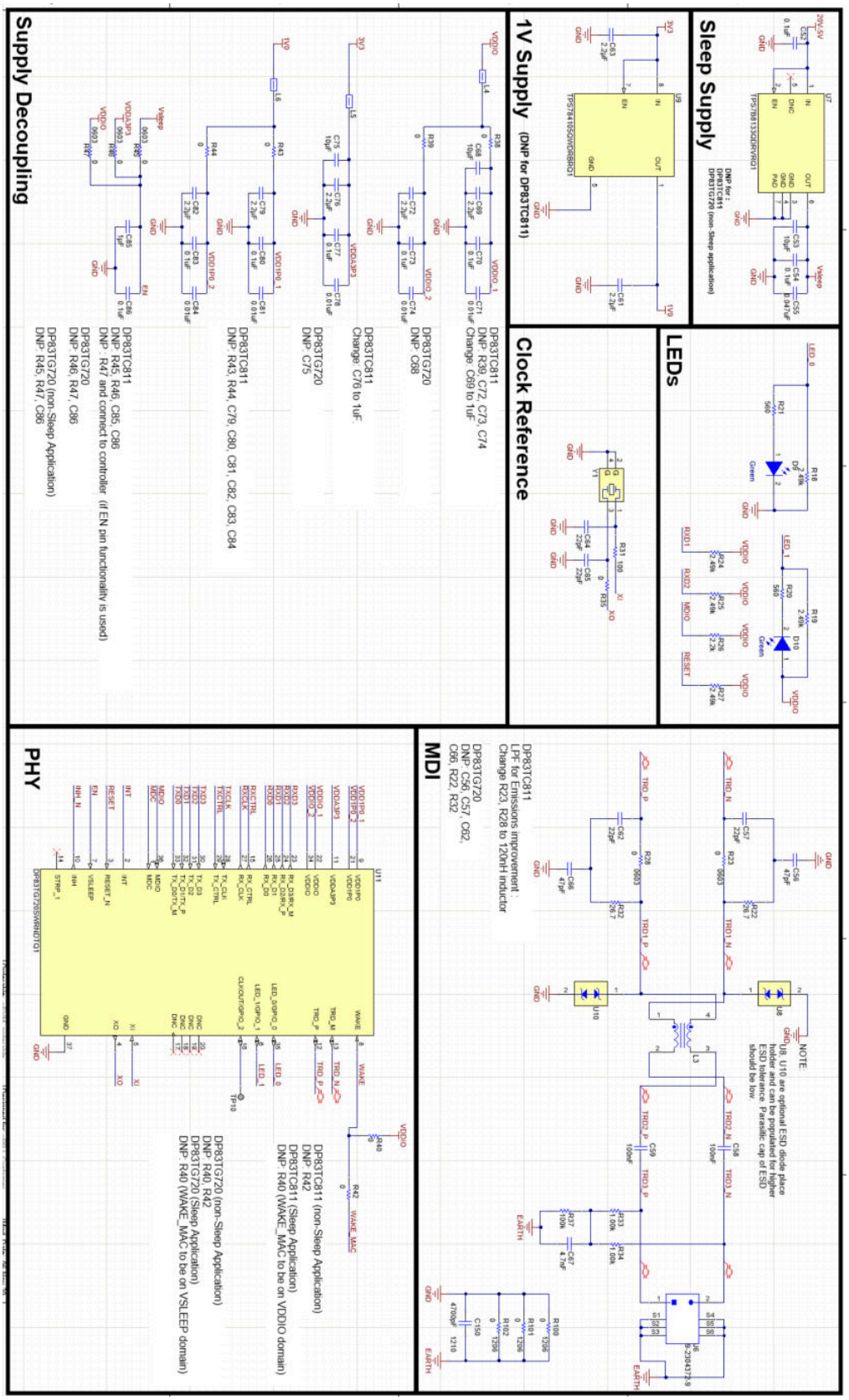

Figure 3-1. Rgmii Reference Schematic

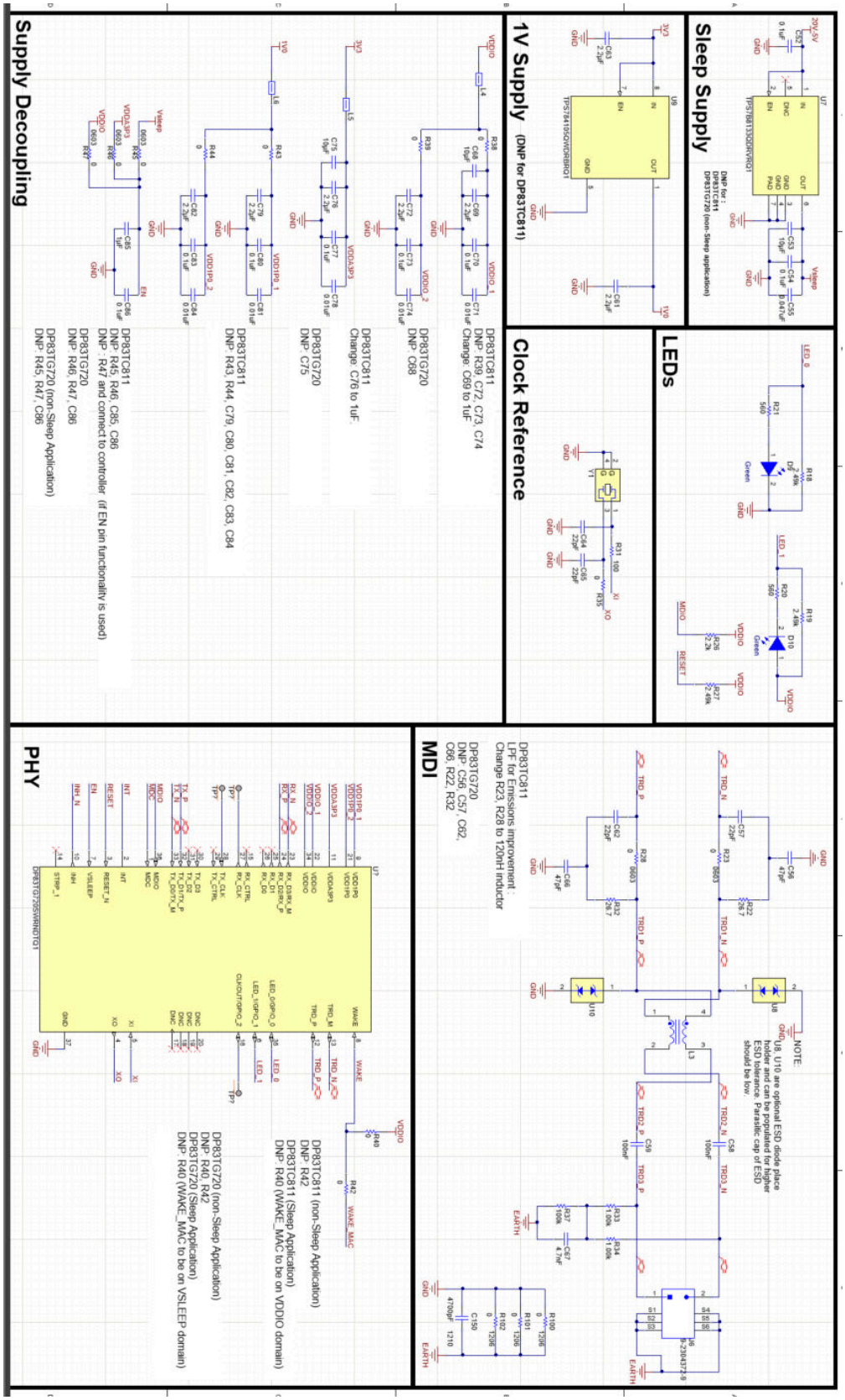

Figure 3-2. Sgmii Reference Schematic

4 Summary

This application note discusses the differences between the two Ethernet PHYs and details how these differences can be accommodated on a single design. With proper component selection and place-holders, same PCB can be re-used for DP83TC811 and DP83TG720. Layout constraints of gigabyte PHY are recommended to be followed (for example RGMII constraints for gigabyte speed) to have the board's parasitics/ delays suitable for both DP83TG720 and DP83TC811.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2020) to Revision A (December 2020)	Page
• Added Power-Supply Comparison Note	8

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