NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P1P2V" represents connection to the +1.2V power plane.
2. The netname "P1P9V" represents connection to the +1.9V power plane.
3. The netname "P3P3V" represents connection to the +3.3V power plane.
4. The netname "P2P5V" represents connection to the +2.5V power plane.
5. The netname "P5V" represents connection to the +5.0V power plane.
6. The netname "P12V" represents connection to the +12.0V power plane.
7. The netname "GND" represents connection to the ground plane.
8. A "Z" suffix on a signal name indicates an active low signal.
9. All components with designators "U*", "Q*", and "D*" are electrostatic discharge sensitive.
10. All components with designators above 500 are mounted solder side of the board.
11. All resistor values are in ohms.
12. All capacitor values in microfarads unless otherwise specified.

COMPUTER GENERATED DRAWING - DO NOT REVISE MANUALLY

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 2128668: Initial Release	12/06/2012	HPC
B	ECO 2134134: REV B	06/18/2013	HPC
C	ECO 2135374: REV C	08/15/2013	HPC

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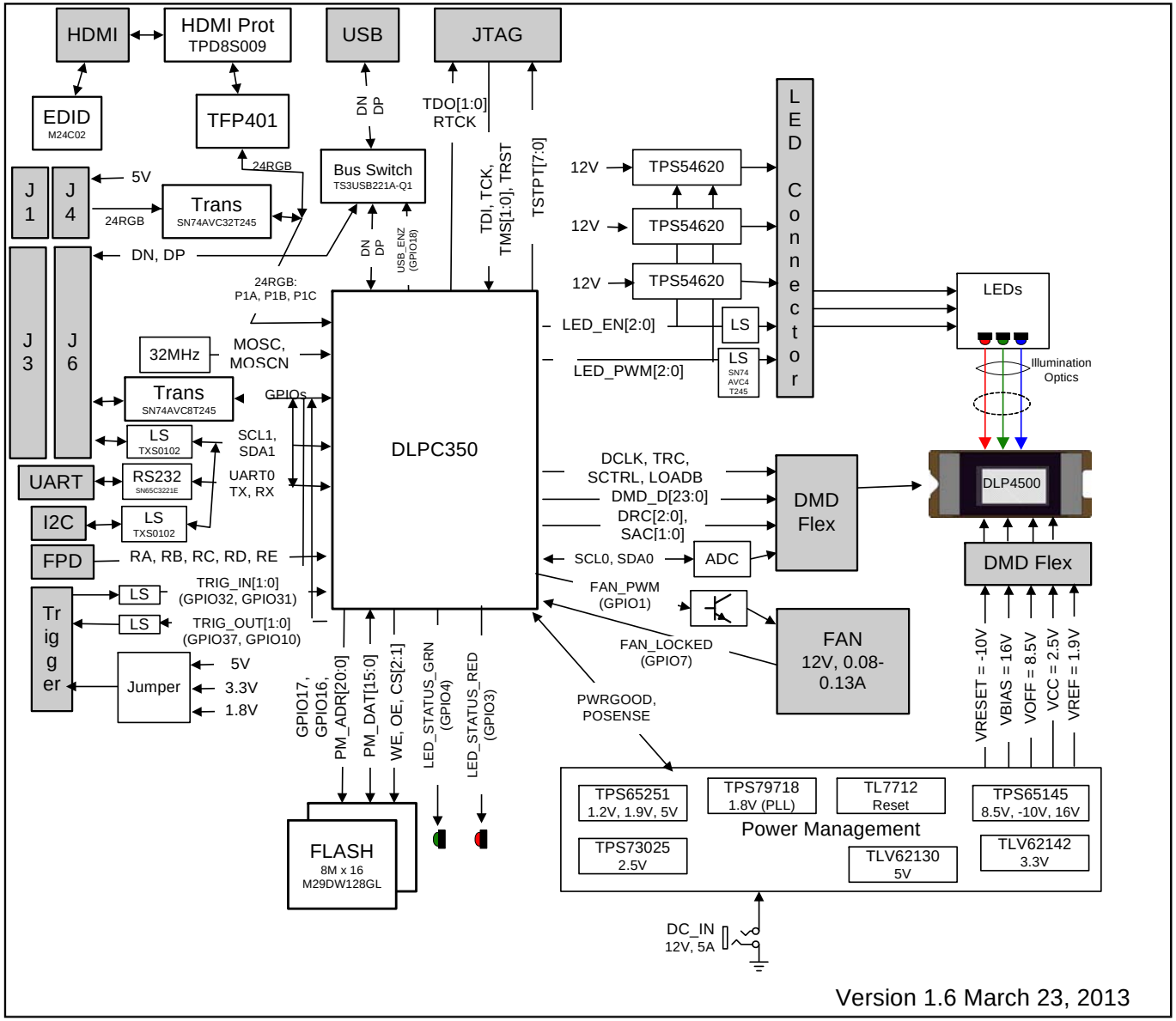
		DWN / DATE 08/15/2013	TEXAS INSTRUMENTS
		ENGR 08/15/2013	© COPYRIGHT 2010 TEXAS INSTRUMENTS ALL RIGHTS RESERVED
		APVD 08/15/2013	
		MFG	TITLE: ESD, LIGHTCRAFTER 4500
N/A	0314PO	QA	
NEXT ASSY	USED ON		A3 / DRAWING NO 2512909 / REV D
APPLICATION		SW Allegro Design Entry 16.5	SCALE / SHEET 1 of 29

BLOCK DIAGRAM



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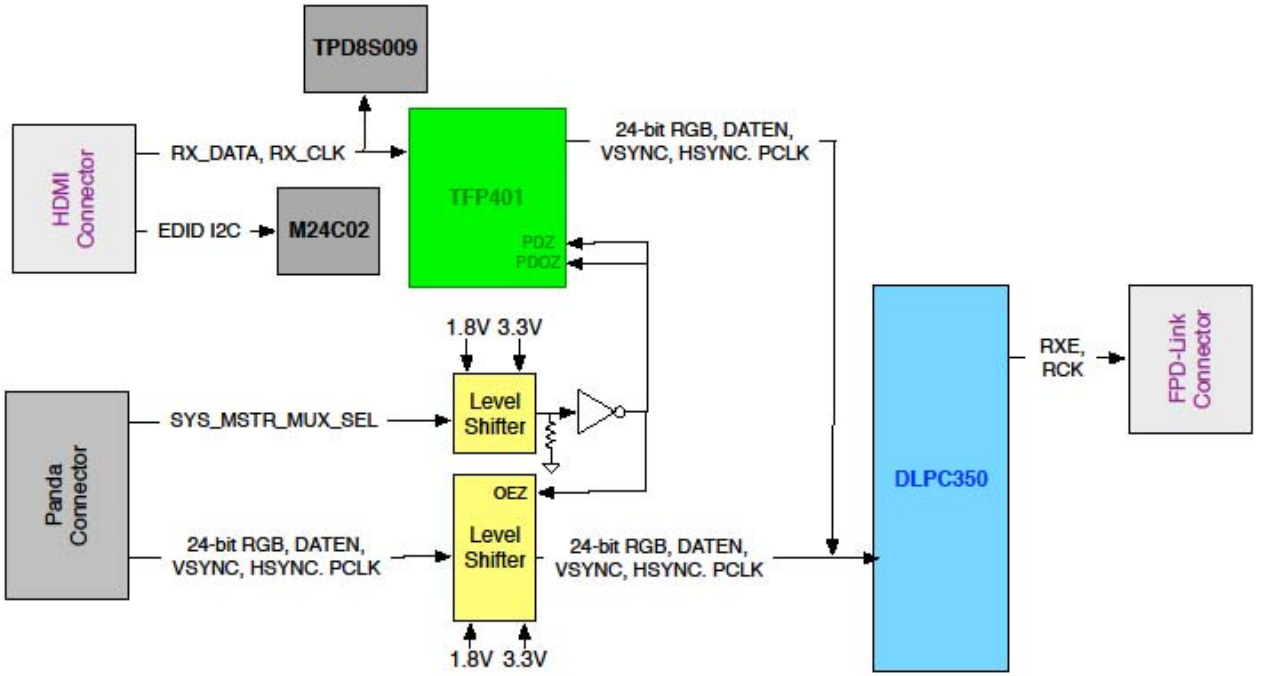
Video Input and Muxing



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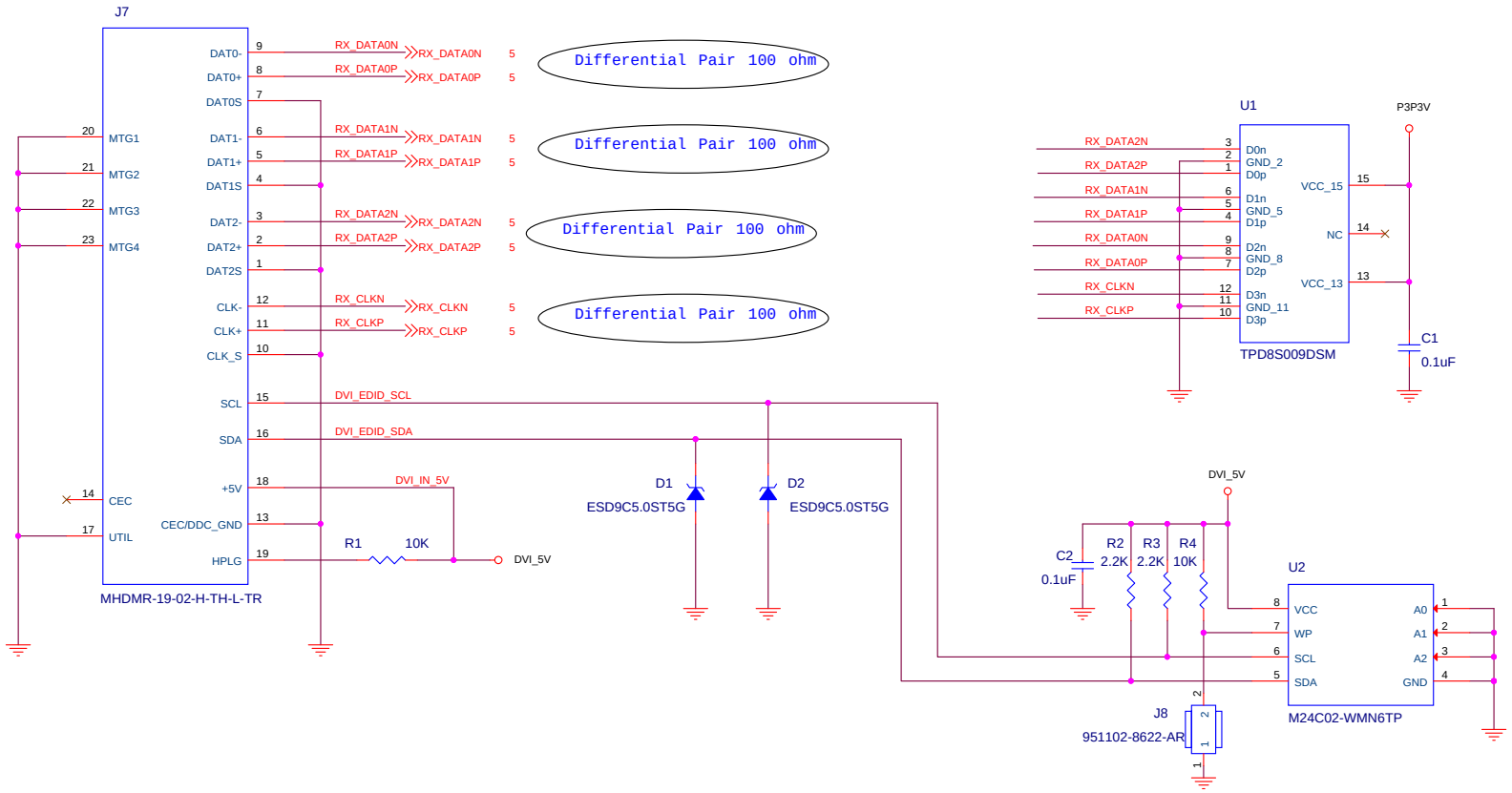

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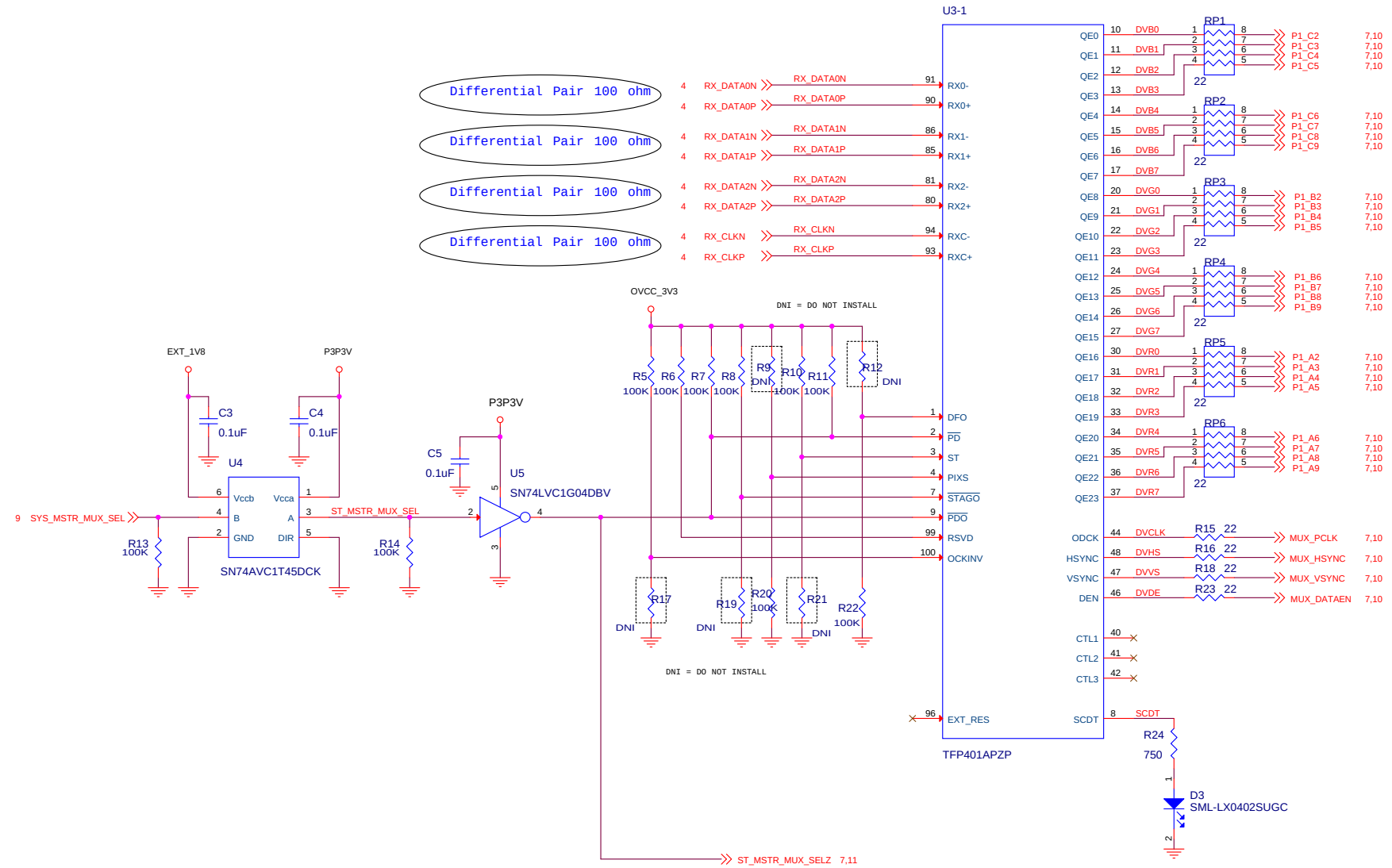
	ISSUE DATE		SCALE	SHEET 4 OF 29	



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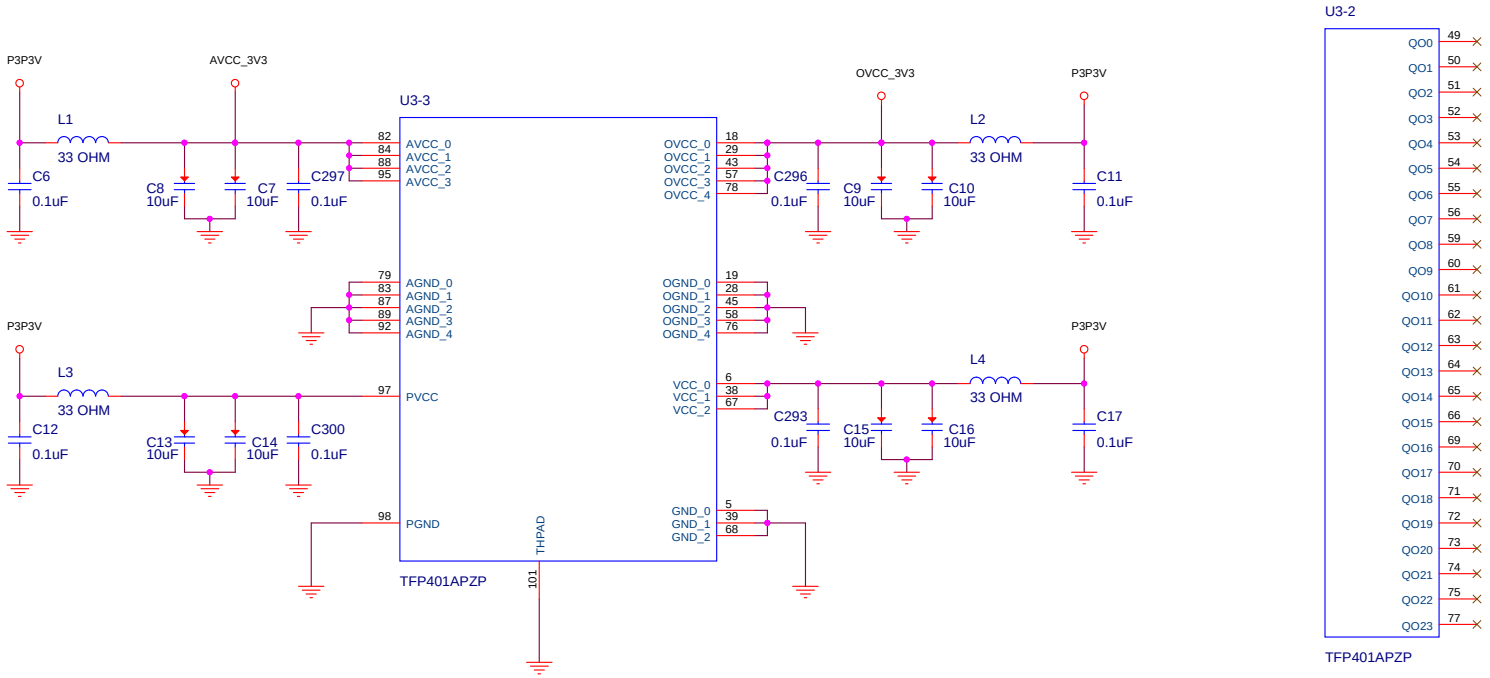
	ISSUE DATE		SCALE	SHEET 5 OF 29	



TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909	REV D
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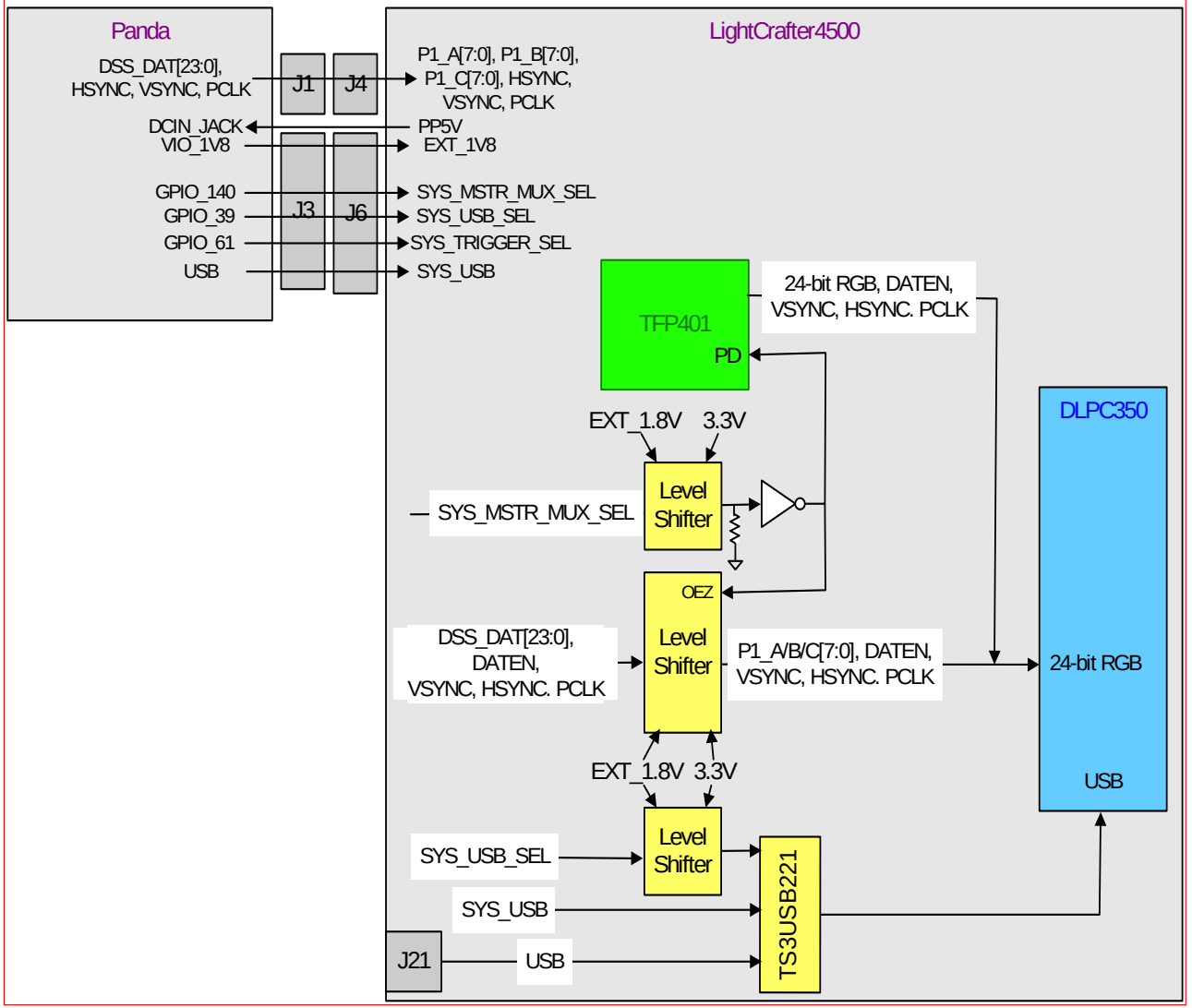
Panda Connections



Panda to LightCrafter 4500 Connections

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV D
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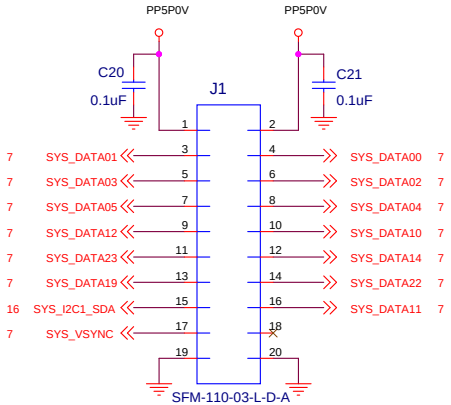
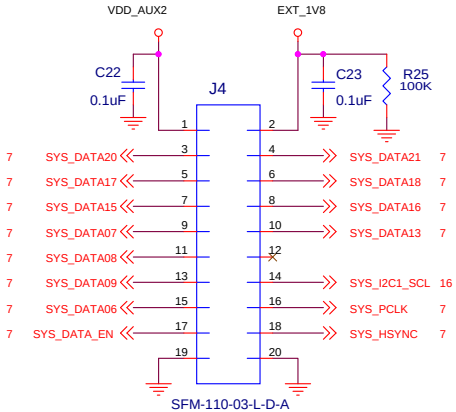
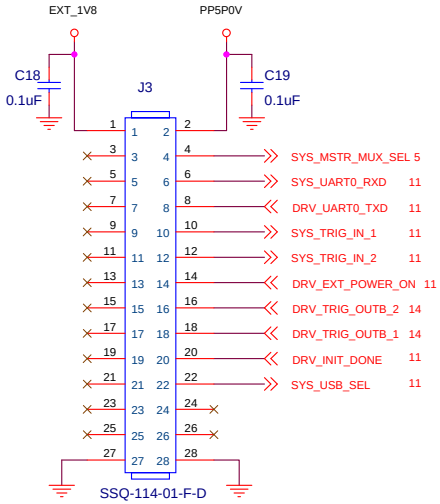
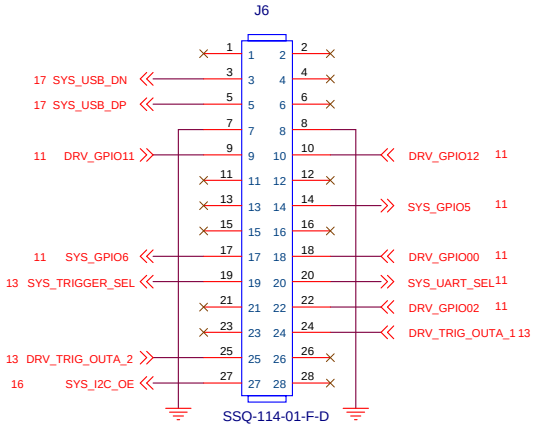




PANDA DATA PATH CONNECTORS



PANDA I/O CONNECTOR



PANDA I/O CONNECTOR

Processor Interface ConnectorS

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV D
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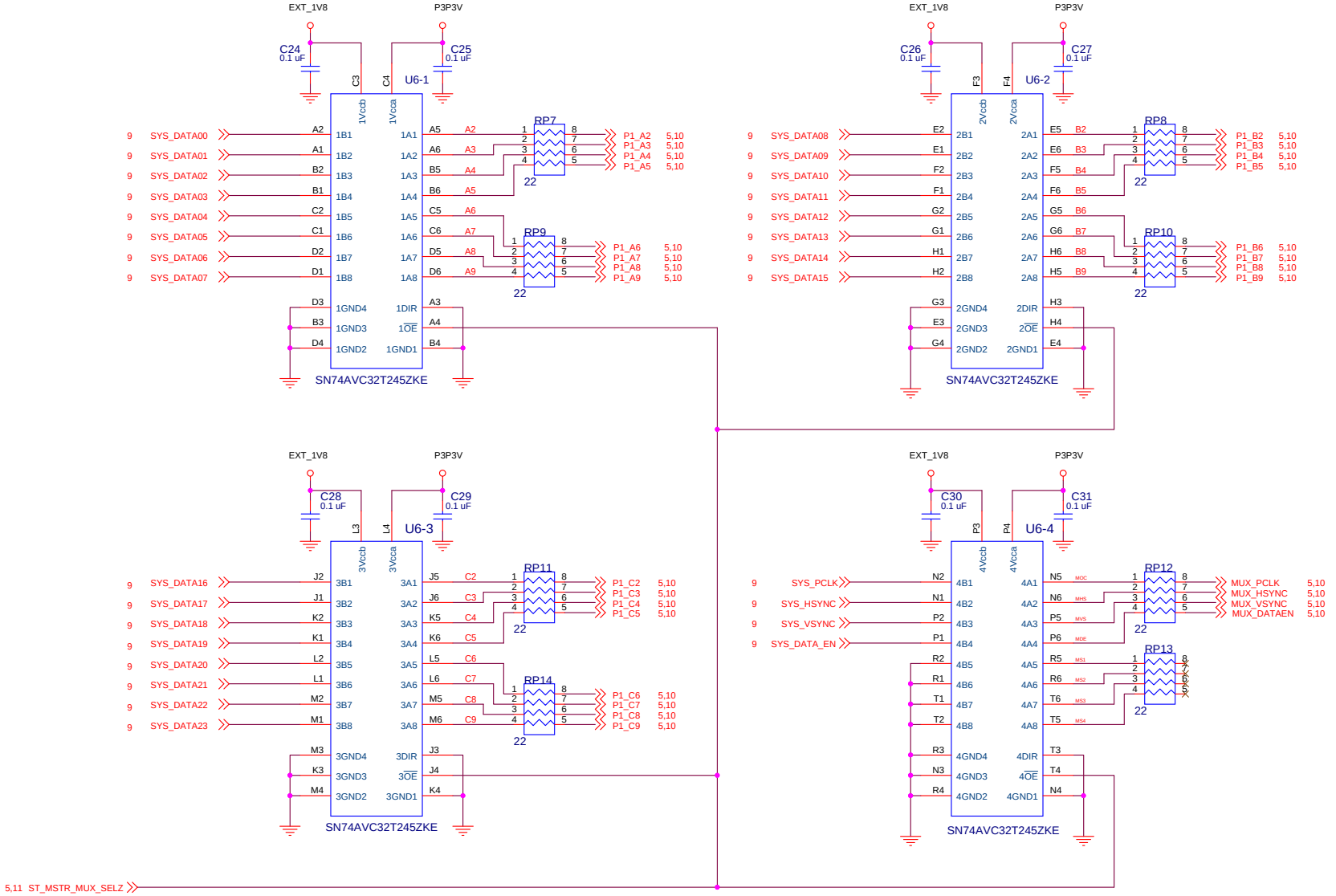

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909	REV D
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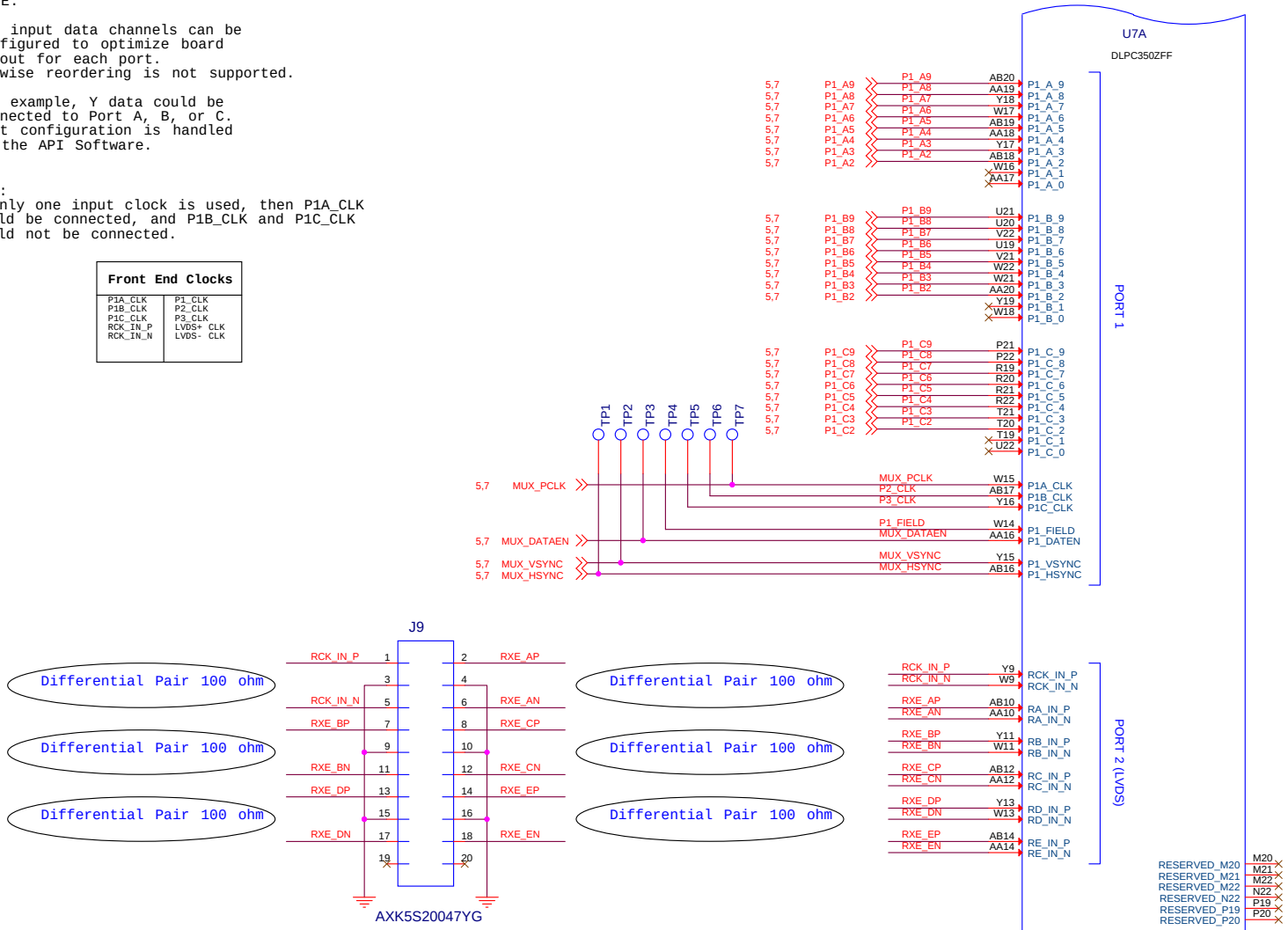
NOTE:

The input data channels can be configured to optimize board layout for each port. Bitwise reordering is not supported.

For example, Y data could be connected to Port A, B, or C. Port configuration is handled in the API Software.

NOTE:
If only one input clock is used, then P1A_CLK should be connected, and P1B_CLK and P1C_CLK should not be connected.

Front End Clocks	
P1A_CLK	P1_CLK
P1B_CLK	P2_CLK
P1C_CLK	P3_CLK
RCK_IN_P	LVDS+ CLK
RCK_IN_N	LVDS- CLK



Front End Interface

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV D
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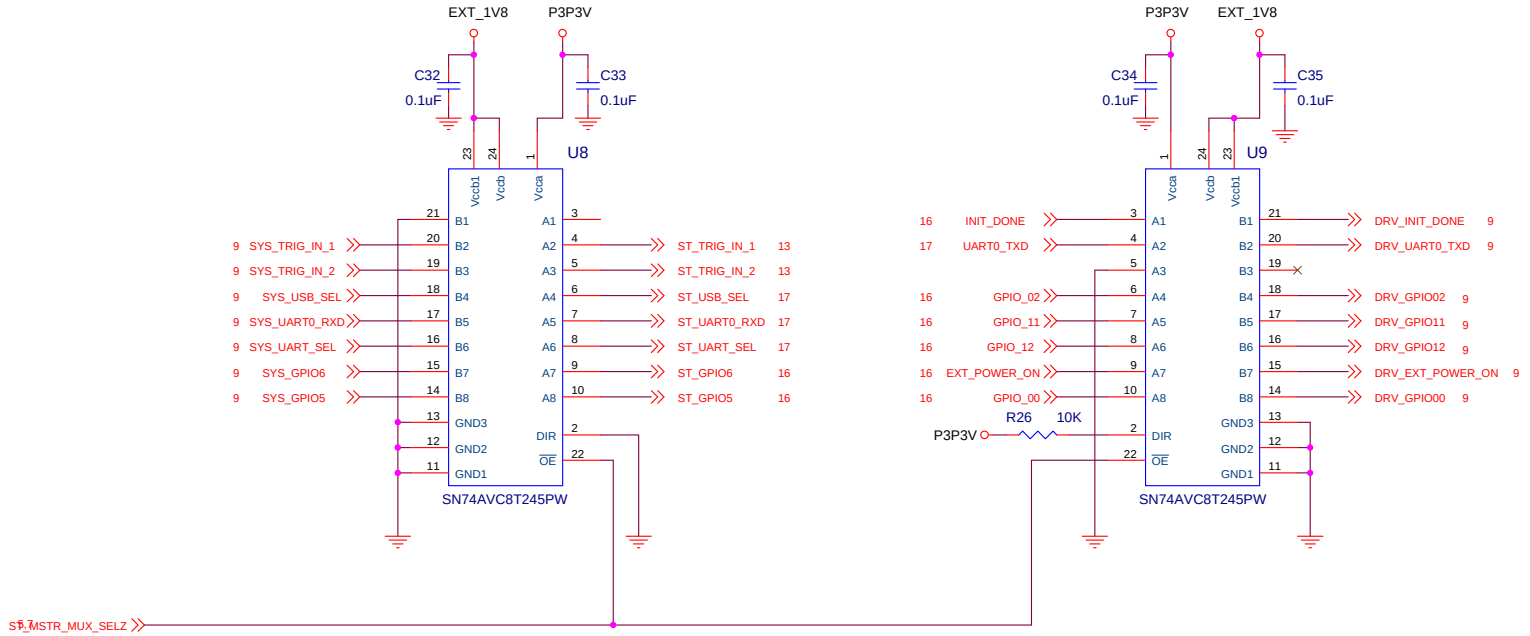

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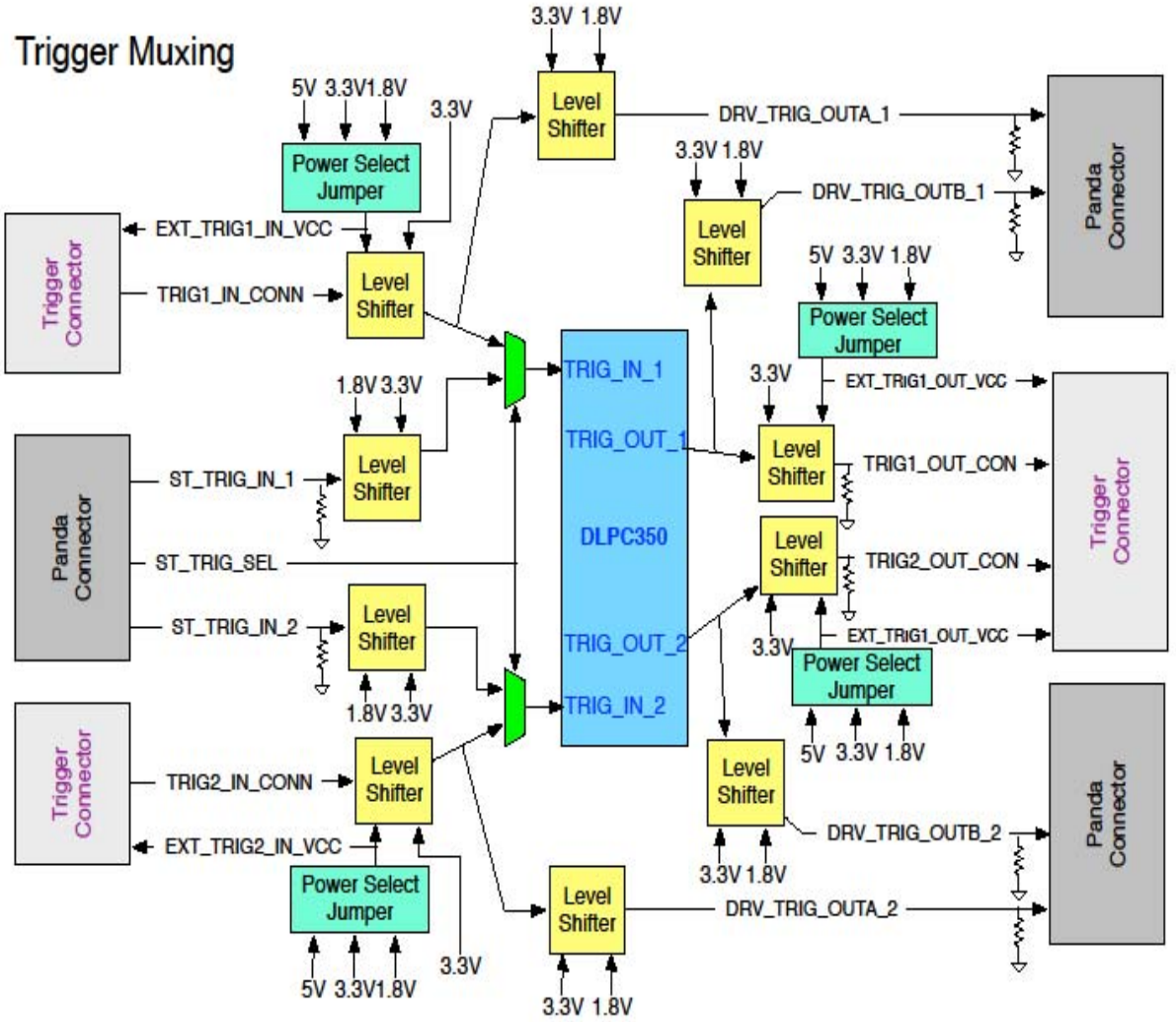

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV D
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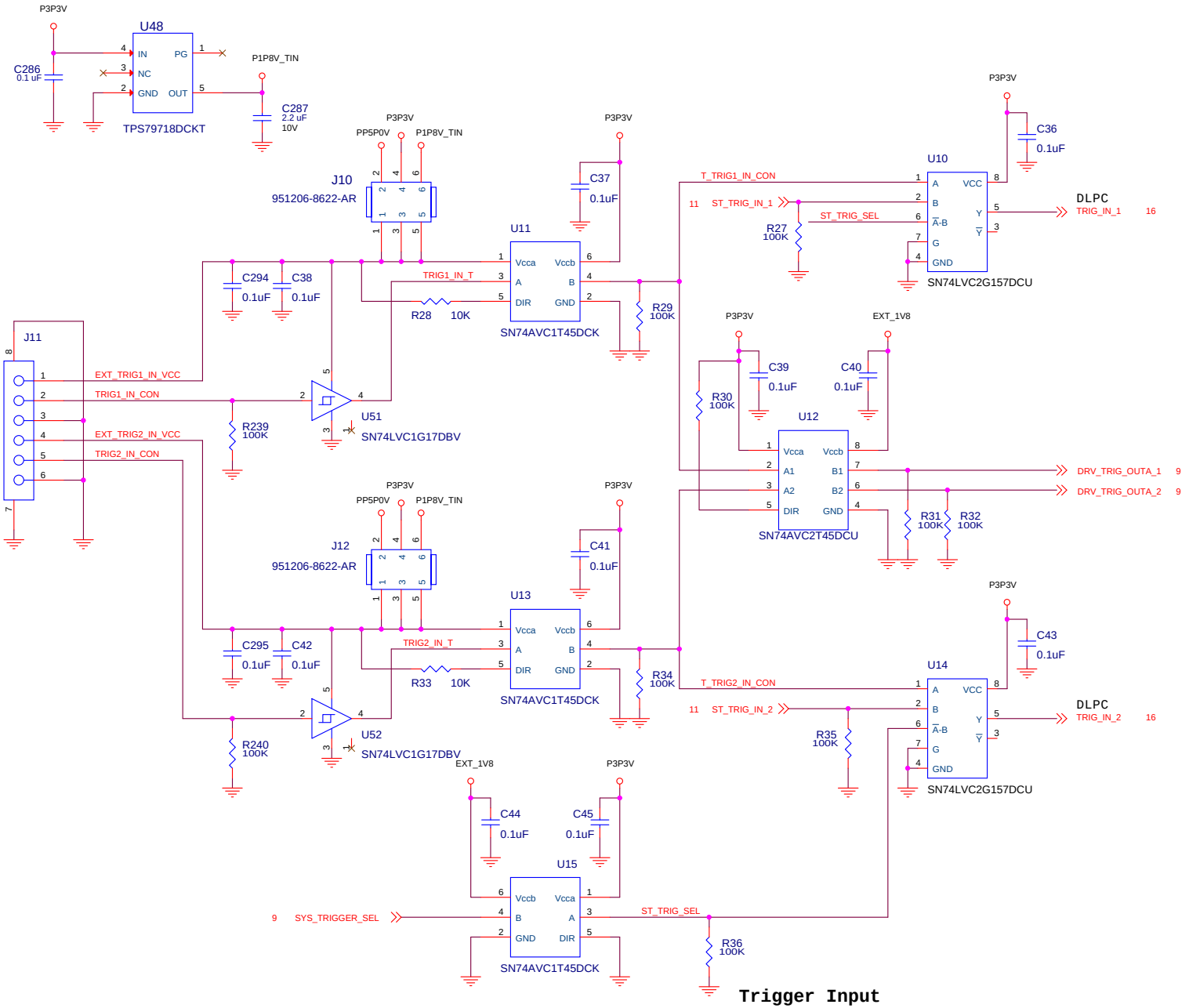
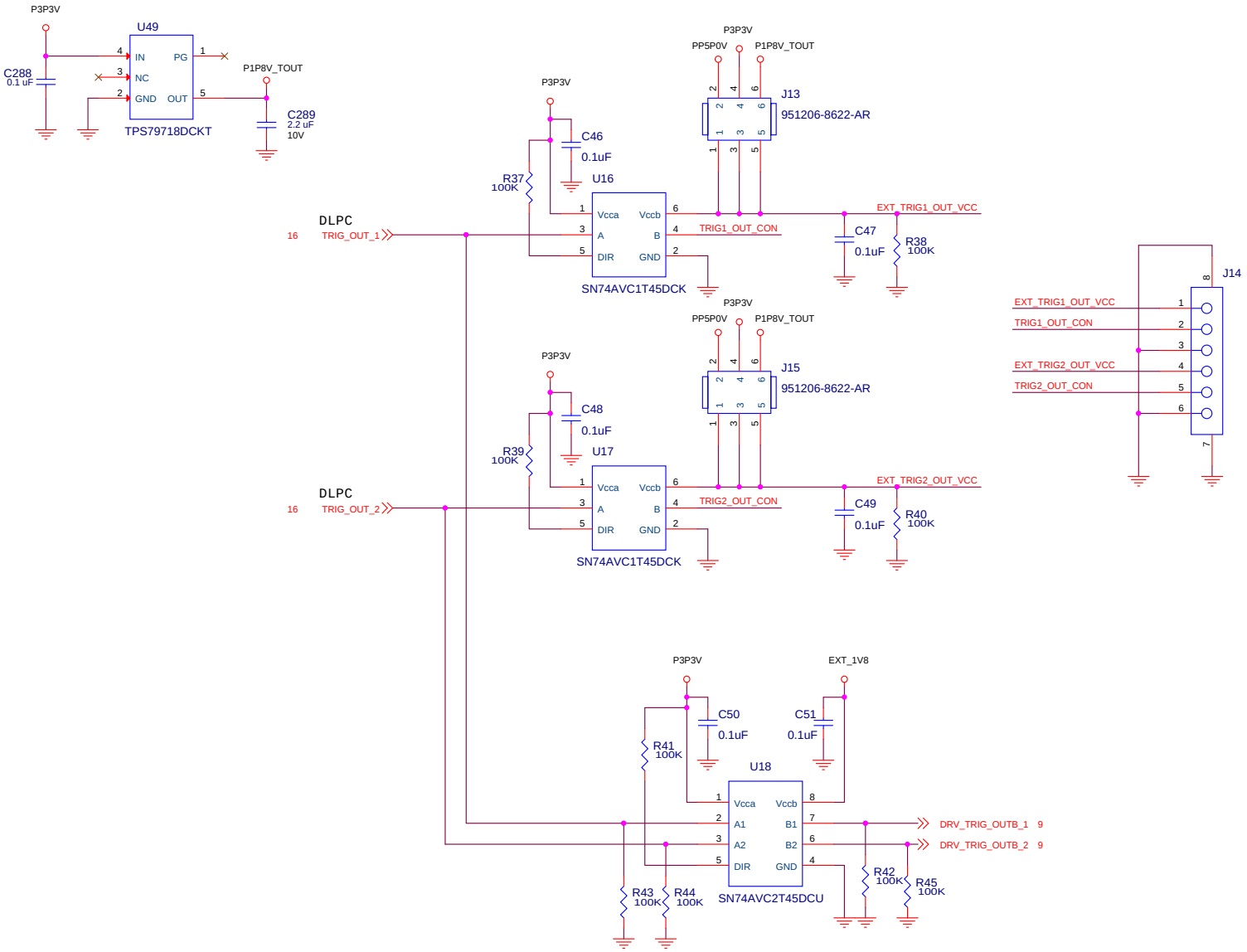


Trigger Input

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909	REV D
	ISSUE DATE		SCALE	SHEET 13 OF 29	



Trigger Output

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV D
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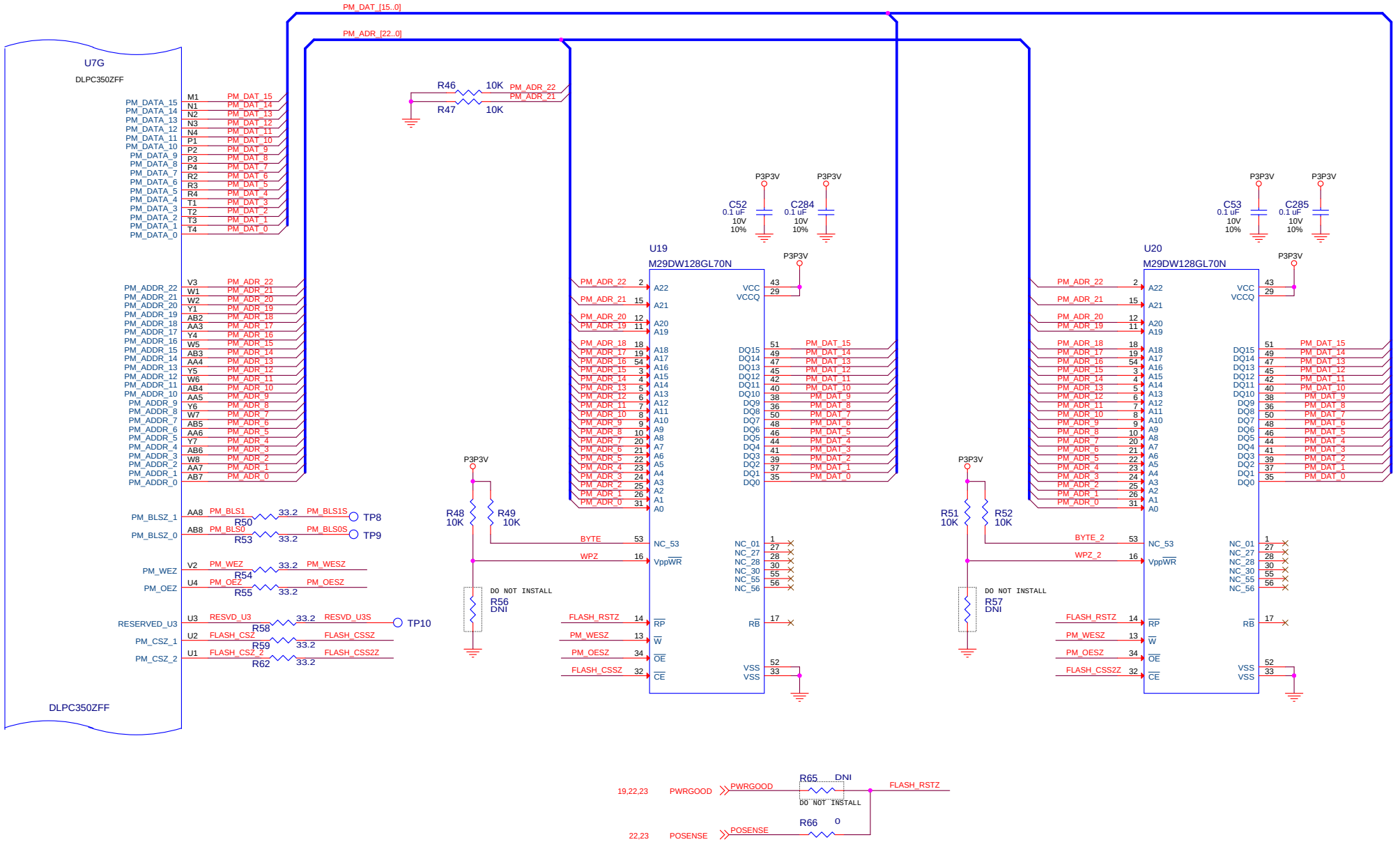

Flash Memory Interface

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV D
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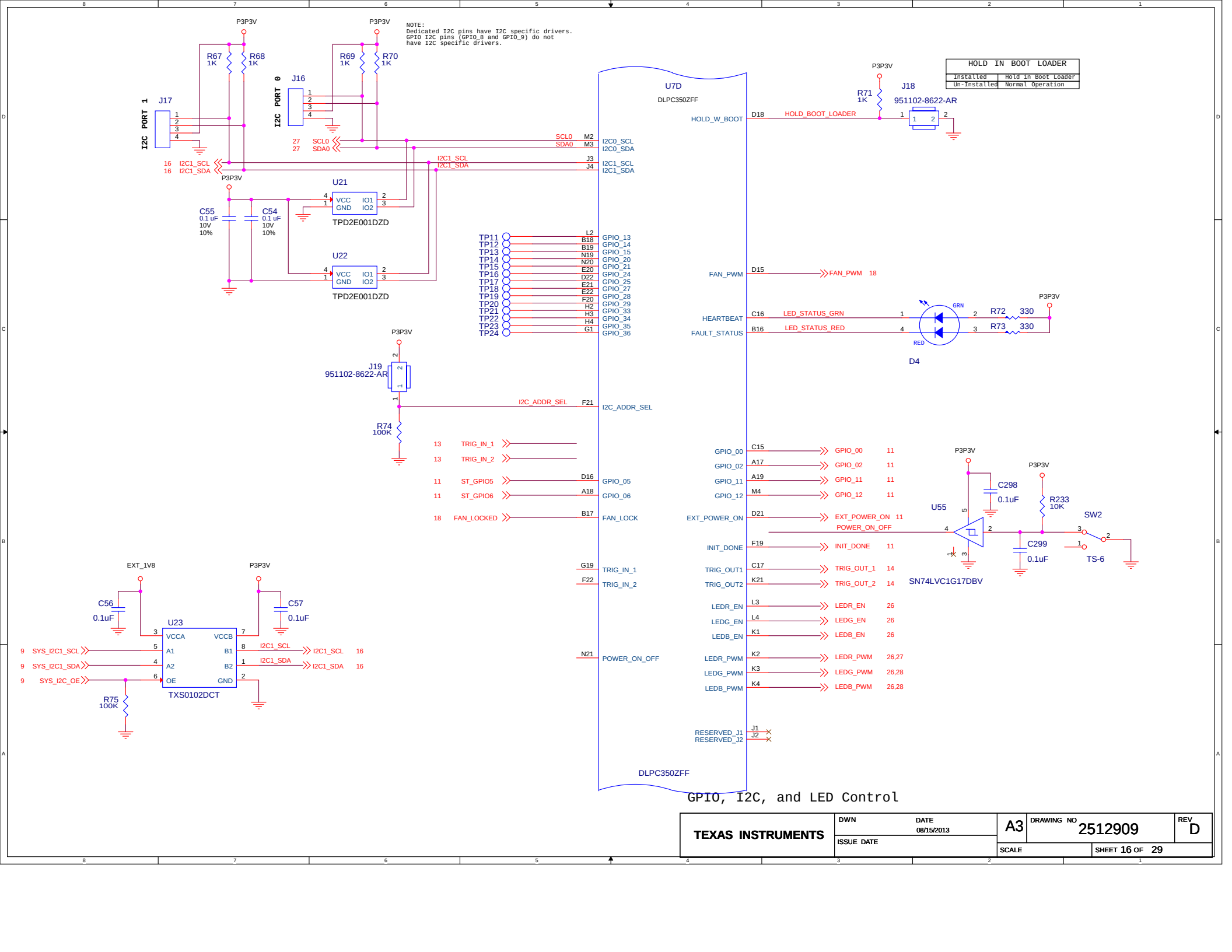
NOTE:
Dedicated I2C pins have I2C specific drivers.
GPIO I2C pins (GPIO_8 and GPIO_9) do not
have I2C specific drivers.
HOLD IN BOOT LOADER
Installed Hold in Boot Loader
Un-Installed Normal Operation
U7D
DLPC350ZFF
J17
J16
J18
951102-8622-AR
J19
951102-8622-AR
U21
U22
TPD2E001DZD
U23
TXS0102DCT
U55
SN74LVC1G17DBV
D4
SW2
TS-6
GPIO, I2C, and LED Control
TEXAS INSTRUMENTS
DRAWING NO 2512909
REV D
A3
SHEET 16 OF 29
DWN
DATE 08/15/2013
ISSUE DATE
SCALE

NOTE:
The RS232 interface is used for test interface and debug. It is not required for production designs.

RS-232 PORT 0

P3P3V
R76 0
U24
MAX3232CPWR
C58 0.1 uF 10V 10%
C59 0.1 uF 50V
C60 0.1 uF 50V
C61 0.1 uF 50V
C62 0.1 uF 50V
VCC GND V+ C1+ C1- V- C2+ C2-
T2OUT R1IN R2IN T1OUT
T2IN R1OUT R2OUT T1IN
SJ-2523-SMT
J20
0 R77 DNI R78
0 R83 DNI R82
0 R84
RS232_TX RS232_RX
UART0_TXD UART0_CTSZ UART0_RXD_DRV UART0_RTSZ
11 UART0_TXD
UART0_RXD

U7F
DLPC350ZFF
L19 UART0_TXD
L20 UART0_CTSZ
L21 UART0_RXD
M19 UART0_RTSZ
RESERVED_F4 RESERVED_F3 RESERVED_D1 RESERVED_C1 RESERVED_D2
F4 SSP0_CLK
F3 SSP0_TXD
D1 SSP0_RXD
C1 SSP0_CS21
D2 SSP0_CS20
P3P3V
R79 3.3K R80 3.3K R81 1K
TP25 TP26 TP27 TP28 TP29

P3P3V
C63 0.1uF
U25
A B A-B G VCC Y Y GND
SN74LVC2G157DCU
11 ST_UART0_RXD
11 ST_UART_SEL
R86 100K R87 100K

NOTE:
The USB interface is used for test interface, debug and high-speed flash memory programming capability. It is not required for production designs where I2C is the primary communication bus.

J21
1734035-2
USB Type-Mini B Jack
USB_DAT_N USB_DAT_P
R90 22 1/10W
R91 22 1/10W
USB_DAT_NS USB_DAT_PS

Note: This buffer prevents the USB host from detecting the slave device before ARM processor initialization.

P3P3V
C65 0.1uF
U27
1DN 1DP 2DP 2DN GND VCC DN DP SEL OEZ
TS3USB221ARSER
DAT_N DAT_P
C18 USB_ENZ
E3 USB_DAT_N
E2 USB_DAT_P
DLPC350ZFF

P3P3V
R88 100K
C64 0.1 uF 10V 10%
VBUS
U26
R85 3.3K
R89 1.5K
SN74LVC1G125DBVR
USB_ENZ

9 SYS_USB_DP
9 SYS_USB_DN
11 ST_USB_SEL
R92 100K

RS-232, Synchronous Serial Port, and USB

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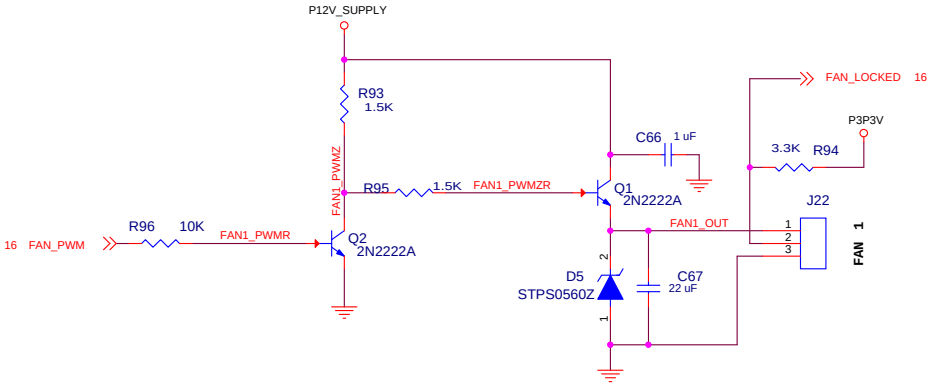

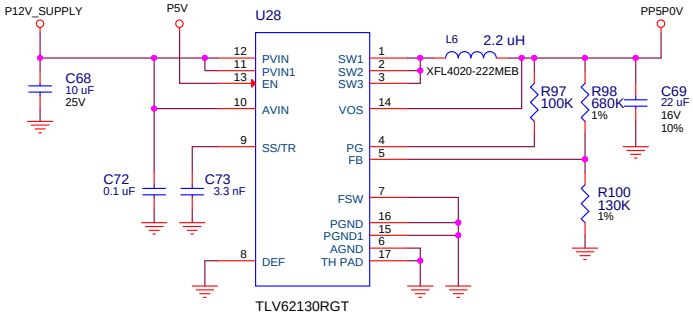

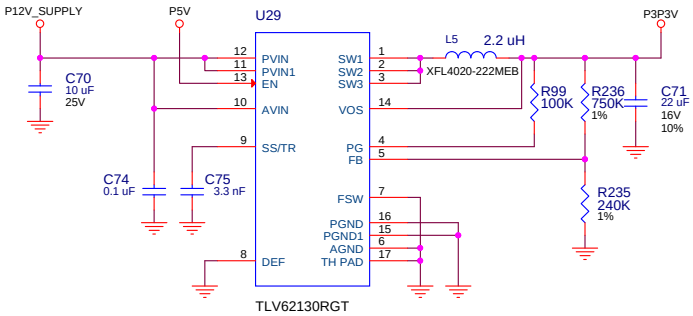

Fan, 3.3V & Panda 5.0V Power Supplies

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MULTI-ICE JTAG I/F

P3P3V

DO NOT INSTALL

R103 1K

R104 10K

R105 10K

R106 10K

R107 10K

R108 10K

R109 10K

J24

2 4 6 8 10 12 14 16 18 20

1 3 5 7 9 11 13 15 17 19

TRSTZ_IN

TDI

TMS2

TCK

RTCK

TDO2

ICE_RSTZ

P3P3V

R101 1K

NOTE:
TRSTZ should be pulled down for production designs.

U30

SN74LVC1G125DBVR

TRSTZ

R110 10K

P3P3V

R102 10K

MAN_RSTZ

J23

951102-8622-AR

MANUAL RESET JUMPER	
INSTALLED	HOLD IN RESET
NOT INSTALLED	NORMAL OPERATION (DEFAULT)

SW1

TL3305AF260

R111 100 1%

P3P3V

C76 0.1 uF 10V 10%

P3P3V

U31

VDD MR RESET CT GND

TPS3838K33DBVT

P3P3V

U32

SN74LVC1G07DBVR

PWRGOOD

PWRGOOD 15,22,23

P3P3V

C77 0.1 uF 10V 10%

JTAG BOUNDARY SCAN

J25

1 TRSTZ

2 TDI

3 TMS1

4 TDO1

5 TCK

6

7

8

53261-0671

NOTE:
JTAG I/F, ARM Trace and Testpoint connectors and signals are for board debug and test. They are not required for production designs.

U7E

DLPC350ZFF

TDO2 M18 RESERVED_M18

TDO1 L18 TDO1

TMS2 V16 RESERVED_V16

TMS1 V15 TMS1

TDI P18 TDI

TCK R18 TCK

TRSTZ V17 TRSTZ

RESERVED_K20 K20 TRACEPKT7R

RESERVED_K19 K19 TRACEPKT6R

RESERVED_J22 J22 TRACEPKT5R

RESERVED_J21 J21 TRACEPKT4R

RESERVED_J20 J20 TRACEPKT3R

RESERVED_J19 J19 TRACEPKT2R

RESERVED_H22 H22 TRACEPKT1R

RESERVED_H21 H21 TRACEPKT0R

RN1

1 2 3 4 5 6 7 8

16 15 14 13 12 11 10 9

33

TRACEPKT7 TP30

TRACEPKT6 TP31

TRACEPKT5 TP32

TRACEPKT4 TP33

TRACEPKT3 TP34

TRACEPKT2 TP35

TRACEPKT1 TP36

TRACEPKT0 TP37

TP38

TP39

RESERVED_F1 F1 TP40

RESERVED_G4 G4 TP41

RESERVED_G3 G3 TP42

RESERVED_F2 F2 TP43

RESERVED_G2 G2 TP44

RTCK G18 RTCKR

R112 33 RTCK

ICTSEN_PD V6 ICTSEN

R113 4.7K

V7 HW_TEST_EN

SPARE E16 SEQ_SYNC

VPGM D17

DLPC350ZFF

R114 10K

Test Points, JTAG and Reset

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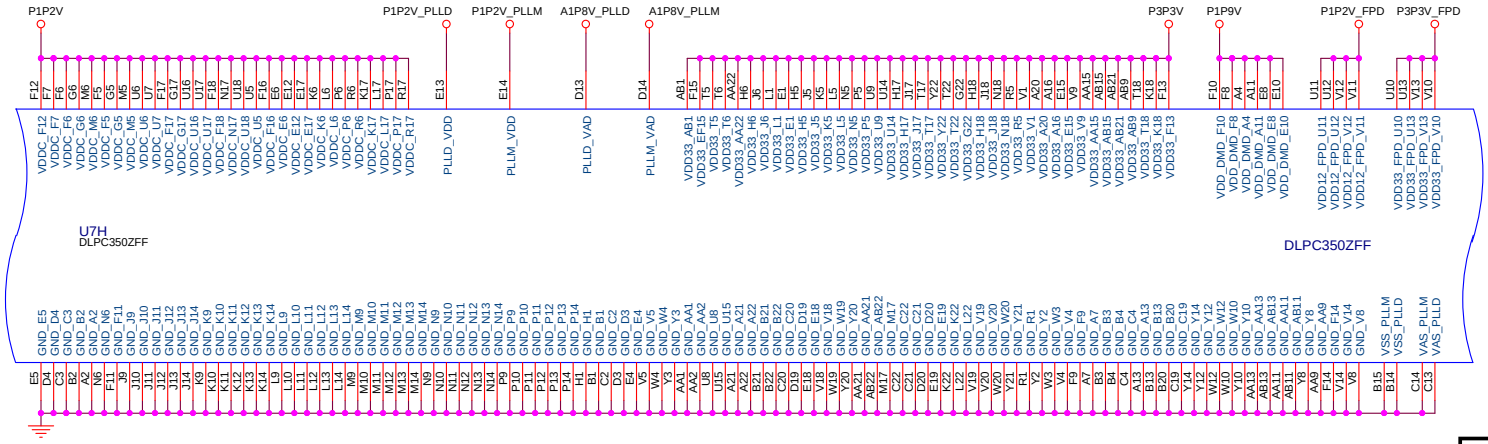
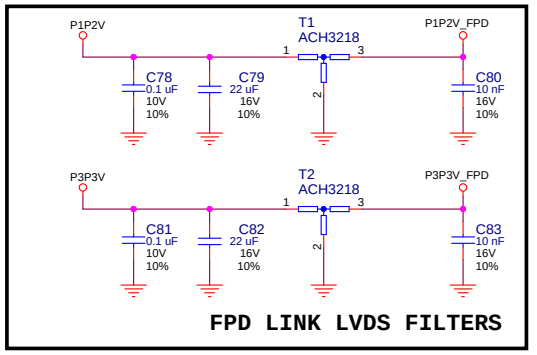
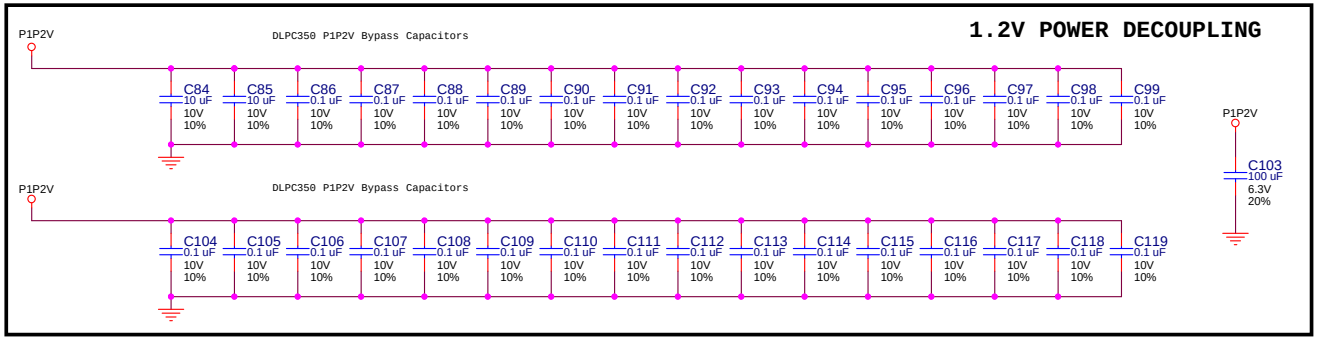
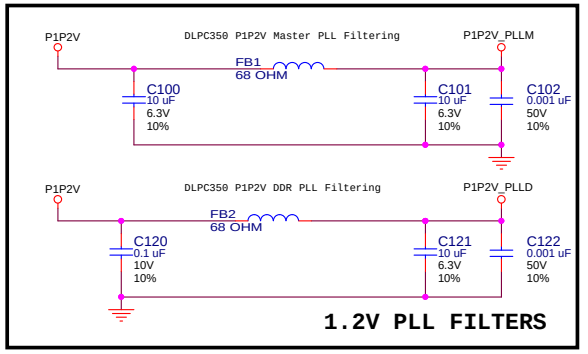
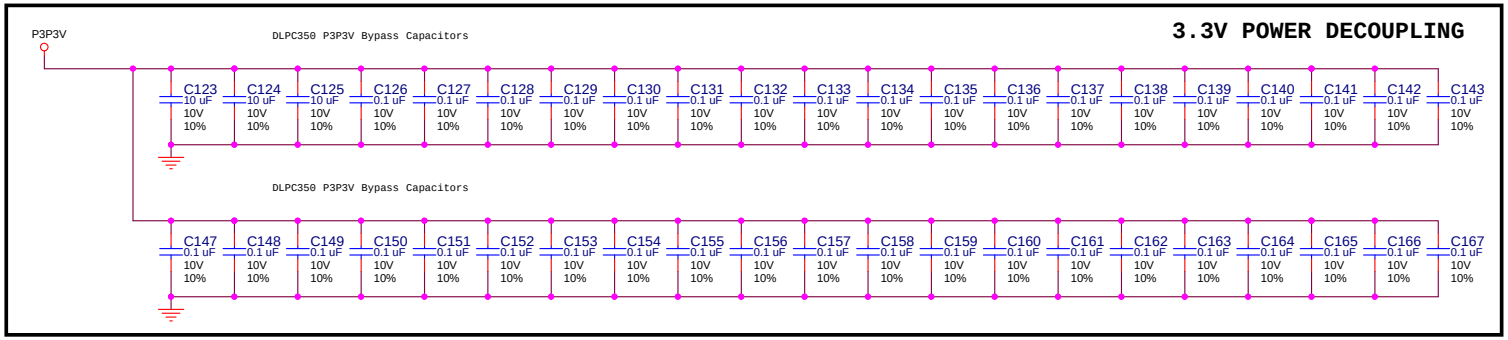
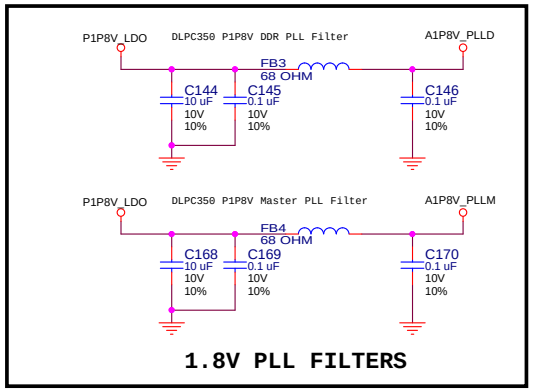


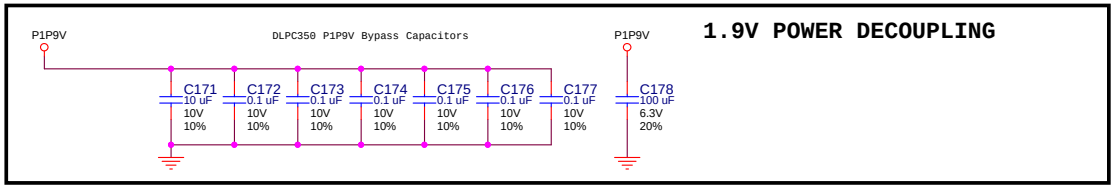






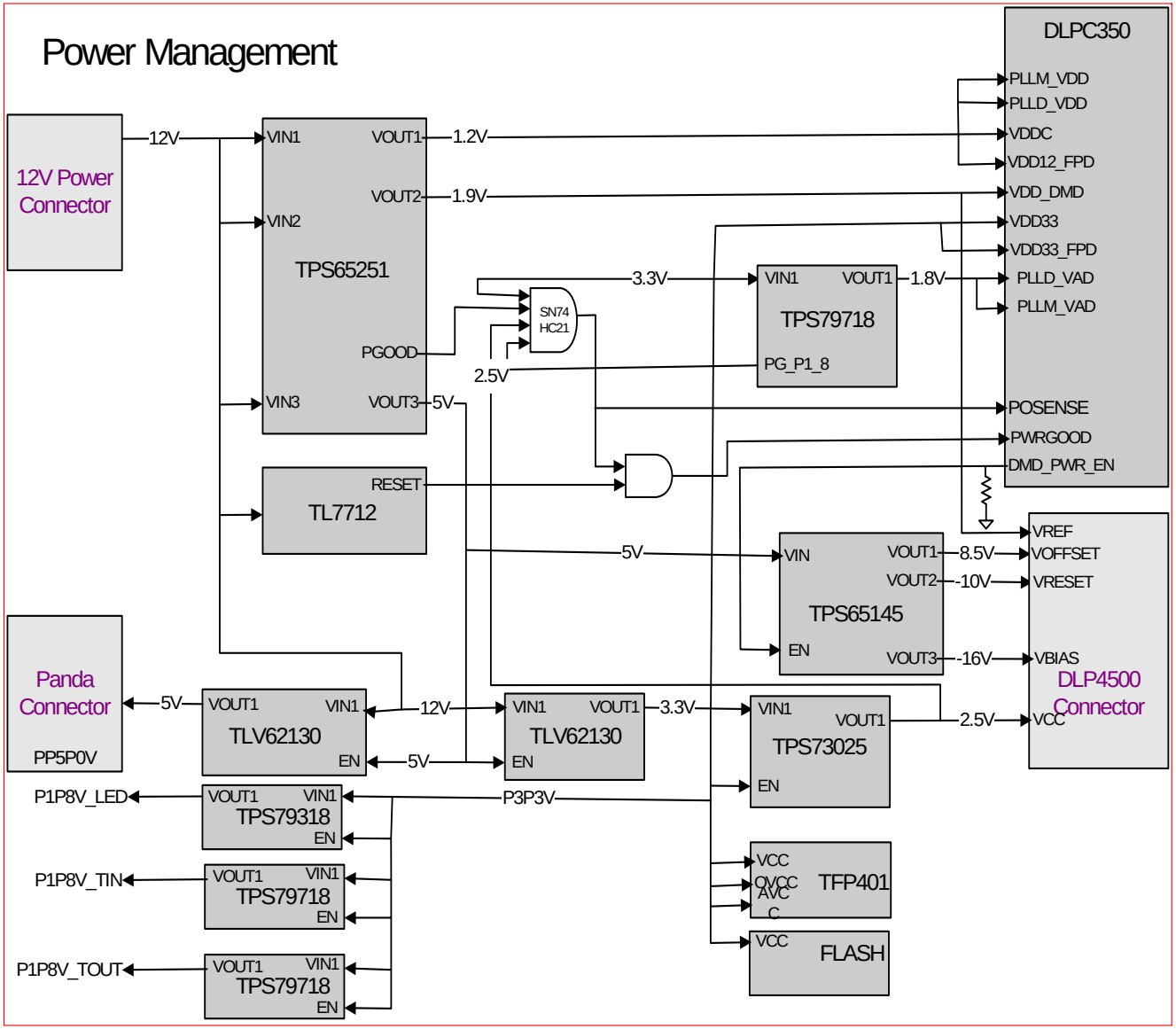






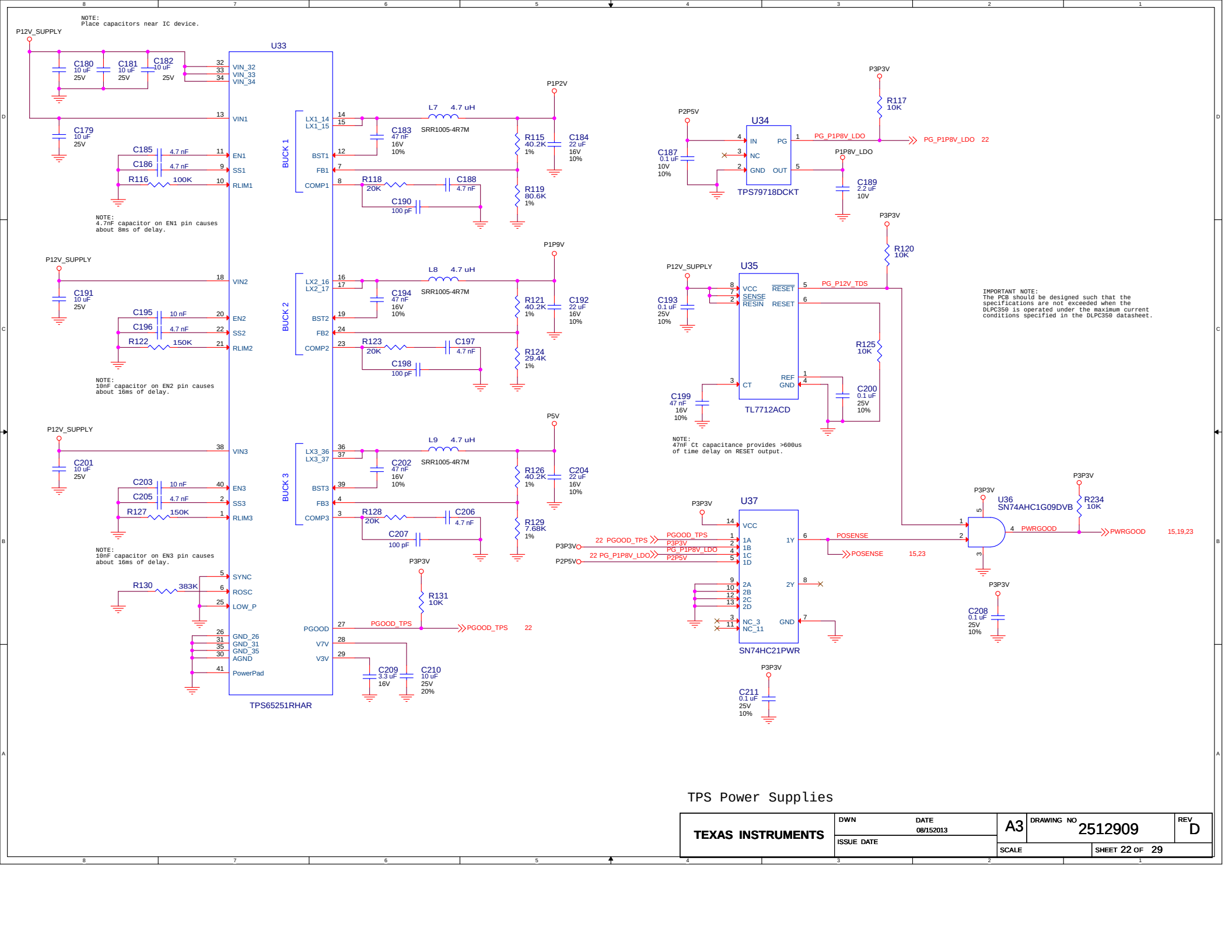
DLPC350 Power and Bypass Capacitors

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV D
	ISSUE DATE		SCALE	SHEET 20 OF 29



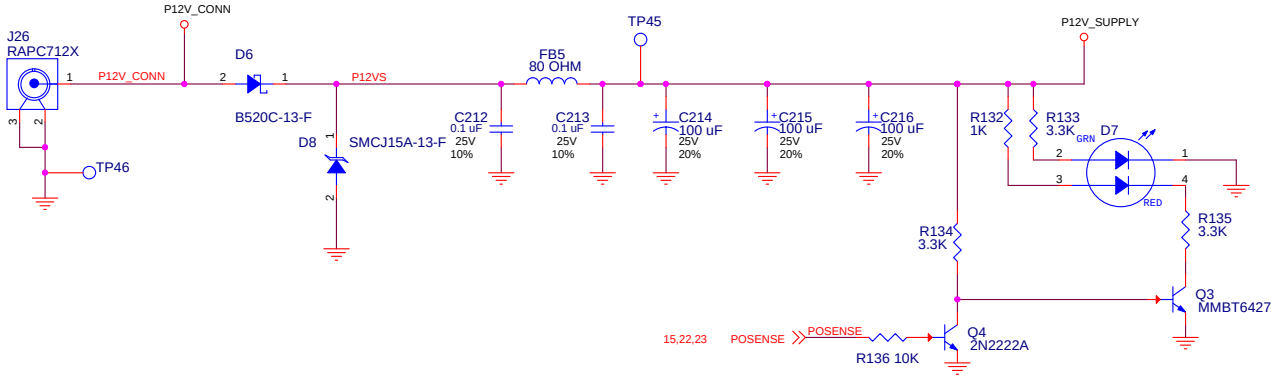
Power Management Block Diagram

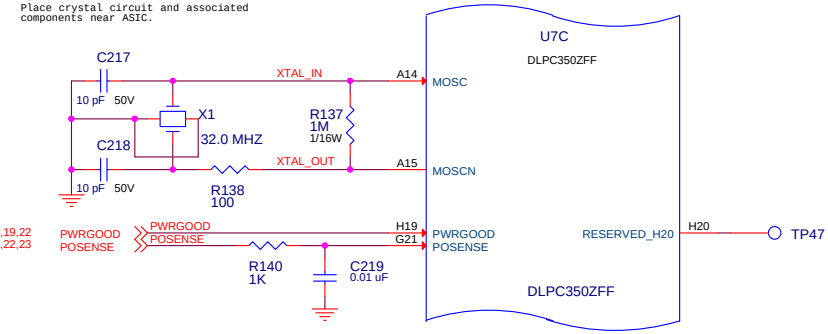
TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV D
	ISSUE DATE		SCALE	SHEET 21 OF 29



TPS Power Supplies

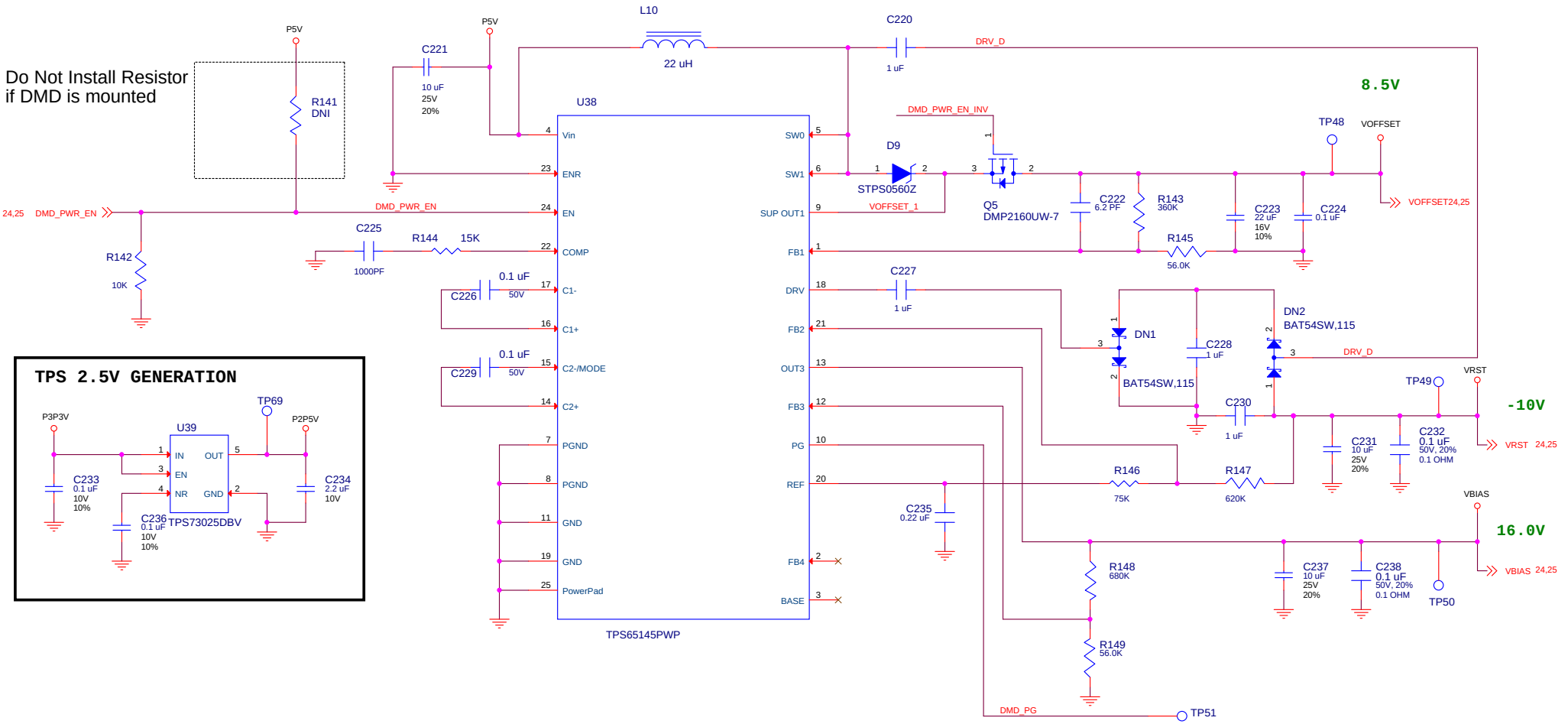
TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV D
	ISSUE DATE		SCALE	SHEET 22 OF 29





Input Power and Oscillator Input

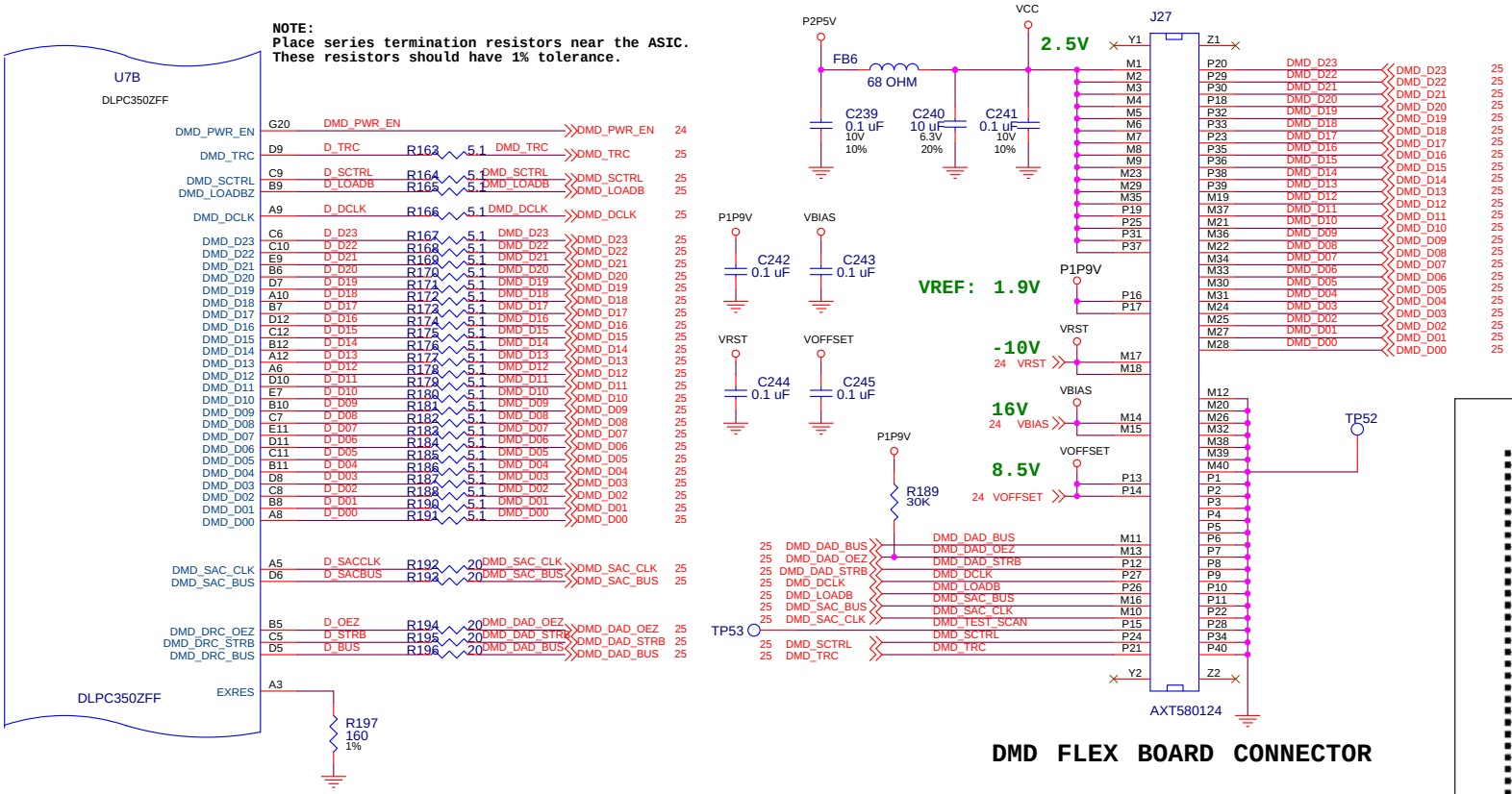
TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV D
	ISSUE DATE		SCALE	SHEET 23 OF 29



DMD Power Supplies

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV D
	ISSUE DATE		SCALE	SHEET 24 OF 29

NOTE:
Place series termination resistors near the ASIC.
These resistors should have 1% tolerance.

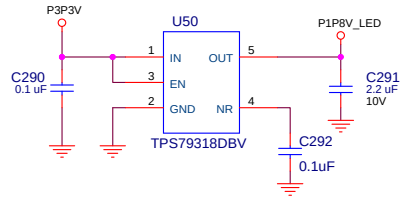


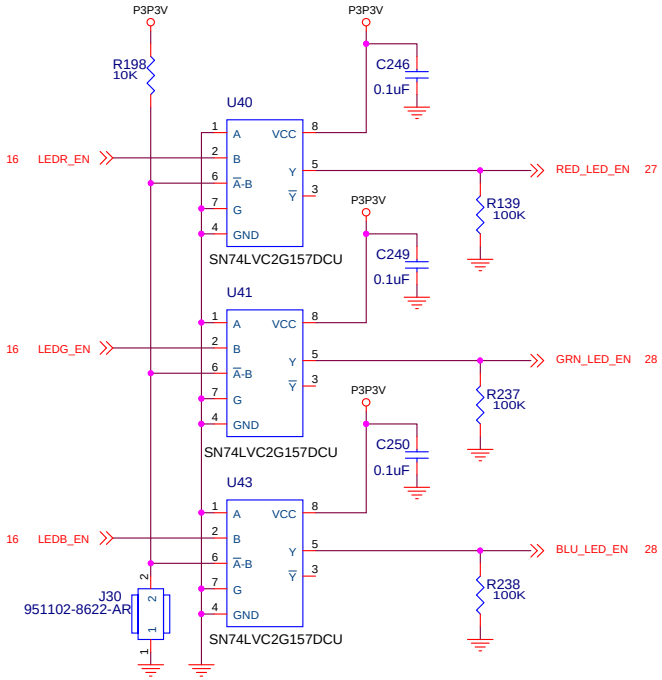
DMD FLEX BOARD CONNECTOR

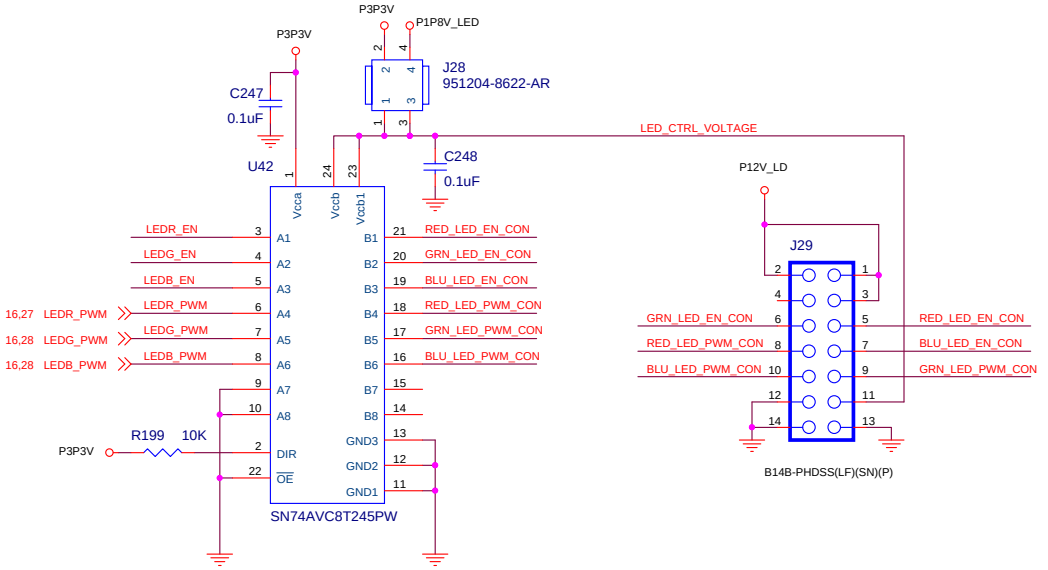
DMD FLEX BOARD CONNECTOR PINOUT

DMD Flex Interface

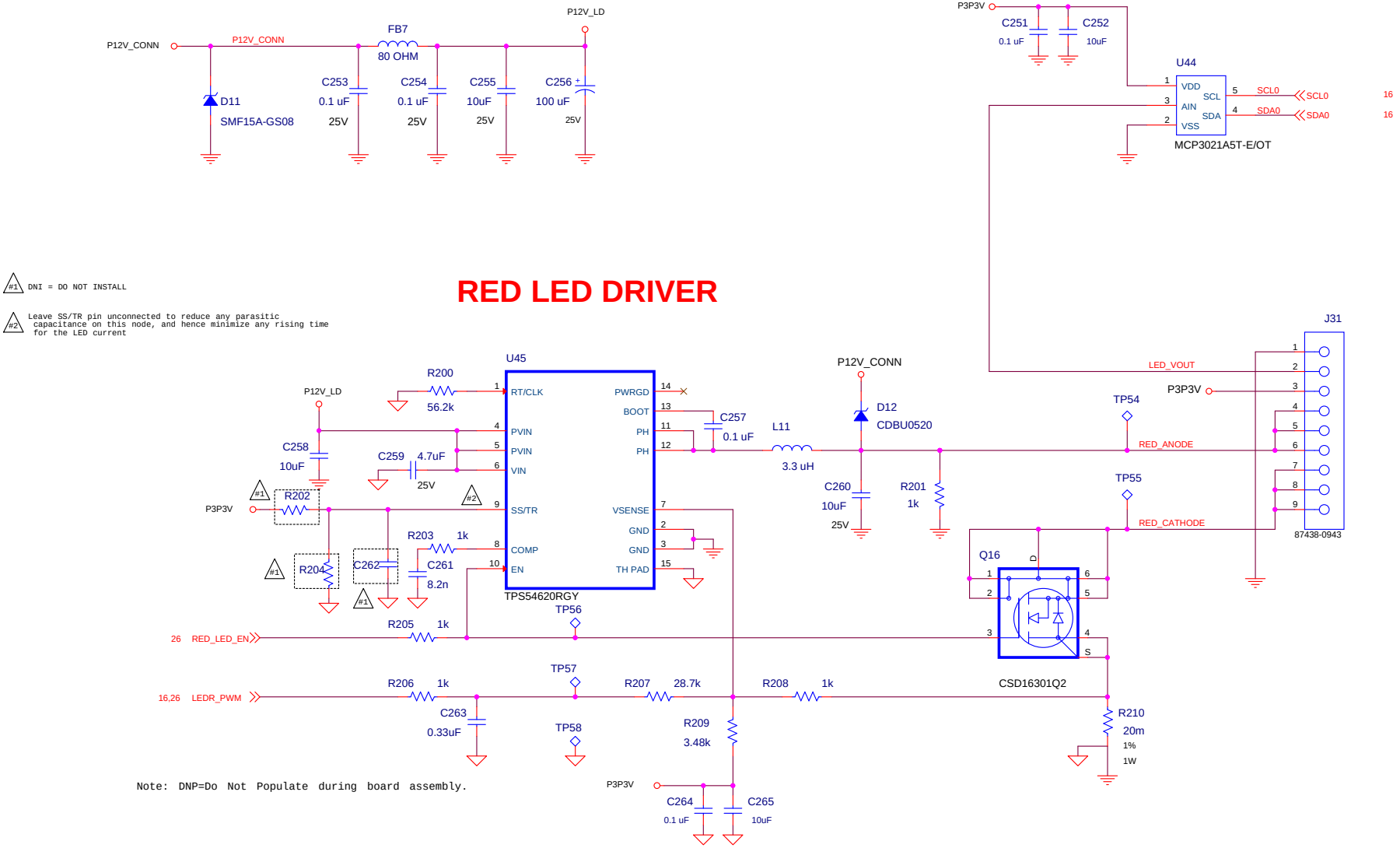
TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909	REV D
	ISSUE DATE			SCALE	SHEET 25 OF 29





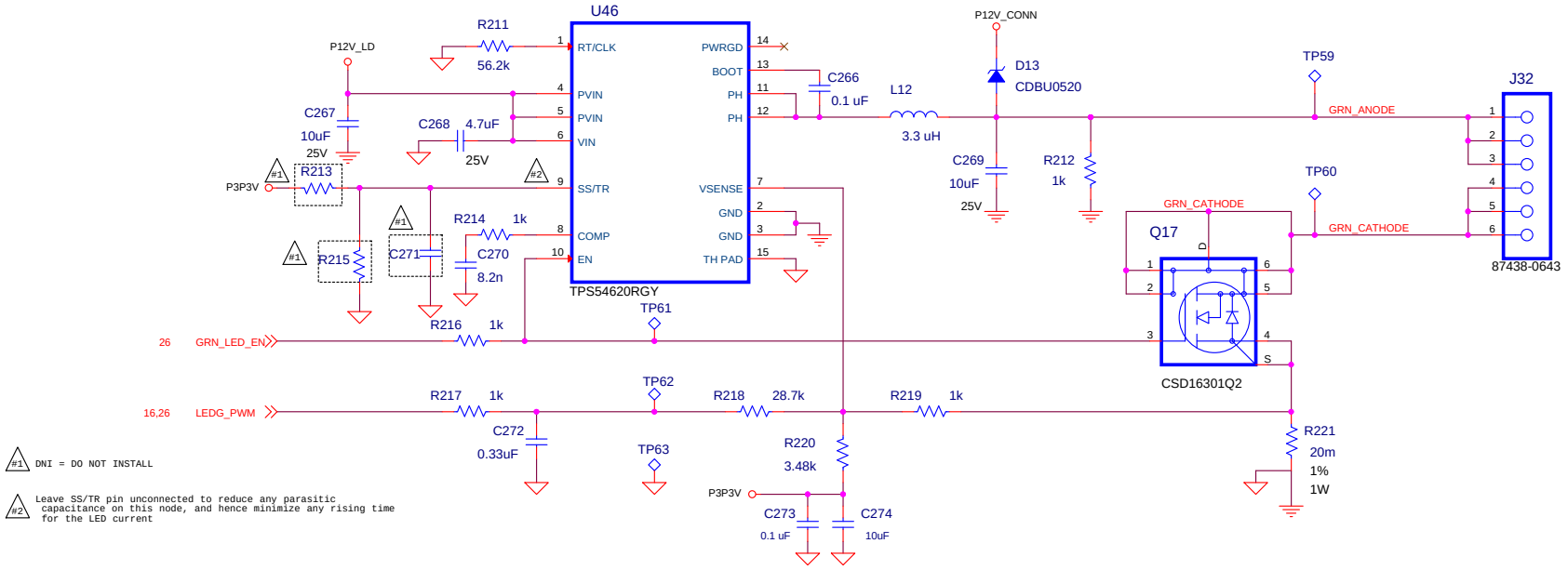


TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV D
	ISSUE DATE		SCALE	SHEET 26 OF 29

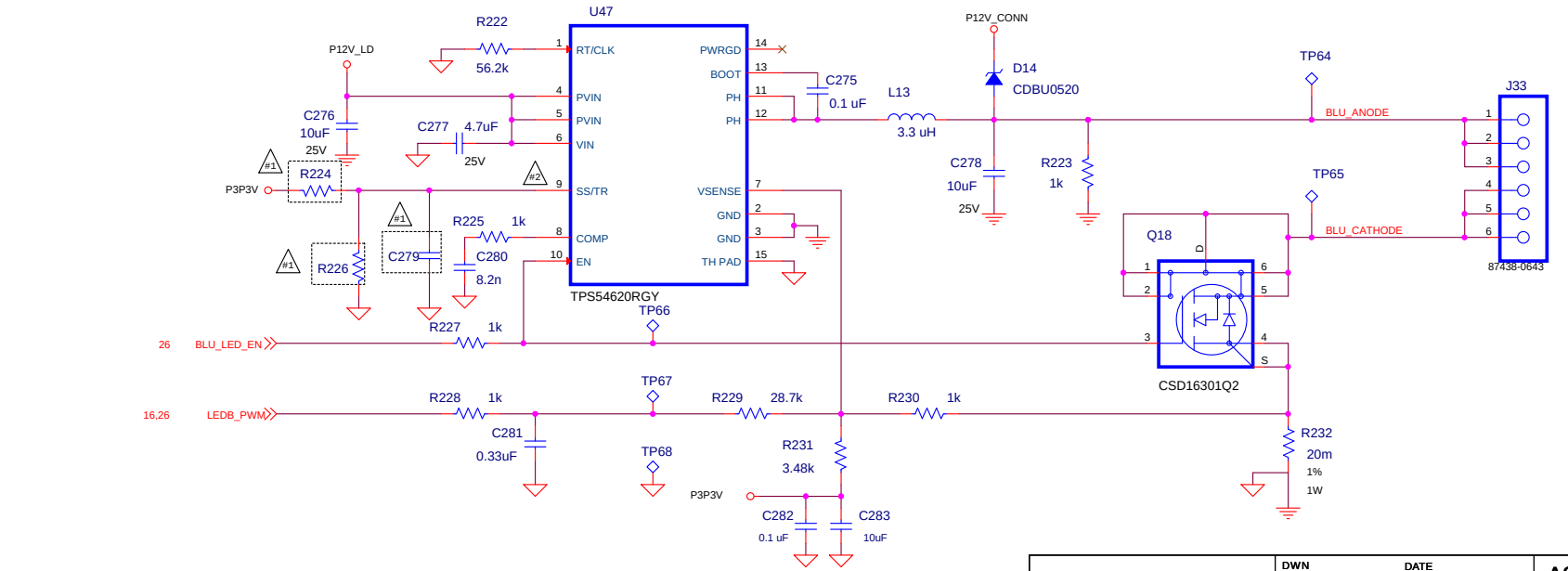


TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909	REV D
	ISSUE DATE		SCALE	SHEET 27 OF 29	

GREEN LED DRIVER



BLUE LED DRIVER



TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV D
	ISSUE DATE		SCALE	SHEET 28 OF 29

Revision History

Rev. A: Initial Release ~ 12/6/2012

Rev. B: Relelase ~ 06/18/2013

Rev. C: Relelase ~ 08/15/2013

All Sheets:
1) Cosmetic changes to reference designators, part values, and fonts
2) Remove unused Off Sheet Connectors
3) Add inter-sheet references
4) Replace obsolete parts in BOM

Sheet 7
1) Add Panda interface connection block diagram

Sheet 15
1) Correct SW2 part number

Sheet 18
1) Correct SW1 part number

Sheet 21
1) Up-date power management block diagram

Rev. D: Update ~ 04/7/2016

1) Changing C262, R202,R204, C279, R226, R224, C271, R215, R213, R78, R82, R19, R21, R9, R12, R17 to DNI (Do Not Install) MR 4/11/2016 .
2) Changing SW1 symbol type to push button and part# to TL3305AF260QG page 19. MR 4/11/2016.

Schematic Revision History

TEXAS INSTRUMENTS	DWN	DATE 08/15/2013	A3	DRAWING NO 2512909 REV D
	ISSUE DATE		SCALE	SHEET 29 OF 29