1. Device configuration,
    a) There are three dedicated configuration pins, CORECLKSEL, and DDRSLRATE1:0. The state of these pins is not latched and must be held at the desired state at all times.
    b) Boot Modes: When implementing the pull-up or pull-down boot scheme selected, TI recommends a 1k resistor to the correct polarity.
2. Clocking
    a) All differential clock input buffers are low jitter clock buffers (LJCBs).
    b) Any unused LJCB inputs should be connected to the appropriate rails to establish a valid logic level.
    c) Because the common mode biasing is included, the clock source must be AC coupled (except where noted in this document and data sheet).(0.1uF)
    d) All clock drivers must be in a high impedance state until CVDD (at a minimum) is at a valid level.
    e) In hardware design guide, "If the both of the SGMII interfaces are not used, the SGMII regulator power pin (VDDR3_SGMII) must still be connected to the correct supply rail with the appropriate decoupling capacitance applied. The EMI/Noise filter is not required when this interface is not utilized."If EMIF filter is not required, why decoupling capacitors still required?

        This pin is still subject to noise and voltage variation, the filter reduces the AC ripple on the power line. Removing the decoupling capacitors would increase the AC ripple and voltage tolerance beyond acceptable limits – we do not recommend nor at this point in time warranty devices where the decoupling capacitors have been removed.
3. Power
    a) TI DSP only requires power variation range, no matter the variation is caused by ripple, noise or anything else.
    b) Does not need to be concerned with the routing skews within the DSP. Only need to match the routed lengths on the PCB.
4. Peripherals
    a) GPIO
        i. GPIOs are enabled at power-up and default to inputs.
        ii. All pins must be driven to a logical state during boot and through POR being released.
        iii. After POR is high the pins are available as GPIO pins.
        iv. It is recommended that GPIOs used as outputs have a series resistance (22 or 33 being typical values).
        v. Input: A pullup resistor value of 1k is recommended to make sure that it over-rides the internal pulldown resistor present on some GPIOs.
        vi. If an external resistor is used to obtain a specific post boot state for any GPIO pin, an external 1k - 4.7k resistor to the appropriate rail is recommended.
    b) HyperLink
        i. All Hyperlink clock and data pins can be left floating when the entire Hyperlink peripheral is not used. Each unused Hyperlink clock and data pin will be pulled low when not in use through internal pulldown resistors.
        ii. In the event a partial number of lanes are used (two lanes instead of four), all clock

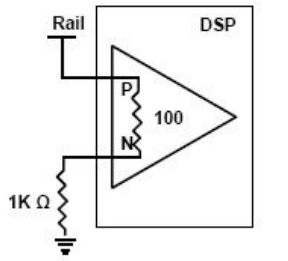
and data pins must be connected. Unused lanes (both transmit and receive) can be left floating.

iii. If the Hyperlink interface is not being used, the peripheral should be disabled in the MMR.

iv. If the Hyperlink interface is not required, the Hyperlink regulator power pin (VDDR1_MCM) must still be connected to the correct supply rail with the appropriate decoupling capacitance applied. The EMI/Noise filter is not required when this interface is not utilized.

v. If unused, the primary Hyperlink clock input shall be configured Pullup shall be to 1.0 variable core supply as the following figure.

Figure 5 Unused Clock Input Connection



c) I2C

i. All I2C clock and data pins (SCL and SDA) can be left floating when the I2C interface is not used.

ii. External pullup resistors to 1.8 V are needed on the DSP I2C signals (SCL, SDA). The recommended pullup resistor value is 4.7k If there are more devices on bus line, users should choose smaller pullup resistor.

iii. The I2C pins are not 2.5 V or 3.3 V tolerant.

d) EMAC

i. The MDIO interface (MDCLK, MDIO) uses 1.8 V LVCMOS buffers.

ii. SGMII utilizes LVDS signaling. The KeyStone DSP uses a CML based SerDes interface that requires AC coupling to interface to LVDS levels; Texas Instruments recommends the use of a 0.1 uF AC coupling capacitors for this purpose.

iii. If both SRIO or SGMII are unused, the primary SRIOSGMIICLK clock input shall be pulled up to 1.0 variable core supply.

e) DDR3

i. Please follow the JEDEC SDRAM specification and all layout instructions from their SDRAM vendor for mirrored SDRAM layout. All TI DDR3 layout guidelines must still be followed of course can be found here: http://www.jedec.org/standards-documents/focus/memory-module-designs-dimms/DDR3/204-pin%20Unbuffered%20SODIMMs.

ii. The only design constraints TI will provide are for valid JEDEC DDR3 fly-by topologies. TI cannot guarantee operation of a T-topology (DDR2 layout) for any Keystone SoC DDR3 design. At the data rates that DDR3 is designed for (DDR3-800 or greater) the reflections that will be encountered in even a well-balanced T-topology would result in a marginal design.

iii. TI strongly recommend you use 0.75V DDR VTT TERMINATION REGULATOR (such as tps51100) for termination.

iv. The DDR3 controller in the TCI6670, TCI6678 DSPs support 2 ranks of memory. DDRCE0, DDR3CLKOUTP/N0, DDRCKE0 and DDRODT0 are all associated with the first rank. DDRCE1, DDR3CLKOUTP/N1, DDRCKE1 and DDRODT1 are all associated with the second rank. If only one rank is implemented, the outputs for the second rank will be unused. You cannot use the second set of clock outputs as that would interfere with the leveling processes. All clock, control, command and address nets must be routed in a matched-length fly-by arrangement to achieve the rated performance. All of these signals fall into those categories.

f) SRIO

i. If the SRIO peripheral is not used, the SRIO link pins can be left floating and the SerDes links should be left in the disabled state.

ii. If the SRIO peripheral is enabled but only one link is used, the pins of the unused link can be left floating.

iii. If both SRIO or SGMII are unused, the primary SRIOSGMIICLK clock input shall be pulled up to 1.0 variable core supply.

g) PCIe

i. All unused PCIe lanes shall be left floating and the unused lanes properly configured in the MMR.

ii. If the PCIe interface is not required, the PCIe regulator power pin (VDDR2_PCIe) must still be connected to the correct supply rail with the appropriate decoupling capacitance applied.

iii. If unused, the PCIe clock shall be pullup to 1.0 variable core supply.

h) AIF

i. For proper operation of the AIF, the SYSCLKP/N (which is the antenna interface SerDes reference clock) and the frame sync clock (RP1CLKP/N) must be generated from the same clock source and must be assured not to drift relative to each other.

ii. All unused AIF transmit and receive lanes shall be left floating and the unused lanes properly disabled in the MMR.

iii. The frame sync clock provided to the FSM has the following requirements:

- RP1 mode:
  - RP1CLKP/N must be 30.72 MHz (8× UMTS chip rate)
  - RP1FBP/N must provide a UMTS frame boundary signal
- Non-RP1 mode:
  - RADSYNC normally be between 1 mS and 10 mS
  - PHYSYNC must provide UMTS frame boundary pulse.

i) JTAG

i. TBD

j) UART

i. The UART interface is intended to operate at 1.8 Vdc.

ii. UART pins (defined with respect to the DSP) are LVCMOS which when not used

can be leave floating.

k) SPI
   i. SPI interface is intended to operate at 1.8 Vdc.
   ii. SPI pins (defined with respect to the DSP) are LVCMOS which when not used can be leave floating.

l) EMIF16
   i. If the EMIF16 peripheral is not used, the EMIF16 inputs can be left unconnected.
   ii. Generally, series resistors should be used on the EMIF16 signals to reduce overshoot and undershoot. Generally acceptable values are 10, 22 or 33 ohms. To determine the optimum value simulations using the IBIS models should be performed to check for signal integrity and AC timings.

m) TSIP
   i. Series resistors should be used on TSIP clock inputs that are edge sensitive. These resistors need to be placed near the signal source.
   ii. If any of the TSIP inputs are not used, they can be left floating since all TSIP pins have internal pulldown resistors.