DDR3 Software Leveling and Registers Configuration

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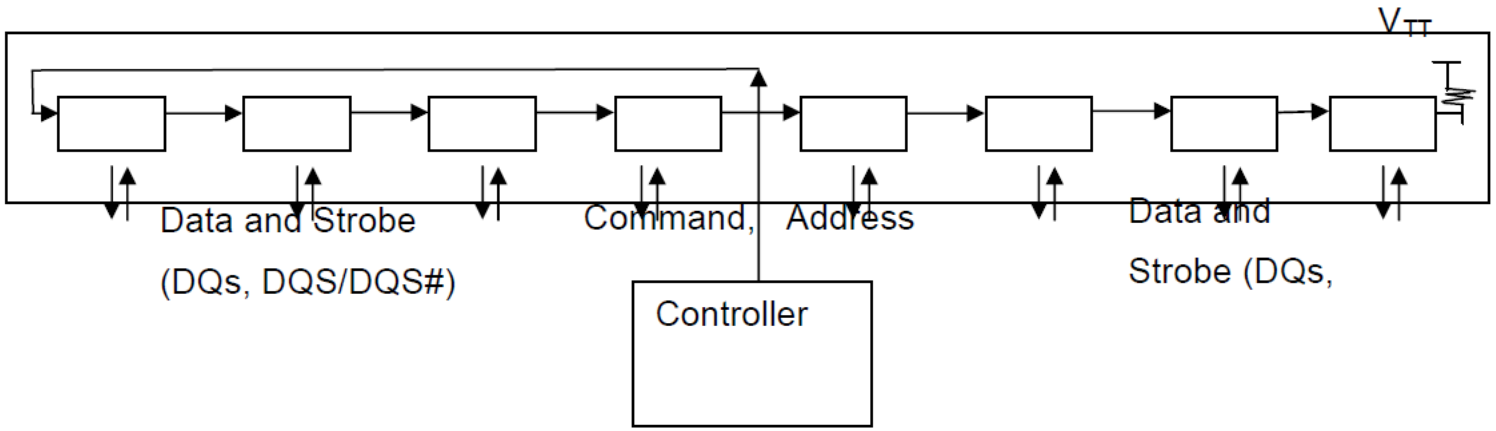
Agenda

- Why leveling
- How to do SW leveling
- Registers configuration

Why Leveling

- Topology
  - DDR3: fly-by topology, better signal integrity at higher speeds than T-branch topology of DDR2



Detailed Reason: see slide comments

Fly-by Topology

- Better signal integrity to reduce the numbers of stubs and stub length
- Easy to apply a single termination at the end of signal

For Example: Timing Diagram of Write Leveling

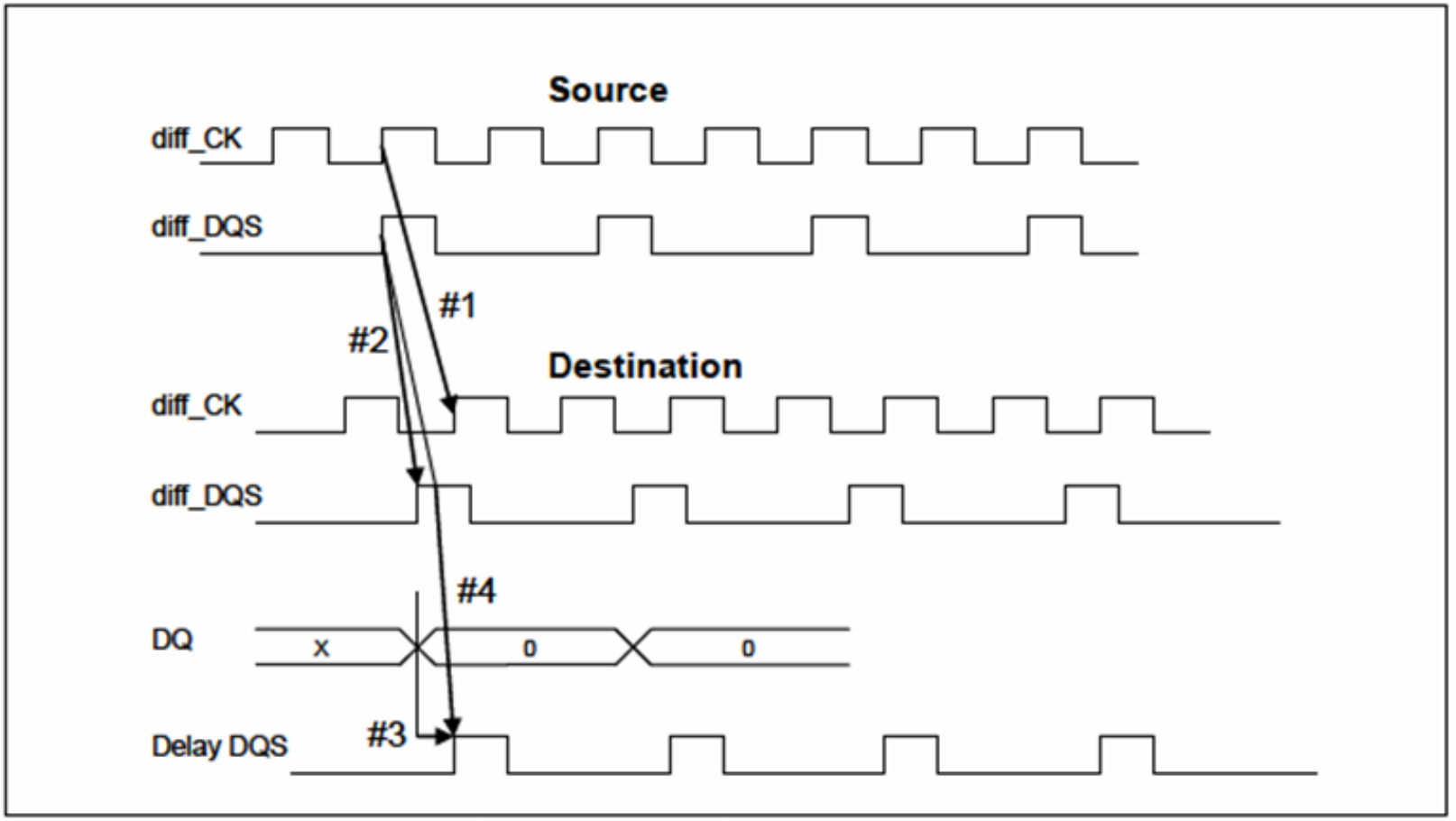


Figure 4. Timing Diagram for Write Leveling

TIMING DIAGRAM WRITE LEVELING

How to do SW leveling

- AM335x HW leveling issue
  - Refer to http://www.ti.com/lit/er/sprz360c/sprz360c.pdf
    - **Advisory 1.0.19 *DDR3: Fully-Automated Hardware READ and WRITE Leveling Not Supported***
- SW Leveling Steps
  - Get optimum seed value
    - Get value of DDR_CK and DDR_DQSx traces and fill them into Ratio Seed Spreadsheet
    - Load DDR3_slave_ratio_search_auto.out and run the code

Seed Value

Trace Length (inches)			
	Byte 0	*Byte 1*	
DDR_CK trace	0.85	0.85	input the average of DDR_CK and DDR_CKn traces. If you have two x8 memories, use the trace lengths for each corresponding byte.
DDR_DQSx trace	0.7	0.85	x can be 0 or 1, corresponding to each byte.

How to get value of DDR_CK and DDR_DQSx traces? Length unit: inches

Enter the trace length (in inches) of each trace. For DDR_CK, this trace is typically in a 'T' configuration for designs with two x8 memories. Ensure that you input the trace length from AM335x to each memory. These lengths should be close to equal if correct design guidelines were met for a 'T' configuration. For fly-by topology, where the trace runs from AM335x to the first memory, and then to the second memory, ensure that you input the total trace length for each byte.

Optimum Value

```
[CortxA8] **********************************************************************
[CortxA8]       The Slave Ratio Search Program Values are...
[CortxA8] **********************************************************************
[CortxA8] PARAMETER                          MAX   |   MIN   | OPTIMUM |   RANGE
[CortxA8] **********************************************************************
[CortxA8] DATA_PHY_RD_DQS_SLAVE_RATIO     0x06f | 0x005 |   0x03a   | 0x06a
[CortxA8] DATA_PHY_FIFO_WE_SLAVE_RATIO    0x1dd | 0x05b |   0x11c   | 0x182
[CortxA8] DATA_PHY_WR_DQS_SLAVE_RATIO     0x0d3 | 0x064 |   0x09b   | 0x06f
[CortxA8] DATA_PHY_WR_DATA_SLAVE_RATIO    0x10a | 0x09c |   0x0d3   | 0x06e
[CortxA8] **********************************************************************
[CortxA8] rd_dqs_range = 0
[CortxA8] fifo_we_range = 1
[CortxA8] wr_dqs_range = 3
[CortxA8] wr_data_range = 2
[CortxA8]
[CortxA8] Optimal values have been found!!
[CortxA8]
[CortxA8] ===== END OF TEST =====
```

How to get registers value

- For EMIF registers configuration, pls refer to <AM335x EMIF Configuration tips>.
  - http://processors.wiki.ti.com/index.php/AM335x_EMIF_Configuration_tips#DDR_PHY_Registers
- AM335x DDR Calculation tool
  - http://processors.wiki.ti.com/images/a/a4/AM335x_DDR_register_calc_tool.zip

DDR Configuration in Gel File

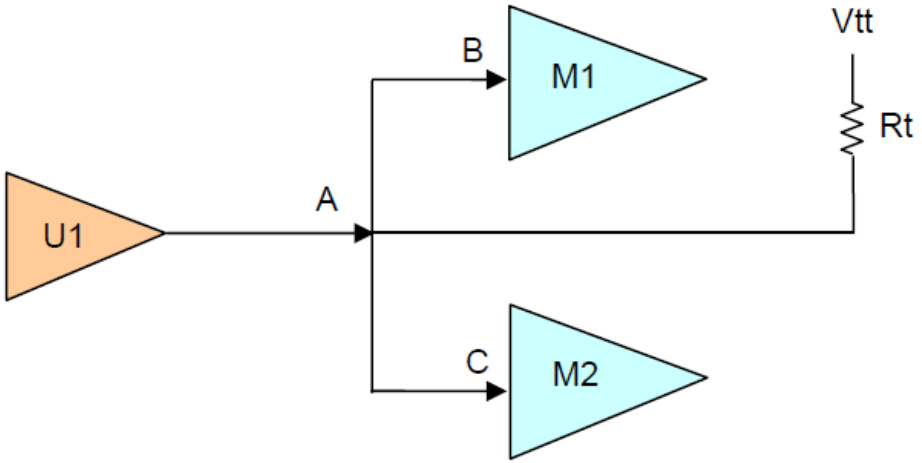
Note: The GEL file can be gotten from StarterWare. There are four GEL file for AM335x in below directory.
AM335X_StarterWare_02_00_00_07\tools\gel

```
//*****************************************************************************
//DDR3=303MHz
//OPP100
//*****************************************************************************

//*****************************************************************************
//DDR3 PHY parameters
//*****************************************************************************

#define   CMD_PHY_CTRL_SLAVE_RATIO          0x40
#define   CMD_PHY_INVERT_CLKOUT             0x1

#define   DATA_PHY_RD_DQS_SLAVE_RATIO       0x3B
#define   DATA_PHY_FIFO_WE_SLAVE_RATIO      0x100 //RD DQS GATE
#define   DATA_PHY_WR_DQS_SLAVE_RATIO       0x85
#define   DATA_PHY_WR_DATA_SLAVE_RATIO      0xC1   //WRITE DATA

#define   DDR_IOCTRL_VALUE                  (0x18B)

//*****************************************************************************
//EMIF parameters
//*****************************************************************************
#define ALLOPP_DDR3_READ_LATENCY     0x06          //RD_Latency = (CL + 2) - 1
#define ALLOPP_DDR3_SDRAM_TIMING1    0x0888A39B
#define ALLOPP_DDR3_SDRAM_TIMING2    0x26337FDA
#define ALLOPP_DDR3_SDRAM_TIMING3    0x501F830F

#define ALLOPP_DDR3_SDRAM_CONFIG     0x61C04AB2   //termination = 1 (RZQ/4)
                                                  //dynamic ODT = 2 (RZQ/2)
```

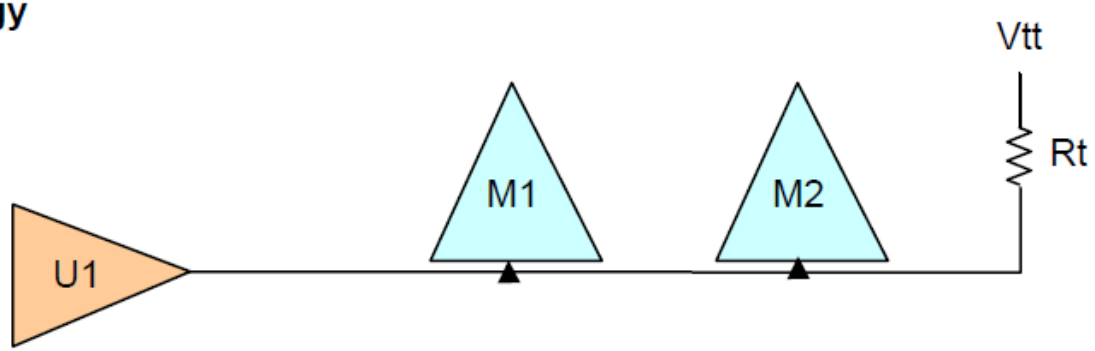
Backup

DDR2 T-Topology

Tree topology



Fly-By topology



DDR CLK

- DDR_CLK frequency = (DDRPLL input clock frequency x mulitplier)/((pre-divider+1)*post-divider)
  - Mulitplier
  - Pre-divider
  - Post-divider

Figure 7-89. DDR2/3/mDDR Subsystem Block Diagram

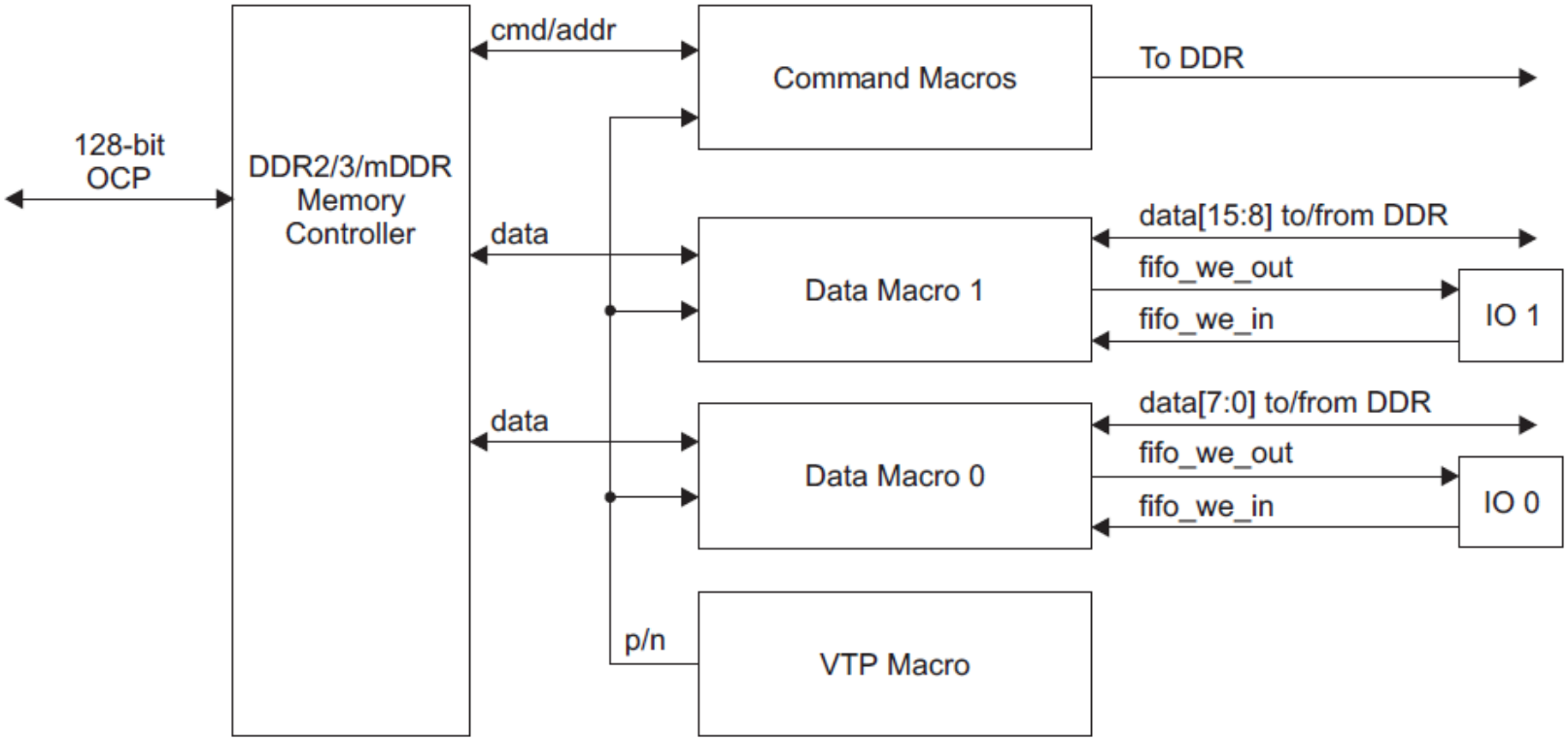


Table 7-99. IBANK, RSIZE and PAGESIZE Fields Information

Bit Field	Bit Value	Bit Description
RSIZE		Defines the number of address lines to be connected to DDR2/3/mDDR memory device
	0	9 row bits
	1h	10 row bits
	2h	11 row bits
	3h	12 row bits
	4h	13 row bits
	5h	14 row bits
	6h	15 row bits
	7h	16 row bits

Bit Field	Bit Value	Bit Description
PAGESIZE		Defines the page size of each page of the external DDR2/3/mDDR memory device
	0	256 words (requires 8 column address bits)
	1h	512 words (requires 9 column address bits)
	2h	1024 words (requires 10 column address bits)
	3h	2048 words (requires 11 column address bits)
IBANK		Defines the number of internal banks on the external DDR2/3/mDDR memory device
	0	1 bank
	1h	2 banks
	2h	4 banks
	3h	8 banks
EBANK		Defines the number of DDR2/3/mDDR memory controller chip selects
	0	CS0 only
	1h	Reserved