DDR3 Design & Debug

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Agenda

- EMIF4 configuration and SW leveling
- Waveform 查看
- Schematics 查看
- Layout 查看
- Debug 方法
- DDR3 Issue分析
- 调试例子

EMIF4 configuration and SW leveling

- 对于DDR3 寄存器配置，及软件leveling，可以参考另一个文档：
  - http://www.deyisupport.com/question_answer/dsp_arm/sitara_arm/f/25/t/17684.aspx

- DDR3 Timing value & EMIF4 register value

```
#define DDR3_EMIF_READ_LATENCY 0x09
#define DDR3_EMIF_TIM1         0x0888A39B
#define DDR3_EMIF_TIM2         0x2E247FDA
#define DDR3_EMIF_TIM3         0x501F821F
#define DDR3_EMIF_SDCFG        0x62C04A32
#define DDR3_EMIF_SDREF        0x0000093B
#define DDR3_ZQ_CFG            0x50074BE4
```

- SW leveling

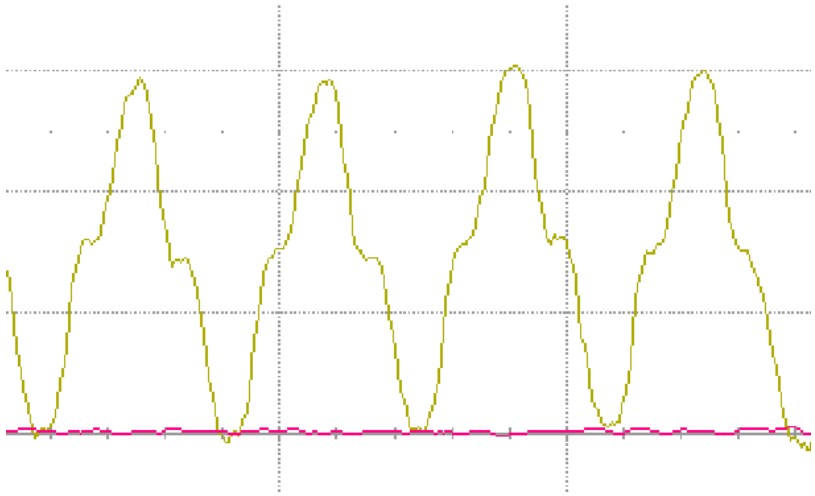
```
#define DDR3_RD_DQS            0X3A //0x3B
#define DDR3_PHY_FIFO_WE       0XA1 //0x10
#define DDR3_WR_DQS            0X3B //0x8
#define DDR3_PHY_WR_DATA       0x77  //0xC
#define DDR3_INVERT_CLKOUT     0x0
```

Parameters		
DDR clock frequency	303	MHz
PHY_INVERT_CLKOUT	0	
Trace Length (inches)		
	Byte 0	*Byte 1*
DDR_CK trace	1.29	1.29
DDR_DQSx trace	1.15	1.15

上述参数在uboot源码目录arch\arm\include\asm\arch-am33xx的ddr_defs.h中

Waveform 查看

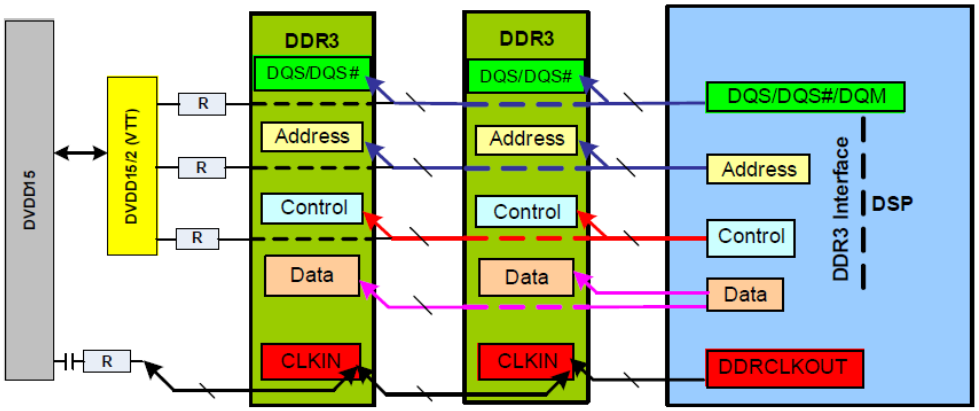
- 在确认寄存器参数配置正确，DDR3读取仍存在问题时，可通过示波器查看DDR3的相关信号。需要查看的信号主要有：
  - CK/CKn
  - DQS/DQSn
  - DQx
  - Ax
- 查看目的：确认上述信号的信号完整性
  - 信号是否有过冲
  - 信号是否有反射



Schematics 查看

- DDR3 原理图
  - 主要检查DDR3的设计是否按照AM335x的DATASHEET上的guide进行
    - 单片16 bit DDR3
    - 双片 8 bit DDR3
  - 可参看starterkit的原理图设计http://www.ti.com/tool/tmdssk3358
    - DDR3 with Vtt termination
  - 或参考Beaglebone-Black的原理图设计 http://beagleboard.org/Products/BeagleBone%20Black
    - DDR3L without Vtt termination

Figure 2 **Typical DDR3 "Fly-By" Architecture**



Note: AM335x 的DDR3参考设计中DQS/DQM未进行Vtt termination

Layout 查看

- DDR3布线检查
  - 严格参考AM335X DATASHEET的“**DDR3 and DDR3L Routing Guidelines**”章节

Debug 方法

- CCS+Emulator
  - 使用CCS+Emulator对DDR3的内存区域内的地址进行读写，查看是否能够正常读写，刷新后是否正常。
- U-boot mtest
  - 通过u-boot中的mtest命令可以简单测试DDR3的读写是否正常。
- Linux booting
  - 在u-boot引导linux kernel启动时，会进行kernel的解压，此时会涉及到内存的频繁操作。所以如果能够成功引导启动，则能说明DDR能够正常读写。

DDR3 Issue分析

- 造成DDR3读写错误或者运行不稳定的可能有：
  - DDR3 EMIF4 寄存器配置不恰当(与对应的DDR3型号不符)
  - Custom board与Starterkit的layout相差比较大，TI默认设置的值无法满足要求，需要重新做SW leveling
  - DDR3原理图设计有误
  - DDR3走线存在问题：未按DATASHEET上的要求走线

调试例子

- **问题描述：**系统能够正常boot，当Linux启动后，运行LCD测试程序会导致系统crash，且出现频率较高，能复现。
- **查看要点：**

a) 是否做过SW leveling

b) 检查 DDR3的timing and EMIF registers设置是否与对应的DDR3型号匹配

c) 检查 DDR3的原理图设计是否有问题

d) 检查DDR3的PCB layout 是否有问题

e) 使用示波器查看关键信号，分析信号完整性

- **问题原因：**查看DDR3布线，发现LCD的数据线走在DDR3的keepout 区域内，且与DDR3数据线距离十分近。

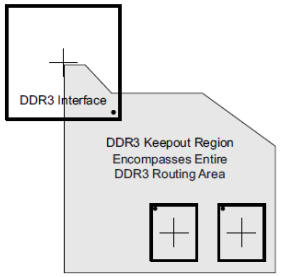


Figure 5-51. DDR3 Keepout Region

Backup

Questions

- How to do single-ended termination for DQS and DQ?

SDRAM termination

- **ZQ calibration**： is intended to control the ODT values and output drivers (Rtt and Ron respectively) of the SDRAM. ZQ calibration is not a controllable feature from the DSP. It is controlled using a precision (1% tolerance) 240 resistor.
- **ODT**： In DDR3, the AM335 controller ODT pins (connected to each SDRAM) serve to turn on or off the SDRAM internal termination. The actual ODT functionality of each SDRAM is controlled using the mode registers (see the respective SDRAM data sheets for additional information).
  - reg_dyn_odt is the dynamic ODT enable/disable feature available in DDR3.
- **SDRAM_CONFIG**:
  - reg_ddr_term is the termination on the DDR. It is used to enable parallel termination on the DDR memory when a WRITE command is issued.

ODT on DDR3

Mode Register

Table 1: MR1 Settings

A9	A6	A2	Rtt_Nom
0	0	0	Nominal ODT disabled
0	0	1	RZQ/4 (60Ω)
0	1	0	RZQ/2 (120Ω)
0	1	1	RZQ/6 (40Ω)
1	0	0	RZQ/12 (20Ω
1	0	1	RZQ/8 (30Ω)
1	1	0	Reserved
1	1	1	Reserved

Table 2: MR2 Settings

A10	A9	Rtt_WR
0	0	Dynamic ODT disabled
0	1	RZQ/4 (60Ω)
1	0	RZQ/2 (120Ω)
1	1	Reserved

Notes: 1. RZQ is a precision 240Ω calibration resistor that is connected on the DRAM from the ZQ ball to VSSQ.

DDR controller termination

- ddr_data0_ioctrl & ddr_data1_ioctrl Register
  - io_config_i：3-bit configuration input to program data IO output impedance.
  - io_config_i_clk：3-bit configuration input to program clock IO pads(DDR_DQS/DDR_DQSn) output impedance.

Table 9-8. DDR Impedance Control Settings [(1)(2)(3)]

I2	I1	I0	Drive Setting Name	Output Impedance (R_{on})	Drive Strength $\|I_{OH}\|$, $\|I_{OL}\|$	Example: R_{on} for R_{ext} = 49.9 ohms	Example: $\|I_{OH}\|$, $\|I_{OL}\|$ for R_{ext} = 49.9 ohms
0	0	0	Drv5	$1.6*R_{ext}$	$0.625*I_{out}$	80 ohms	5 mA
0	0	1	Drv6	$1.33*R_{ext}$	$0.75*I_{out}$	67 ohms	6 mA
0	1	0	Drv7	$1.14*R_{ext}$	$0.875*I_{out}$	57 ohms	7 mA
0	1	1	Drv8	R_{ext}	I_{out}	50 ohms	8 mA
1	0	0	Drv9	$0.88*R_{ext}$	$1.125*I_{out}$	44 ohms	9 mA
1	0	1	Drv10	$0.8*R_{ext}$	$1.250*I_{out}$	40 ohms	10 mA
1	1	0	Drv11	$0.73*R_{ext}$	$1.375*I_{out}$	36 ohms	11 mA
1	1	1	Drv12	$0.67*R_{ext}$	$1.5*I_{out}$	33 ohms	12 mA

(1) These values are programmed in the following registers: ddr_cmd0_ioctrl, ddr_cmd1_ioctrl, ddr_cmd2_ioctrl, ddr_data0_ioctrl, ddr_data1_ioctrl.

(2) Values for DDR_CMDx_IOCTRL.io_config_i_clk should be programmed to the same value.

(3) R_{ext} is the external VTP compensation resistor connected to DDR_VTP terminal.

– io_config_sr：2 bit to program data IO Pads output slew rate.
– io_config_sr_clk： 2 bit to program clock IO Pads (DDR_DQS/DDR_DQSn) output slew rate.

Table 9-7. DDR Slew Rate Control Settings[(1)(2)]

sr0	sr1	Turn-on Time Level	Interface	Turn-on Time for Drv8 Setting (ps) [(3)]	Max Noise on IO Supply for Drv8 Setting [(4)]
0	0	Fastest	1.5 V	117	0.43
			1.8 V	116	0.6
0	1	Fast	1.5 V	430	0.17
			1.8 V	443	0.24
1	0	Slow	1.5 V	530	0.15
			1.8 V	567	0.21
1	1	Slowest	1.5 V	790	0.13
			1.8 V	815	0.18

(1) These values are programmed in the following registers: ddr_cmd0_ioctrl, ddr_cmd1_ioctrl, ddr_cmd2_ioctrl, ddr_data0_ioctrl, ddr_data1_ioctrl.
(2) Values for DDR_CMDx_IOCTRL.io_config_sr_clk should be programmed to the same value.
(3) Value is obtained at nominal PTV.
(4) Value is the average across PTVs.

- DDR_PHY_CTRL_1 Register

9-8	reg_phy_rd_local_odt	R/W	0h	Value to drive on the 2-bit local_odt (On-Die Termination) PHY outputs when output enable is not asserted and a read is in progress (where in progress is defined as after a read command is issued and until all read data has been returned all the way to the controller.) Typically this is set to the value required to enable termination at the desired strength for read usage. 00 = ODT off. 01 = ODT off. 10 = Full thevenin load. Effective ODT is equivalent to 1x the output driver impedance setting in DDR_DATAx_IOCTRL.io_config_i register bits. 11 = Half thevenin load. Effective ODT is equivalent to 2x the output driver impedance setting in DDR_DATAx_IOCTRL.io_config_i register bits.

Leveling

- **Read Leveling**

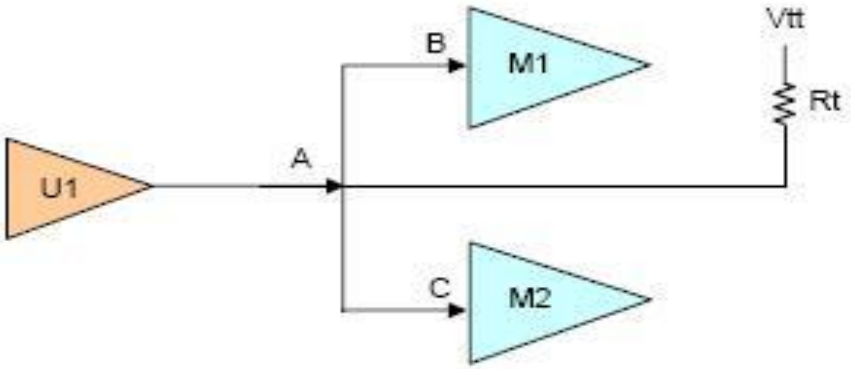
  The memory controller also automatically corrects for delay skew between SDRAMs during Read Leveling. Read Leveling takes advantage of values loaded into the SDRAMs multi-purposed register (MPR). The values loaded into this register are used by the DDR3 controller to calibrate each signal path relative to skew. Each respective SDRAM byte is then internally corrected thus improving performance.

- **Write Leveling**

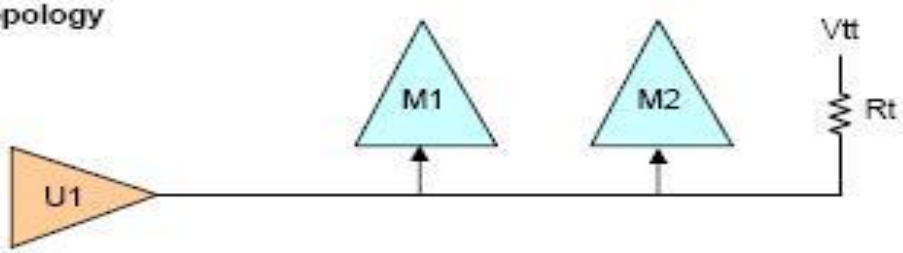
  The memory controller automatically corrects for delay skew between SDRAMs during Write Leveling. During Write Leveling, correction for SDRAM skew (the tDQSS, tDSS and tDSH) is handled using a programmable DQS delay to shore up the timing relationship to the clock and strobe signals. During the Write Leveling procedure the DDR3 controller will delay the DQS until a valid change of state is detected at the SDRAM clock (CK) signal.

DDR3 Topology

Tree topology



Daisy Chain topology



Fly-By topology