KeyStone 2 Self Test Kit on ARM Release Note

Applies to Release 1.0

Publication Date: March 13, 2015

# Overview

This document is the Release Notes of KeyStone 2 Self Test Kit (STK) based on ARM. This software release gives users the ability to debug the KeyStone 2 device and test the performance of KeyStone device, the source code can also be used as reference for customer’s driver code development.

# Platform and Device Support

This release supports the Texas Instruments K2H, K2K, K2E and K2L high performance Multicore DSP+ARM KeyStone 2 System-on-Chip (SoC).

The release is tested and verified on the ARM core of K2H/K EVM, K2E EVM and K2L EVM.

# Dependencies

This release requires following software components and tools versions to successfully function:

* CCS6.1 or higher;
* CSL header files in pdk\_keystone2\_3\_01\_01\_04

# Releases

Below is a summary of the features of all modules.

## Memory Test

|  |  |
| --- | --- |
| **Features** | **Status** |
| Test Masters | All ARM cores, All EDMA TCs |
| Tested memories | MSRAM (Multicore Shared RAM), DDR3A, DDR3B, cache, prefetch buffer |
| Test algorithm | Data pattern filling; Addressing; Bit walking |
|  |  |
| DDR3A configuration | 32 bits x 1333MTS, 64 bits x 1600 MTS |
| DDR3B configuration | 64 bits x 1600 MTS |

## Memory Performance

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Test Masters | ARM core, All EDMA TCs |
| Tested memories | MSRAM, DDR3A, DDR3B |
| Cache/Prefetch buffer configuration cases | No cache and no prefetch; cache and perfetchable |
| ARM core memory copy throughput | √ |
| ARM core read/write latency | √ |
| EDMA memory copy throughput | √ |
| EDMA transfer overhead | √ |
| EDMA test with different ACNT | √ |
| EDMA test with different Index | √ |
|  |  |
| DDR3A configuration | 32 bits x 1333MTS, 64 bits x 1600 MTS |
| DDR3B configuration | 64 bits x 1600 MTS |

## Multicore Navigator

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Test Masters | ARM core, QMSS Packet DMA 1 and 2, PA packet DMA |
| Test with different memory buffer | MSRAM, DDR3A |
| Descriptor types | Host, Monolithic |
| Tested Queue Manager | QM1, QM2 |
| Tested INTD | INTD1, INDT2 |
| linking RAM | Internal, External |
| Core Cycles for PUSH/POP operation through VBUSP and VBUSM | √ |
| Interrupt latency for queue pending | √ |
| descriptor accumulation latency | √ |
| descriptor Reclamation latency | √ |
| Packet DMA Throughput | √ |
| Packet DMA transfer overhead | √ |

## Timer

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| one-shot pulse and interrupt | √ |
| continual clock and interrupts | √ |
| square waves with special duty cycle | √ |
| watch-dog and exception | √ |

## HyperLink

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Test Master | ARM core, EDMA |
| Test with different memory buffer | MSRAM, DDR3A, DDR3B |
| Internal loopback | Serdes loopback |
| Test between two devices | √ |
| Integrity test | Data pattern filling; Addressing test |
| ARM core memory copy throughput | √ |
| ARM core read/write latency | √ |
| EDMA memory copy throughput | √ |
| EDMA transfer overhead | √ |
| Interrupts test | √ |
|  |  |
| Speed | 3.125Gbps, 5Gbps |

## PCIE

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Test Master | ARM core, EDMA |
| Test with different memory buffer | MSRAM, DDR3A, DDR3B |
| Internal loopback | Serdes loopback |
| Test between two devices | √ |
| Integrity test | Data pattern filling; Addressing test |
| ARM core memory copy throughput | √ |
| ARM core read/write latency | √ |
| EDMA memory copy throughput | √ |
| EDMA transfer overhead | √ |
| Interrupts test | √ |
|  |  |
| Speed | 5Gbps, 2.5Gbps |

## GE (Gigabit Ethernet)

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Internal loopback | EMAC, SGMII, Serdes loopback |
| Test between two devices | External loopback, data from device 0 to device 1 |
| Test with different memory buffer | MSRAM, DDR3A |
| Multiple ports test | √ |
| Throughput test | √ |
| Interrupts test | √ |
|  |  |
| Speed | 10Mbps, 100Mbps, 1000Mbps |

## SPI

|  |  |
| --- | --- |
| **Features** | **Status** |
| Test Masters | ARM core, EDMA |
| internal loopback | √ |
| FLASH test | Data pattern filling; Addressing |
| Max test Speed | 66MHz |

## UART

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Test Masters | ARM core, EDMA |
| internal loopback | √ |
| Tests between EVM and PC | Echo to PC; continuous data patterns transfer between EVM and PC |
| Max test Speed | 3Mbps |

## GPIO

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Direction | input, output |
| loopback test | √ |
| Interrupts | √ |

## Robust features

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Test masters | ARM core, EDMA |
| Memory Protection | MSRAM, DDR, Reserved space |
| EDC | MSRAM, DDR |
| MPU (Peripherals protection) | √ |
| watch-dog and exception | √ |
| EDMA error handling | √ |

## EMIF

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| NAND FLASH | √ |
| NOR FLASH | √ |

## I2C

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| internal loopback | √ |
| EEPROM test | √ |
| I2C speed | 400K |

## USIM

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Read ATR | √ |
| Read ICCID | √ |