AM389x /C6A816x Schematic Review Checklist

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Introduction

This article applies to the following devices:

- AM3894
- AM3892
- TMS320C6A8168
- TMS320C6A8167

General Recommendations

THIS SECTION IS TRANSCLUDED FROM HARDWARE DESIGN CHECKLIST. ONLY INFO GENERIC TO ALL DEVICES BELONGS HERE SINCE IT APPEARS IN ALL SCHEMATIC CHECKLISTS.

As you are creating the schematics for your project here are a few things to consider.

Before you begin

Documentation

Make sure you have the latest version of documentation, especially the data sheet and silicon errata.

TIP: Try searching the documentation for words such as: "must", "require", "do not", "shall", "note:", etc. Important criteria for the device will typically contain one or more of these words. This is an easy way to make sure you have not missed anything important.

TIP: - on each ti.com device product folder there is a button "Alert me about changes to this product". Registration here will enable proactive automatic notification of device errata.

Pin out

- Have you verified that your pin labels correspond to the correct pin numbers?
- Have you verified that the power pins are connected to the correct supply rails?
- Pullups/Pulldowns: If opposing an internal resistor use 1k resistor. To complement use weaker value such as 4.7k resistor.

Critical Connections

Decoupling Capacitors

Voltages from traces on a printed circuit board can couple to each other in places where it is not desired, (like power supply planes). To decouple the traces, we add capacitors to absorb some of the voltage and help reduce this effect. For more information on how to correctly place decoupling caps, see the data sheet section for power-supply decoupling.

PLL and some analog supplies benefit from filters or ferrite beads to keep the noise from causing clock jitter. The minimum recommendation is a ferrite bead with a resonance at 100 MHz along with at least one capacitor on the device side of the bead. Additional recommendation is to add one capacitor just before the bead to form a Pi filter. The filter needs to be as close as possible to the device pin, with the device side capacitor being the most important thing to be close to the device pin. PLL pins close together can be combined on the same supply. PLL pins farther away from each other may need their own filtered supply.

Refer to General Hardware Design/ BGA PCB Design/BGA Decoupling Wiki [1]

Power Sequencing

Are all requirements being met in terms of the order, delays, etc. of the power supplies?

Clocking

Make sure your input clock/crystal meets the data sheet requirements. For example:

- Frequency
- ESR for crystal
- Crystal and caps placed physically close to processor
- Double check proper voltage level for clock (some devices will use core voltage, others I/O voltage).
- If there are any PLL configuration pins make sure they are set such that the resulting frequency is within device spec. Also, having alternate population options for those PLL pins could be handy.

Reset

Make sure that reset is kept asserted for the processor as the power supplies are ramping. You must not release the processor from reset until all the proper voltage/clocking is in place as specified by the data sheet. Conversely make sure that something on the board is actually RELEASING the reset once power and clocks are stable!

A useful tip is to place a 0.1uF cap near the reset pin to help avoid ESD-induced resets.

Also, you might want to have a reset button on your board as it can be helpful for development.

Boot modes

- Double check that the boot configuration pins are set to the correct option.
- It's highly recommended to have some population options to be able to easily change the reset mode. This can be handy in a variety of circumstances. For example, if you were doing a NOR flash boot and you ever accidentally put in some bad code you might end up in a scenario where you can't connect to the device with emulator because it's in a bad state, and you can't reprogram the flash as a result! Having an alternate boot mode can be a life saver!
- **CAUTION:** Be careful if *anything* is hooked up to these pins (i.e. if the pins are have multiple uses such as GPIO or other peripherals). You must make sure that the boot pins are at the proper levels when power-on reset occurs such that the correct values are latched in order for the device to boot correctly!

Pin Muxing

Although pin muxing is frequently software configurable, often the initial configuration is dependent on several configuration pins (e.g. are they high or low when reset is released). Make sure that the initial pin muxing corresponds properly with your boot modes so that any interfaces necessary for boot will be available. On some devices this could potentially be handled by the boot ROM, but to be certain you should configure the initial pin muxing appropriately.

Peripherals

USB

- Check that there are no unnecessary USB_DM or USB_DP connections that would form stubs.
- Check that there is nothing on the DP/DM lines (except for possibly a USB 2.0 certified surge suppressor)
- Check that the USB PCB routing guidelines will be followed.
- USB supports hot insertion and removal so it is very vulnerable to ESD resulting from this. External ESD protection like the Semtech RClamp0502B is recommended. Any USB 2.0 certified ESD protection chip is acceptable as long as the USB PCB routing guidelines are followed.

DDR2 Routing Checklist

Each device contains very specific requirements for DDR2 routing in the data sheet. Those requirements must be strictly adhered to. Here are some general tips. Although this is not a comprehensive list, it gives the main points of the document in checklist form.

Stackup

- All layers with DDR2 routing have an adjacent ground plane
- No cuts in the ground plane under DDR2 routing

Placement

- DDR2 devices placed within maximum distances from DSP
- Non-DDR2 signals are kept outside the DDR2 keep out region
- 1.8V power plane covers entire DDR2 keep out region

Bypass Capacitors

- Each bypass capacitor has its own power and ground vias not shared with DSP or memory balls.
- Number and value of bypass capacitors used meets minimums required by spec

Topology

- CK and ADDR_CTRL net classes use balanced T topology
- Skew matching has been performed properly according to spec
- No trace length exceeds the longest Manhattan distance +50 mils (or whatever datasheet specifies) for each net class

Other

- Make sure ODT pin on DDR2 device is grounded

I2C

- ~5K pull ups on both lines (only one set, or two sets of 10K pull ups) are recommended
- Make sure all devices on a given I2C bus have unique addresses (often this is configurable through a pin to enable multiple of the same device)

UART

This simple peripheral is frequently hooked up incorrectly. Make sure it's connected as follows:

- `TX ---> RX`
- `RX <--- TX`

Debug Considerations

JTAG/Emulation

This is something often done incorrectly which can severely impact your ability to develop code!

- Please follow these recommendations when designing your JTAG interface.
- You might also want to look at the article JTAG Connectors when deciding which header to put on the board. Double-check the pin-out!

Signal Visibility

For debugging purposes you may need to look at a signal on an oscilloscope. Therefore you'll want to make sure you can get access to the signals, particularly with BGA devices where it might otherwise be impossible. This can be done by bringing a via all the way through the board or other times where a pullup/pulldown is needed you can probe at the resistor. Having a GPIO brought to a test point or an LED can be useful as well.

Other

Voltage Level Changes

Can you change the supply voltage with some simple resistor changes? Sometimes a pin-for-pin compatible release is made at a higher speed, sometimes requiring higher voltage and so having this flexibility on your board can save you trouble later.

Signal Terminations

Careful attention should be paid to any notes in the data sheet regarding the correct termination of pins. In particular make sure that termination instructions are exactly followed on reserved pins. Also, there are often pins that have special significance at the time the device reset is released. Often these are documented with something like "do not oppose this pin at reset" meaning that if there is an internal pullup or pulldown on that pin, you should not drive that pin in the opposite direction at reset. This would include not putting an opposing pullup/pulldown and also making sure that anything connected to that pin does not drive the pin opposite the intended direction.

For any unused pin you should pay attention to how it is terminated. Frequently pins will default to an input state and if they are left floating they may pick up noise and toggle at a high frequency. This can cause significant unwanted current consumption. Unused pins should be checked to see if they can be configured through software as outputs so they are not floating. If there is an internal pull-up/down you should configure the level of the output (high/low) to match the pull-up/down for lowest current consumption.

References

This article began from spraa34 which was a design checklist for the DM642. It has been generalized a bit to make it more applicable to all designs.

References

[1] http://processors.wiki.ti.com/index.php/General_hardware_design/BGA_PCB_design/BGA_decoupling

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