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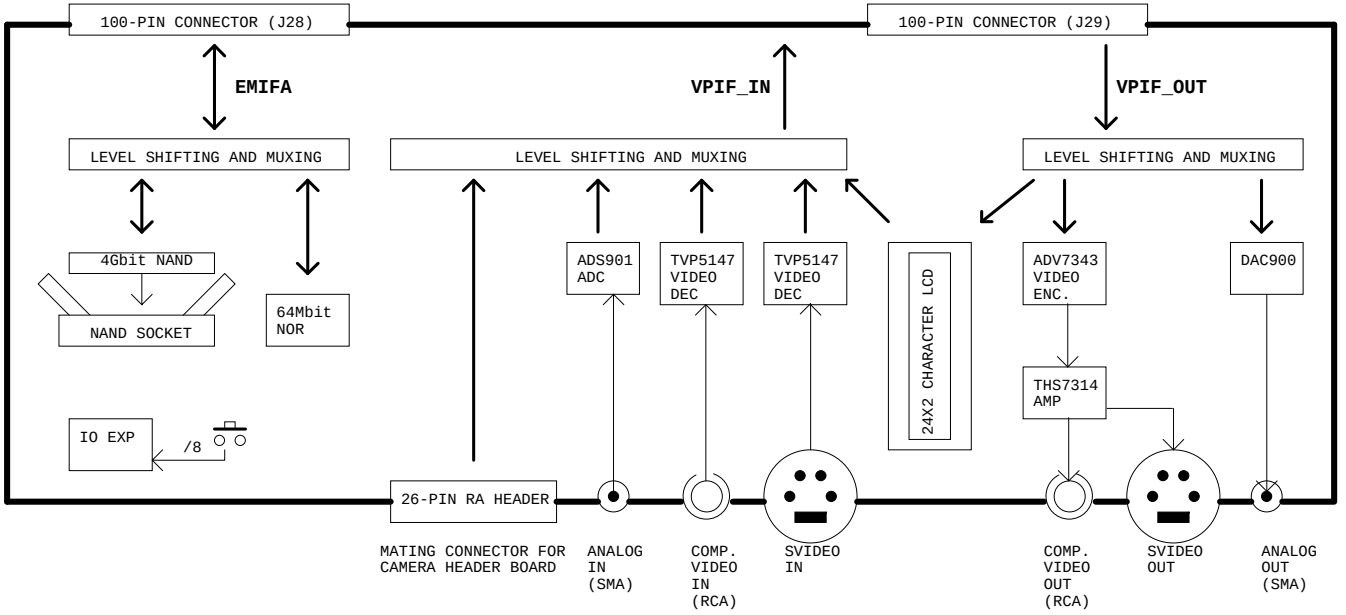
SYSTEM BLOCK DIAGRAM



IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

3) DESIGN NOTES in red are critical, and must be understood and followed.

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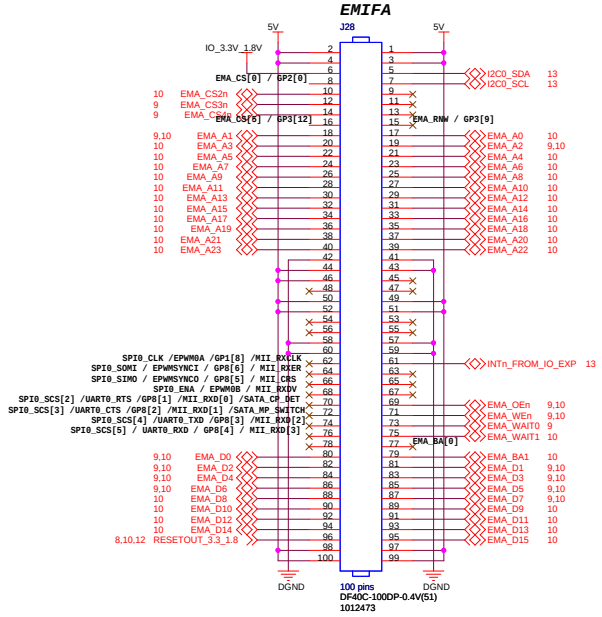
I2C ADDRESSING

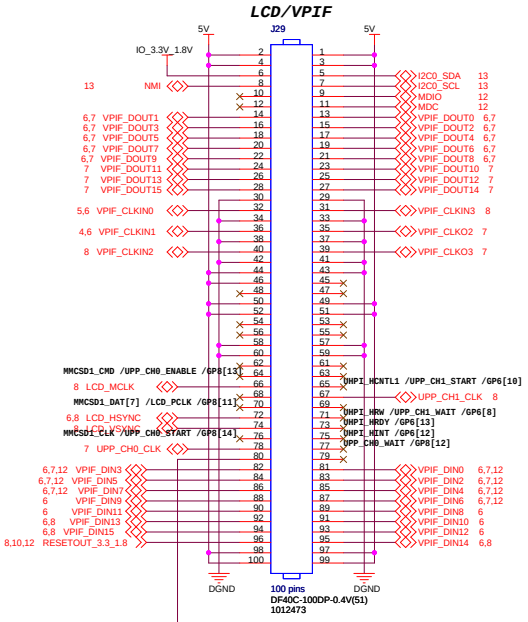
(ALL DEVICES ARE ON PROCESSOR I2C0)

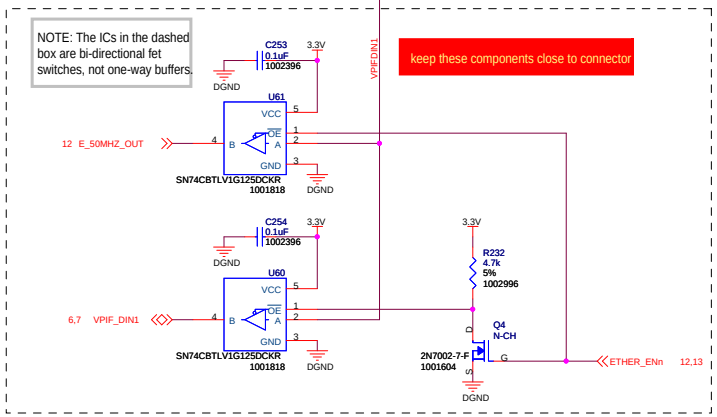
FUNCTION	DEVICE	ADDRESS
COMP & S VIDEO ENC.	ADV7343	0101 010
COMP. VIDEO DEC.	TVP5147	1011 101
S-VIDEO DEC.	TVP5147	1011 100
CAMERA IMAGE SENSOR**	VARIES	VARIES
IO EXPANDER	PCF8575	0100 000
CLOCK SYNTHESIZER	CDCE913	1100 101

**I2C address of camera image sensor will vary depending on which camera is used. Consult your camera's datasheet for image sensor I2C address.

02 - BASEBOARD CONNECTORS







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Title TI FREON UI DAUGHTERCARD		
Size C	Number 1013887	Rev 1
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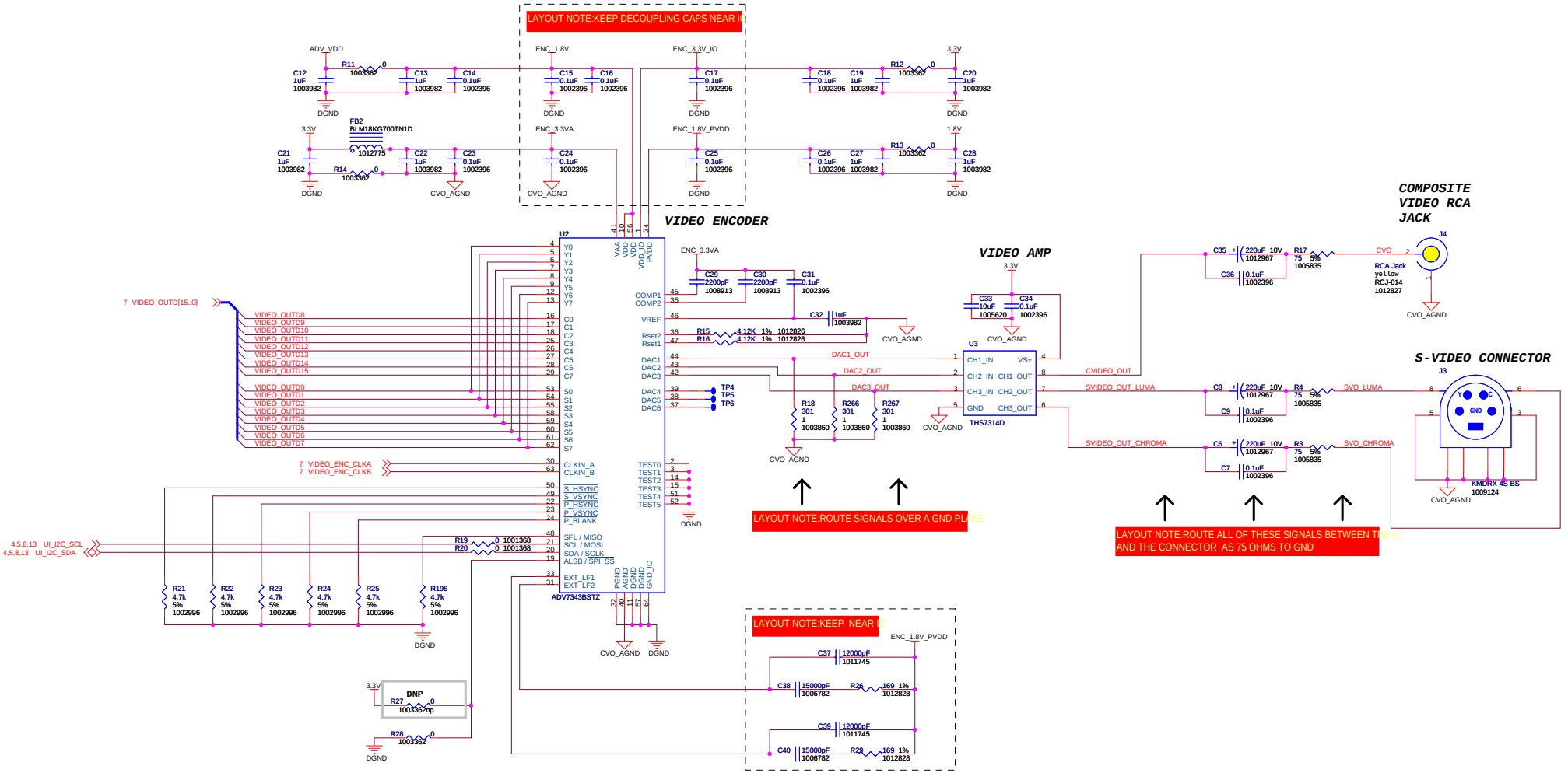
04 - VIDEO OUT



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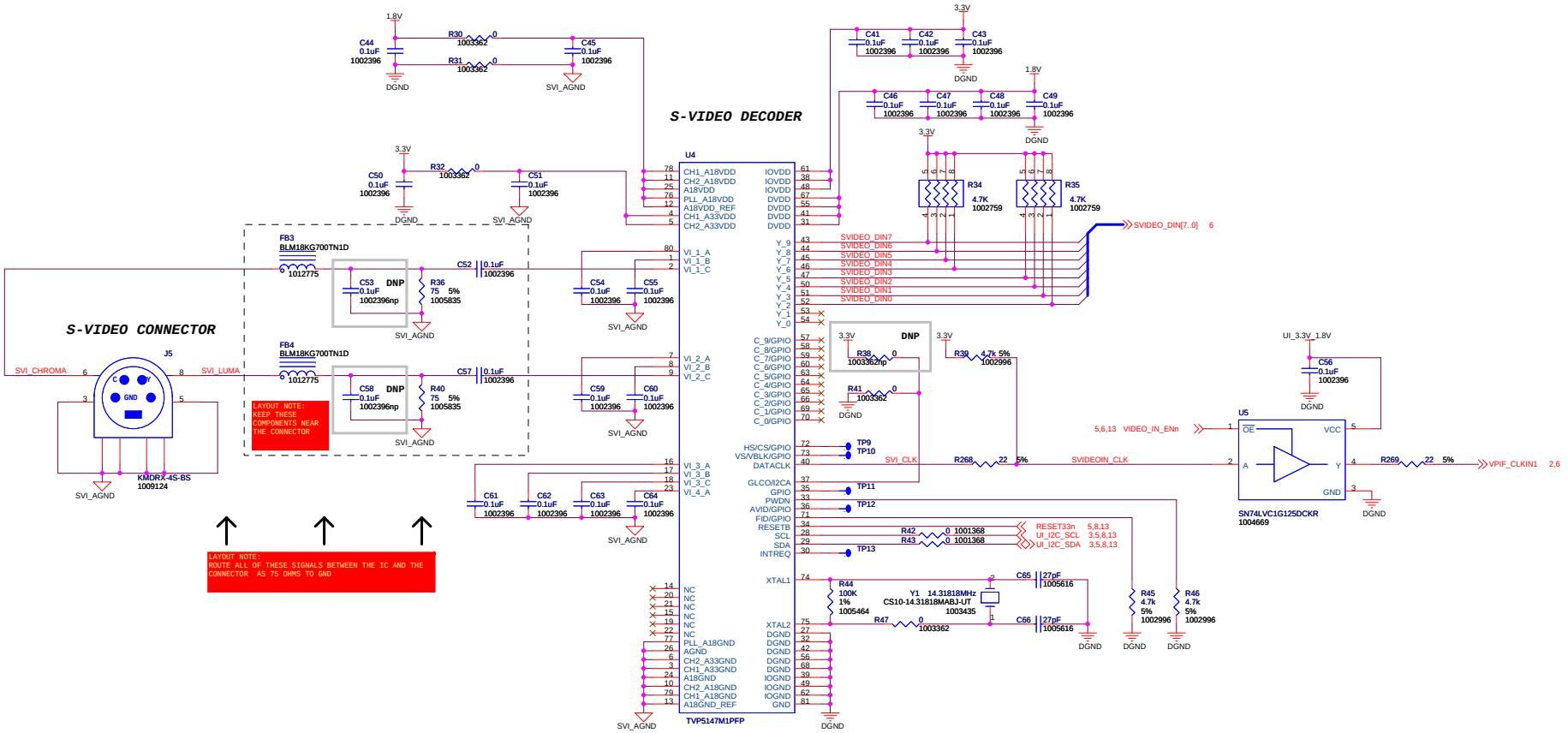
05 - S-VIDEO IN



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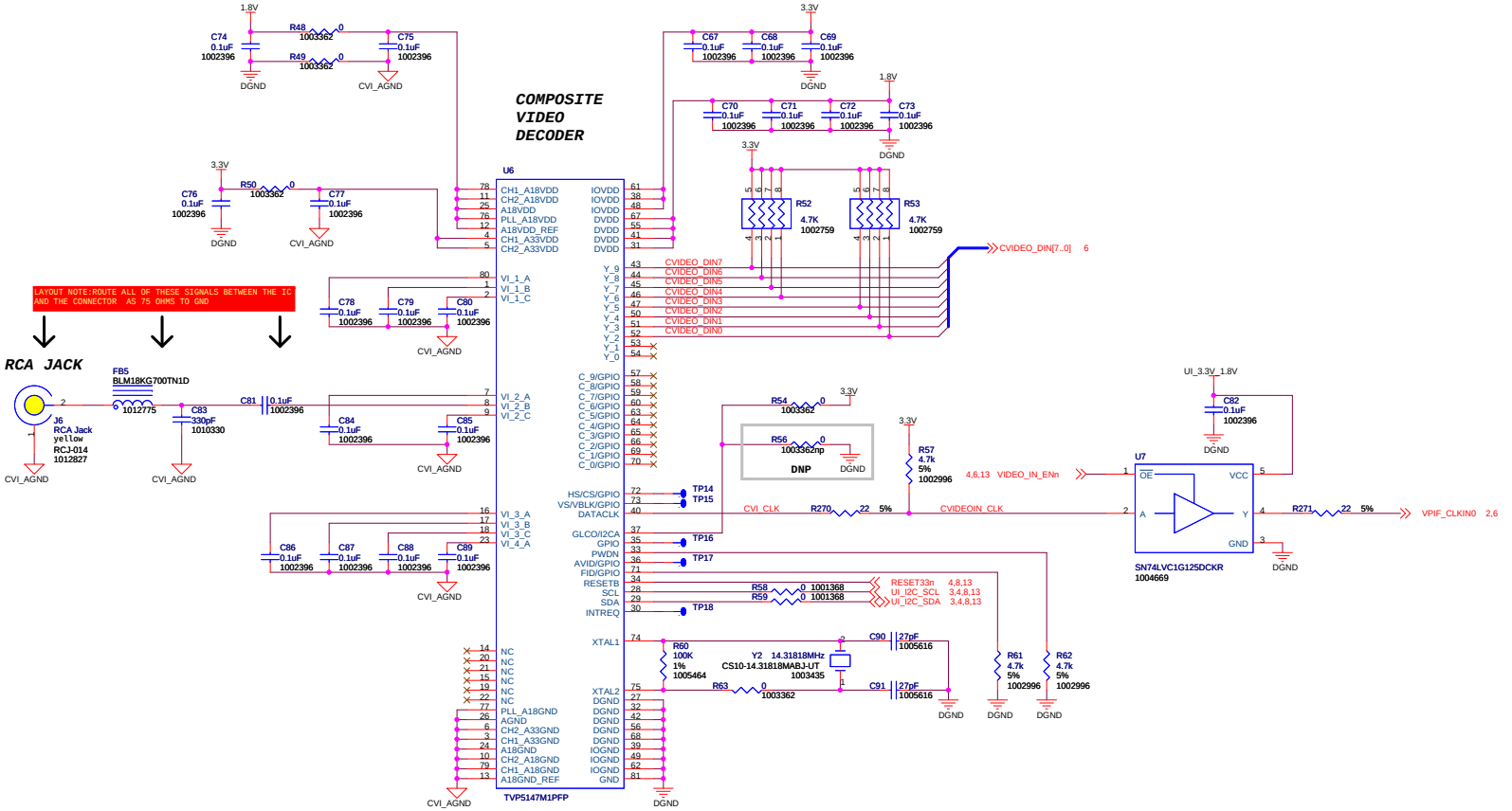
06 - COMP VIDEO IN



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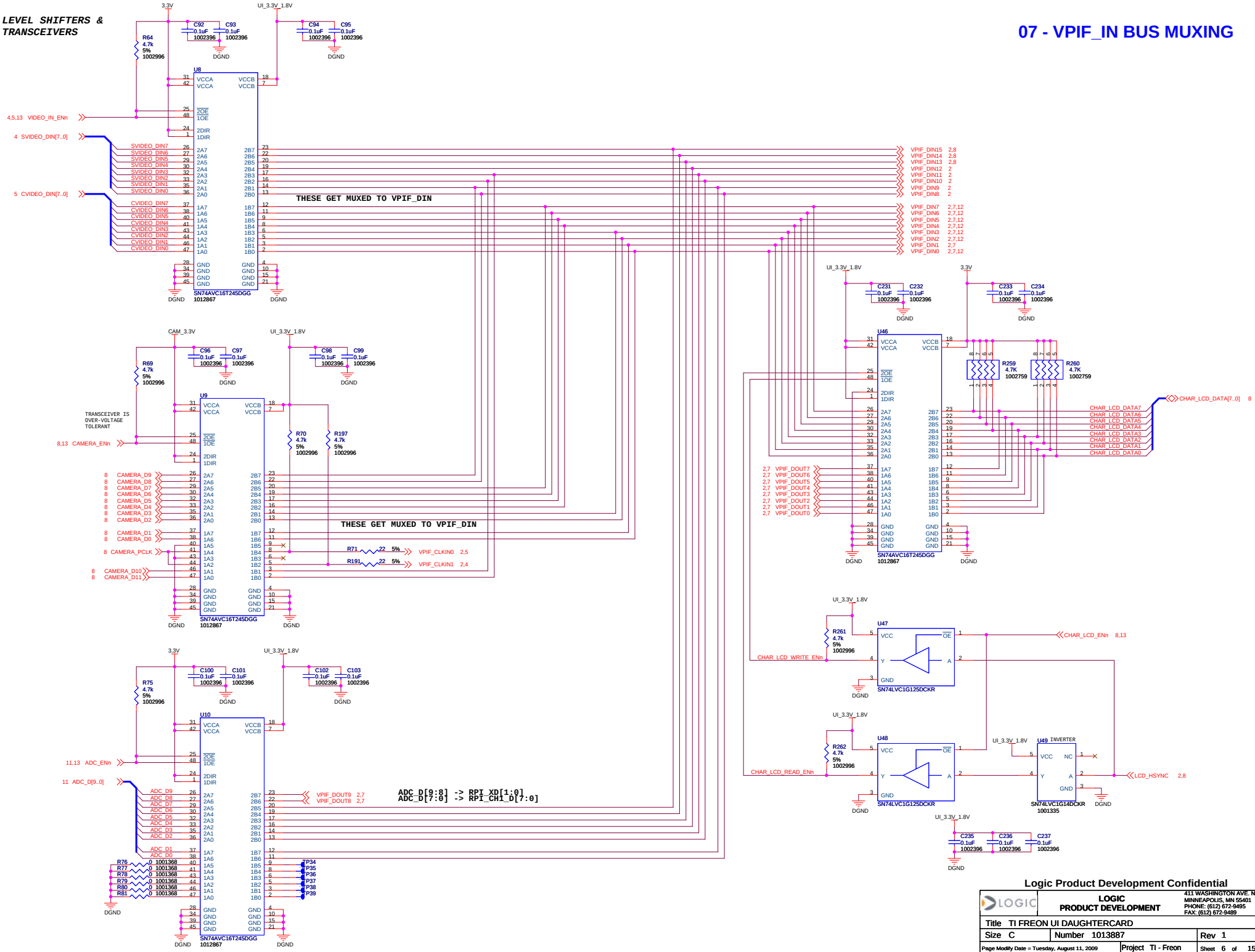
LEVEL SHIFTERS & TRANSCEIVERS

07 - VPIF_IN BUS MUXING



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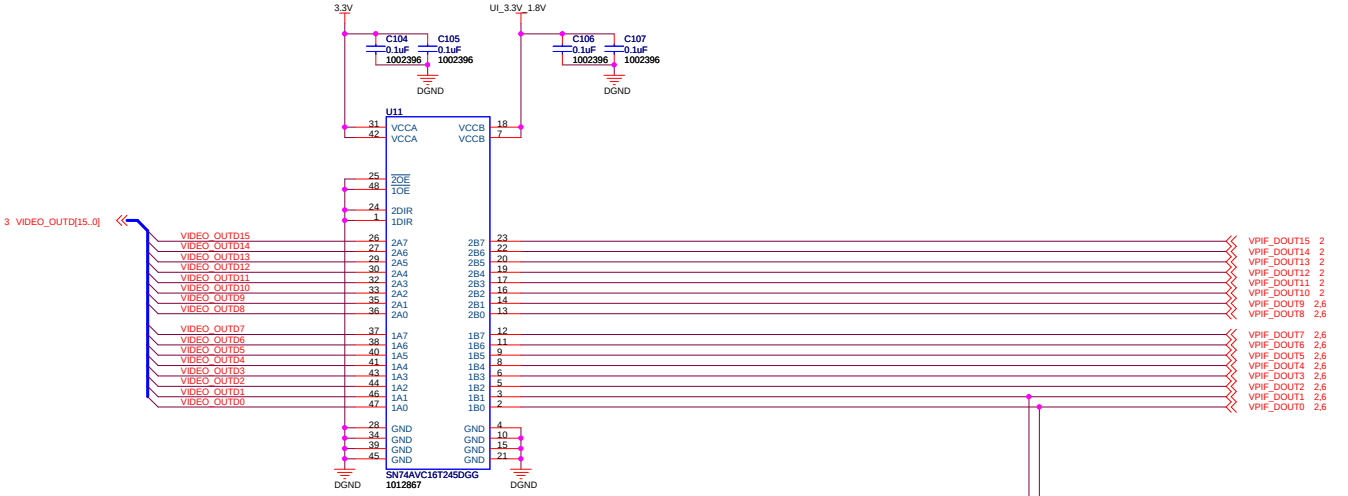
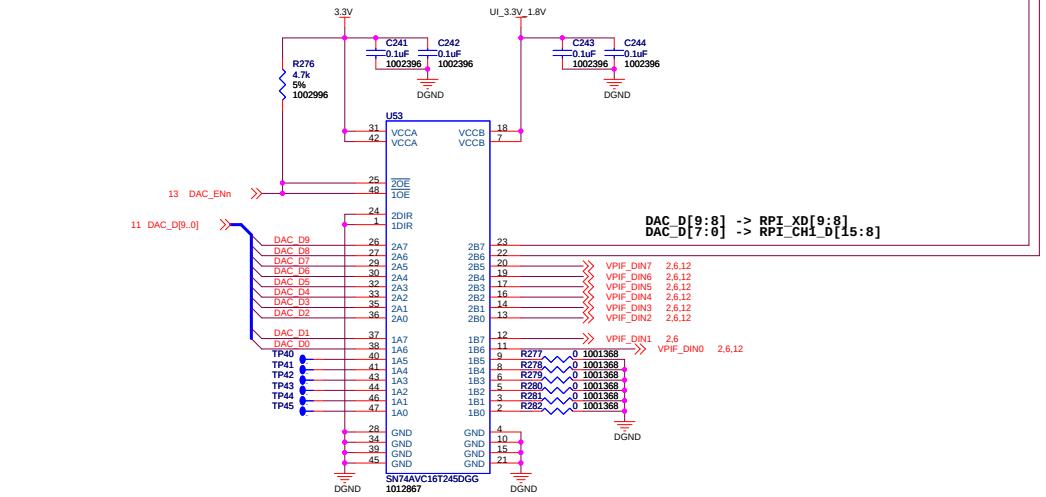
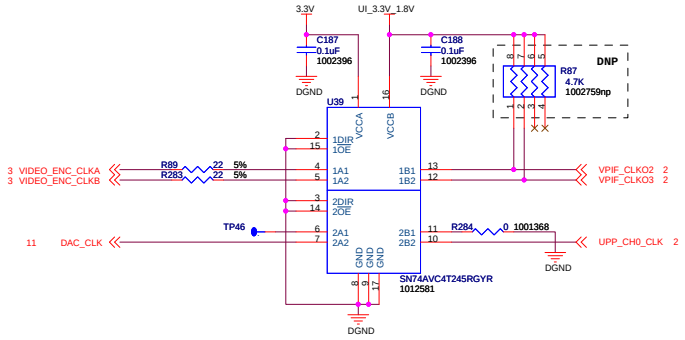
LEVEL SHIFTERS & TRANSCEIVERS

08 - VPIF_OUT BUS MUXING







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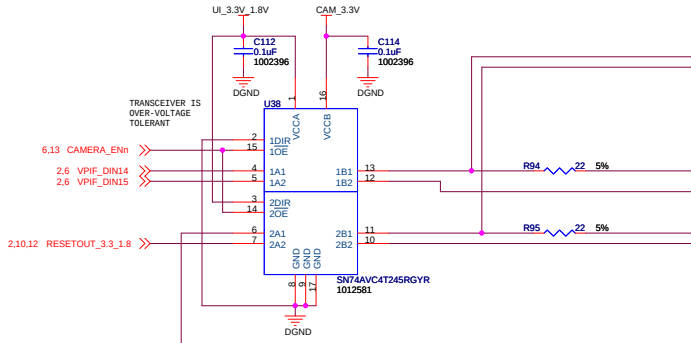
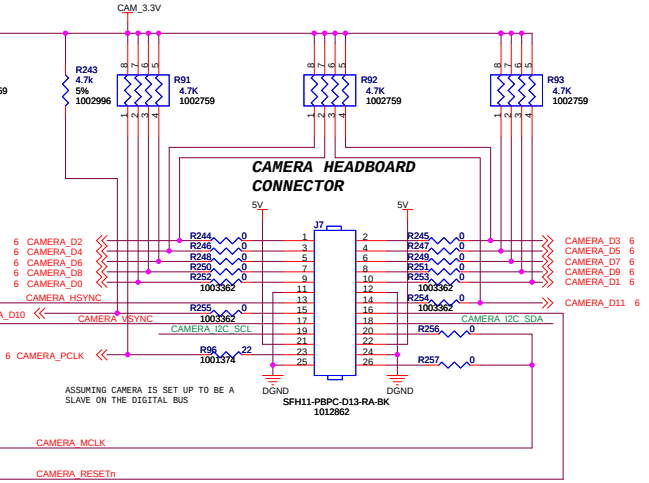
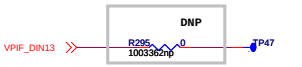
9 - CAMERA & CHARACTER LCD

LEVEL SHIFTER & TRANSCEIVER

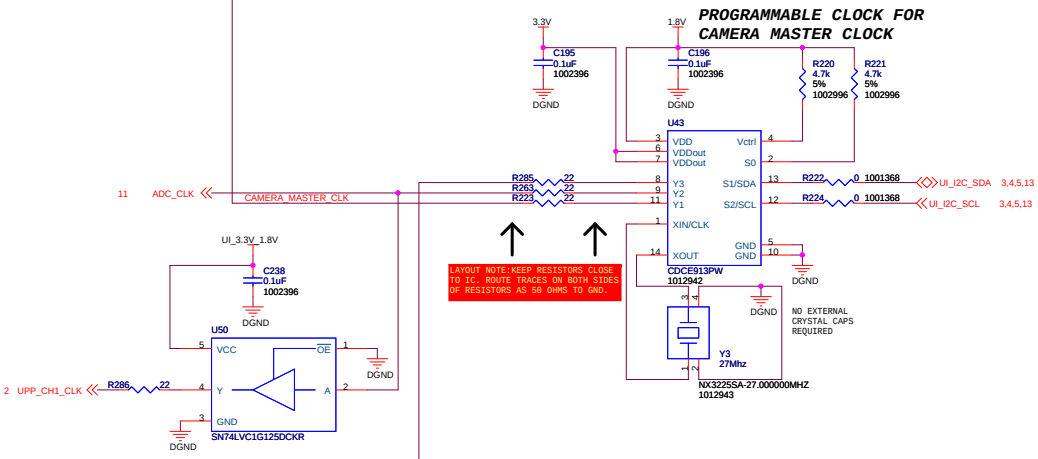


CAMERA HEADBOARD CONNECTOR

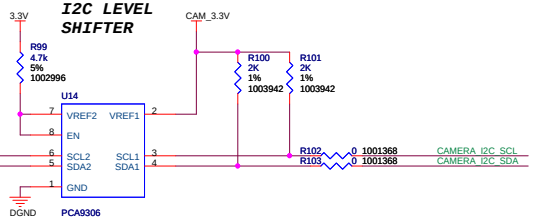




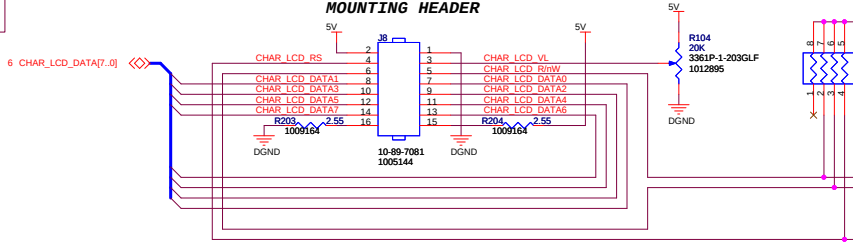
PROGRAMMABLE CLOCK FOR CAMERA MASTER CLOCK



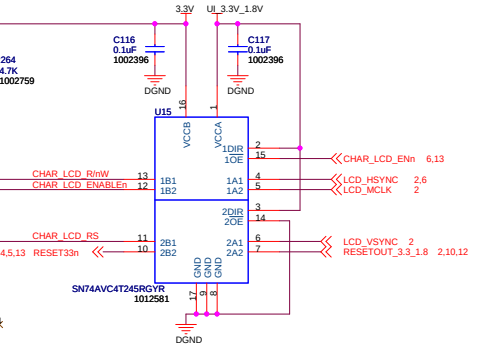
I2C LEVEL SHIFTER



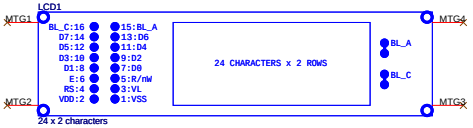
CHARACTER DISPLAY MOUNTING HEADER

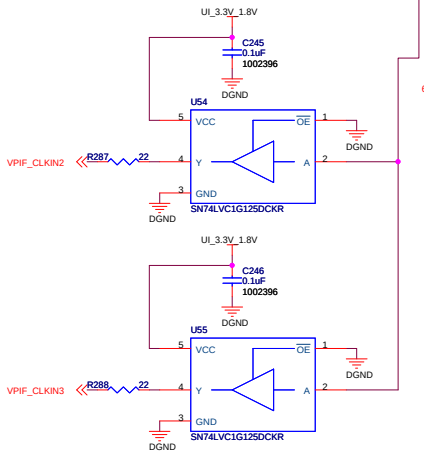


LEVEL SHIFT



24X2 CHARACTER DISPLAY





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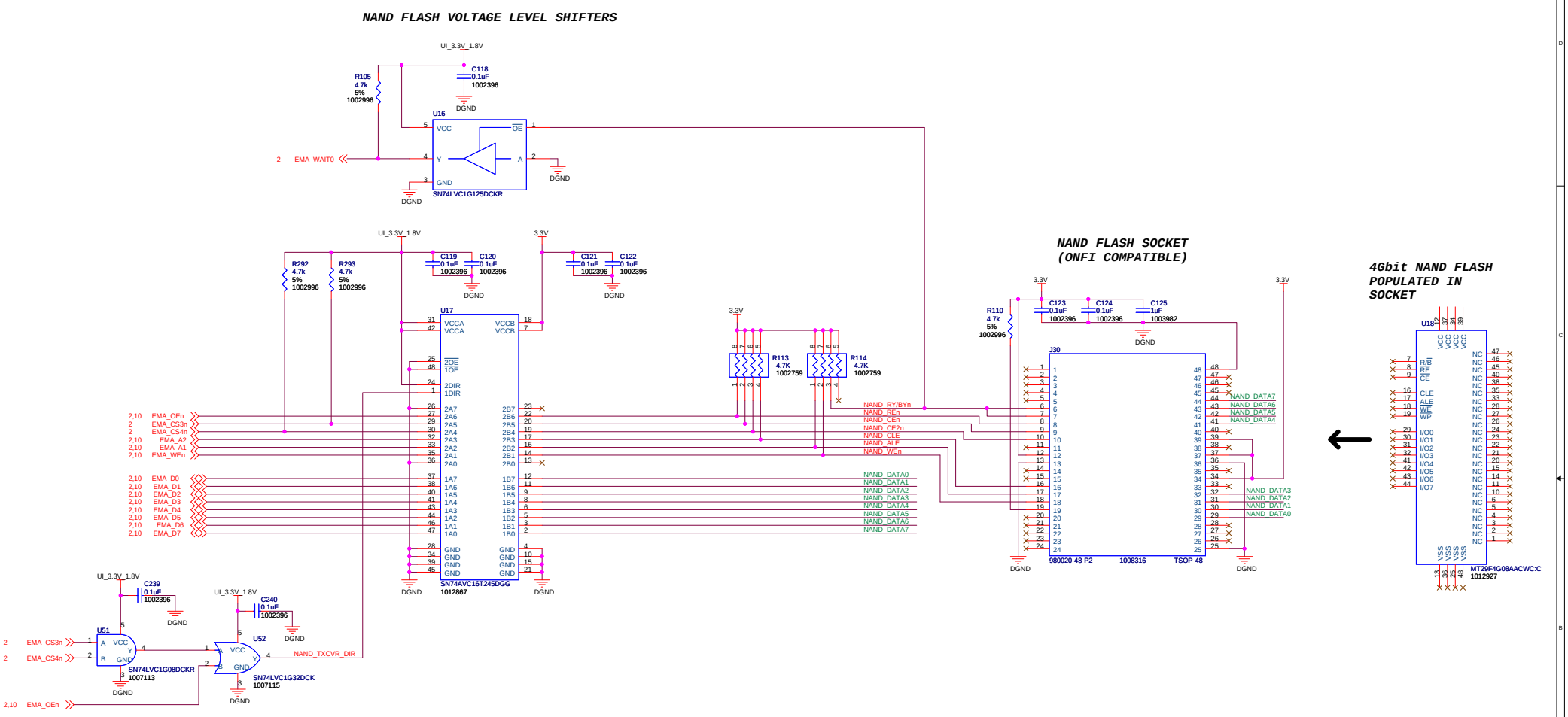
10 - NAND BOOT FLASH



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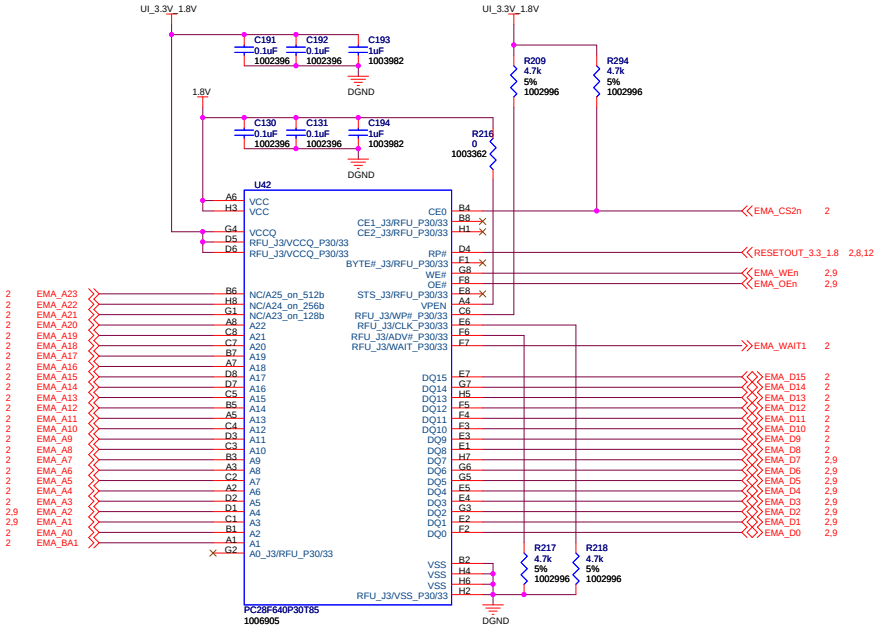
11 - NOR BOOT FLASH



NOTE: NOR FLASH IS SET UP FOR ASYNCHRONOUS MODE ONLY.

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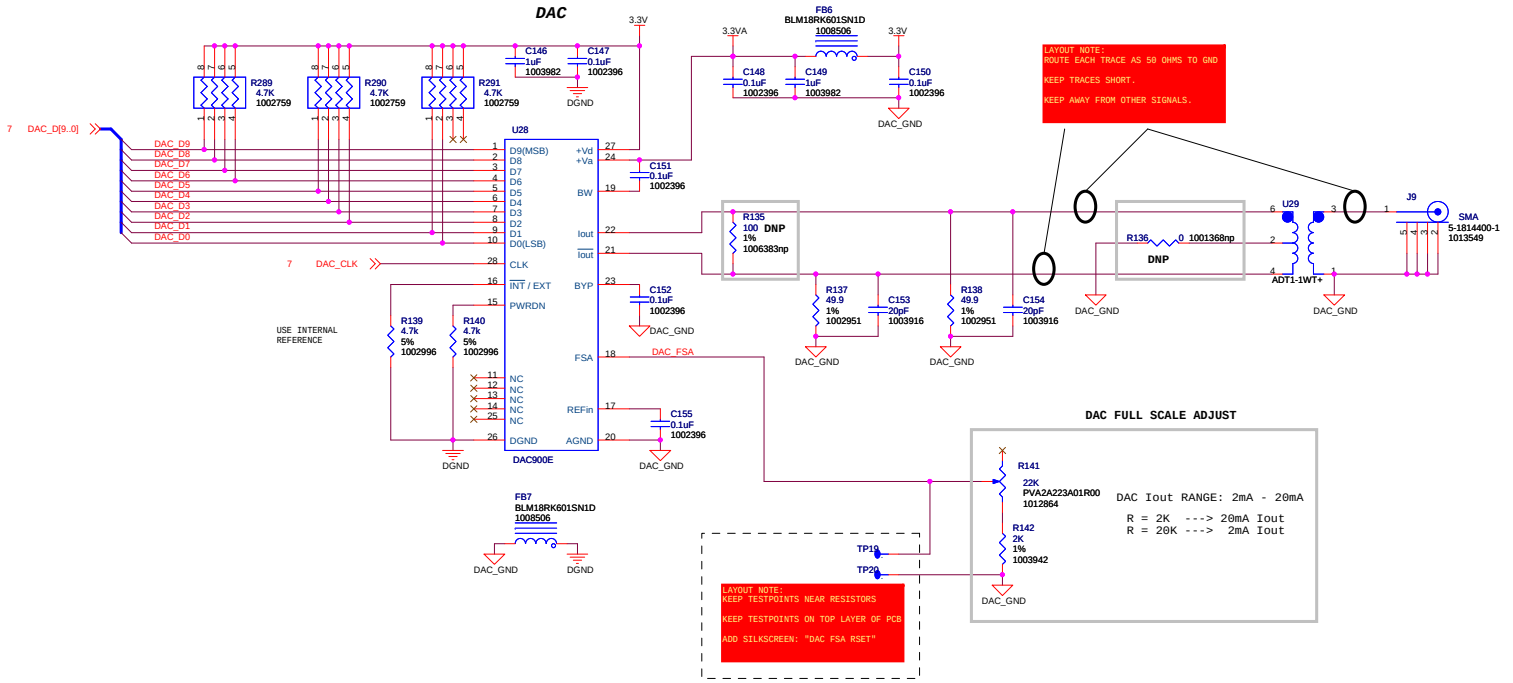
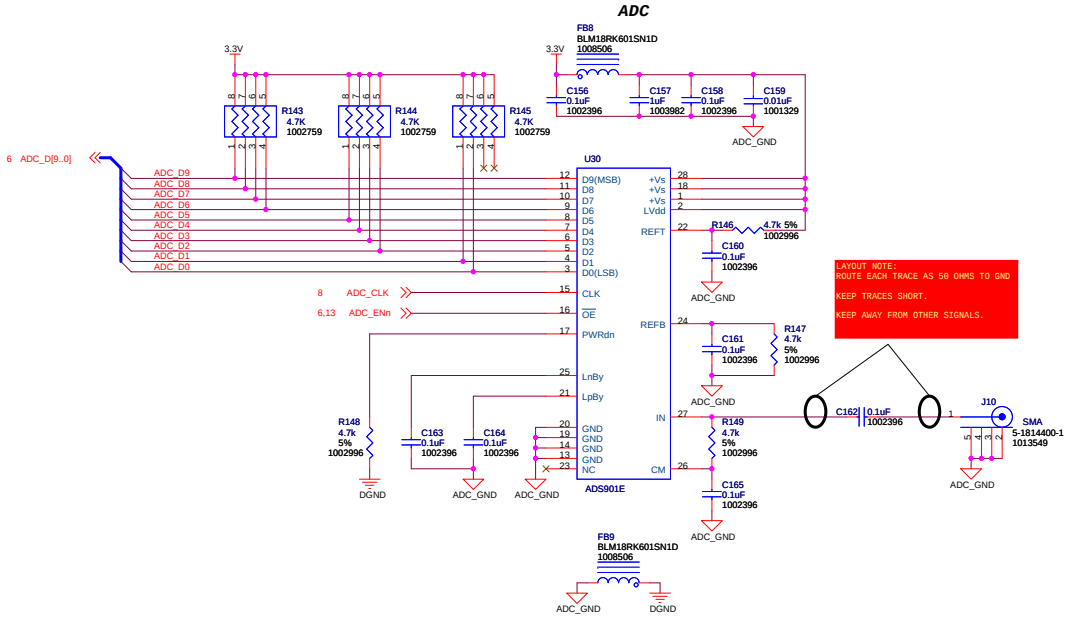
12 - DAC & ADC





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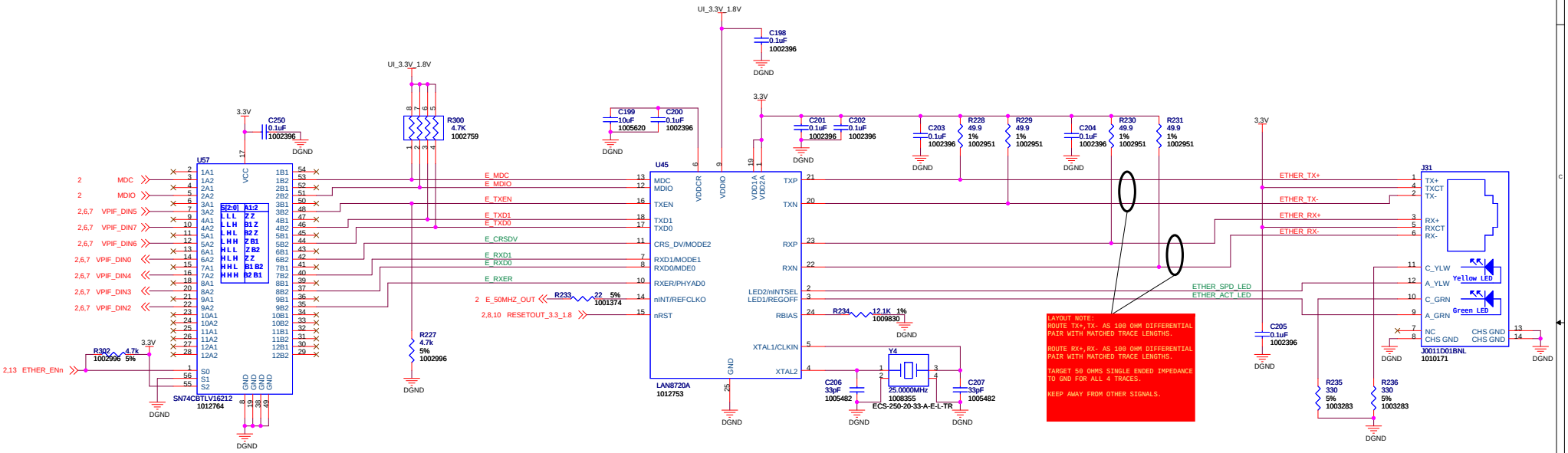
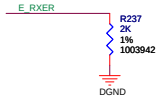
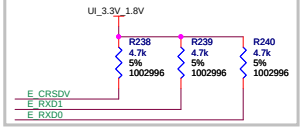
13- ETHERNET



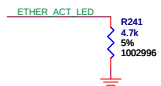
PHY ADDRESS 0



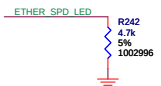
MODE = "111" = ALL CAPABLE



OUTPUT 50MHZ CLOCK



INTERNAL 1.2V REGULATOR ON



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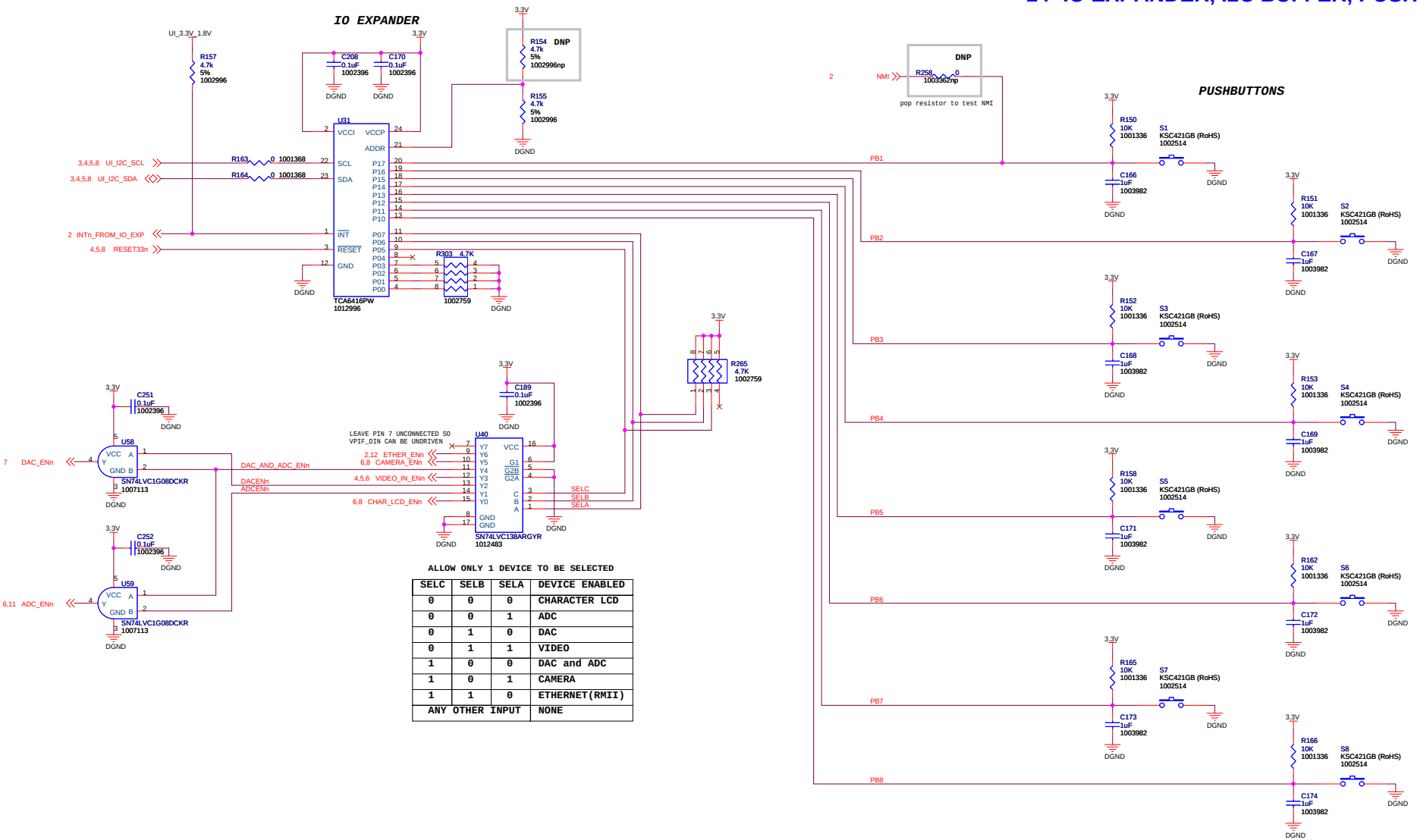
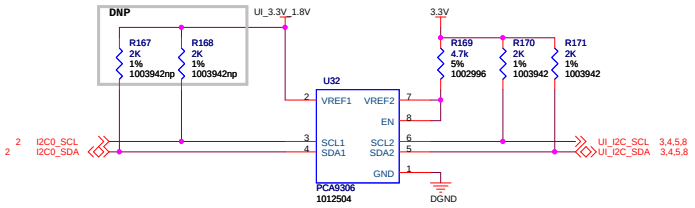
14- IO EXPANDER, I2C BUFFER, PUSHBUTTONS



ALLOW ONLY 1 DEVICE TO BE SELECTED

SELC	SELB	SELA	DEVICE ENABLED
0	0	0	CHARACTER LCD
0	0	1	ADC
0	1	0	DAC
0	1	1	VIDEO
1	0	0	DAC and ADC
1	0	1	CAMERA
1	1	0	ETHERNET(RMII)
ANY OTHER INPUT			NONE

I2C LEVEL SHIFTER



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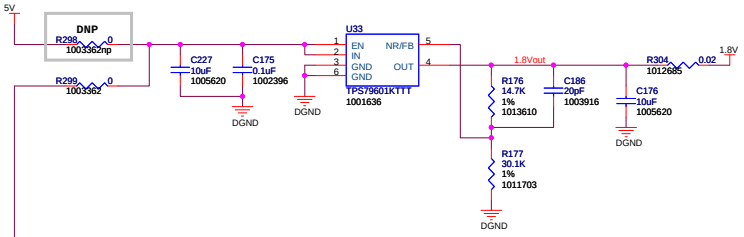
15 - POWER

GROUND REFERENCE PROBE TESTPOINTS

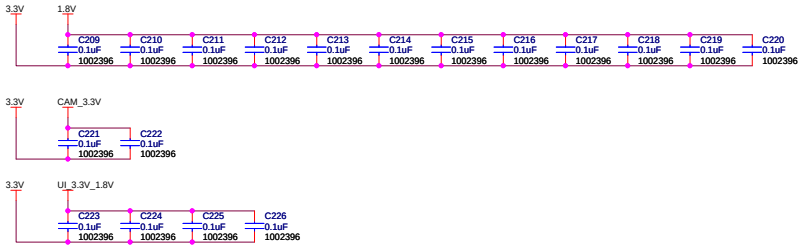
J32 TSW-102-23-T-S 1003098
J33 TSW-102-23-T-S 1003098
J34 TSW-102-23-T-S 1003098
J35 TSW-102-23-T-S 1003098

LAYOUT NOTE: DISTRIBUTE THESE AROUND THE BOARD IN EASILY ACCESSED LOCATIONS

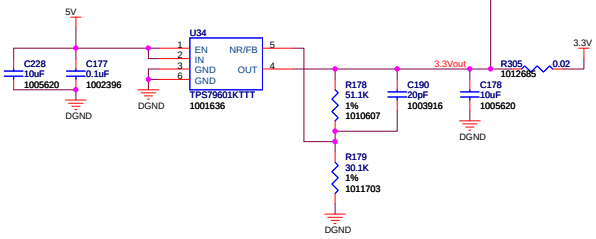
1.8V SUPPLY



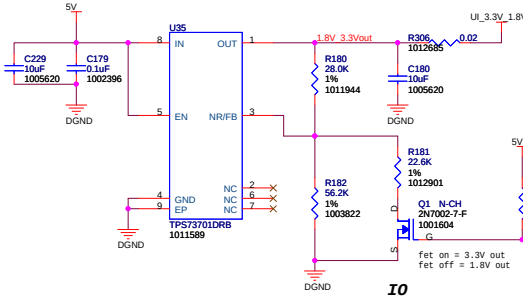
LAYOUT NOTE: STITCHING CAPS - PLACE THESE WHERE DIGITAL SIGNALS CROSS THE 1.8V POWER POUR.



3.3V SUPPLY

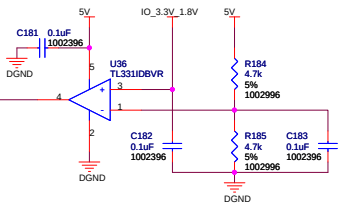


1.8V / 3.3V SUPPLY



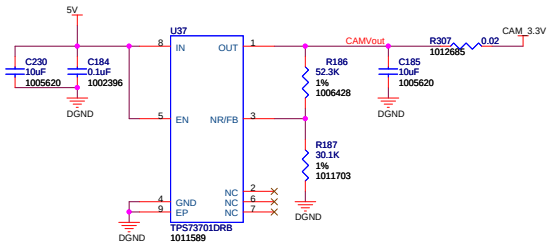
IO VOLTAGE COMPARATOR

compare IO volatge to 2.5V - use this to select IO power supply

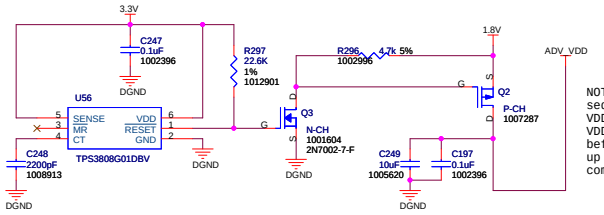


IO VOLTAGE SWITCH

CAMERA IO SUPPLY



ADV7343 POWER SEQUENCING



NOTE: The ADV7343 requires power sequencing between it's VDD and VDDIO(3.3V) power supplies. If VDDIO doesn't come up 250uS+ before VDD, the device may power up in SPI mode, and may not communicate over I2C.

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16 - CHANGE LOG

Revision Control for Project Phase Beta		
Rev	**Description**	**Date**
0.1	Copied from first beta schematic(1013703).	08-10-09
1	SH:8 Net on U15.12 had 2 names: CHAR_LCD_ENABLEn and CHAR_LCD_ENn. The net kept the name CHAR_LCD_ENn, which caused U15.12 to be shorted to U15.15, because both nets had the same name. This change will ensure the nets have different names.	08-11-09

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