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DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

3) DESIGN NOTES in red are critical, and must be understood and followed.

IMPORTANT NOTICE:

IMPORTANT NOTICE:

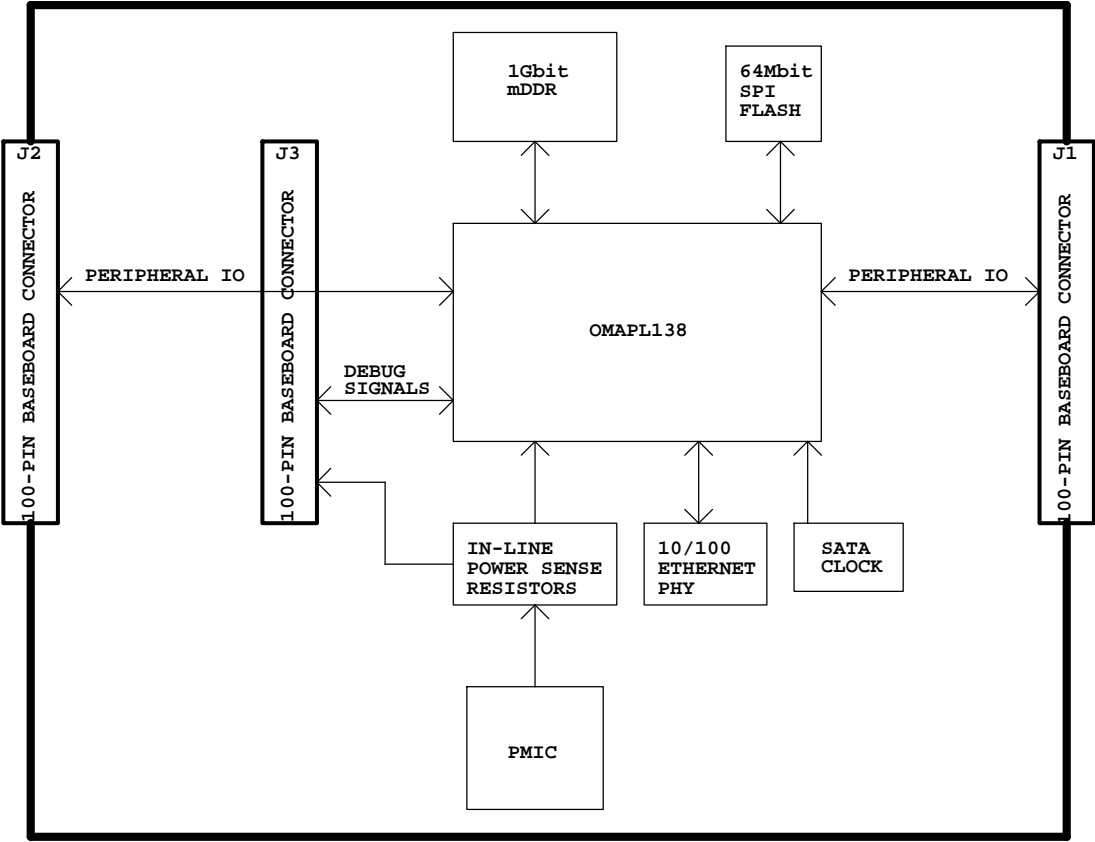
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SYSTEM BLOCK DIAGRAM

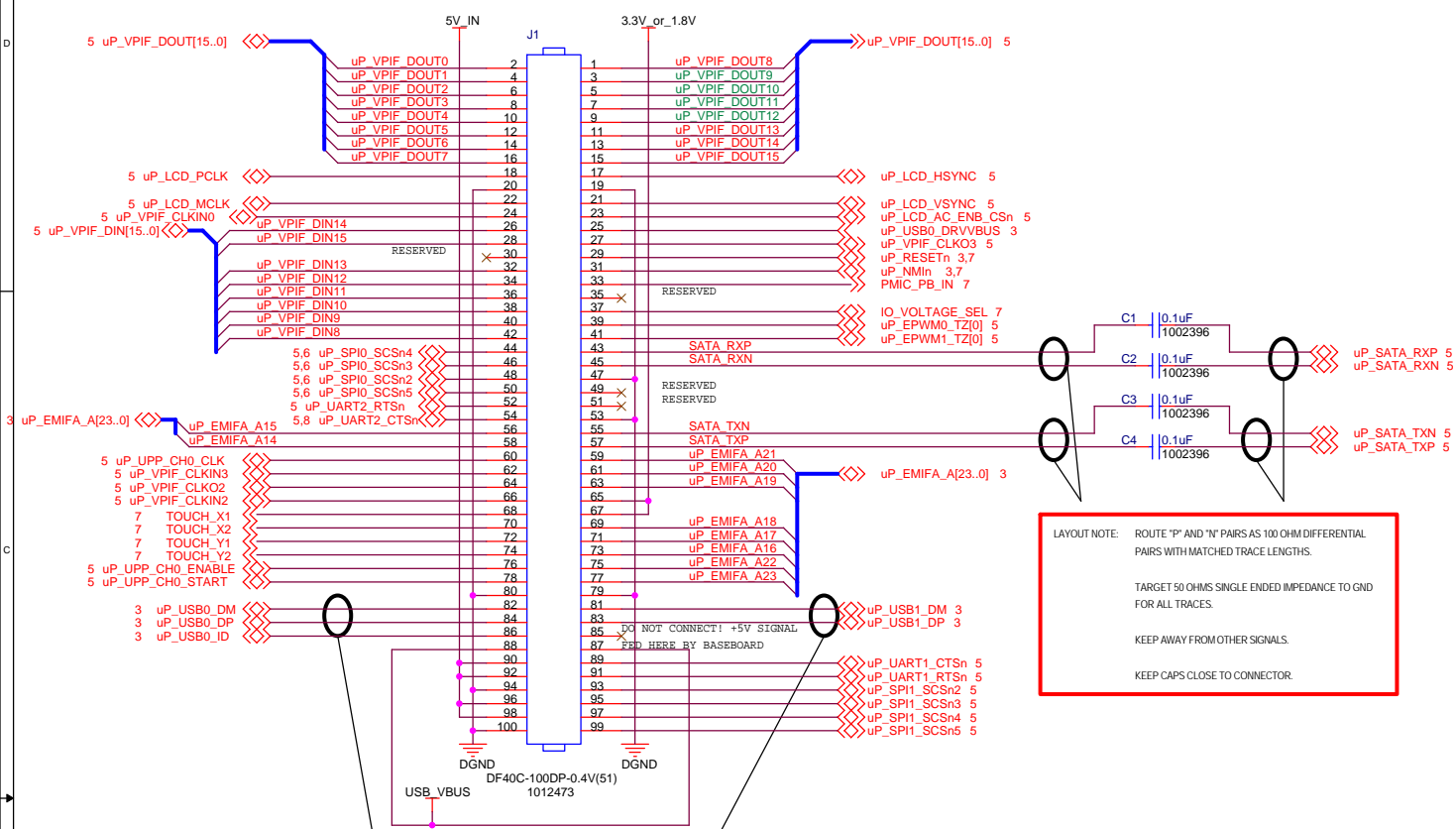


I2C ADDRESSING

FUNCTION	DEVICE	ADDRESS	I2C BUS
PMIC	TPS65070	100 1000	PROC I2C0
5V IN	INA219	100 0000	PMDC I2C
PMIC 3.3V SW	INA219	100 0001	PMDC I2C
PMIC 1.8V/3.3V SW	INA219	100 0010	PMDC I2C
PMIC 1.2V SW	INA219	100 0011	PMDC I2C
PMIC 1.2V LDO	INA219	100 0100	PMDC I2C
PMIC 1.8V LDO	INA219	100 0101	PMDC I2C
RTC 1.2V LDO	INA219	100 0110	PMDC I2C

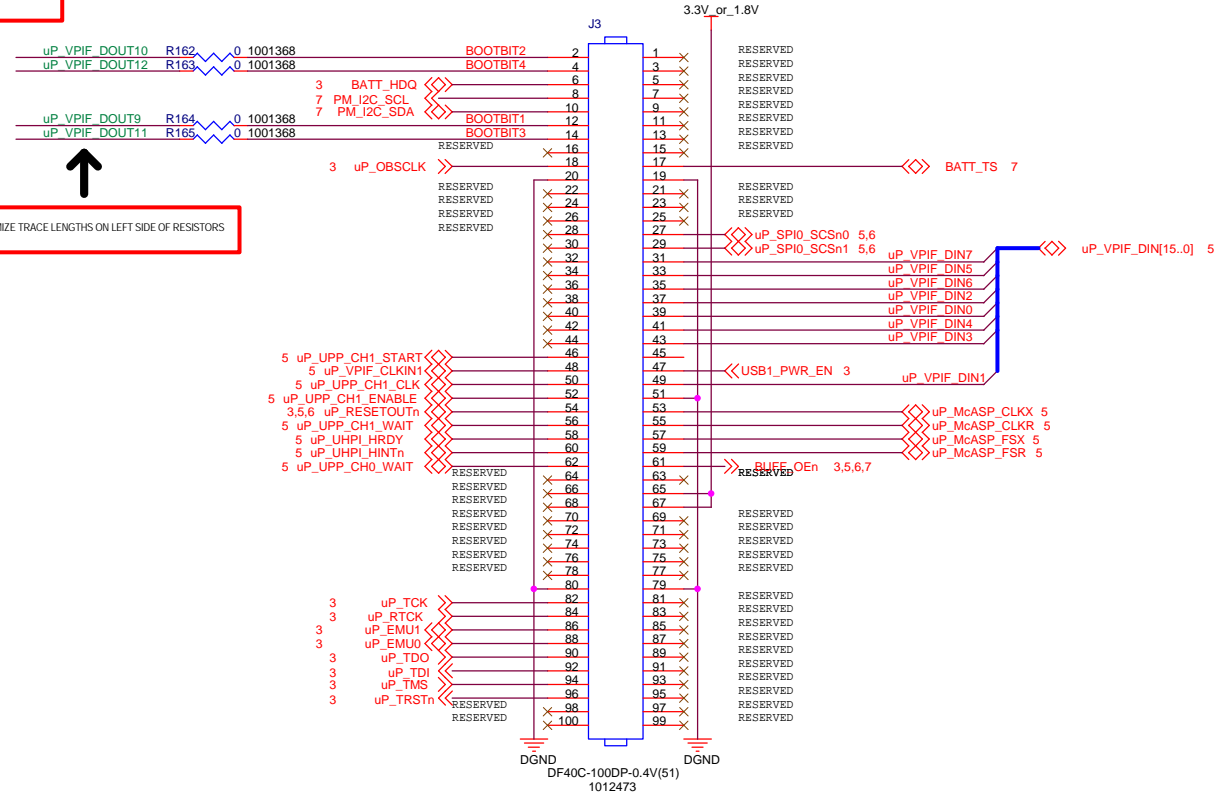
02 - BASEBOARD CONNECTORS

PERIPHERAL IO



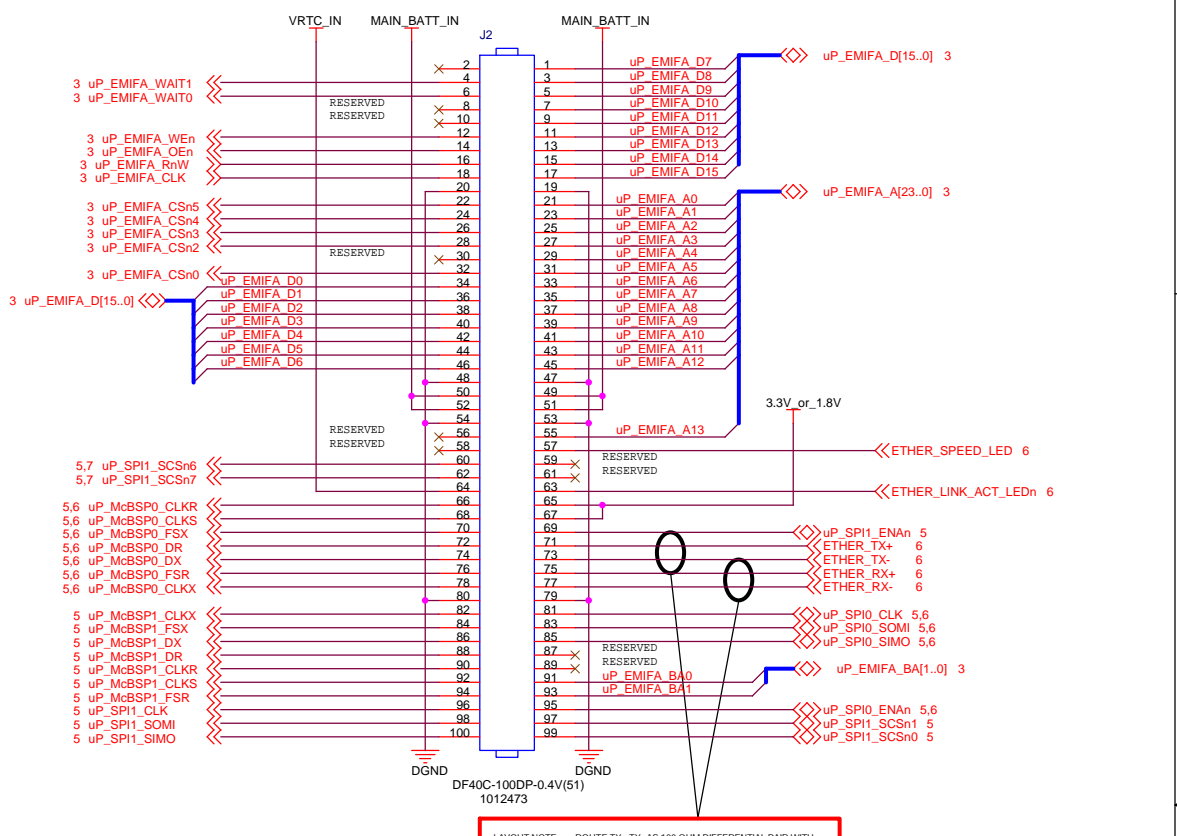
LAYOUT NOTE: ROUTE "P" AND "N" PAIRS AS 100 OHM DIFFERENTIAL PAIRS WITH MATCHED TRACE LENGTHS.
TARGET 50 OHMS SINGLE ENDED IMPEDANCE TO GND FOR ALL TRACES.
KEEP AWAY FROM OTHER SIGNALS.
KEEP CAPS CLOSE TO CONNECTOR.

DEBUG IO




LAYOUT NOTE: MINIMIZE TRACE LENGTHS ON LEFT SIDE OF RESISTORS

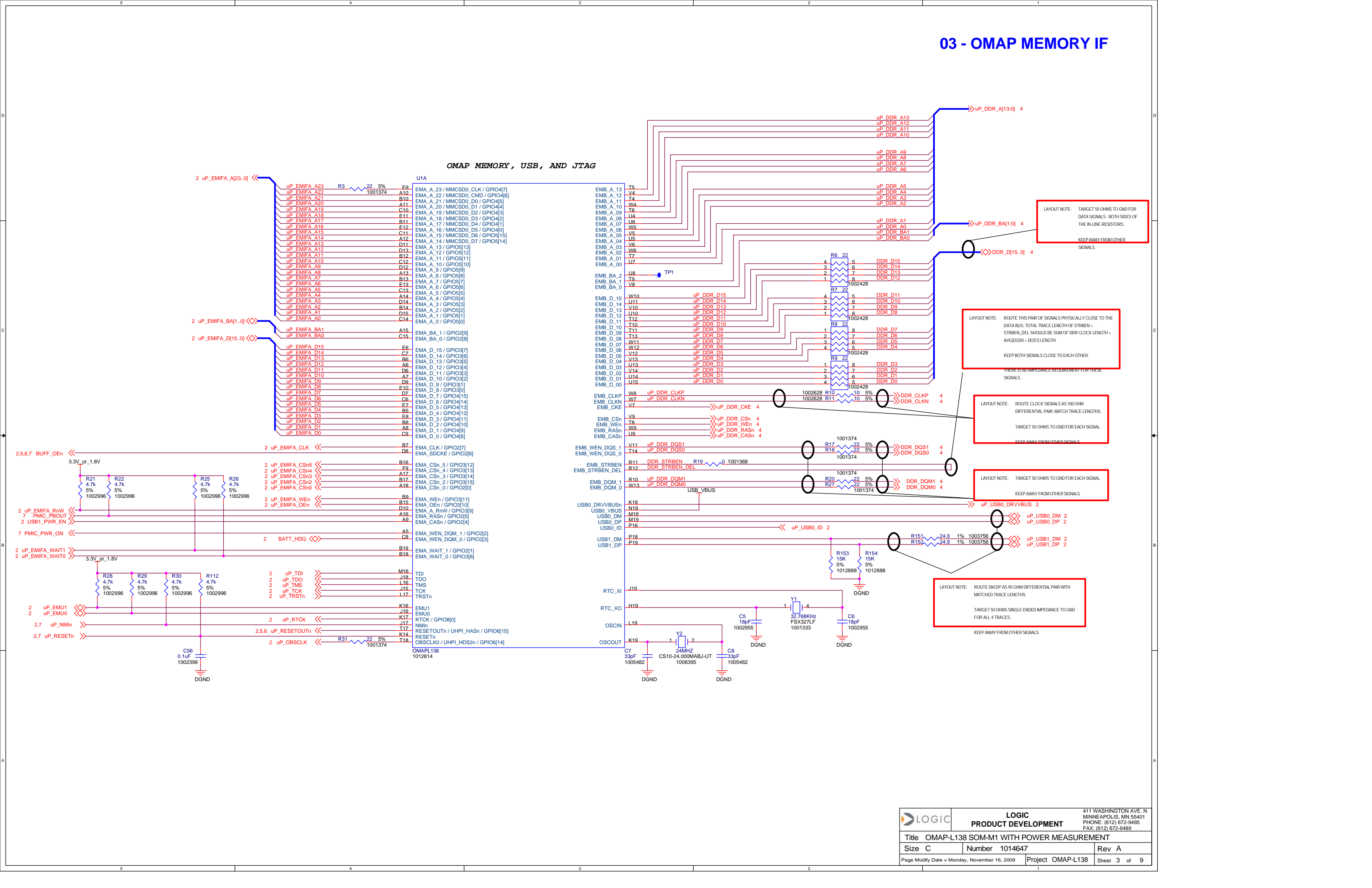
PERIPHERAL IO



LAYOUT NOTE: ROUTE TX+,TX- AS 100 OHM DIFFERENTIAL PAIR WITH MATCHED TRACE LENGTHS.
ROUTE RX+,RX- AS 100 OHM DIFFERENTIAL PAIR WITH MATCHED TRACE LENGTHS.
TARGET 50 OHMS SINGLE ENDED IMPEDANCE TO GND FOR ALL 4 TRACES.
KEEP AWAY FROM OTHER SIGNALS.

	LOGIC PRODUCT DEVELOPMENT		411 WASHINGTON AVE. N MINNEAPOLIS, MN 55401 PHONE: (612) 672-9495 FAX: (612) 672-9489	
Title OMAP-L138 SOM-M1 WITH POWER MEASUREMENT				
Size C		Number 1014647		Rev A
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03 - OMAP MEMORY IF



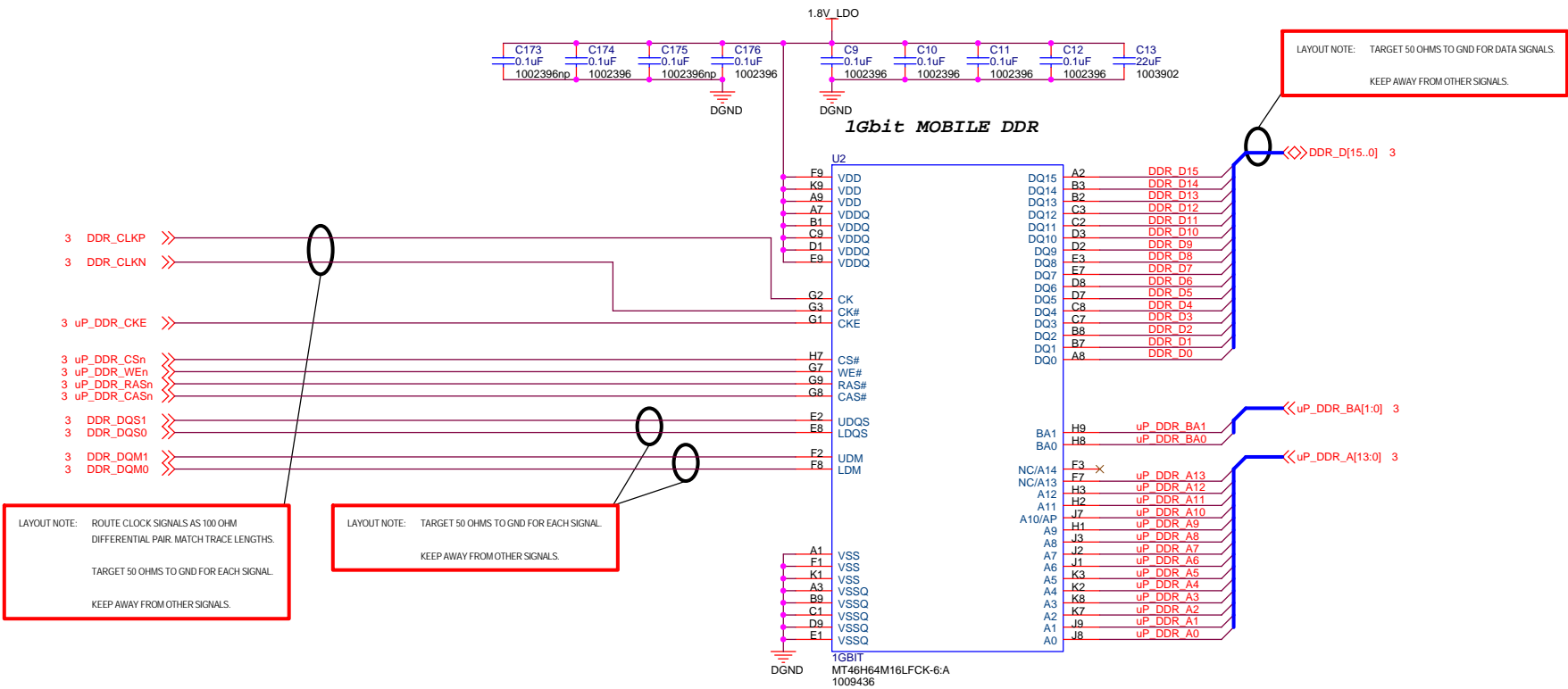
LAYOUT NOTE: TARGET 50 OHMS TO GND FOR DATA SIGNALS - BOTH SIDES OF THE IN-LINE RESISTORS.
KEEP AWAY FROM OTHER SIGNALS.

LAYOUT NOTE: ROUTE THIS PAIR OF SIGNALS PHYSICALLY CLOSE TO THE DATA BUS. TOTAL TRACE LENGTH OF STRBEN + STRBEN_DEL SHOULD BE SUM OF DDR CLOCK LENGTH + AVG(DQS0 + DQS1) LENGTH.
KEEP BOTH SIGNALS CLOSE TO EACH OTHER.

LAYOUT NOTE: ROUTE CLOCK SIGNALS AS 100 OHM DIFFERENTIAL PAIR. MATCH TRACE LENGTHS.
TARGET 50 OHMS TO GND FOR EACH SIGNAL.
KEEP AWAY FROM OTHER SIGNALS.

LAYOUT NOTE: TARGET 50 OHMS TO GND FOR EACH SIGNAL.
KEEP AWAY FROM OTHER SIGNALS.

LAYOUT NOTE: ROUTE DM,DP AS 90 OHM DIFFERENTIAL PAIR WITH MATCHED TRACE LENGTHS.
TARGET 50 OHMS SINGLE ENDED IMPEDANCE TO GND FOR ALL 4 TRACES.
KEEP AWAY FROM OTHER SIGNALS.

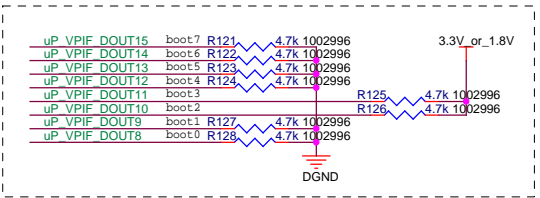


05 - OMAP PERIPHERAL IF

OMAP MUXED PERIPHERAL INTERFACES



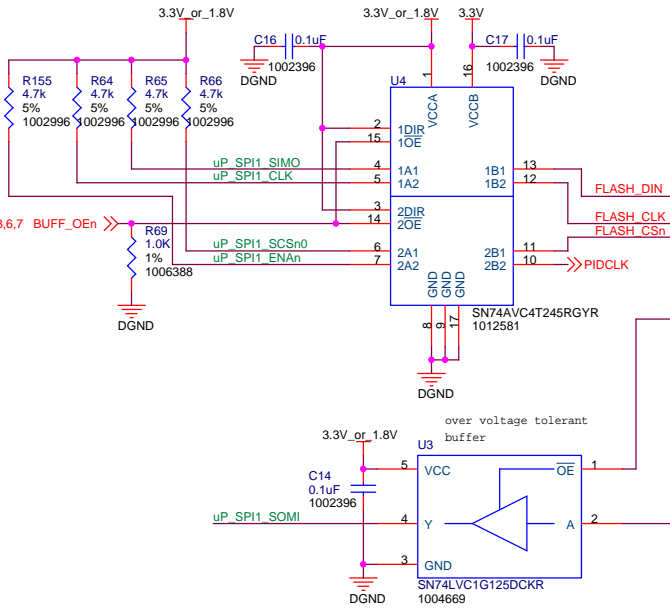
BOOTSTRAPS: DEFAULT IS SPI1



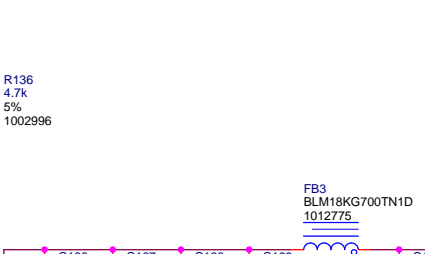
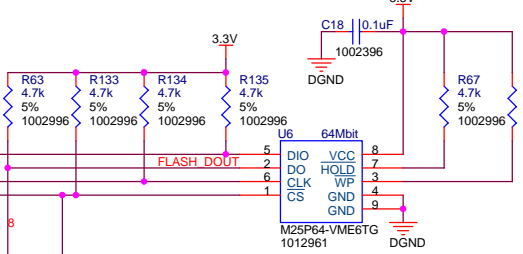
BOOT DEVICE OPTIONS

BOOT DEVICE	BOOT BITS[4:1]
NOR EMIFA	0001
NAND-8 EMIFA	0111
SPI0 FLASH	0101
SPI1 FLASH(default)	0110
UART0	1011
EMULATOR DEBUG	1111

VOLTAGE TRANSLATION



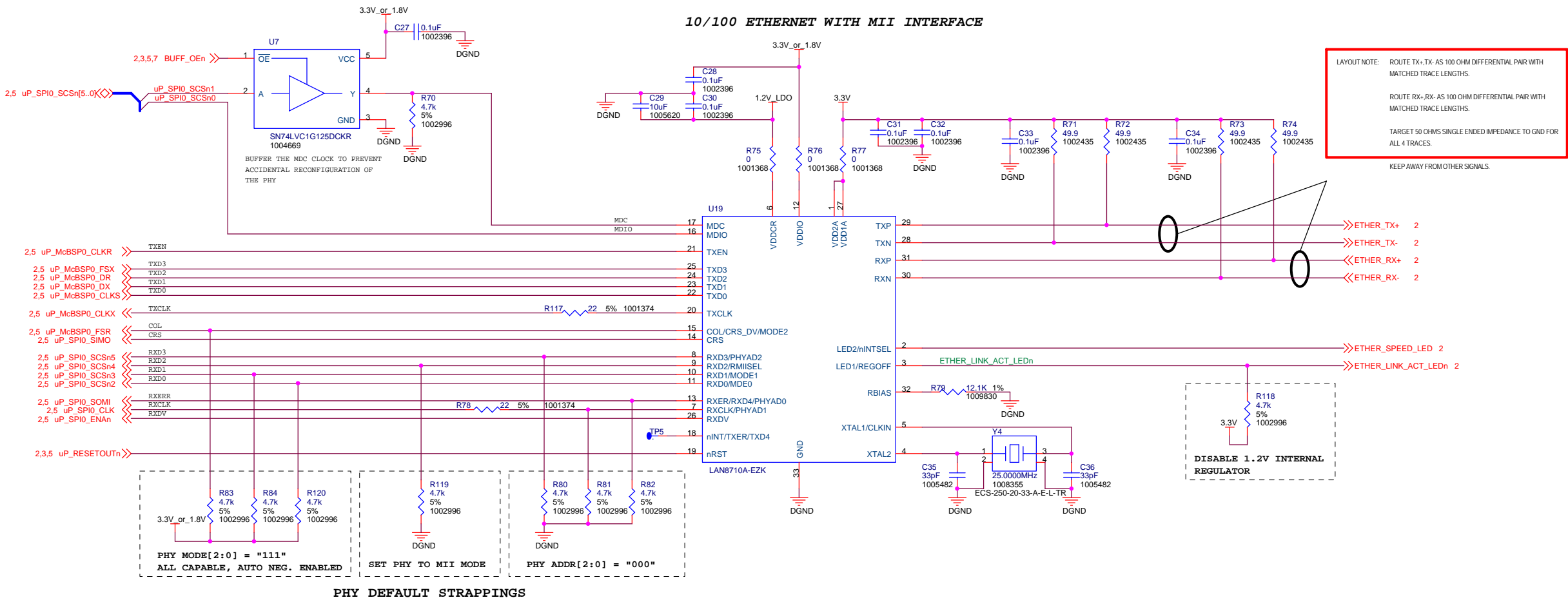
64Mbit BOOT FLASH



OSCILLATOR SETTINGS:

INPUT CRYSTAL: 25MHZ
PRESALER DIVIDER: 3
FEEDBACK DIVIDER: 24
OUTPUT DIVIDER: 6
OUTPUT FREQUENCY: 100MHZ
OUTPUT TYPE: LVDS

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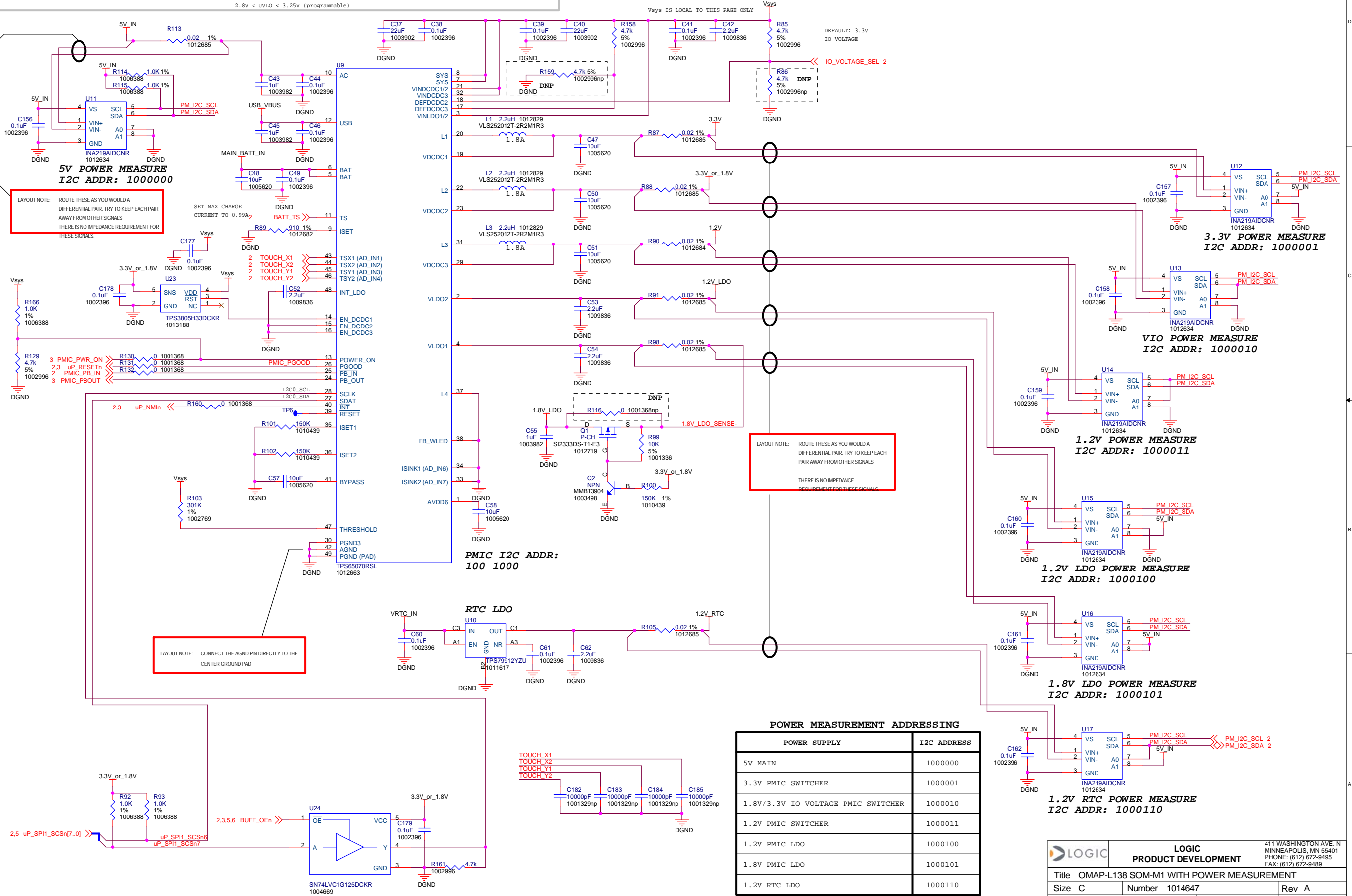
PHY MODE CONFIGURATION TABLE

MODE[2:0]	MODE DEFINITION
000	10BASE-T HALF DUPLEX. AUTO-NEGOTIATION DISABLED.
001	10BASE-T FULL DUPLEX. AUTO-NEGOTIATION DISABLED.
010	100BASE-TX HALF DUPLEX. AUTO-NEGOTIATION DISABLED. CRS IS ACTIVE DURING TRANSMIT & RECEIVE.
011	100BASE-TX FULL DUPLEX. AUTO-NEGOTIATION DISABLED.CRS IS ACTIVE DURING RECEIVE.
100	100BASE-TX HALF DUPLEX IS ADVERTISED. AUTONEGOTIATION ENABLED.CRS IS ACTIVE DURING TRANSMIT & RECEIVE.
101	REPEATER MODE. AUTO-NEGOTIATION ENABLED.100BASE-TX HALF DUPLEX IS ADVERTISED.CRS IS ACTIVE DURING RECEIVE.
110	POWER DOWN MODE.
111	ALL CAPABLE. AUTO-NEGOTIATION ENABLED.

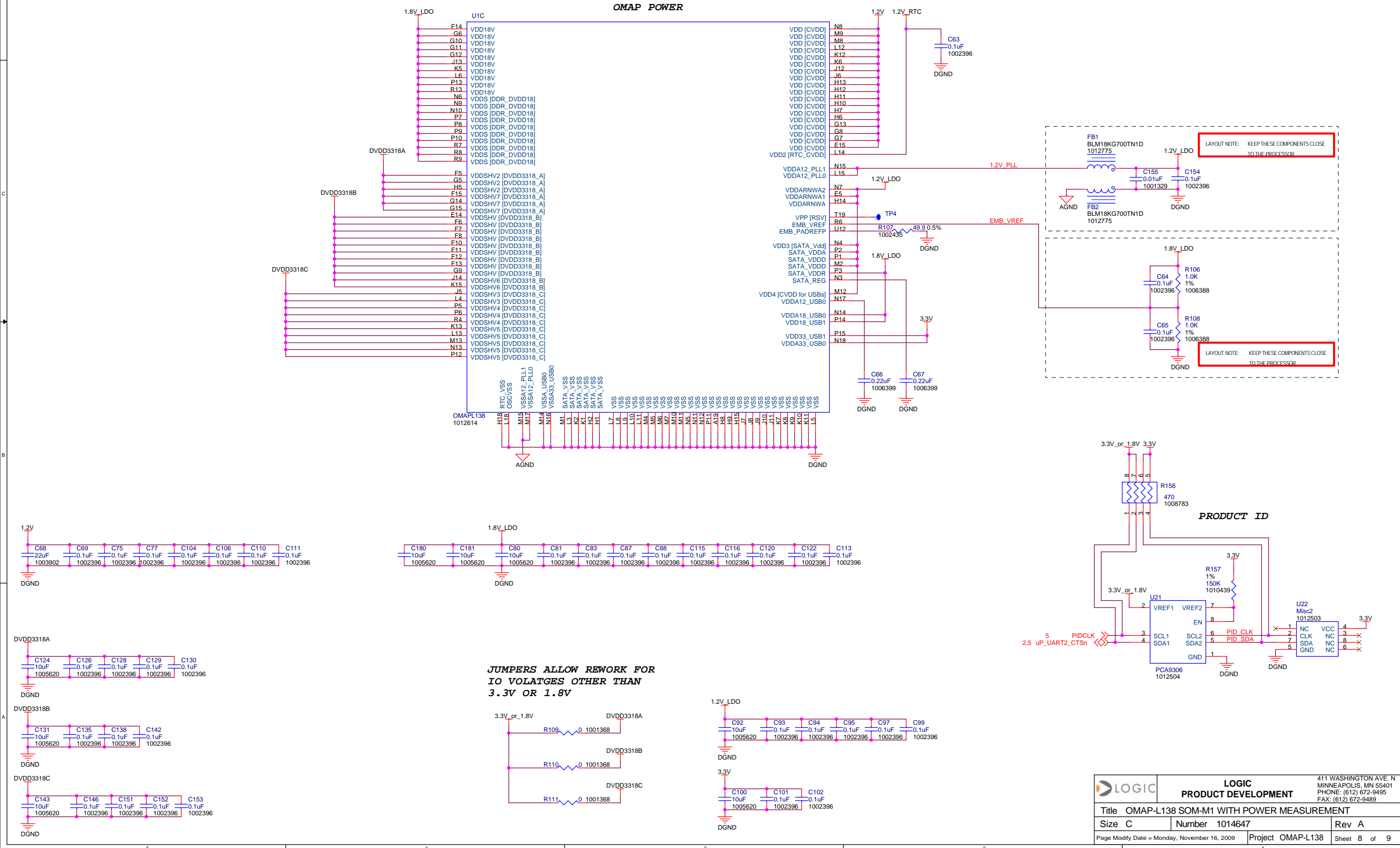
07 - PMIC

Applying power to 5V_IN will cause SOM to power up immediately.
For startup, 5V_IN range is:
3.6V < 5V_IN < 5.8V
At runtime, 5V_IN range is:
UVLO < 5V_IN < 5.8V
UVLO = UnderVoltage LockOut
UVLO = 3.0V (default)
2.8V < UVLO < 3.25V (programmable)

Applying power to MAIN_BATT_IN will NOT cause SOM to power up immediately.
SOM will power up when power is supplied to MAIN_BATT_IN, and then PMIC_PB_IN is pulsed low.
PMIC_PB_IN must be pulsed low AFTER power is applied to MAIN_BATT_IN.
For startup, MAIN_BATT_IN range is:
3.6V < MAIN_BATT_IN < 4.2V
At runtime, MAIN_BATT_IN range is:
UVLO < MAIN_BATT_IN < 4.2V
UVLO = UnderVoltage LockOut
UVLO = 3.0V (default)
2.8V < UVLO < 3.25V (programmable)



08 - OMAP POWER



Revision Control				
ECO Number	Phase	Rev	Description	Date
	beta	0.1	STARTED FROM BETA OMAP-L138 SOM SCHEMATIC	06-23-09
		1	increase rev to 1 for release to Agile	07-08-09
		2	SH: 5,7: changed all 6 I2C pullups(R51,R52,R92,R93,R114,R115) to 1K from 4.7K. 4.7K on I2C0 was too weak and caused I2C0 bus failures during preliminary beta testing. I2C1 and PM_I2C pullups were changed so they're the same as I2C0. SH: various: changed style of all layout notes so the text will always be visible. An Orcad quirk causes the solid red boxes to cover the text inside them.	07-30-09
C06619		3	SH: 7: Changed R166 to 1K from 4.7K. 4.7K pull-up on PMIC POWER_ON was not always strong enough to pull POWER_ON above 1.2V (Vih).	07-31-09
C07034	beta2	A	SH: 5: Changed U3.1 to connect to net FLASH_CSn SH: 7: Added C182-C185	11-16-09