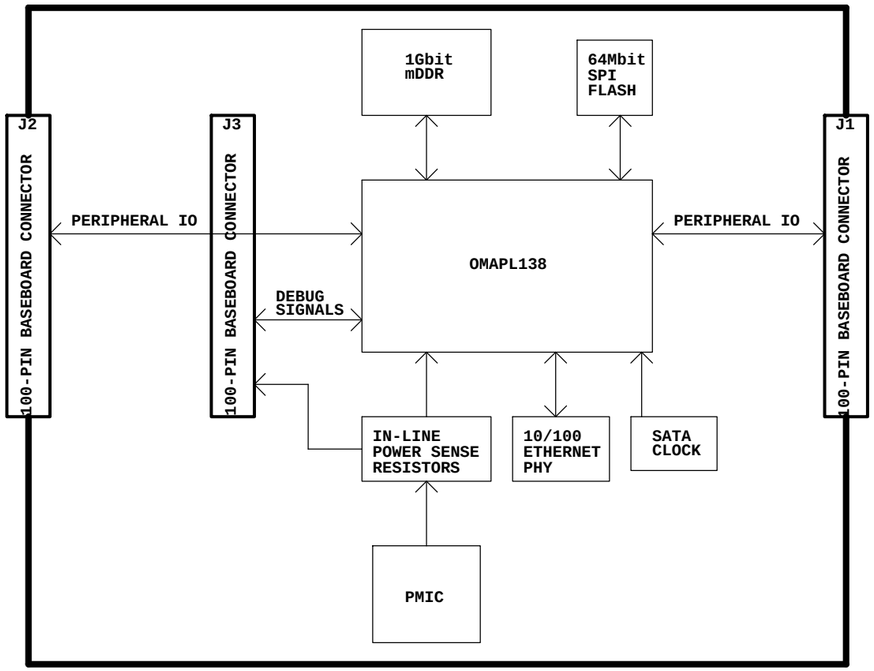
SYSTEM BLOCK DIAGRAM



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8	OMAP POWER
9	CHANGE LOG

IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

3) DESIGN NOTES in red are critical, and must be understood and followed.

I2C ADDRESSING

FUNCTION	DEVICE	ADDRESS	I2C BUS
PMIC	TPS65070	100 1000	PROC I2C0
5V IN	INA219	100 0000	PMDC I2C
PMIC 3.3V SW	INA219	100 0001	PMDC I2C
PMIC 1.8V/3.3V SW	INA219	100 0010	PMDC I2C
PMIC 1.2V SW	INA219	100 0011	PMDC I2C
PMIC 1.2V LDO	INA219	100 0100	PMDC I2C
PMIC 1.8V LDO	INA219	100 0101	PMDC I2C
RTC 1.2V LDO	INA219	100 0110	PMDC I2C

IMPORTANT NOTICE:

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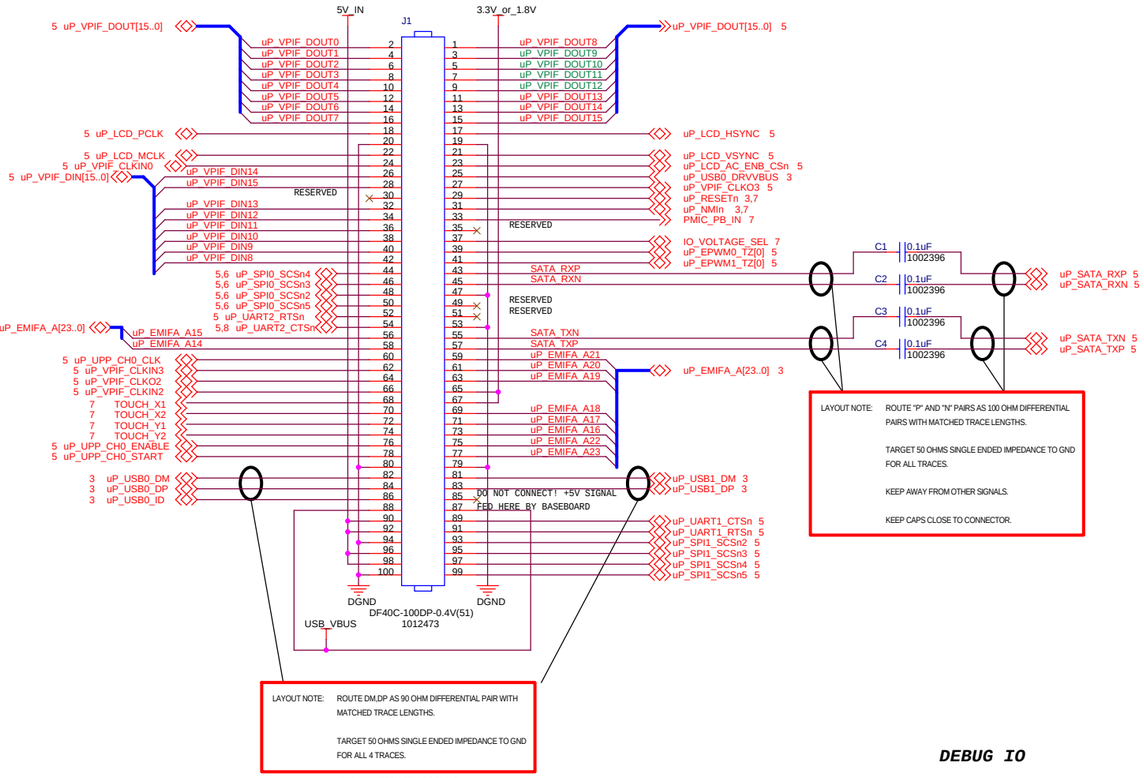
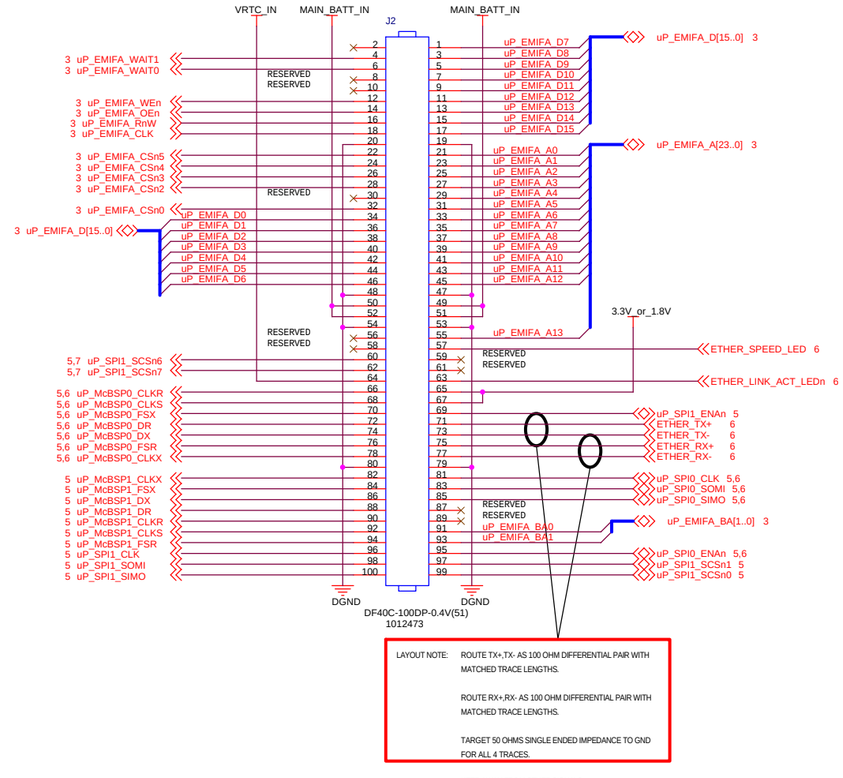
02 - BASEBOARD CONNECTORS

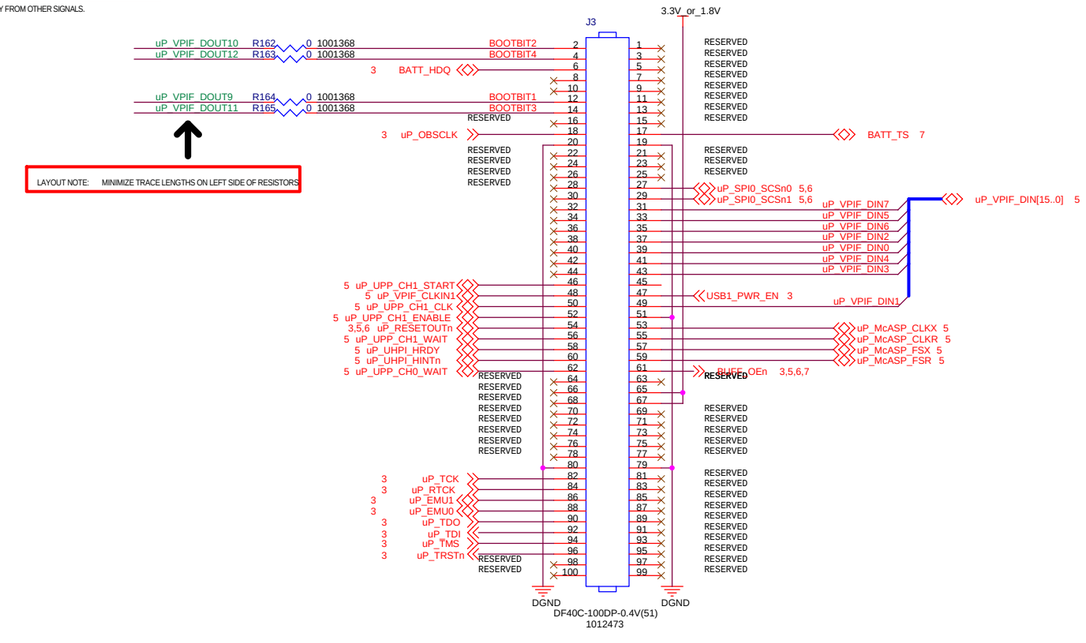
PERIPHERAL IO



PERIPHERAL IO



DEBUG IO



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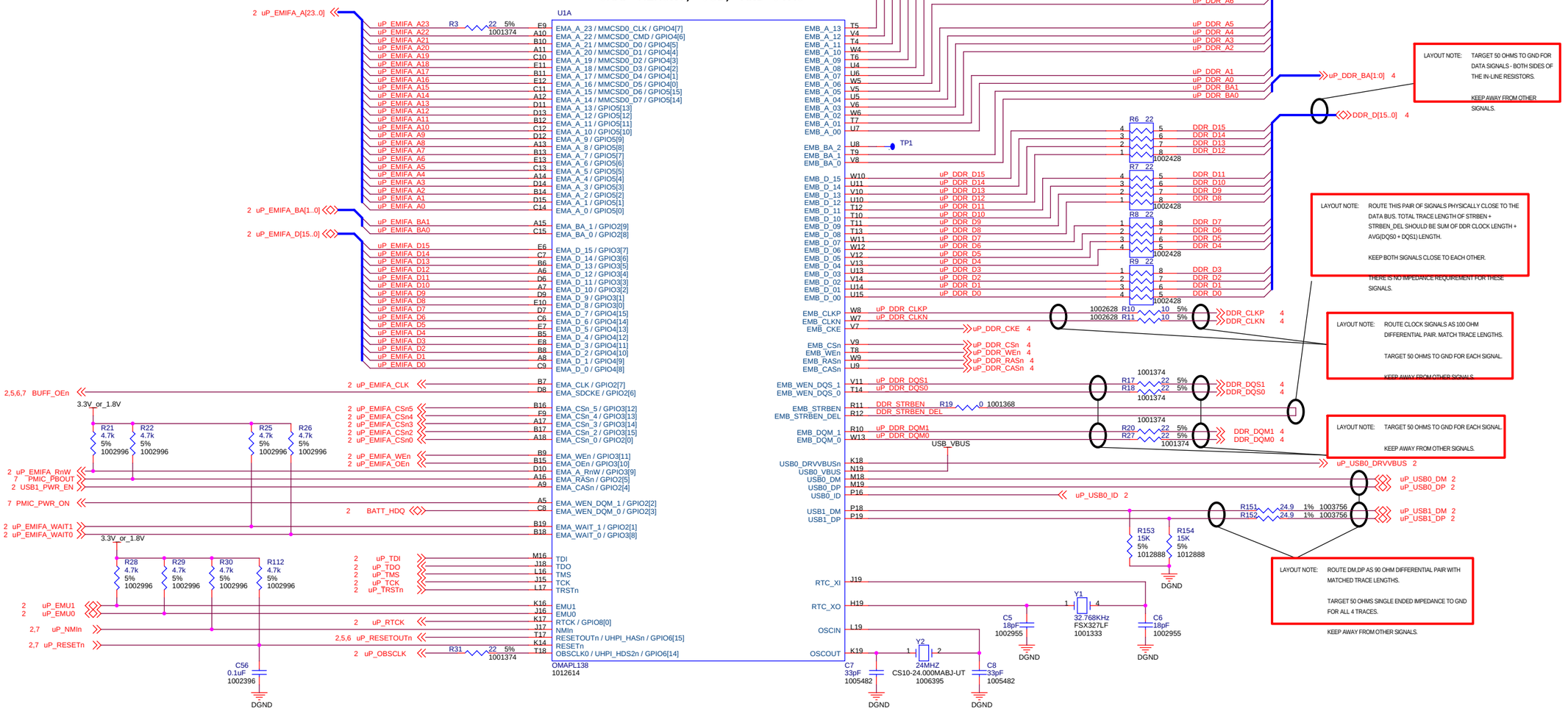
03 - OMAP MEMORY IF

OMAP MEMORY, USB, AND JTAG



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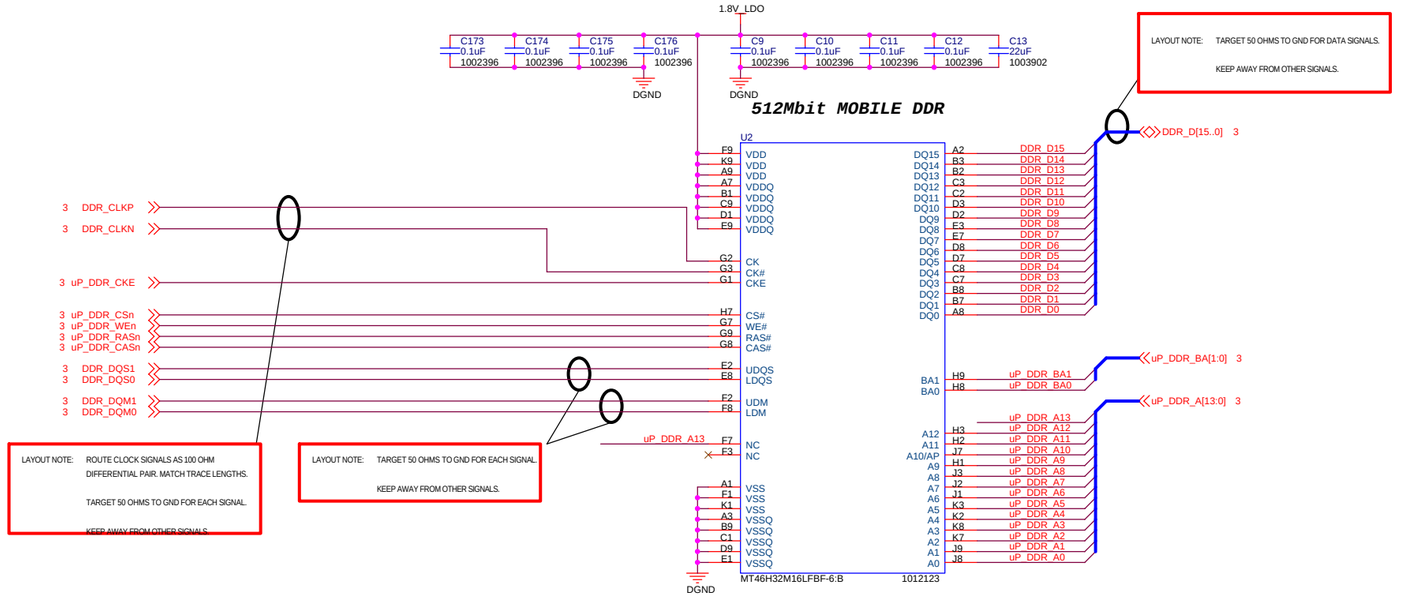
04 - DDR



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05 - OMAP PERIPHERAL IF

OMAP MUXED PERIPHERAL INTERFACES

U1B

OMAPL138
1012614

BOOTSTRAPS: DEFAULT IS SPI1

3.3V_or_1.8V

uP_VPIF_DOUT15	boot7 R121	4.7k 1002996	
uP_VPIF_DOUT14	boot6 R122	4.7k 1002996	
uP_VPIF_DOUT13	boot5 R123	4.7k 1002996	
uP_VPIF_DOUT12	boot4 R124	4.7k 1002996	
uP_VPIF_DOUT11	boot3	R125 4.7k 1002996	
uP_VPIF_DOUT10	boot2	R126 4.7k 1002996	
uP_VPIF_DOUT9	boot1 R127	4.7k 1002996	
uP_VPIF_DOUT8	boot0 R128	4.7k 1002996	

DGND

BOOT DEVICE OPTIONS

BOOT DEVICE	BOOT BITS[4:1]
NOR EMIFA	0001
NAND-8 EMIFA	0111
SPI0 FLASH	0101
SPI1 FLASH(default)	0110
UART0	1011
EMULATOR DEBUG	1111

VOLTAGE TRANSLATION

SN74AVC4T245RGYR
1012581

over voltage tolerant buffer

SN74LVC1G125DCKR
1004669

64Mbit BOOT FLASH

M25P64-VME6TG
1012961

FB3
BLM18KG700TN1D
1012775

LVDS 100MHZ CLOCK GENERATOR

CDCM61001RHBT
1012876

LAYOUT NOTE: ROUTE "P" AND "N" PAIRS AS 100 OHM DIFFERENTIAL PAIRS WITH MATCHED TRACE LENGTHS.

TARGET 50 OHMS SINGLE ENDED IMPEDANCE TO GND FOR ALL TRACES.

KEEP AWAY FROM OTHER SIGNALS.

LAYOUT NOTE: KEEP IN-LINE CAPS CLOSE TO U20

LAYOUT NOTE: KEEP RESISTOR CLOSE TO PROCESSOR

OSCILLATOR SETTINGS:

INPUT CRYSTAL: 25MHZ

PRESCALER DIVIDER: 3

FEEDBACK DIVIDER: 24

OUTPUT DIVIDER: 6

OUTPUT FREQUENCY: 100MHZ

OUTPUT TYPE: LVDS

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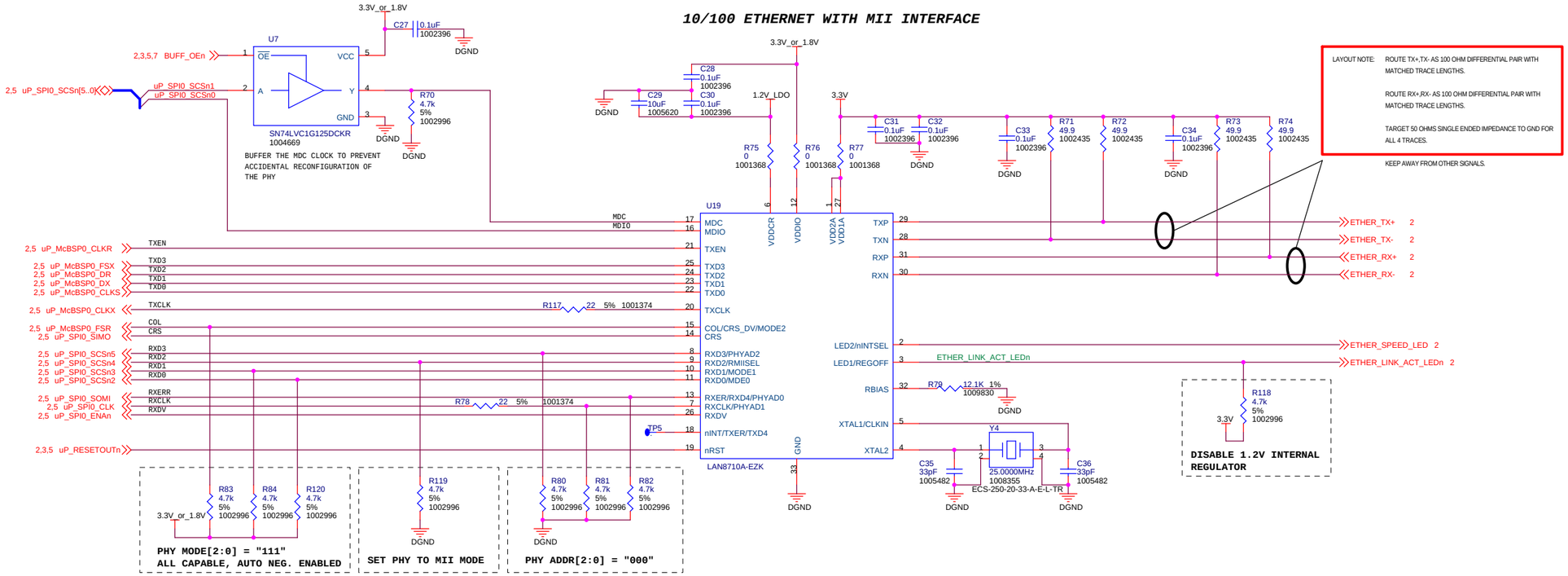
06 - ETHERNET PHY

10/100 ETHERNET WITH MII INTERFACE



PHY DEFAULT STRAPPINGS

PHY MODE CONFIGURATION TABLE

MODE[2:0]	MODE DEFINITION
000	10BASE-T HALF DUPLEX. AUTO-NEGOTIATION DISABLED.
001	10BASE-T FULL DUPLEX. AUTO-NEGOTIATION DISABLED.
010	100BASE-TX HALF DUPLEX. AUTO-NEGOTIATION DISABLED. CRS IS ACTIVE DURING TRANSMIT & RECEIVE.
011	100BASE-TX FULL DUPLEX. AUTO-NEGOTIATION DISABLED.CRS IS ACTIVE DURING RECEIVE.
100	100BASE-TX HALF DUPLEX IS ADVERTISED. AUTONEGOTIATION ENABLED.CRS IS ACTIVE DURING TRANSMIT & RECEIVE.
101	REPEATER MODE. AUTO-NEGOTIATION ENABLED.100BASE-TX HALF DUPLEX IS ADVERTISED.CRS IS ACTIVE DURING RECEIVE.
110	POWER DOWN MODE.
111	ALL CAPABLE. AUTO-NEGOTIATION ENABLED.

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07 - PMIC

Applying power to 5V_IN will cause SOM to power up immediately.

For startup, 5V_IN range is:
3.6V < 5V_IN < 5.8V

At runtime, 5V_IN range is:
UVLO < 5V_IN < 5.8V

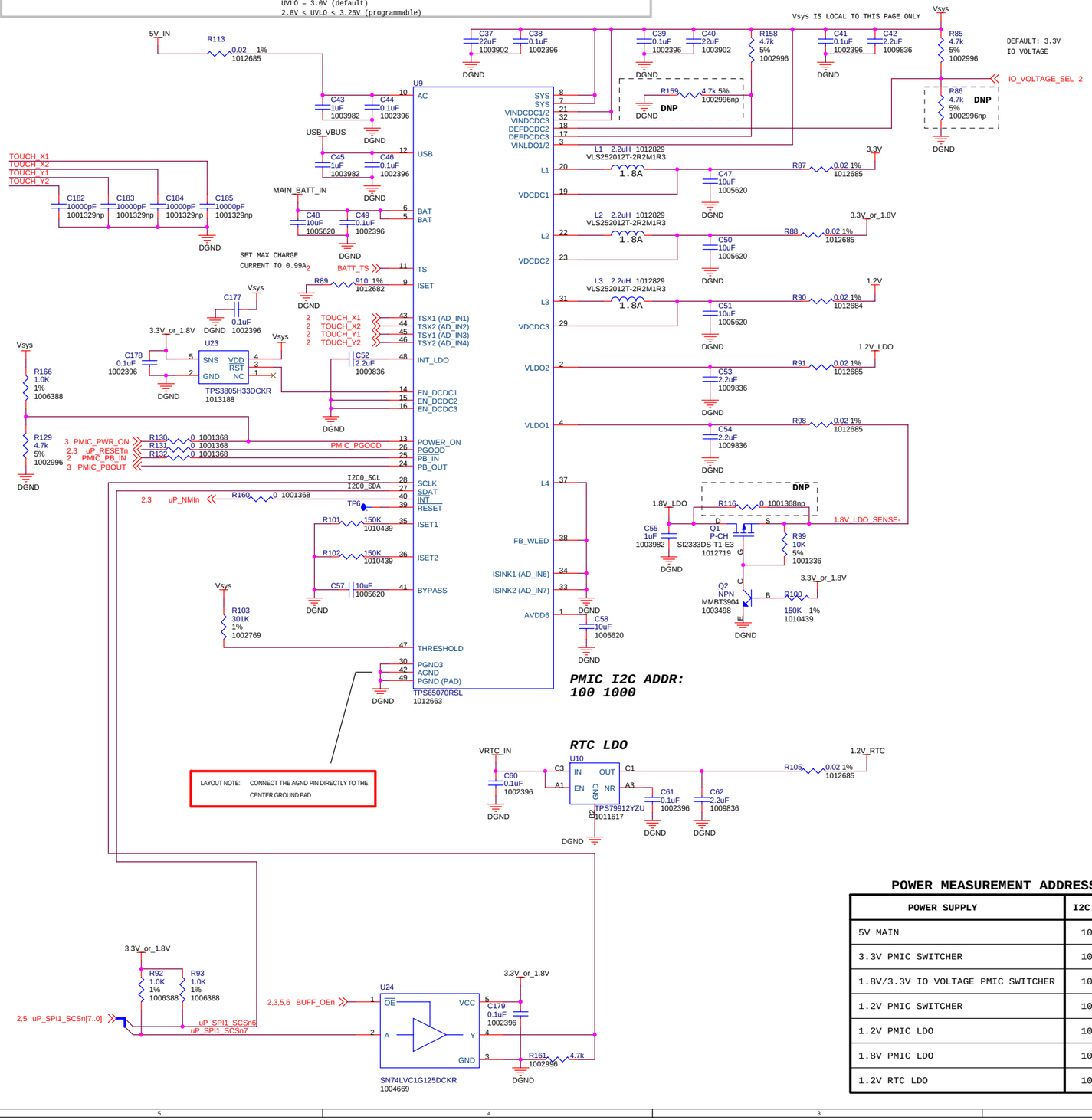
UVLO = UnderVoltage LockOut
UVLO = 3.0V (default)
2.8V < UVLO < 3.25V (programmable)

Applying power to MAIN_BATT_IN will NOT cause SOM to power up immediately.
SOM will power up when power is supplied to MAIN_BATT_IN, and then PMIC_PB_IN is pulsed low.
PMIC_PB_IN must be pulsed low AFTER power is applied to MAIN_BATT_IN.

For startup, MAIN_BATT_IN range is:
3.6V < MAIN_BATT_IN < 4.2V

At runtime, MAIN_BATT_IN range is:
UVLO < MAIN_BATT_IN < 4.2V

UVLO = UnderVoltage LockOut
UVLO = 3.0V (default)
2.8V < UVLO < 3.25V (programmable)



POWER MEASUREMENT ADDRESSING

POWER SUPPLY	I2C ADDRESS
5V MAIN	1000000
3.3V PMIC SWITCHER	1000001
1.8V/3.3V IO VOLTAGE PMIC SWITCHER	1000010
1.2V PMIC SWITCHER	1000011
1.2V PMIC LDO	1000100
1.8V PMIC LDO	1000101
1.2V RTC LDO	1000110

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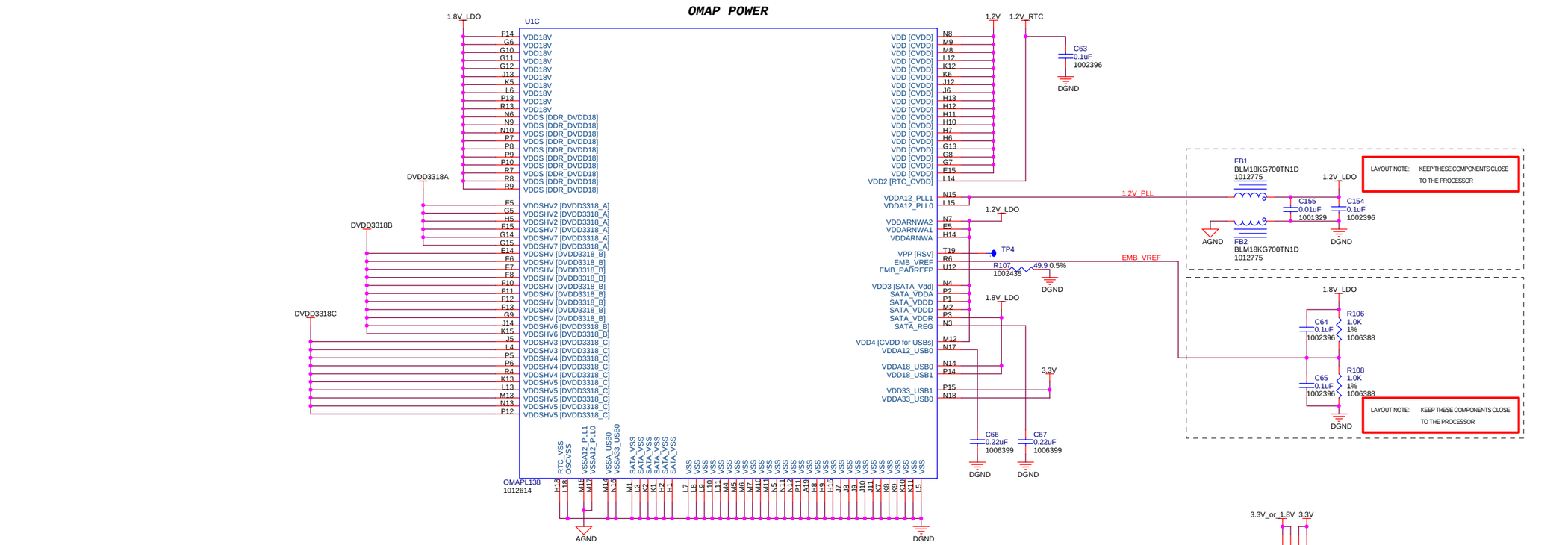
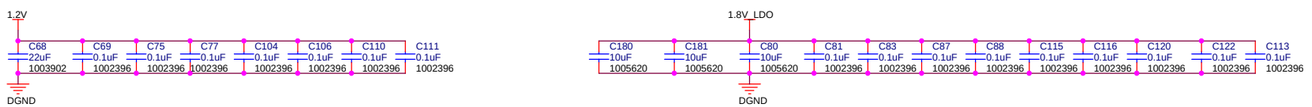
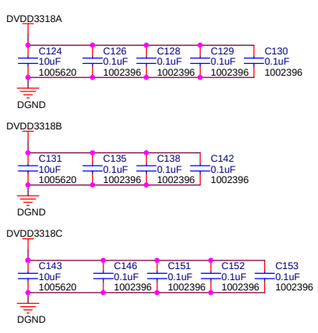
08 - OMAP POWER

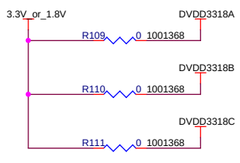
OMAP POWER

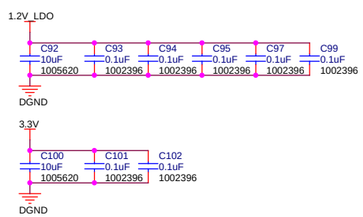


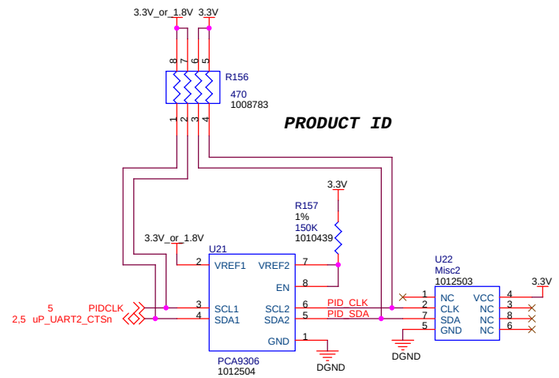




JUMPERS ALLOW REWORK FOR IO VOLATGES OTHER THAN 3.3V OR 1.8V







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Revision Control

ECO Number	Phase	Rev	Description	Date
	beta	0.1	STARTED FROM ALPHA SCHEMATIC SH:1: Corrected PMIC I2C address in table. Also corrected all I2C addresses to be 7 bits instead of 8. Removed socket and insulator plate symbols. Also changed PCB number. SH:2: Routed off-SOM boot bits to baseboard connector J3 on pins that are common with Shiva off-SOM boot pins. This provides commonality for testing. This shift also caused the testability pin BOFF_OEn to move to a different location on J3. SH:3,4: Removed in-line resistors on DDR address and control lines to ease DDR routing in layout. Removed one in-line resistor on STRBEN, STRBEN_DEL signals. Also changed layout note to indicate correct trace length for these signals. SH:4,8: Changed bulk cap on DDR to 22uF. Changed C80 on 1.8V_LDO to 10uF and added 2 more 10uF bulk caps to that rail. These changes were done to meet TI's DDR routing guidelines. SH:7: Added buffer to PMIC I2C clock signal to prevent accidental access to PMIC. Added TPS3805 for proper power sequencing. Added pullup to VSYS on PMIC DEFDCDC3 pin to generate proper core voltage. Also added no-pop pulldown in case PMIC is improperly programmed again. Tied unused PMIC inputs: L4, FB_WLED, ISINK1, ISINK2 to GND. Changed ISETx resistors to 150K - were 0 ohm. Added zero ohm in-line resistor on NMI to make potential rework easier. Updated PMIC symbol so it has the corrected footprint with center pad offset SH:various: Where appropriate, changed pullups/pulldowns to 4.7K to be consistent. SH:2: Moved uP_SPI0_SCSn0 from J3<45> to J3<27> Moved uP_SPI0_SCSn1 from J3<47> to J3<29> Moved BUFF_OEn from J3<29> to J3<61> SH:3: Changed EMA_CASn / GPIO2[4] function from SW_RST to USB1_PWR_EN. Moved from J1<85> to J3<47> SH:7: Changed POWER_ON pull from pull-down to pull-up w/ divider to protect uP pin from overvoltage	05-15-09
		0.2	SH:3: vertically mirrored rpacks on DDR data to match layout SH:4: removed R41 - 100 ohm resistor across DDR clock signals SH:6,8: changed all 49.9 ohm resistors to 1/2% tolerance. R107 on sheet 8 must be 1/2%, so all 49.9 ohm resistors were changed to 1/2% for commonality. SH:7: removed C59,R104 from PMIC THRESHOLD PIN. THRESHOLD will be pulled up to Vsys, since RESETn output is not used. Changed R161 to be a pulldown. SH:various: changed look of comments and layout notes to match style called out on title page.	06-15-09
		0.3	SH: various: changed all testpoints to no-pop so the don't show up in Agile BOM	06-19-09
		0.4	SH: various: all LPD numbers are now visible	06-21-09
		1	increase rev to 1 for release to Agile	07-08-09
		2	SH: 5,7: changed all 4 I2C pullups(R51,R52,R92,R93) to 1K from 4.7K. 4.7K on I2C0 was too weak and caused I2C0 bus failures during preliminary beta testing. I2C1 pullups were changed so they're the same as I2C0. SH: various: changed style of all layout notes so the text will always be visible. An Orcad quirk causes the solid red boxes to cover the text inside them.	07-30-09
C06619		3	SH: 7: Changed R166 to 1K from 4.7K. 4.7K pull-up on PMIC POWER_ON was not always strong enough to pull POWER_ON above 1.2V (Vih).	07-31-09
C07034	beta2	A	SH: 5: Changed U3.1 to connect to net FLASH_CSn SH: 7: Added C182-C185	11-16-09

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