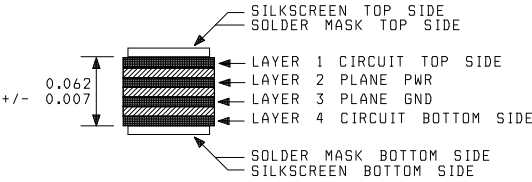


NOTE:

1. MATERIAL SELECTION:  
4 LAYER. EPOXY GLASS, NEMA GRADE FR-4, 0.062 +/- 0.007 THICK,  
1 1/2 OZ. FINAL COPPER EXTERNAL LAYERS, 1/2 OUNCE INTERNAL.  
SOLDERABLE SURFACES TO BE ImAg IMMERSION SILVER.
2. SOLDER RESIST: THE USE OF SOLDER RESIST COATING SHALL BE IN  
ACCORDANCE WITH THE REQUIREMENTS OF IPC-SM-840. ALL SOLDERABLE  
SURFACES ARE TO BE FREE OF SOLDER RESIST. COLOR - GREEN.  
USE LIQUID PHOTOIMAGEABLE RESIST.
3. SILKSCREEN: USE WHITE NON-CONDUCTIVE INK. ALL COMPONENT AND  
TESTPOINT LANDS ARE TO BE FREE OF INK.
4. MANUFACTURER'S IDENTIFICATION: ADD IN ETCH BOTTOM SIDE OR TO SILKSCREEN.
5. ELECTRICAL BARE BOARD TEST REQUIRED.
6. DRILL SIZES ARE FINISHED SIZE AFTER PLATING.
7. FABRICATE TO MEET EU RoHS DIRECTIVE.
8. BOARD SHALL MEET THE REQUIREMENTS OF UL796  
WITH A FLAMMABILITY RATING OF 94V-0.
9. BOARD TO BE IMPEDANCE CONTROLLED.  
50 OHM SINGLE ENDED CALCULATED WITH .012 INCH LINE ON LAYER 1 AND 4.  
100 OHM DIFFERENTIAL CALCULATED WITH .008 INCH TRACE/ .008 INCH SPACE ON LAYER 1.  
75 OHM COPLANAR IMPEDANCE CALCULATED WITH .006 INCH TRACE ON LAYER 4 WITH  
.006 INCH GAP. LAYER 3 TO 4 DIELECTRIC .0076 INCH
10. BOARD TO BE SCORED AT DESIGNATED LINE. SCORING TO BE 30 DEG  
AND A MINIMUM OF 0.020 INCHES BOARD MATERIAL IN CHANNEL.
11. BOARD VENDOR TO ADD TEAR SHAPING TO OUTER LAYERS.



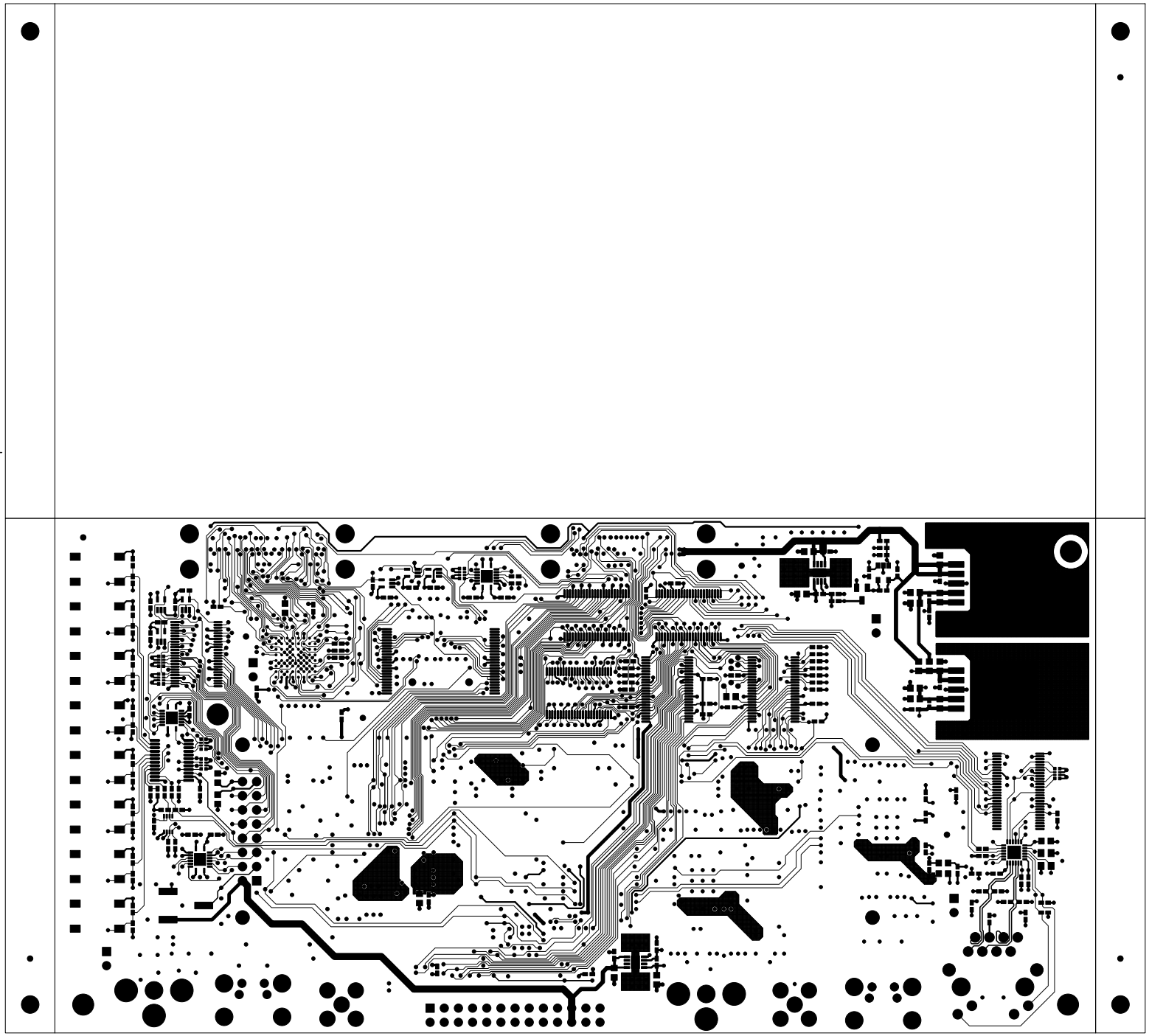
4 LAYER STACK-UP

REVISION CHANGES

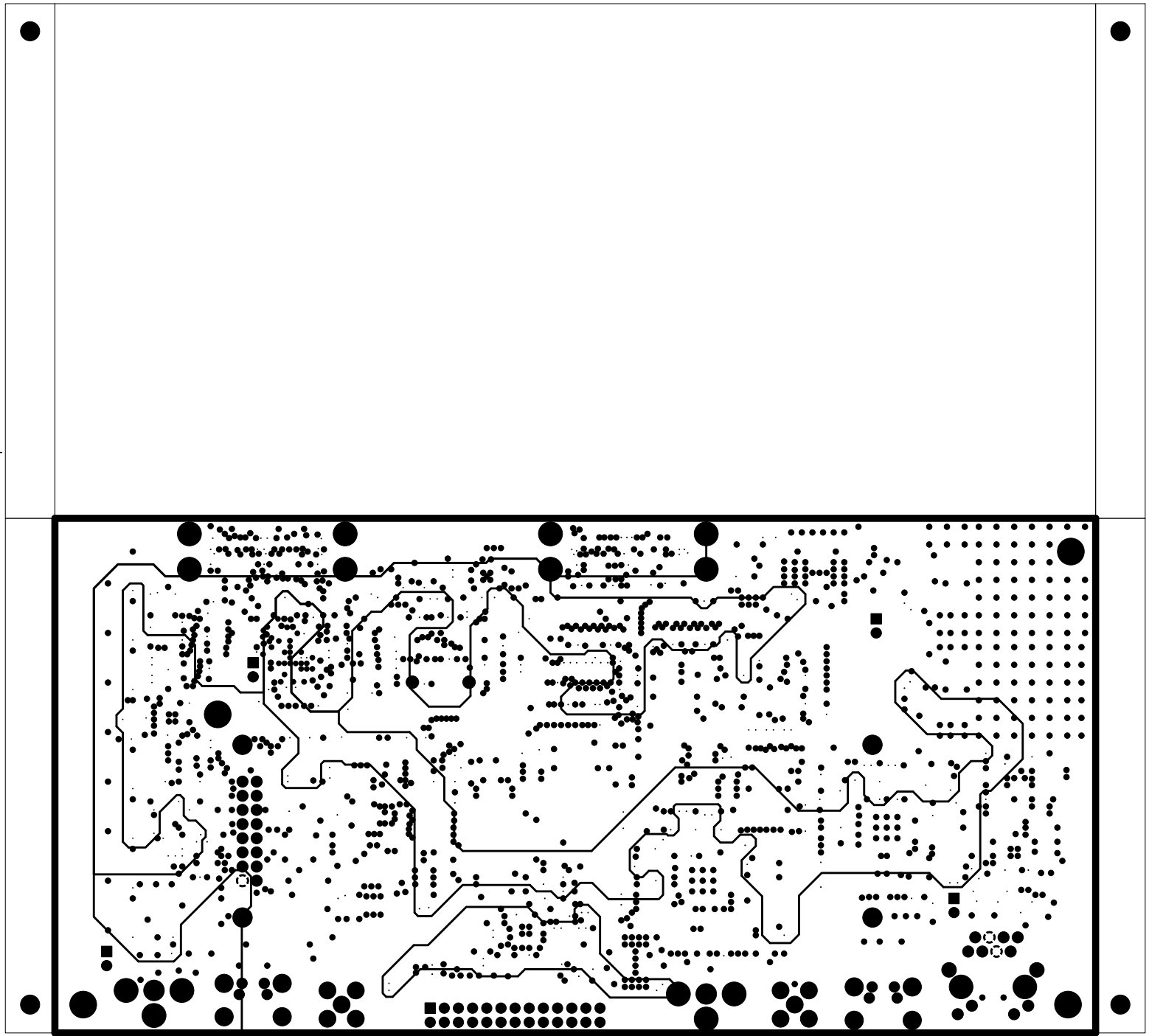
PART NO.	REV	DATE	CHANGES
1012949	A	04-09-2009	--
1013357	A	06-05-2009	--
1013479	A	07-08-2009	SEE BELOW #1,2
1013867	A	08-10-2009	SEE BELOW #3

1. VIDEO OUTPUT CONSOLIDATED TO ONE IC
2. POWER SUPPLIES CHANGED
3. FIXED CHARACTER LCD ENABLE

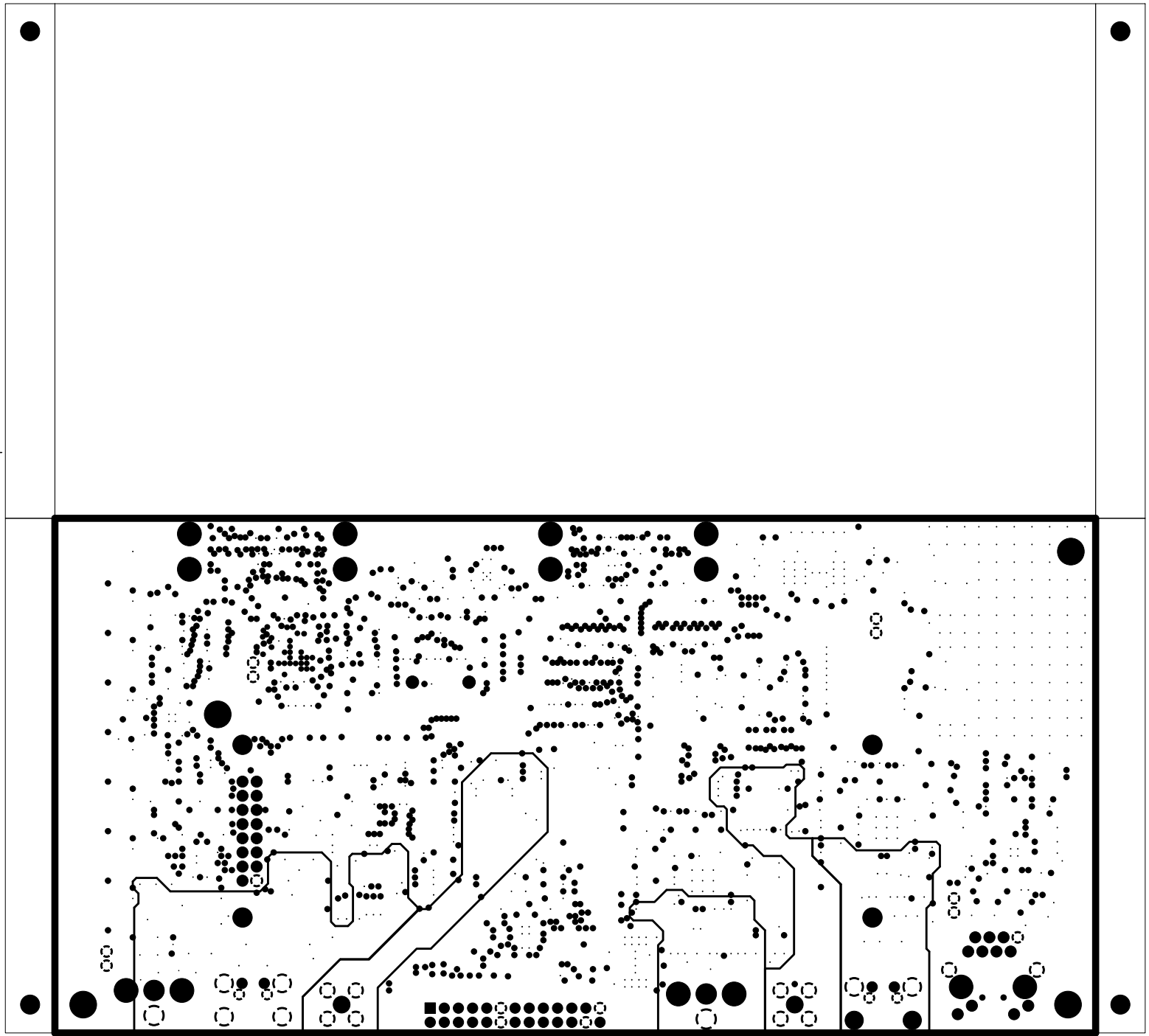
DRILL CHART				
SYM	DIAM	TOL	QTY	NOTE
x	0.010	+/-0.003	34	PLATED
+	0.012	+/-0.003	1589	PLATED
◇	0.035	+/-0.003	8	PLATED
⊠	0.040	+/-0.003	46	PLATED
⊞	0.045	+/-0.003	16	PLATED
⊟	0.050	+/-0.003	2	NON-PLATED
△	0.064	+/-0.003	2	PLATED
×	0.067	+/-0.003	10	PLATED
⊗	0.067	+/-0.003	2	PLATED
+	0.090	+/-0.003	8	PLATED
◇	0.096	+/-0.003	4	PLATED
o	0.098	+/-0.003	4	NON-PLATED
⊞	0.102	+/-0.003	6	PLATED
⊞ <sub>A</sub>	0.128	+/-0.003	2	NON-PLATED
⊞ <sub>B</sub>	0.129	+/-0.003	8	NON-PLATED
⊞ <sub>C</sub>	0.150	+/-0.003	4	NON-PLATED
TOTAL			1745	



LOGIC PRODUCT DEVELOPMENT  
LAYER 1 TOP

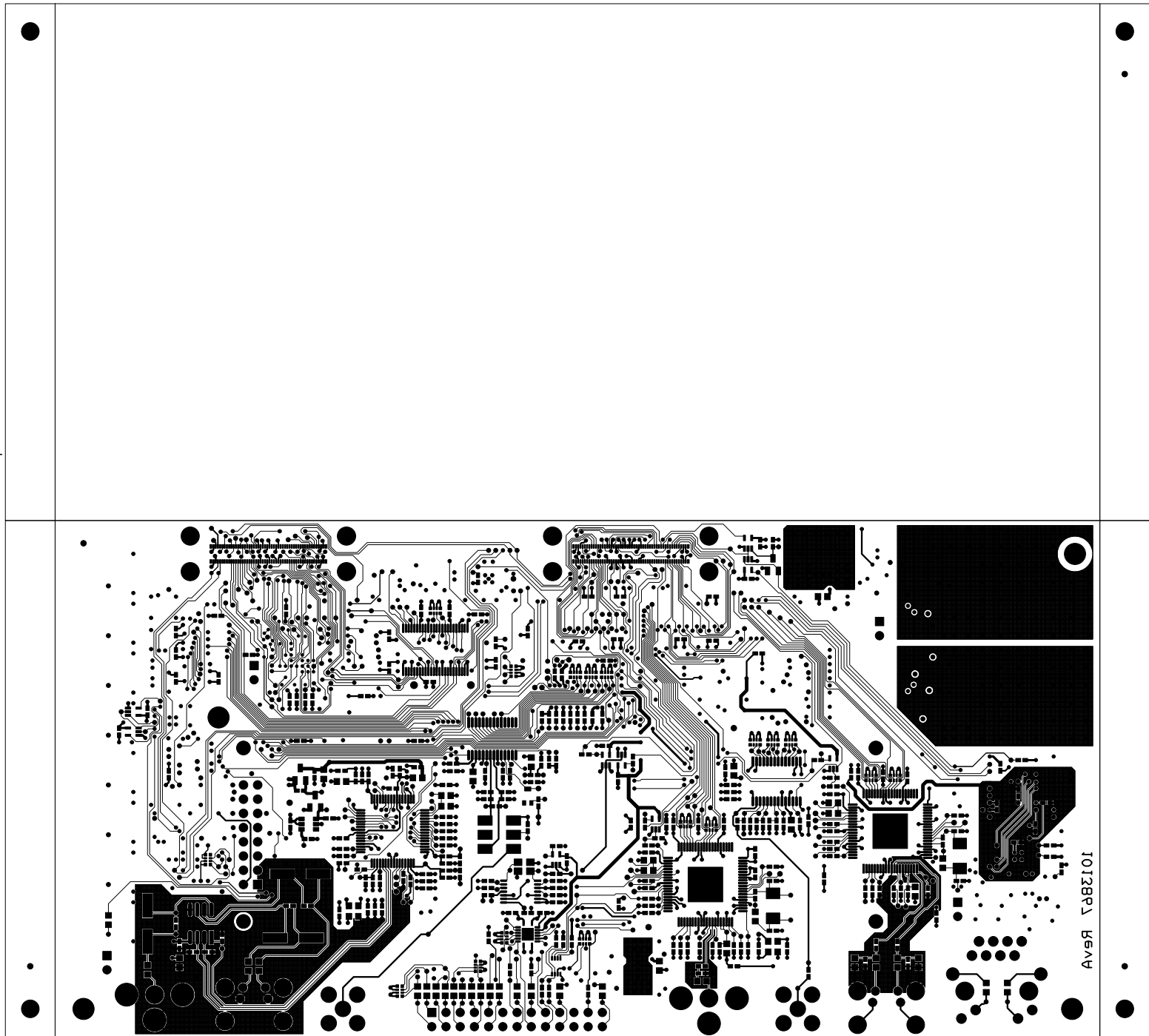


LOGIC PRODUCT DEVELOPMENT  
LAYER 2 PWR



LOGIC PRODUCT DEVELOPMENT

LAYER 3 GND



10128P1 RevA

