AM335x DDR3 Software Leveling Program MLO User Guide

User Step:

1. Insert the SD card with the MLO inside the FAT32 disk, then booting the board.
2. You'll see the output from the console (UART0) as below.

```
AM335x DDR3 Software Leveling -- Version: Beta 2.0 -- Program Start

Please input the AM335x EMIF Timing Configuration:
-- AM335x Default EMIF Timing configuration (for StarterKit EVM) --
DDR3_EMIF_SDRAM_TIM_1 : 0x0888A39B
DDR3_EMIF_SDRAM_TIM_2 : 0x26337FDA
DDR3_EMIF_SDRAM_TIM_3 : 0x501F830F
DDR3_EMIF_SDRAM_CONFIG : 0x61C04AB2

Your choice:  1. Use the default one; 2. Input your own one.
```

3. Set the DDR3 Frequency & EMIF timing parameters:
   a. If you are doing the software leveling for StarterKit EVM or use the same timing configuration, you can input "1" for the next step.

```
Your choice:  1. Use the default one; 2. Input your own one.
1
You will use the Default EMIF Timing Configuration for this software leveling program!
```

   b. If the default timings are not suitable for your design (most belongs to this case), choose "2" to set your DDR3 frequency & Timing parameters.
   When you use the DDR running@303MHz, please input "1"; "2" for running @400MHz. You'll see the confirm information after the choice is made.

```
Please Choose The DDR3 Frequency:  1. 303MHz; 2. 400MHz.
DDR3 Frequency is Set at 400MHz!
```

Then set the TIMING parameter according to the AM335x_DDR_register_calc_tool spreadsheet.

SDRAM_TIM_1

	reserved[31:29]	REG_T_RP[28:25]	REG_T_RCD[24:21]	REG_T_WR[20:17]	REG_T_RAS[16:12]	REG_T_RC[11:6]	REG_T_RRD[5:3]
Bit field values (hex)	0	5	5	5	D	13	3
Bit field values (binary)	000	0101	0101	0101	01101	010011	011
Register value (hex) optimized	0AAAD4DB						

SDRAM_TIM_2

	reserved[31]	REG_T_XP[30:28]	REG_T_ODT[27:25]	REG_T_XSNR[24:16]	REG_T_XSDR[15:6]	REG_T_RTP[5:3]	REG_T_CKE[2:0]
Bit field values (hex)	0	2	3	6B	1FF	3	2
Bit field values (binary)	0	010	011	001101011	0111111111	011	010
Register value (hex) optimized	266B7FDA						

SDRAM_TIM_3

	REG_T_PDLL_UL[31:28]	reserved[27:21]	REG_ZQ_ZQCS[20:15]	reserved[14:13]	REG_T_RFC[12:4]	REG_T_RAS_MAX[3:0]
Bit field values (hex)	5	0	3F	0	67	F
Bit field values (binary)	0101	0000000	111111	00	001100111	1111
Register value (hex) optimized	501F867F					

Input the values: The SDRAM_CONFIG can be got according to the DDR spec and AM335x TRM.

```
Please input your DDR3_EMIF_SDRAM_TIM_1 conifguration (in Hex) :
0x0AAAD4DB
Please input your DDR3_EMIF_SDRAM_TIM_2 conifguration (in Hex) :
0x266B7FDA
Please input your DDR3_EMIF_SDRAM_TIM_3 conifguration (in Hex) :
0x501F867F
Please input your DDR3_EMIF_SDRAM_CONFIG conifguration (in Hex) :
0x61C05332
Your input EMIF Timing configuration --
DDR3_EMIF_SDRAM_TIM_1 :         0xAAAD4DB
DDR3_EMIF_SDRAM_TIM_2 :         0x266B7FDA
DDR3_EMIF_SDRAM_TIM_3 :         0x501F867F
DDR3_EMIF_SDRAM_CONFIG :        0x61C05332
```

4. Set the DDR PHY ratio seeds. The ratio seeds value can be got from the RatioSeed_AM335x_boards spreadsheet. After all the inputs are done, the software leveling program will start. You'll be able to get the result shown as below:

RatioSeed SpreadSheet

Parameters			Comments
DDR clock frequency	400	MHz	input maximum frequency you will use
PHY_INVERT_CLKOUT	0		If (DDR_CK length) < (DDR_DQS length), then use 1. If (DDR_CK length) > (DDR_DQS length), then use 0.
Trace Length (inches)			
	Byte 0	*Byte 1*	
DDR_CK trace	0.948	0.948	input the average of DDR_CK and DDR_CKn traces. If you have two x8 memories, use the trace lengths for each corresponding byte.
DDR_DQSx trace	0.916	0.798	x can be 0 or 1, corresponding to each byte.
Intermediate values (per byte lane)			
WR DQS	0	2	these are just used for the calculations below
RD DQS	40	40	these are just used for the calculations below
RD DQS GATE	73	6E	these are just used for the calculations below
Seed values used in CCS code			
DATAx_PHY_RD DQS_SLAVE_RATIO	**40**		
DATAx_PHY_FIFO_WE_SLAVE_RATIO	**70**		
DATAx_PHY_WR DQS_SLAVE_RATIO	**1**		
Register value			
CMDx_PHY_CTRL_SLAVE_RATIO	**80**		

Console output:

```
Please Enter the PHY_INVERT_CLKOUT value (0 or 1) from the spreadsheet :
0
Please Enter the Seed RD_DQS_SLAVE_RATIO Value in Hex to search the RD DQS Ratio Window :
40
Please Enter the Seed FIFO_WE_SLAVE_RATIO Value in Hex to search the RD DQS Gate Window :
70
Please Enter the Seed WR_DQS_SLAVE_RATIO Write DQS Ratio Value in Hex to search the Write DQS Rati
o Window :
1
Please Enter the Seed PHY_CTRL_SLAVE_RATIO Value in Hex :
80
The ratio seeds for the DDR3 Software Leveling :
invert_clkout =          0x0
RD_DQS_RATIO_VAL =       0x40
FIFO_WE_SLAVE_RATIO =    0x70
WR_DQS_SLAVE_RATIO =     0x1
PHY_CTRL_SLAVE_RATIO =   0x80

        The Slave Ratio Search Program Values are...
**************************************************************
DATA_PHY_RD_DQS_SLAVE_RATIO is :0x37
DATA_PHY_FIFO_WE_SLAVE_RATIO is : 0x9C
DATA_PHY_WR_DQS_SLAVE_RATIO is : 0x1C
DATA_PHY_WR_DATA_SLAVE_RATIO is : 0x3E
**************************************************************
rd_dqs_range = 55
fifo_we_range = 156
wr_dqs_range = 28
wr_data_range = 62

Optimal values not reached, rerunning program with new values...

        The Slave Ratio Search Program Values are...
**************************************************************
DATA_PHY_RD_DQS_SLAVE_RATIO is :0x38
DATA_PHY_FIFO_WE_SLAVE_RATIO is : 0x98
DATA_PHY_WR_DQS_SLAVE_RATIO is : 0x29
DATA_PHY_WR_DATA_SLAVE_RATIO is : 0x5A
**************************************************************
rd_dqs_range = 1
```

Result:

```
Optimal values not reached, rerunning program with new values...

        The Slave Ratio Search Program Values are...
*****************************************************************
DATA_PHY_RD_DQS_SLAVE_RATIO is :0x38
DATA_PHY_FIFO_WE_SLAVE_RATIO is : 0x98
DATA_PHY_WR_DQS_SLAVE_RATIO is : 0x38
DATA_PHY_WR_DATA_SLAVE_RATIO is : 0x73
*****************************************************************
rd_dqs_range = 0
fifo_we_range = 0
wr_dqs_range = 3
wr_data_range = 2

Optimal values have been found!!

*****************************************************************
DATA_PHY_RD_DQS_SLAVE_RATIO is :0x38
DATA_PHY_FIFO_WE_SLAVE_RATIO is : 0x98
DATA_PHY_WR_DQS_SLAVE_RATIO is : 0x38
DATA_PHY_WR_DATA_SLAVE_RATIO is : 0x73
*****************************************************************

===== END OF TEST =====
DDR3 software leveling done!
```

References:

For Step 3 details, you can refer to the link:

http://processors.wiki.ti.com/index.php/AM335x_EMIF_Configuration_tips

For Step 4 details, you can refer to the Link:

http://processors.wiki.ti.com/index.php/AM335x_DDR_PHY_register_configuration_for_DDR3_using_Software_Leveling