

Antenna Interface 2 (AIF2) Training

Part-2 -- Introducing AIF2 Key modules

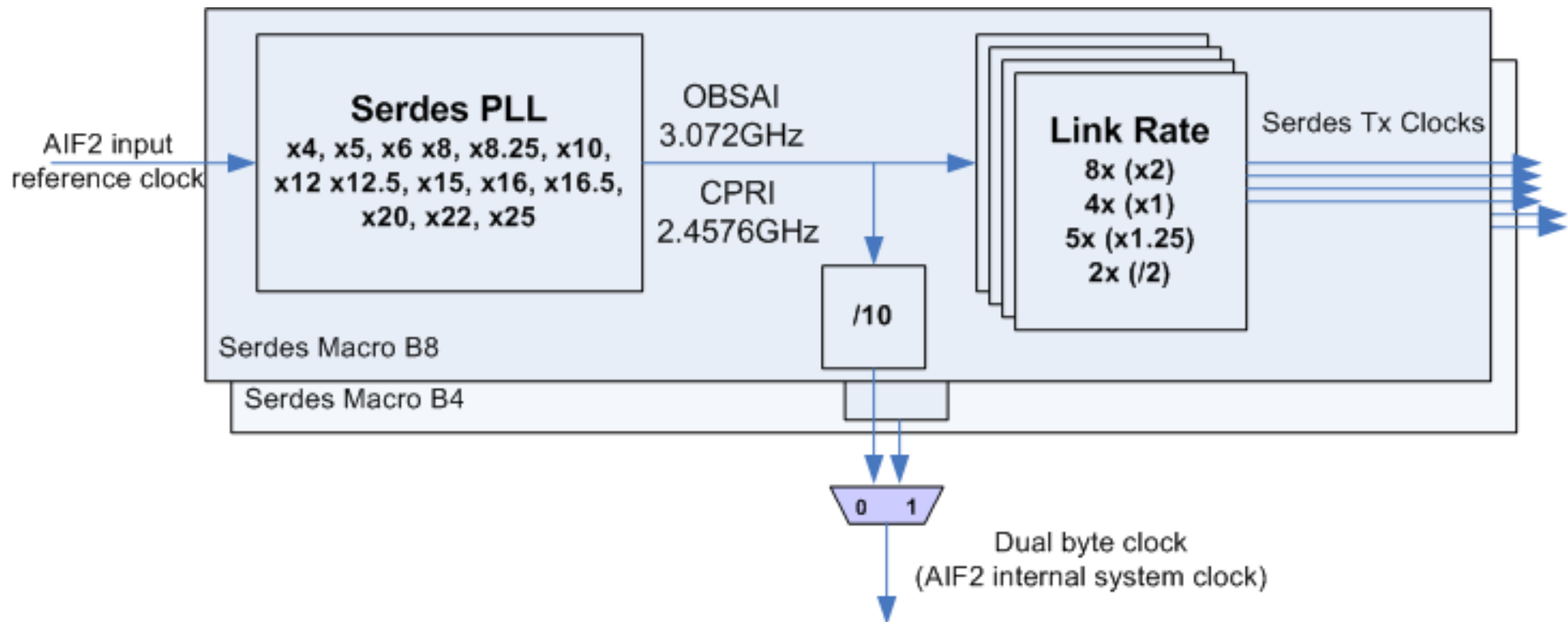
Brighton Feng

2012-6-3

Agenda

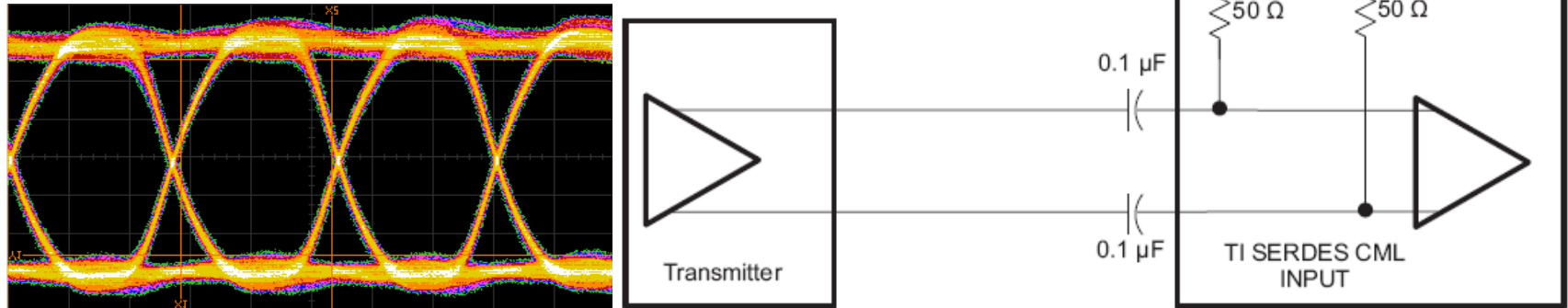
- **Introducing AIF2 Key modules**
 - AIF2 clock, Serdes (SD), AIF2 Timer (AT)
 - Protocol Encoder (PE), Protocol Decoder (PD)
 - AIF2 Data Buffer (DB), AIF2 DMA (AD)
 - AIF2 Direct IO (DIO)

AIF2 Clocks



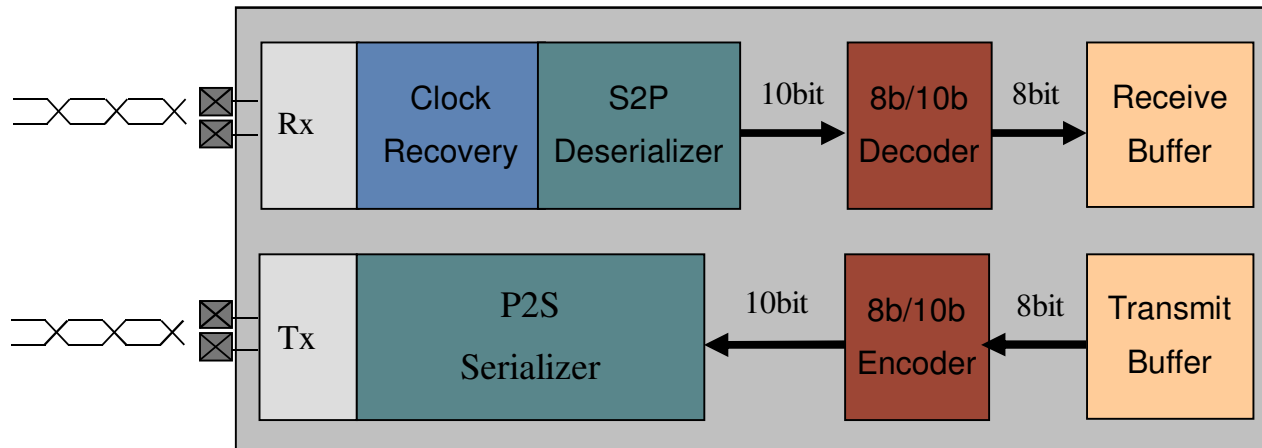
- Input clock are recommended to be between 122.88MHz and 800MHz.
- The dual byte clock, 307.2MHz for OBSAI or 245.76MHz for CPRI, is used internally for AT, TM, PE, PD...
- Each link can use different link rate.

AIF2 SerDes



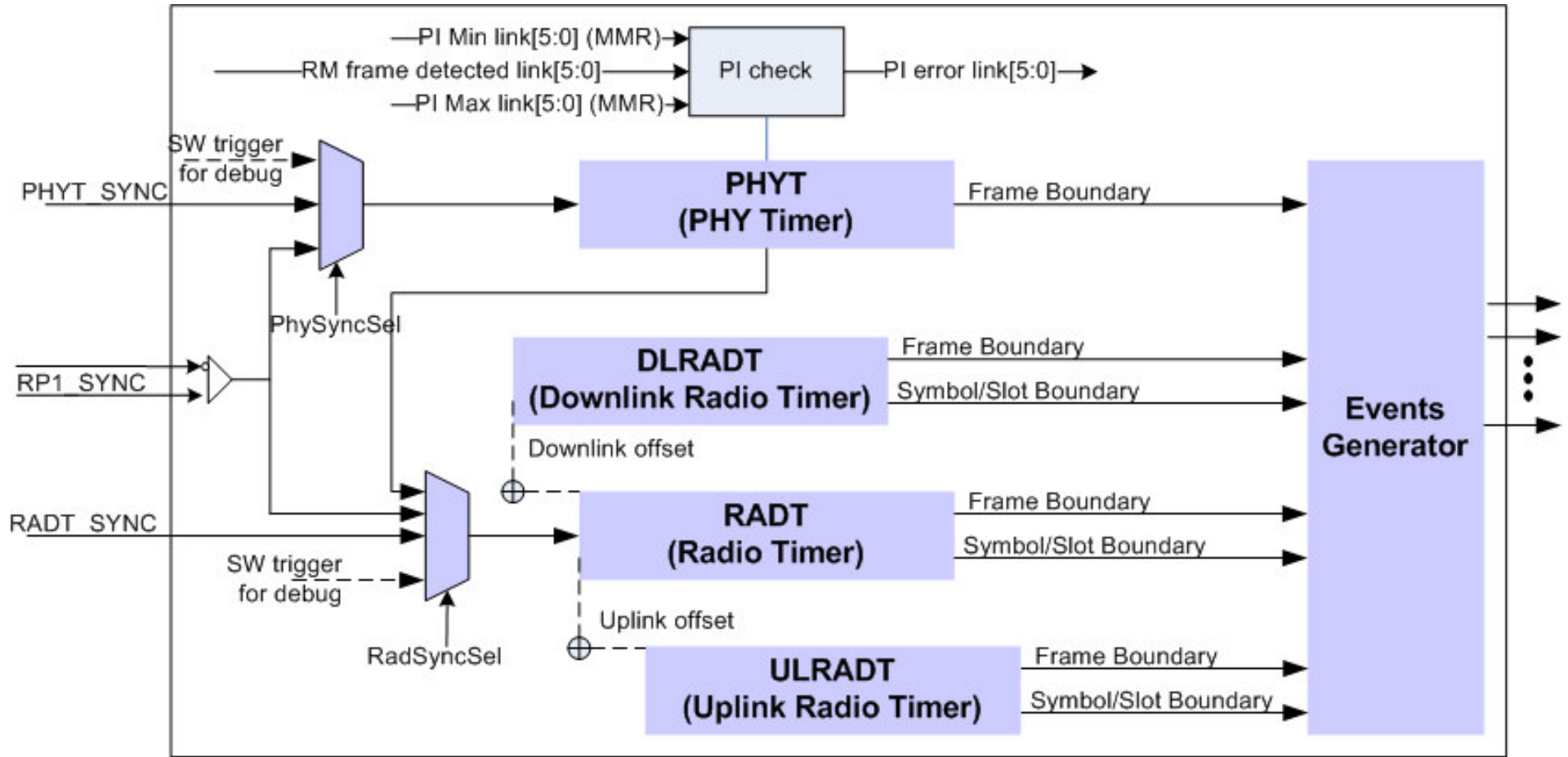
- Differential AC-coupled signal, 760mv~1220mv swing.
- Current Mode Logical (CML), receivers include 100 ohm termination and internal biasing.
- High speed, up to 6.144Gbps
- Scrambling for OBSAI 8x link (not support for CPRI)
- disable for each link to save power
- Supports internal loopback for test and debug

SerDes Block Diagram



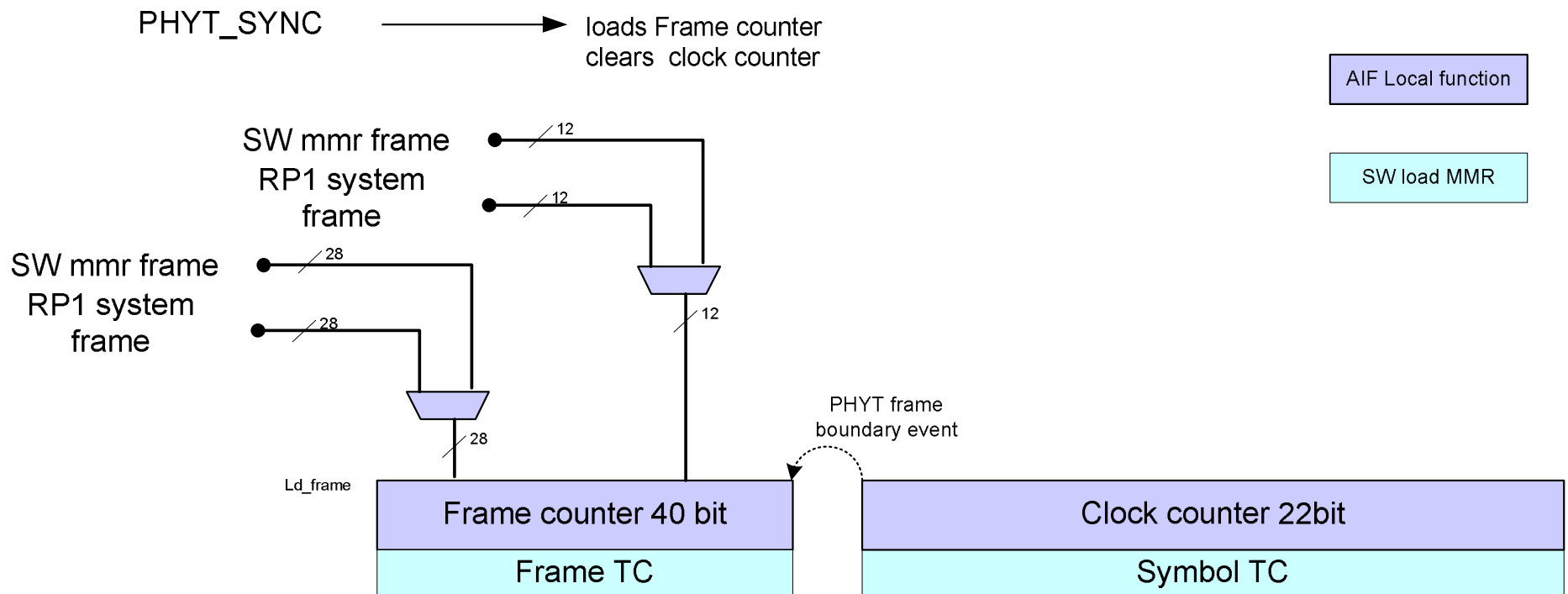
- **SerDes stands for Serializer/Deserializer, which transfer parallel data byte in serial signals.**
- **No dedicated clock signal, receiver recovers the clock according data transitions.**
- **8b/10b Codec ensure adequate data transitions for the clock recovery.**

AIF2 Timer (AT) Module



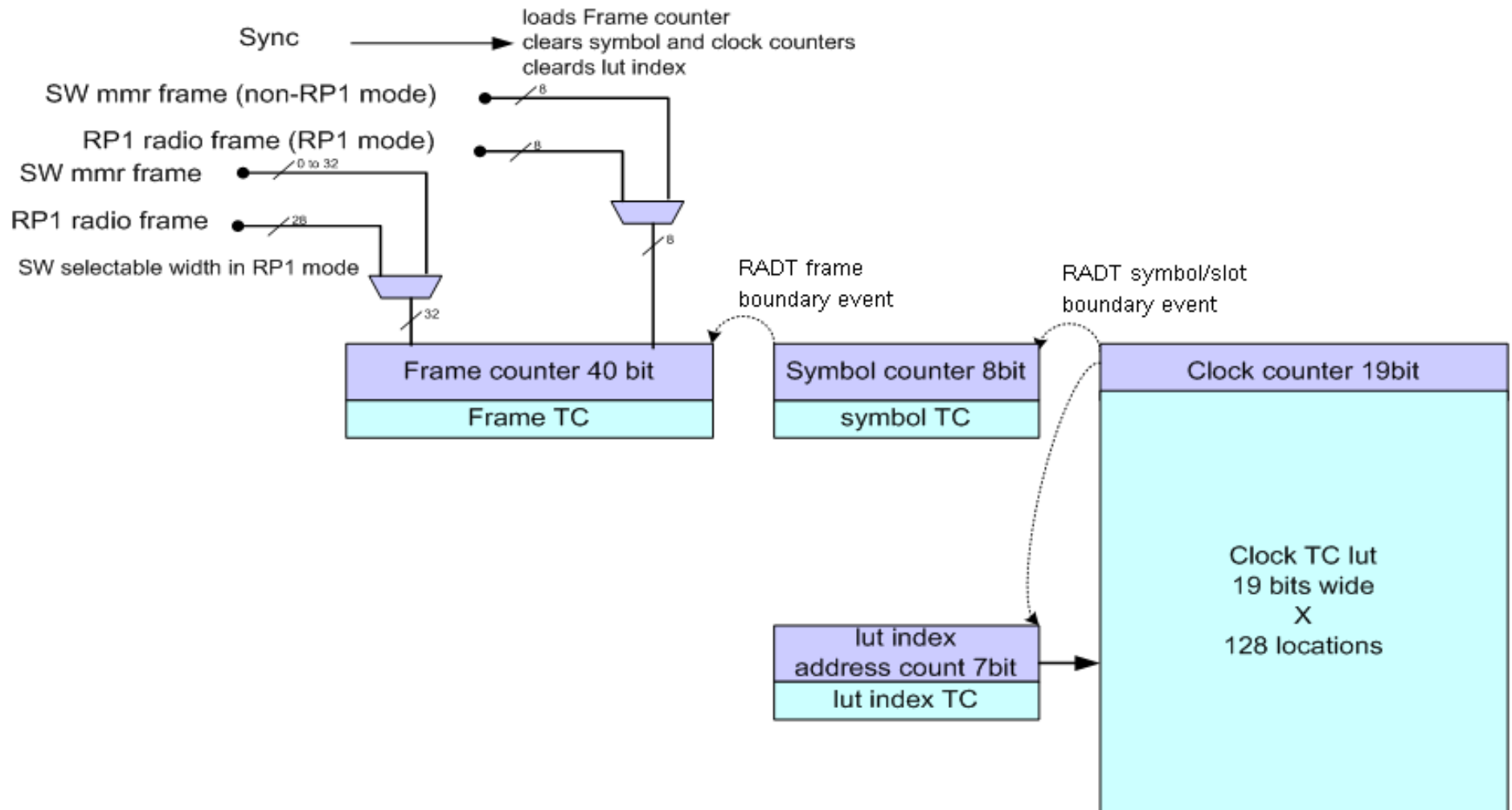
- Rad Timer (RADT) supports various frame size for various radio standards.
- AT also supports separate UL and DL timers for application.
- UL and DL offset is configured by setting init value registers.

AT PHY Timer (PHYT)



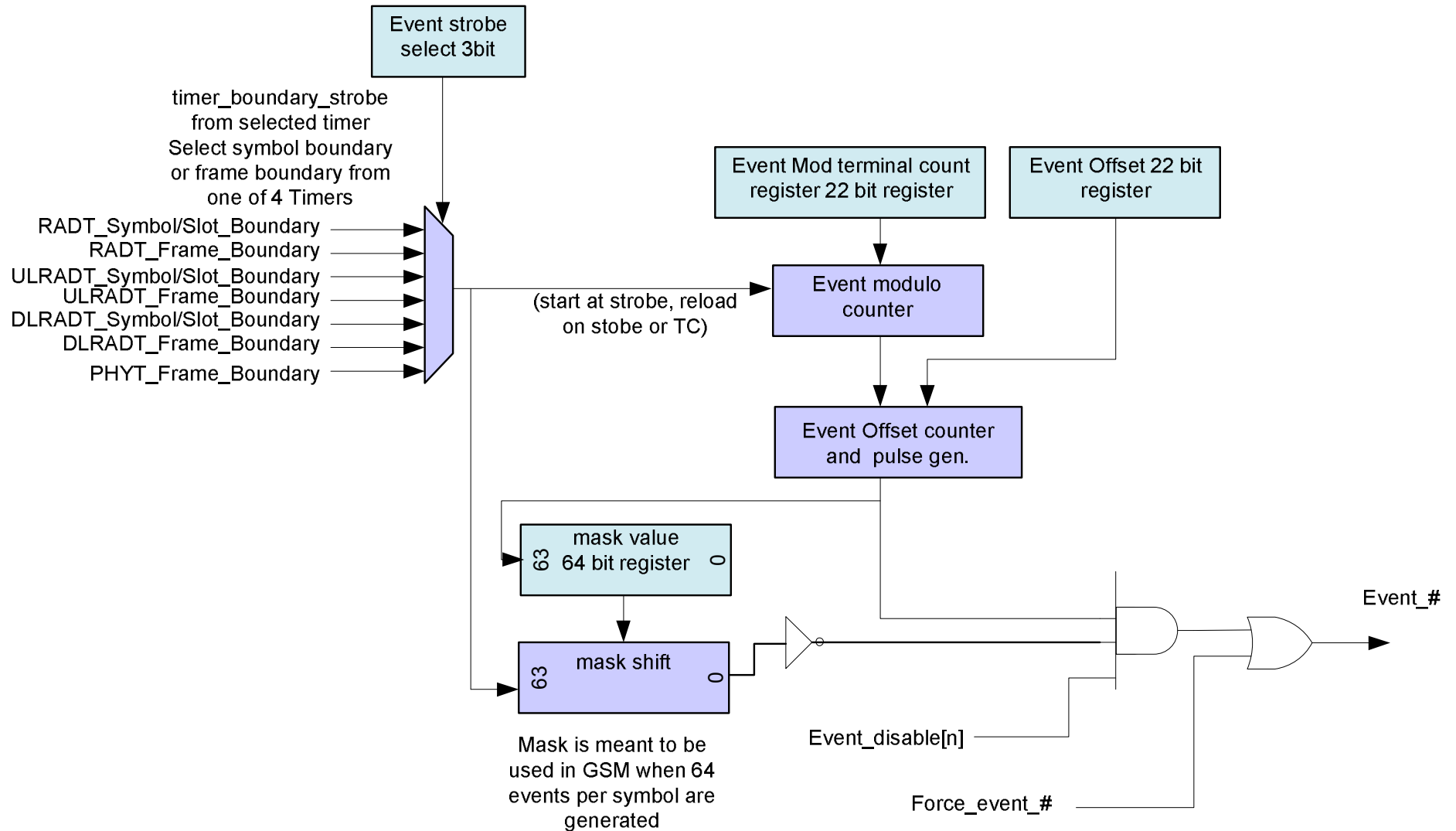
- Phy Frame size must be 10 ms and clock counter TC (Terminal Count) for this will be 3072000-1 (OBSAI) and 2457600-1 (CPRI).
- All AIF2 internal 10ms events are generated by PHYT.

AT Radio Timer (RADT)

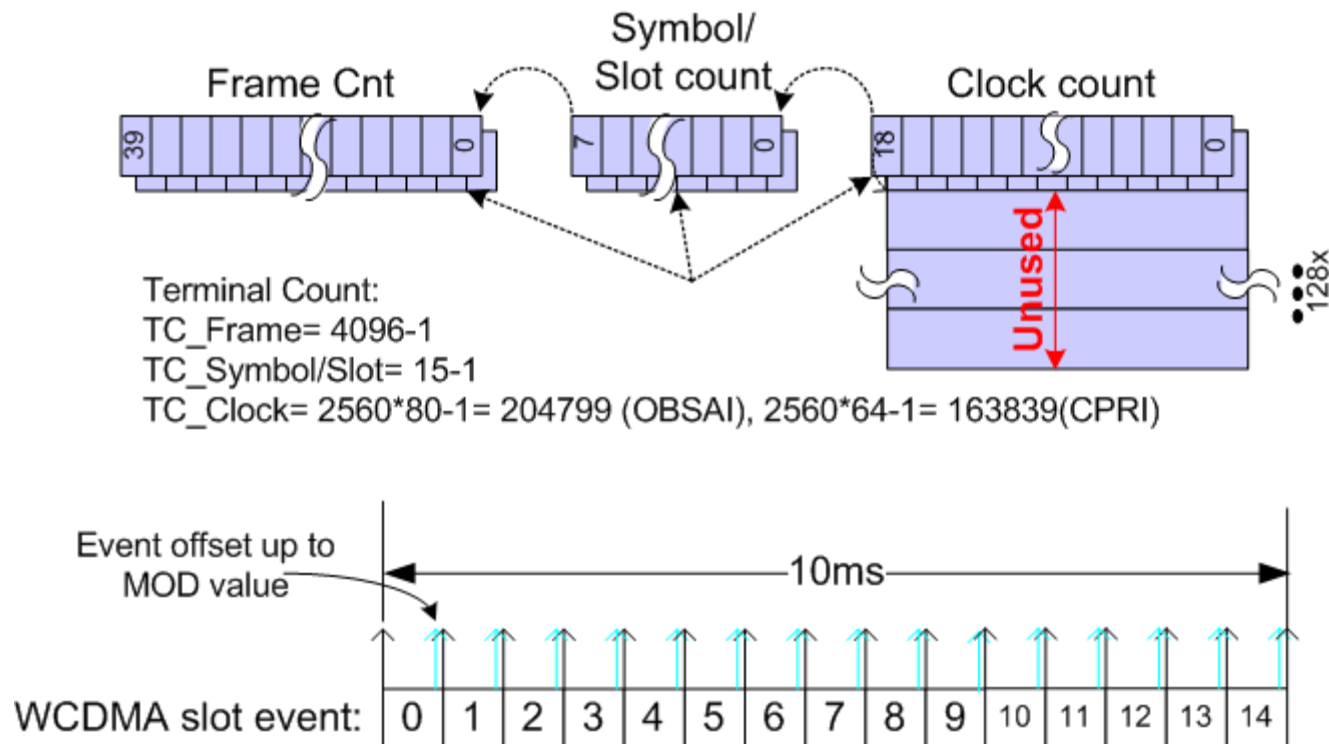


- RADT period can be any value (not limited to 10ms)
- LUT index address terminal counter is used for various size of symbols.

AT Events generation



WCDMA Events Counter Example



Frame event:

- Strobe= RADT_FB
- MOD= clocks of frame -1
- Offset = 0~ clocks of frame -1

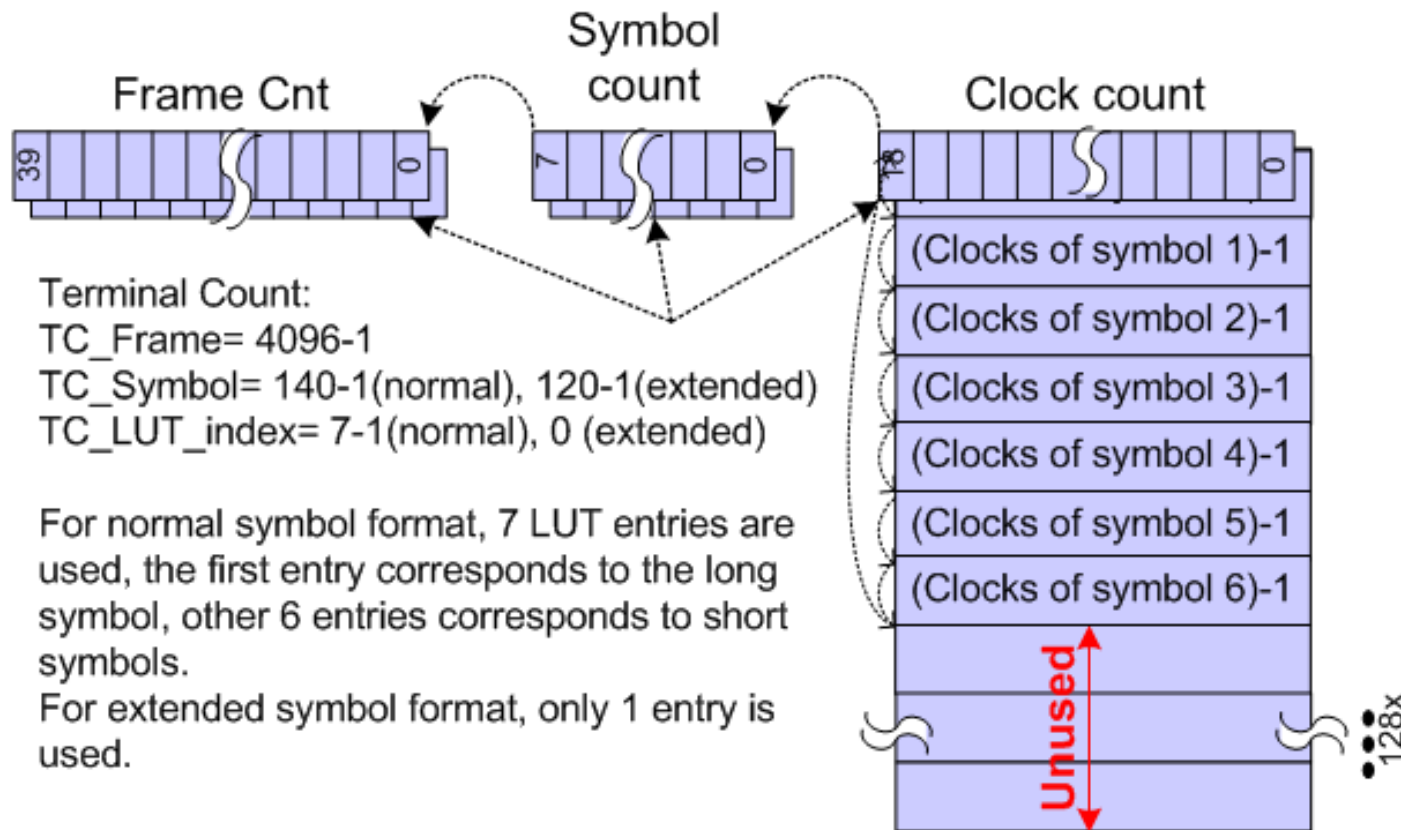
Slot event:

- Strobe= RADT_SB
- MOD= clocks of slot -1
- Offset = 0~ clocks of slot -1

4 chips event for DIO:

- Strobe= RADT_SB
- MOD= clocks of 4 chips -1
- Offset = 0~ clocks of 4 chips -1

LTE Event Counter Example



Frame event:

- Strobe= RADT_FB
- MOD= clocks of frame -1
- Offset = 0~ clocks of frame -1

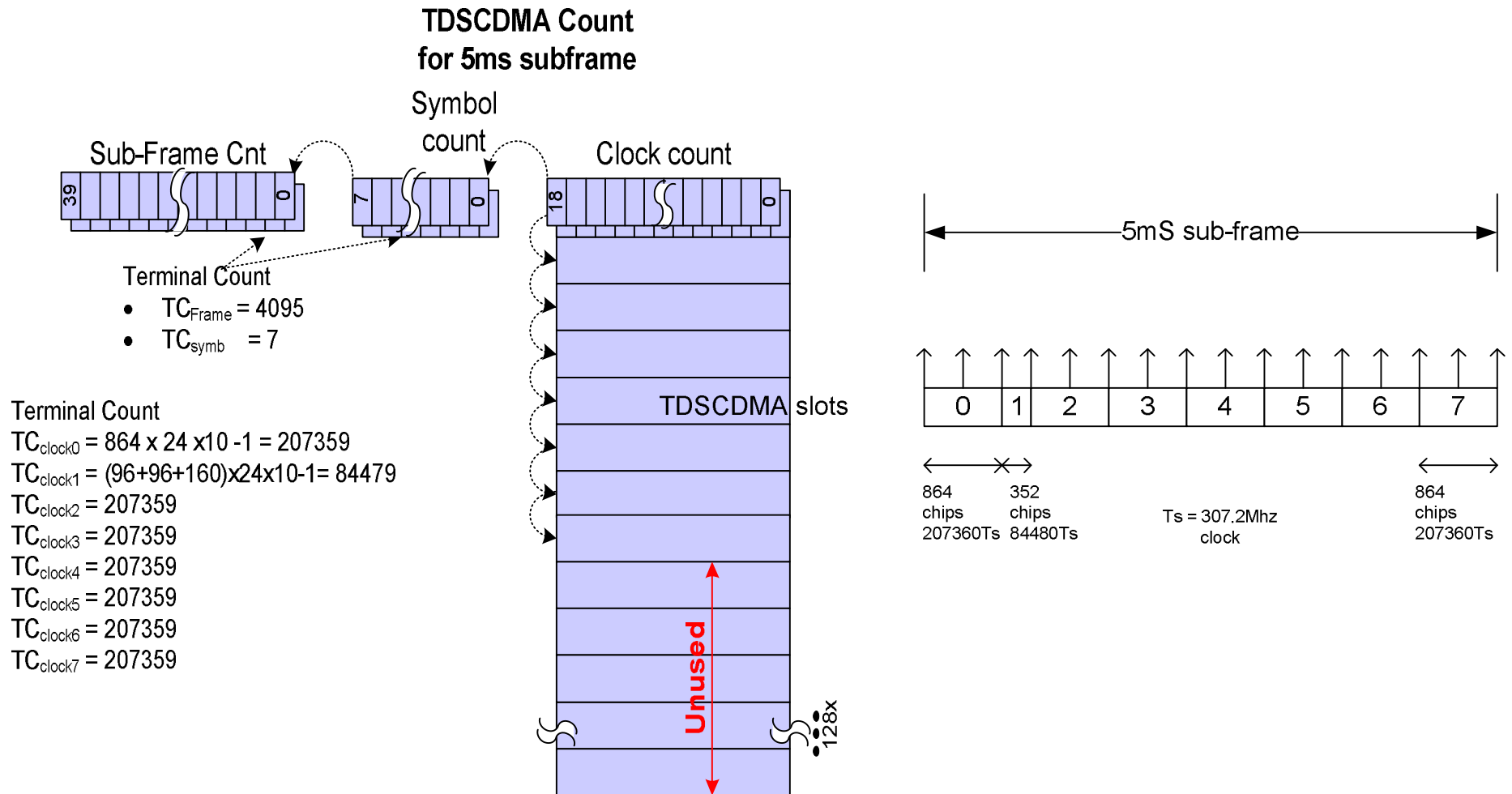
Slot event:

- Strobe= RADT_FB
- MOD= clocks of slot -1
- Offset = 0~ clocks of slot -1

Symbol Event

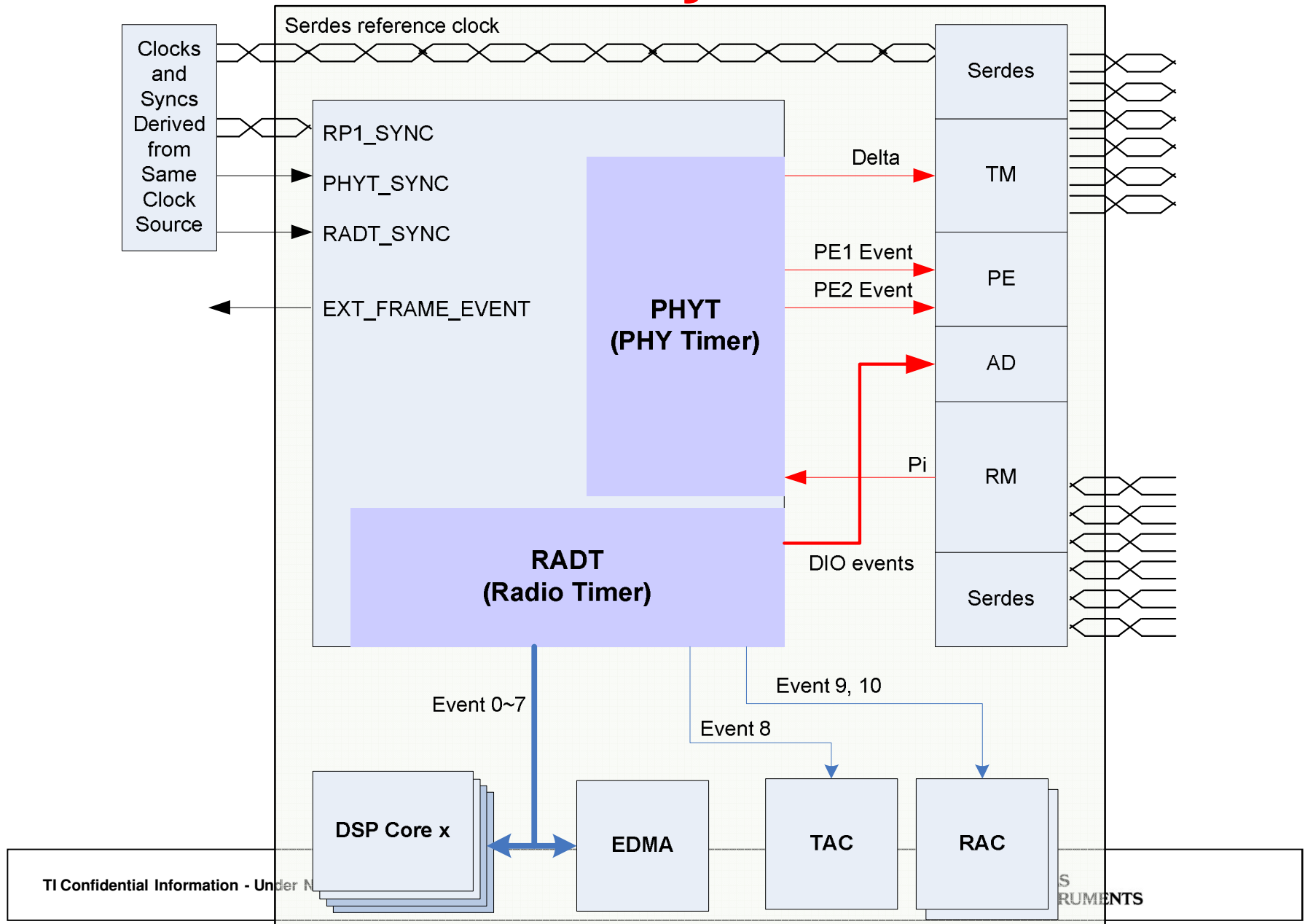
- Strobe= RADT_SB
- MOD= 0x3FFFFFF
- Offset = 0 ~ clocks of short symbol

TD-SCDMA Event Counter Example



*This example is for OBSAI, for CPRI the $T_s = 245.76$ MHz clock period

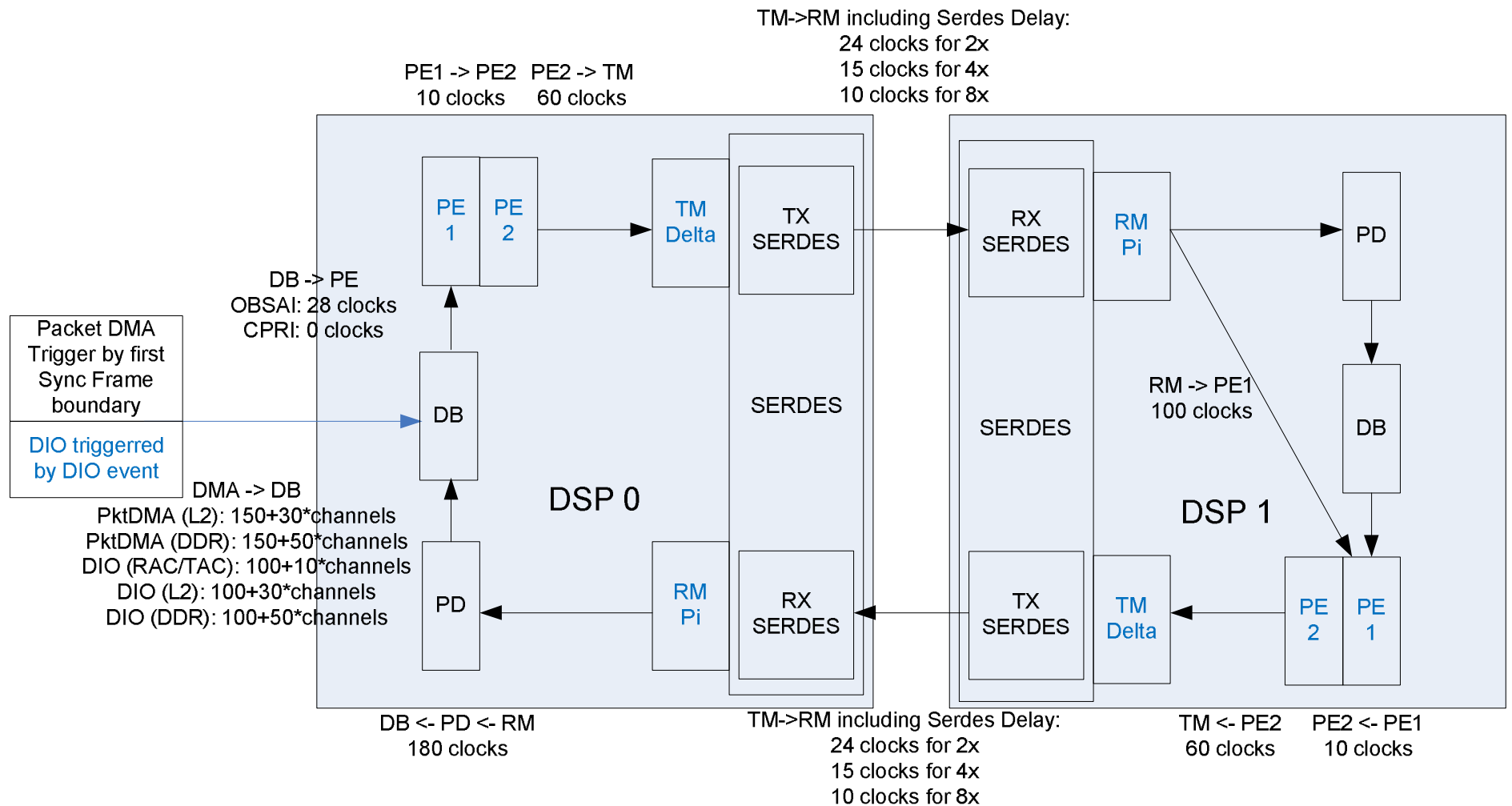
Antenna Interface Synchronization



AT Events

Events	Typical Period
Event 0~7 to DSP core	Frame, Slot or Symbol
Event 8 for TAC	4 chips
Event 9 for RAC_A, Event 10 for RAC_B	32 chips
12 DIO events to AIF2	4~32 chips
Delta, PE1, PE2 and Pi for AIF2	Frame

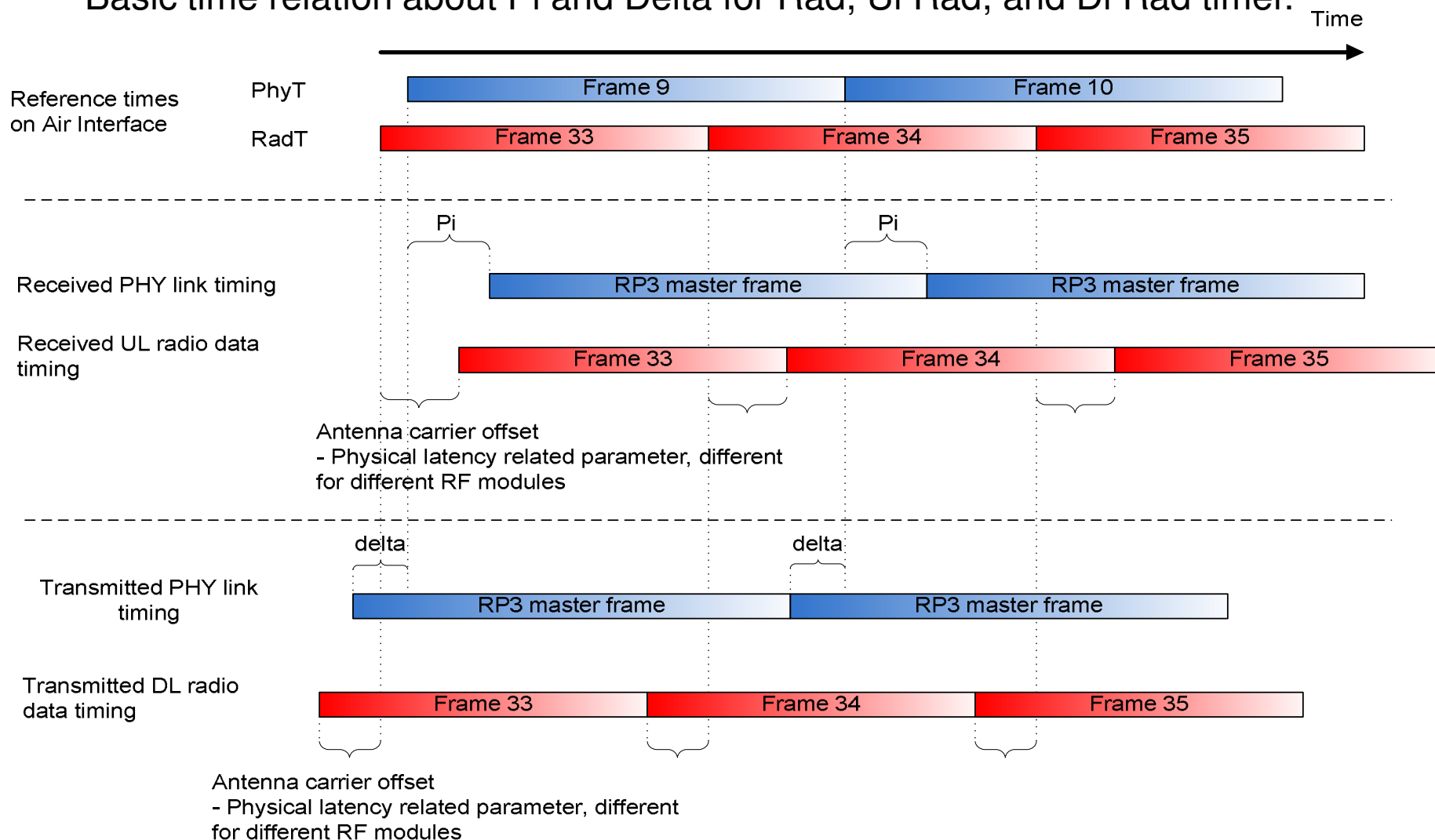
Typical AIF2 delay timing



- ❖ The above clock is dual-byte clock
- ❖ The timing parameters marked in blue need be calculated, and corresponding AIF2 timer events need be configured by software.

Timing Example

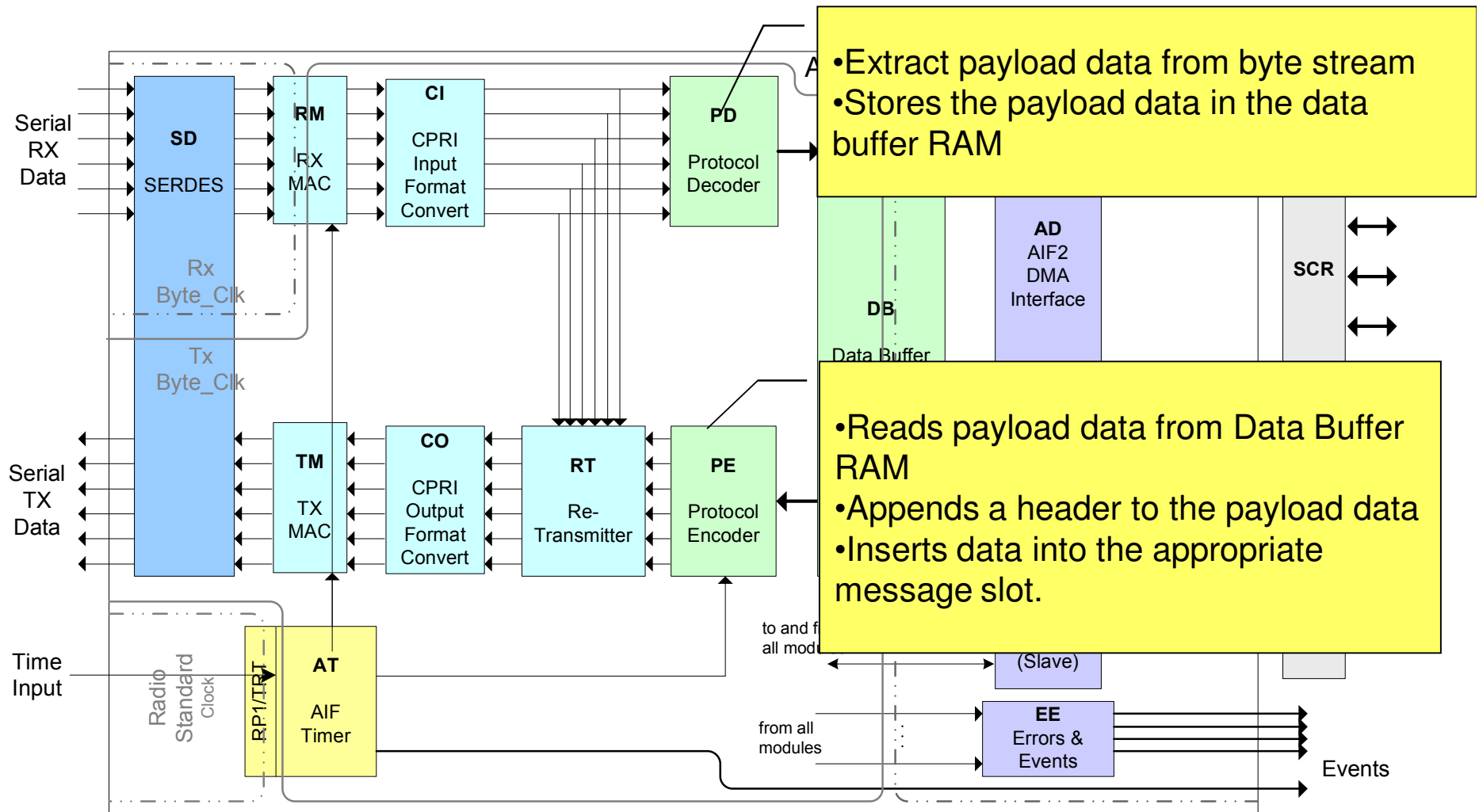
Basic time relation about Pi and Delta for Rad, UI Rad, and DI Rad timer.



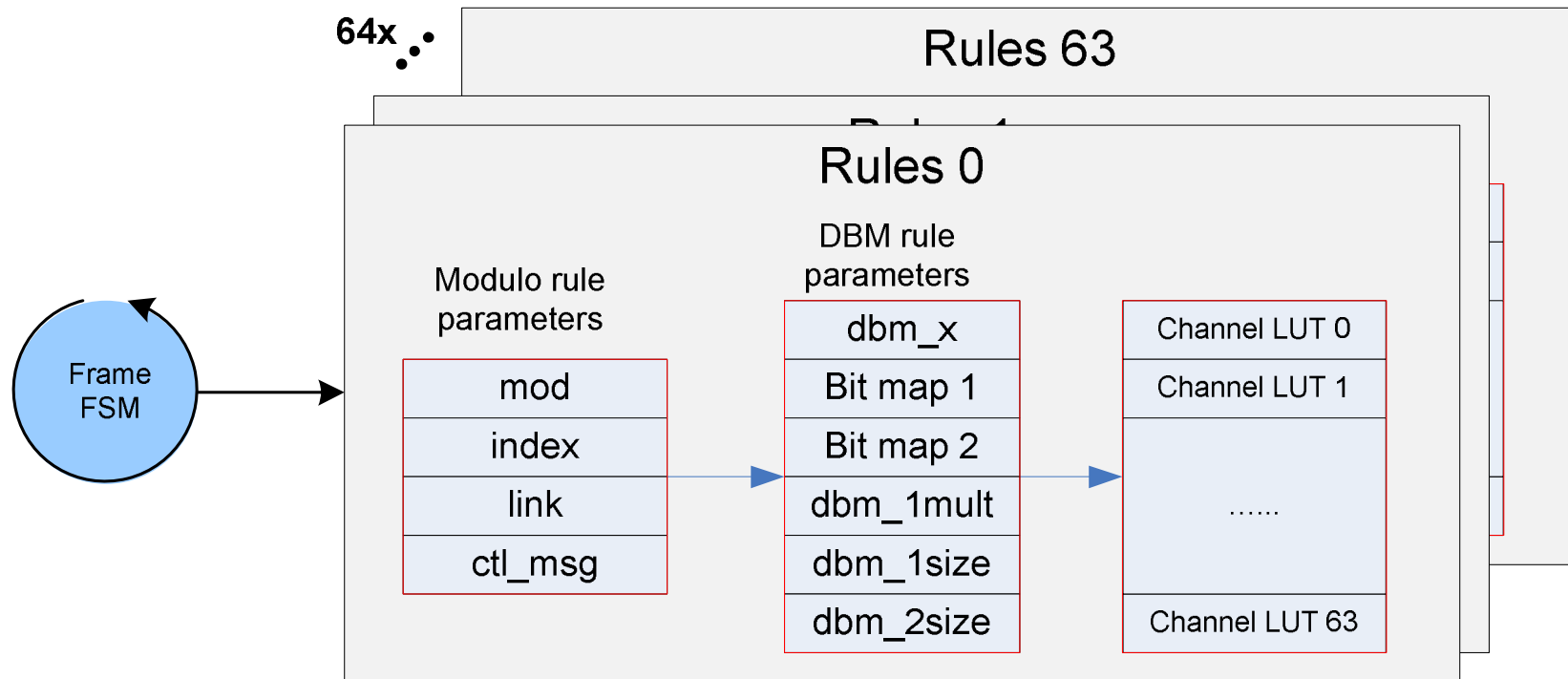
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AIF: Protocol Decoder/ Encoder

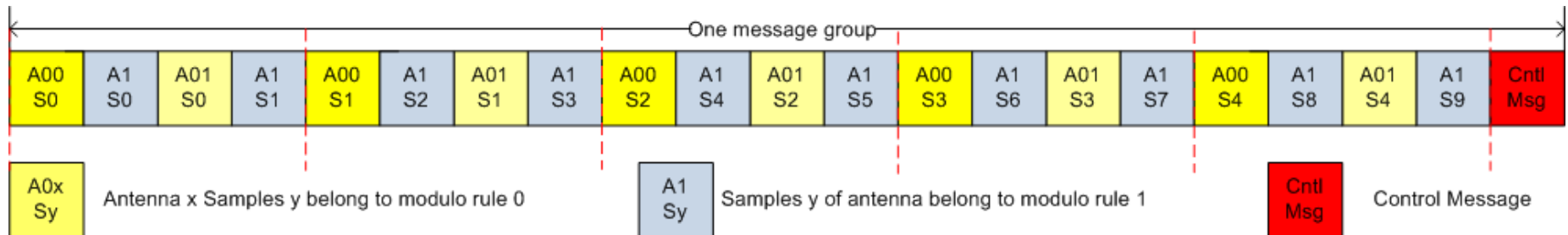


Link bandwidth allocation between antenna streams - PE OBSAI Rules



- Module rules can allocate bandwidth equally between channels. To use this method solely, it requires that link bandwidth is multiple of the bandwidth for a channel;
- The DBM rules actually implement rate matching by insert some dummy data (called “bubble”) when the link bandwidth is not multiple of these radio stream channels.

Example Rules



RuleModulo = 2-1;

RuleIndex = **0**;

link = 0;

DbmX = **2-1**;

Dbm1Map[0] = 0x0;

Dbm1Size= 0;

RuleModulo = 2-1;

RuleIndex = **1**;

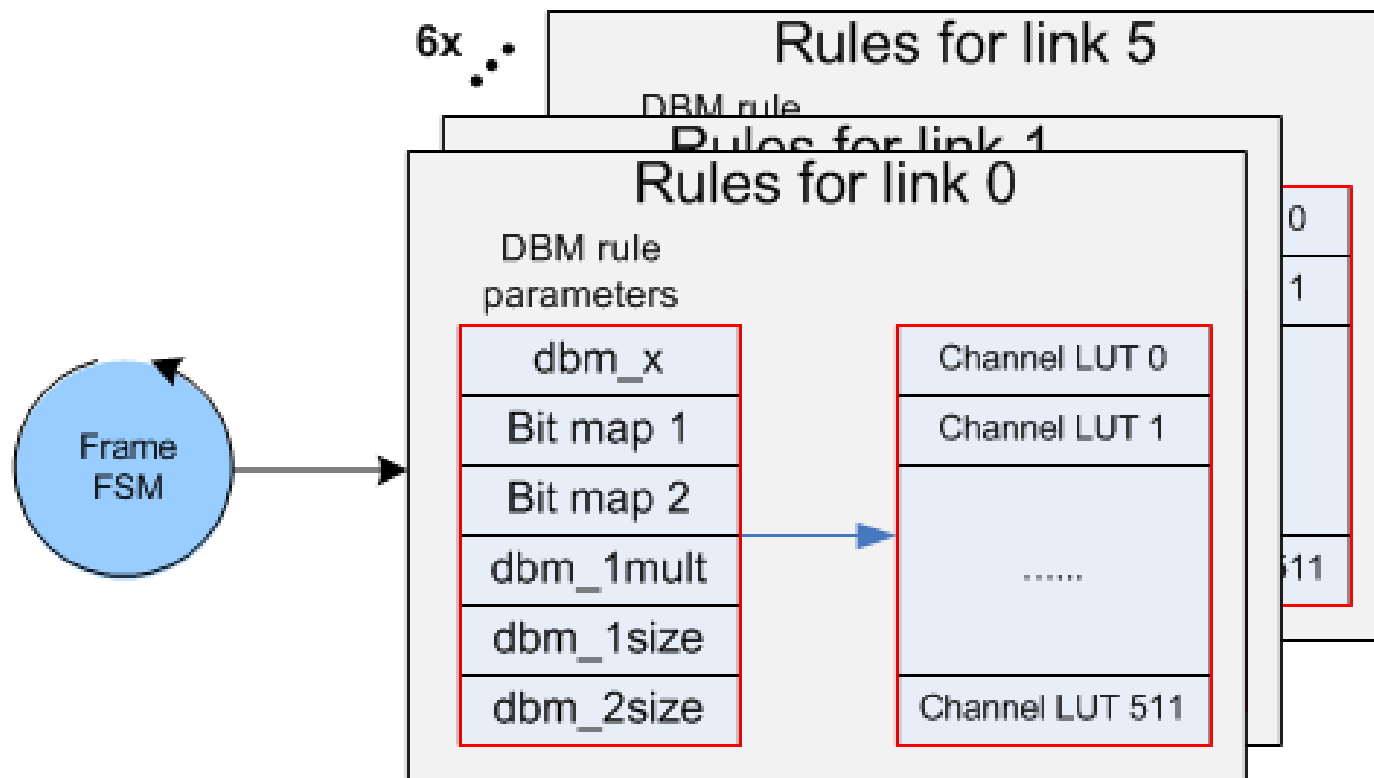
link = 0;

DbmX = **1-1**;

Dbm1Map[0] = 0x0;

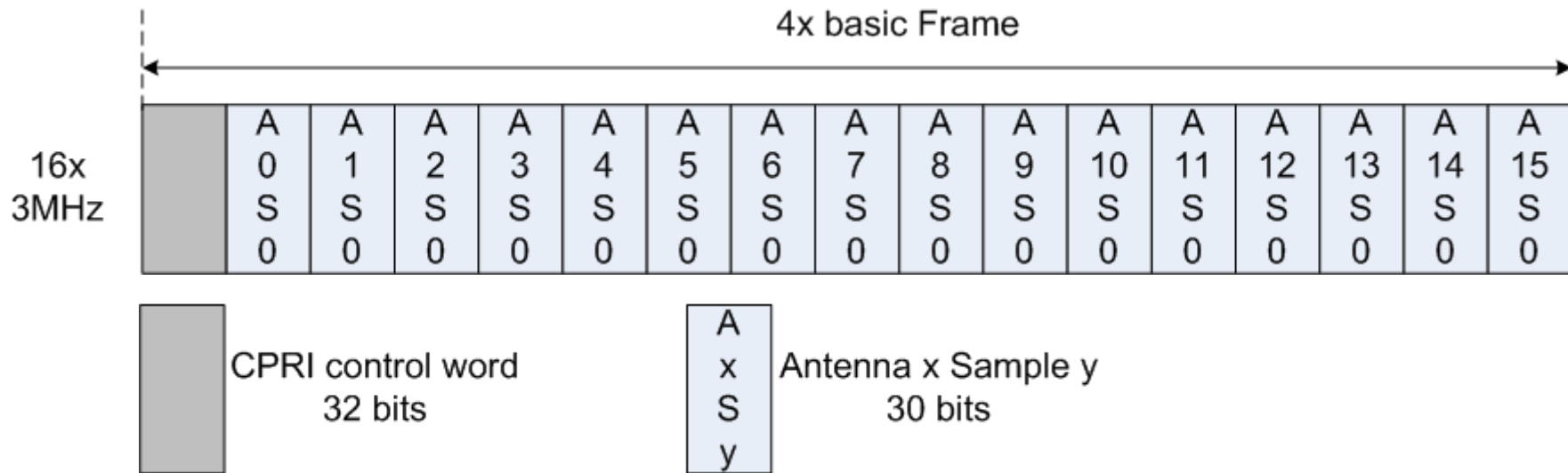
Dbm1Size= 0;

Link bandwidth allocation between antenna streams - CPRI Rules



- PE use same channel LUT RAM for CPRI and OBSAI.
- In OBSAI mode, it is organized as 64*64 entries.
- In CPRI mode, it is organized as 8*512 entries, but normally only 6*64 entries are used.

Example rules



RuleModulo = 0;

RuleIndex = 0;

DbmX = 16-1;

Dbm1Map[0] = 0x0;



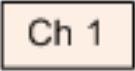
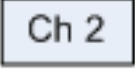
Dbm1Size= 0;

Summary of bandwidth allocation rules

	PE (TX)	PD (RX)
OBSAI	Modulo, DBM	N/A
CPRI AxC slots	DBM	DBM

- OBSAI control slot and AxC (Antenna stream Carrier) slots must use different modulo rule configuration entry.
- PD maps OBSAI message to a channel according to the message header. A channel receives a message only if the information (such as type and address) in the header matches the setup for that channel.
- For CPRI mode, DBM rules only apply to CPRI AxC slots.
- Each CPRI control words can be configured to map to a specific data channels with separate configuration registers.

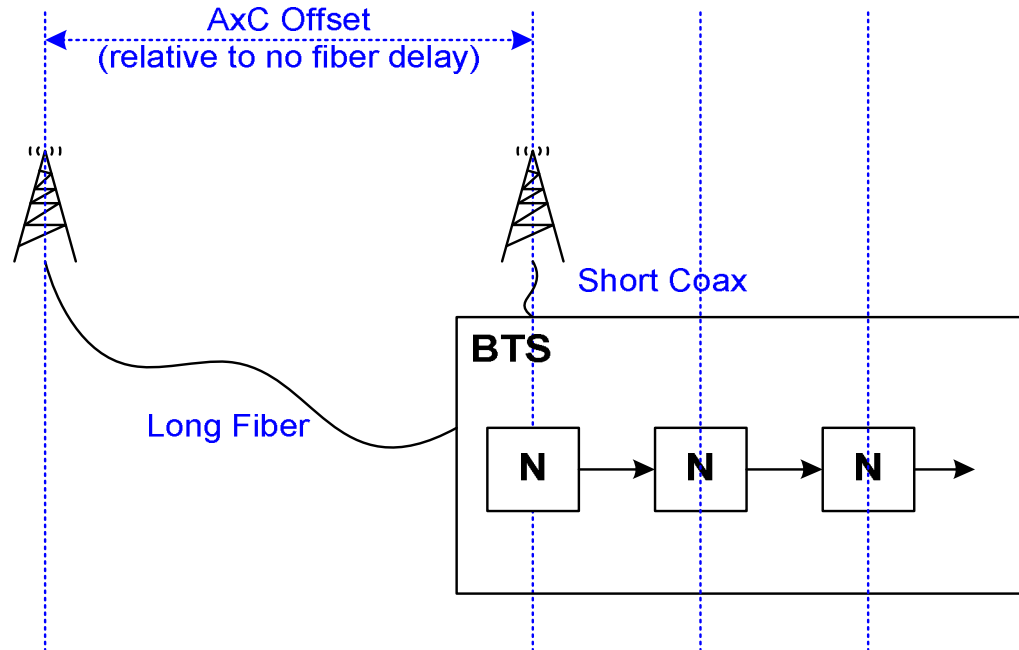
CPRI control words mapping

	Xs = 0	1	2	3	
Ns = 0					 Used or reserved by CPRI
1					
2					
3					
4					
5					
·					 Unused
·					
·					
·					
·					 Ch 1 Used by Channel 1
·					
·					
·					
·	Ch 1	Ch 1	Ch 1	Ch 1	 Ch 2 Used by Channel 2
·	Ch 1	Ch 1	Ch 1	Ch 1	
·					
·					
·	Ch 2	Ch 2	Ch 2	Ch 2	
·					
·					
·					
62	Ch 2	Ch 2	Ch 2	Ch 2	
63					

- Each link has a mapping table with 256 entries to map the 256 control words of a CPRI Hyper frame to 4 control data channels.
- The 4 control channels of each link can be mapped to 128 global data channels.

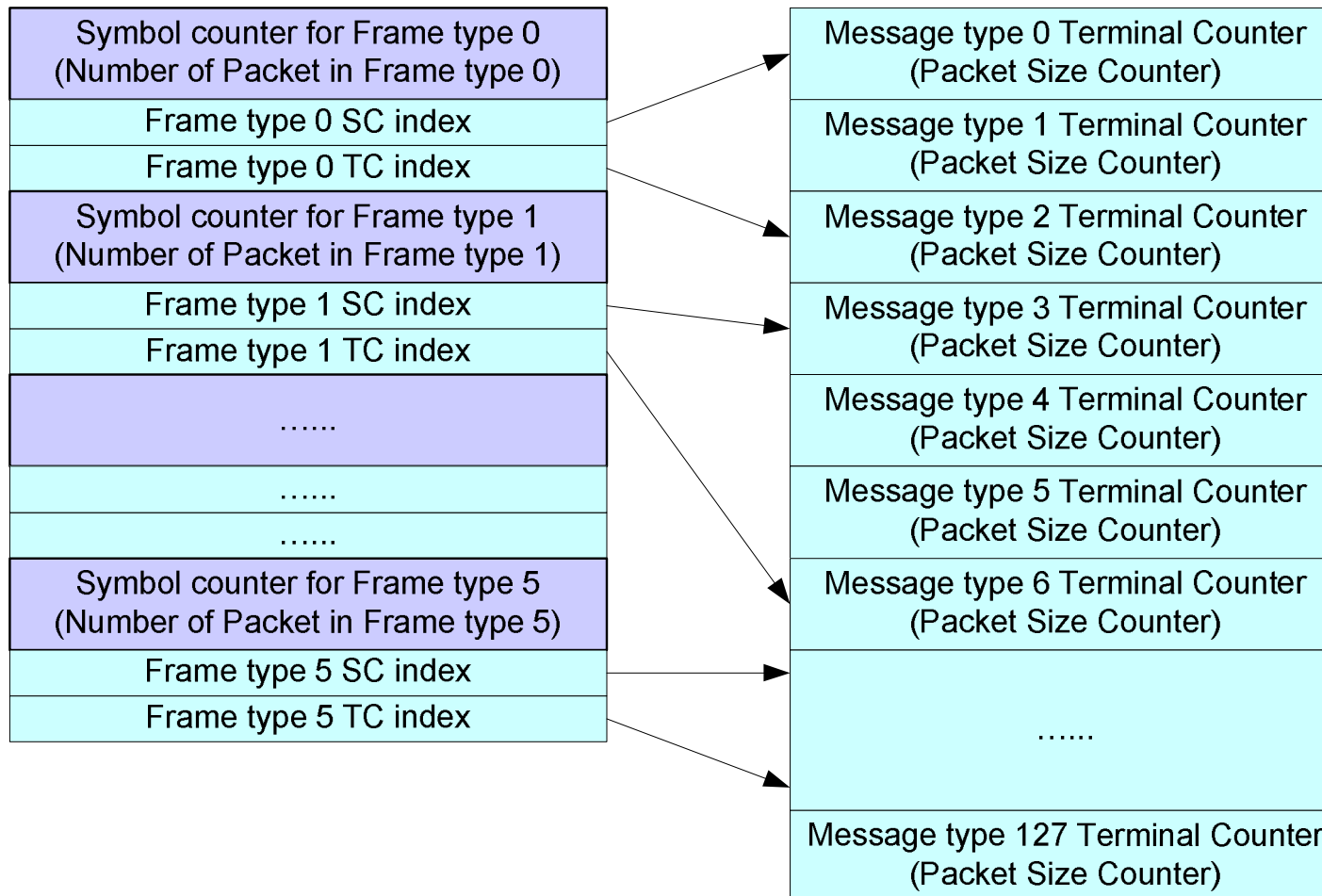
AxC Offset

- Multiple antenna stream in same link may have different delay (AxC offset).
- AxC offset is configurable for each antenna stream. For PD with CPRI mode, its configuration is different from other modes:



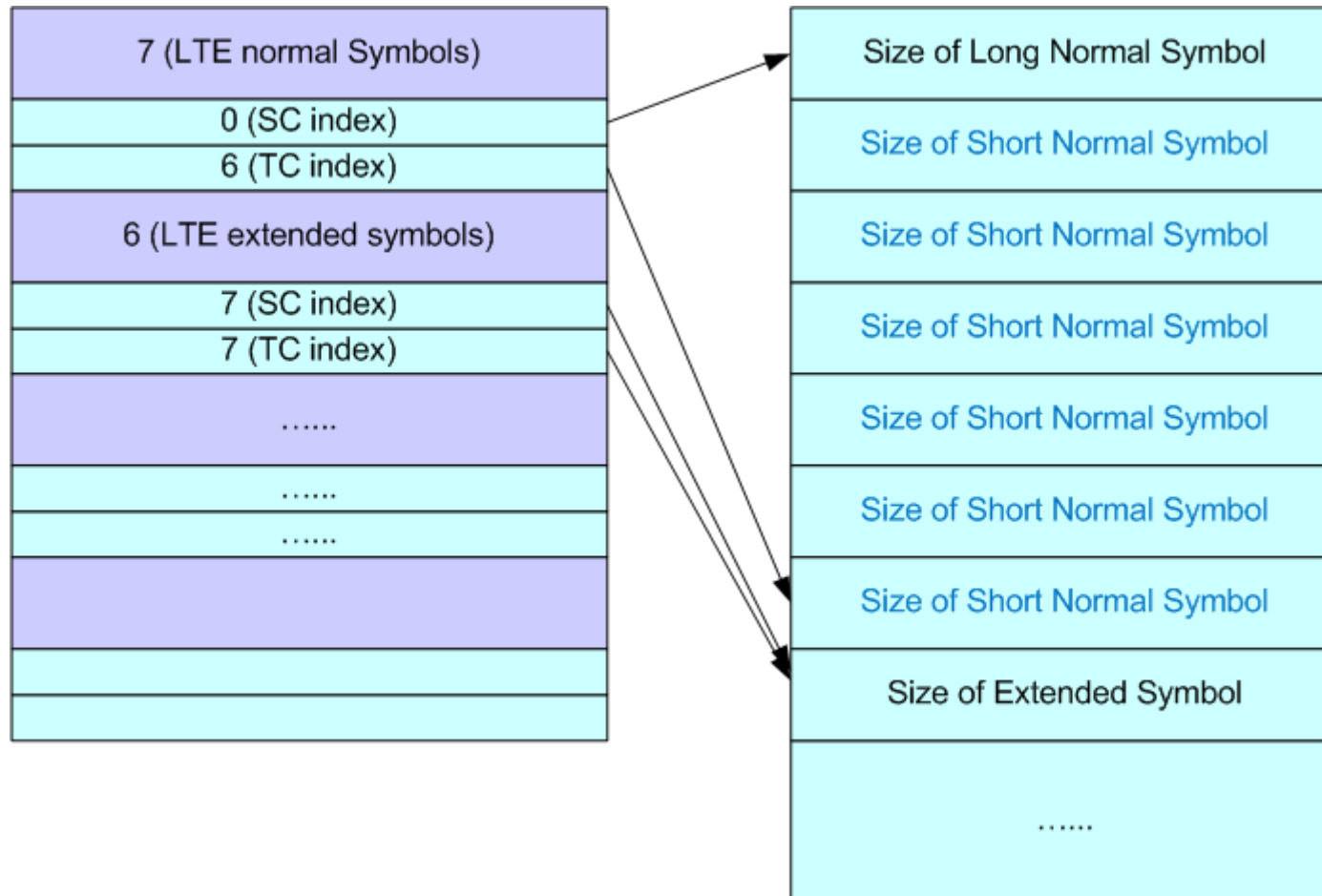
	CPRI	OBSAI
PE	Dual-byte clocks refer radio timer frame boundary	
PD	Number of quad samples refer CPRI link frame boundary (K28.5+HFN0)	Dual-byte clocks refer radio timer frame boundary

PD, PE Radio Framing Counter



Each antenna stream should use one of the 6 framing formats, and it can switch between one frame structure to another frame structure on any frame boundary.

Radio framing counter example for LTE



LTE 20MHz, 10MHz, 5MHz need different framing counters.

Difference between PE/PD radio framing counters and AT counter

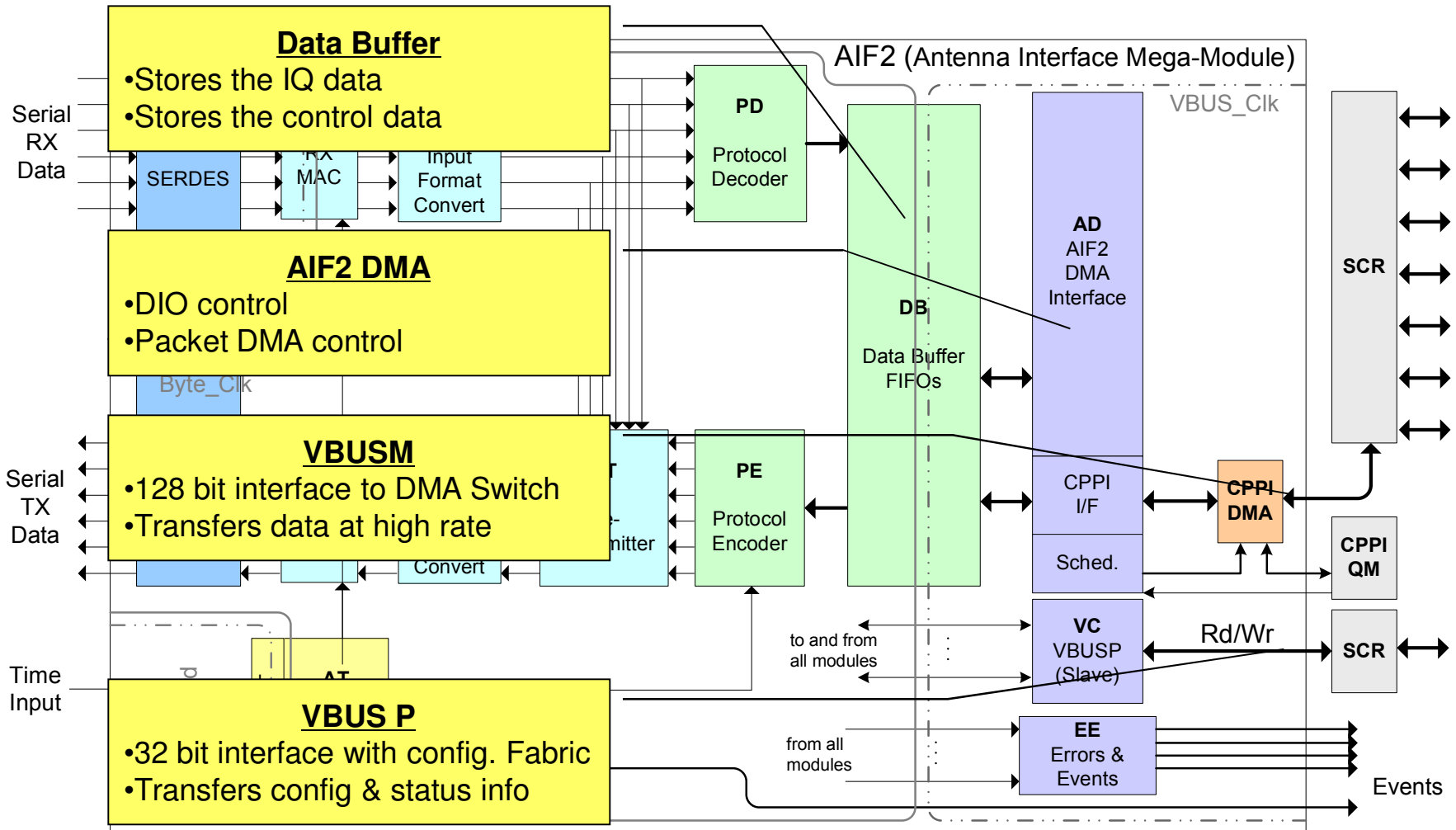
- PD/PE simultaneously supports 6 different sets of terminal counts (6 different frame structures); while AT supports only one set of terminal counts (one frame structure).
- AT counts dual-byte clocks, while PD/PE counts data bytes (CPRI) or messages (OBSAI). Below table summarize the difference.

AT	Dual-byte clocks	
OBSAI	OBSAI messages (16 bytes payload)	
CPRI	Groups of 4 bytes (PE)	Groups of 16 bytes (PD)

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AIF: Internal Interface Modules



DB (Data Buffer) Module

- 128-bit (quad word) interface
- DB Data RAM – 16K bytes for Ingress and 16KB for egress.
- Supports up to 128 buffer channels (AxC's and packet mode flows)
 - Ingress and egress has its own 128 buffers
- FIFO/Buffer size per channel is programmable
- Buffer channel programmable data swapping
- Buffer channel programmable IQ ordering

AD (AIF2 DMA) Module

- Support Packet DMA and Direct IO.
 - All AxC channels must use same mode (PktDMA or DIO).
 - Non-AxC channel (Control channels, generic data channels) always use PktDMA, even AxC channels use DIO mode.
- Supports separate ingress scheduler and egress scheduler
- Supports EOP counter for both directions (useful for debug)
- Maximum DMA Burst size is 64 bytes, inefficient for accessing DDR, recommend to put antenna data buffer in internal memory.

AIF2 PKTDMA (Packet DMA) Module

- Similar as many of other Packet DMAs in the DSP.
- 128 TX channels and 128 RX channels
 - Each TX channel (0~127) bind with one TX queue.
 - Each RX channel (0~127) bind with one RX flow.
- DIO actually use PKTDMA channel 128 to transfer AxC data. That is, AIF2 packet DMA must be configured and channel 128 must be enabled for DIO mode.

AIF2 PKTDMA (Packet DMA) features

- AIF2 PKTDMA supports host descriptor and Monolithic descriptor.
 - Monolithic mode is recommended for antenna data which is timing sensitive.
 - Host packet requires read descriptor first then the read data separately, the first piece of data may miss timing requirement.
 - Host packet may be used for generic packet transfer (CPRI should use Monolithic for this).
- TX_AIF_MONO_MODE
 - Tx AIF Specific Monolithic Packet Mode: This field, when set, packet should be pushed with the Descriptor Size field = 3.
 - The FFTC pushes its output packets with a Descriptor Size field = 1.
 - This mode should be disabled for automatic (CPU free) transfers from the FFTC to AIF2.

AIF2 Packet DMA Protocol-Specific Field in Descriptor

Bits	Name	Description
31:16	Reserved	
15	Ingress/Egress	0: Ingress 1: Egress
14:7	Symbol Number	Symbol number (0x00 – 0xFF)
6:0	AxC Number	AxC number (0x00 – 0x7F)

- The Monolithic packet descriptor header for AIF2 is exactly 16 bytes (one VBUS 128 data phase)
- Protocol Specific field is not mandatory, but it is helpful for error checking.

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Direct IO (DIO)

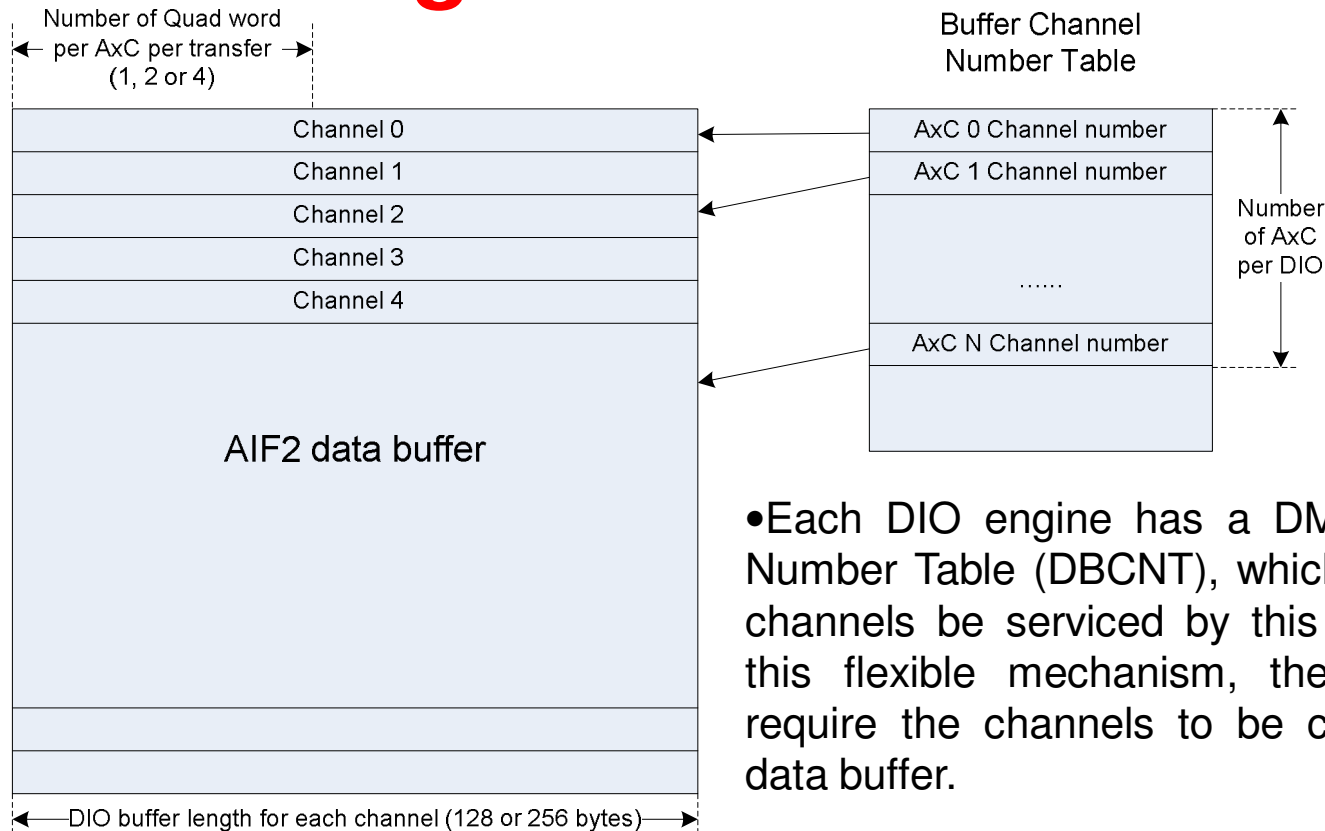
- **There are three egress DIO engines and three ingress DIO engines. Each engine can be configured to support:**
 - Uplink WCDMA antenna data format for RAC. It is also called “UL RSA” data format in some documents for compatibility with old AIF1.
 - Downlink WCDMA antenna data format for TAC.
 - User defined antenna data structure. For some application, WCDMA antenna stream may be processed by DSP core or RSA (Rake Search Accelerator) instead of RAC or TAC. For the case, the antenna data structure in DSP memory can be freely defined by software. A typical structure is collect antenna data for each stream into a separate buffer instead of interleaving antenna streams into a single buffer link RAC or TAC buffer.

DIO configuration parameters

- DIO can be looked as a customized EDMA for AIF2

DIO parameter	Equivalent EDMA parameter
Number of quad words (at AIF2 DB buffer)	ACNT
Number of AxC (at AIF2 DB buffer)	BCNT
DBCN (Dio Buffer Channel Number) table (addressing inside AIF2 DB buffer)	N/A
Number of blocks	CCNT
burst size (1,2,4 QW) (at DSP memory)	ACNT
Burst address stride (at DSP memory)	BIDX
Block address stride (at DSP memory)	CIDX
DIO base address (at DSP memory)	SRC, DST

DIO configuration for AIF2 Data buffer



- Each DIO engine has a DMA Buffer Channel Number Table (DBCNT), which is used to select channels be serviced by this DIO engine. With this flexible mechanism, the DIO does NOT require the channels to be continuous in AIF2 data buffer.

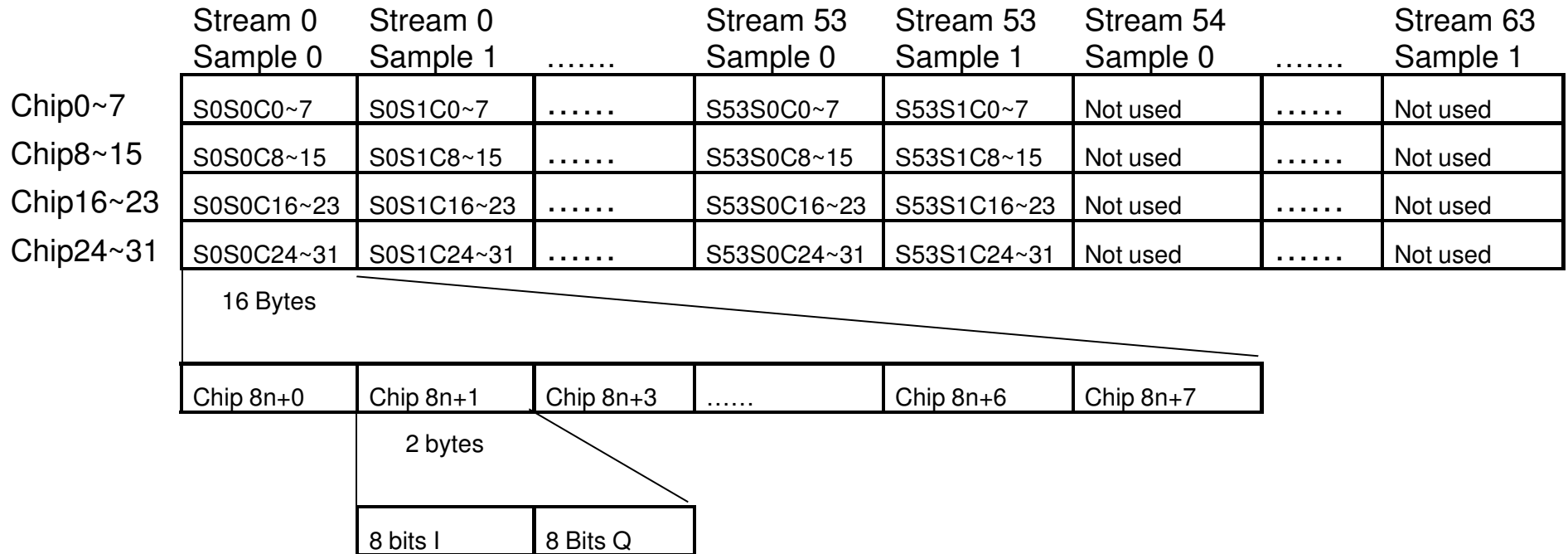
- Each DIO engine is trigger by corresponding DIO events from AIF2 timer. With each trigger event, the DIO engine transfers a block of (number of quad word) x (number of AxC). For the next event, the DIO engine will increase the access pointer in each channel buffer by (number of quad word), if the address reaches the end of the buffer, the DIO will automatically wrap it to the beginning of the buffer. So, the buffer for each channel is actually used as a circular buffer by DIO engine.

DIO configuration for AIF2 Data buffer

Parameters	Configuration	Comments
DIO buffer length	128 or 256 bytes	For WCDMA stream, 128 bytes is OK. For LTE stream, 256 bytes should be used.
Number of Quad word per AxC	1, 2 or 4	Number of quad word (16 bytes) transferred by one trigger.
Number of AxC	≤ 64	Support maximum 64 antenna streams per DIO engine.

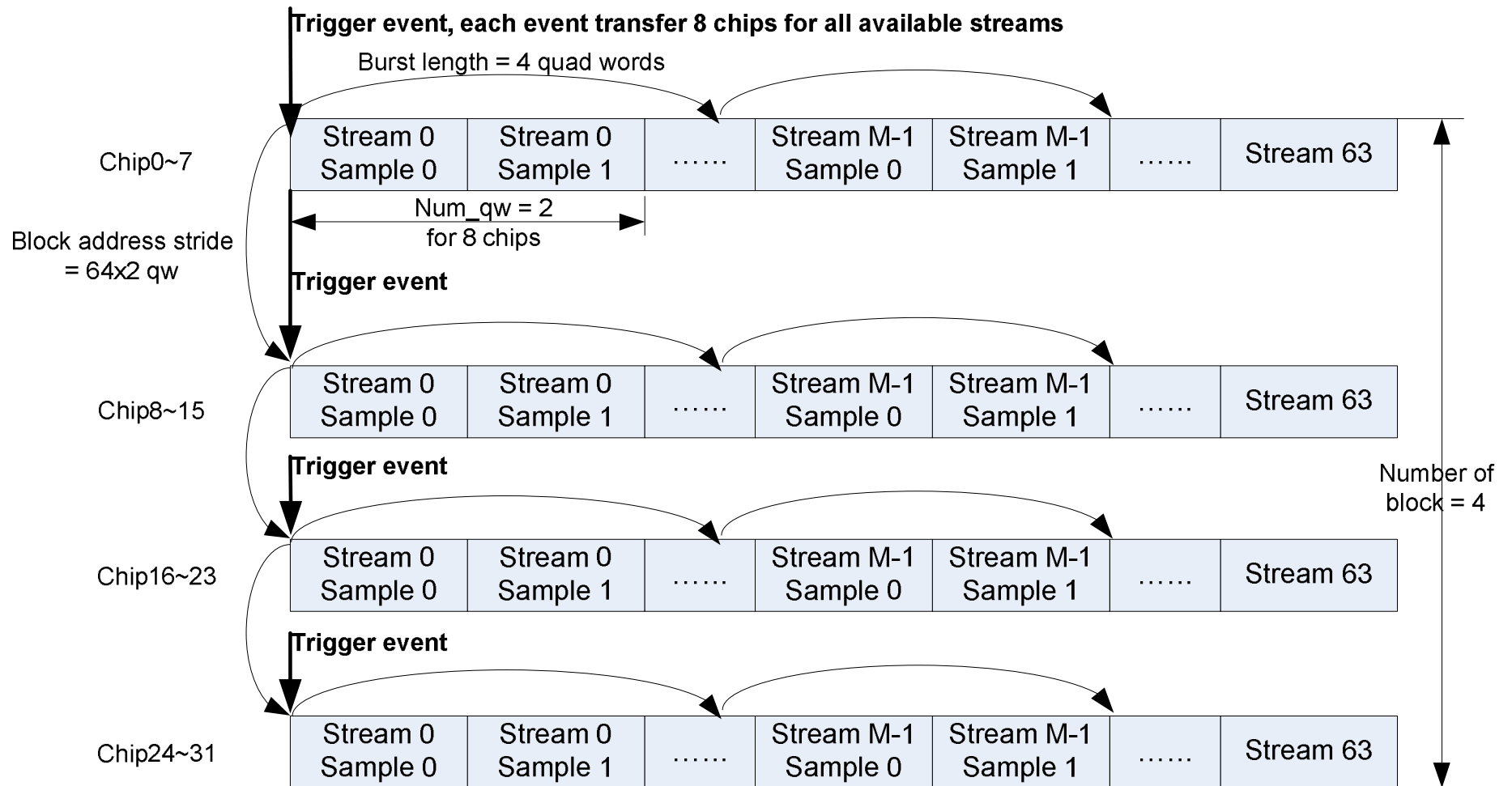
- All DIO channel buffer length must be same, while PacketDMA mode support different buffer length for each channel
- Some configuration register fields should be configured with expected value minus one. For example, if you want to support 4 AxC, the num_axc field should be set as $4-1 = 3$.

RAC antenna data buffer structure



- The RAC input buffer is a circular buffer which can hold 32 chips of data for each stream.
- The RAC supports 54 streams, but the buffer is organized for the size of 64 streams, the location for stream 54~63 are not used.
- DIO is triggered every 8 chips for antenna data transferred to RAC. DIO transfers 8 chips for multiple streams with each trigger event.

DIO transfer to RAC



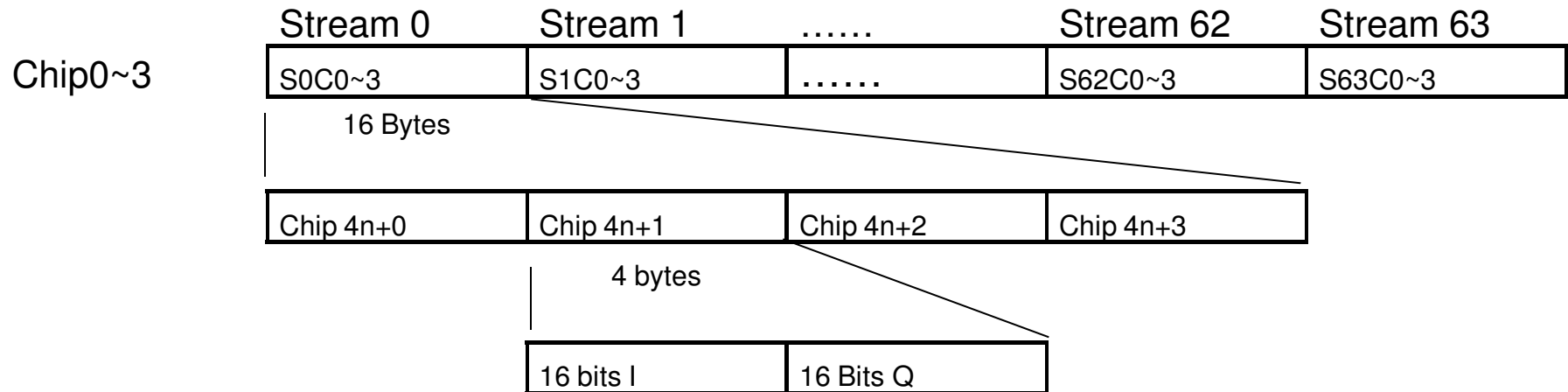
DIO configuration for RAC

Parameters	Configuration	Comments
Number of Quad word per AxC	2	Corresponding to 8 chips
Number of AxC	≤ 54	Support maximum 54 antenna streams per RAC.
Number of blocks	4	$4 \times 8 = 32$ chips this is the size of RAC input buffer.
DMA burst length	4 quad words	One burst include data of two antennas
burst address stride	4 quad words	
block address stride	64×2 quad words	

•Please note, the read and write operations of DIO engine are independent. Actually, num_qw specifies the minimal size of DIO accessing AIF2 buffer; burst length specifies the minimal size of DIO accessing RAC buffer. So, with above configuration, num_qw = 2 and burst length = 4, the DIO operations include:

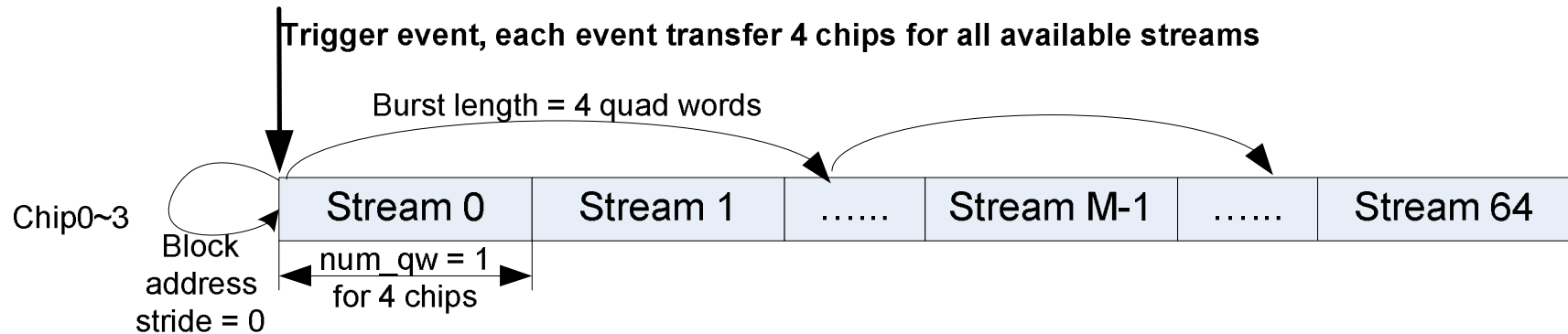
- DIO reads 2 quad words from the first AIF2 antenna channel buffer
- DIO reads 2 quad words from the second AIF2 antenna channel buffer
- DIO combines the 4 quad words and writes them to the RAC buffer.

TAC antenna data buffer structure



- The TAC supports 64 streams.
- The TAC buffer is a circular buffer which can only hold 4 chips of data for each stream.
- DIO is triggered every 4 chips for antenna data transferred from TAC. DIO transfers 4 chips for multiple streams with each trigger event.

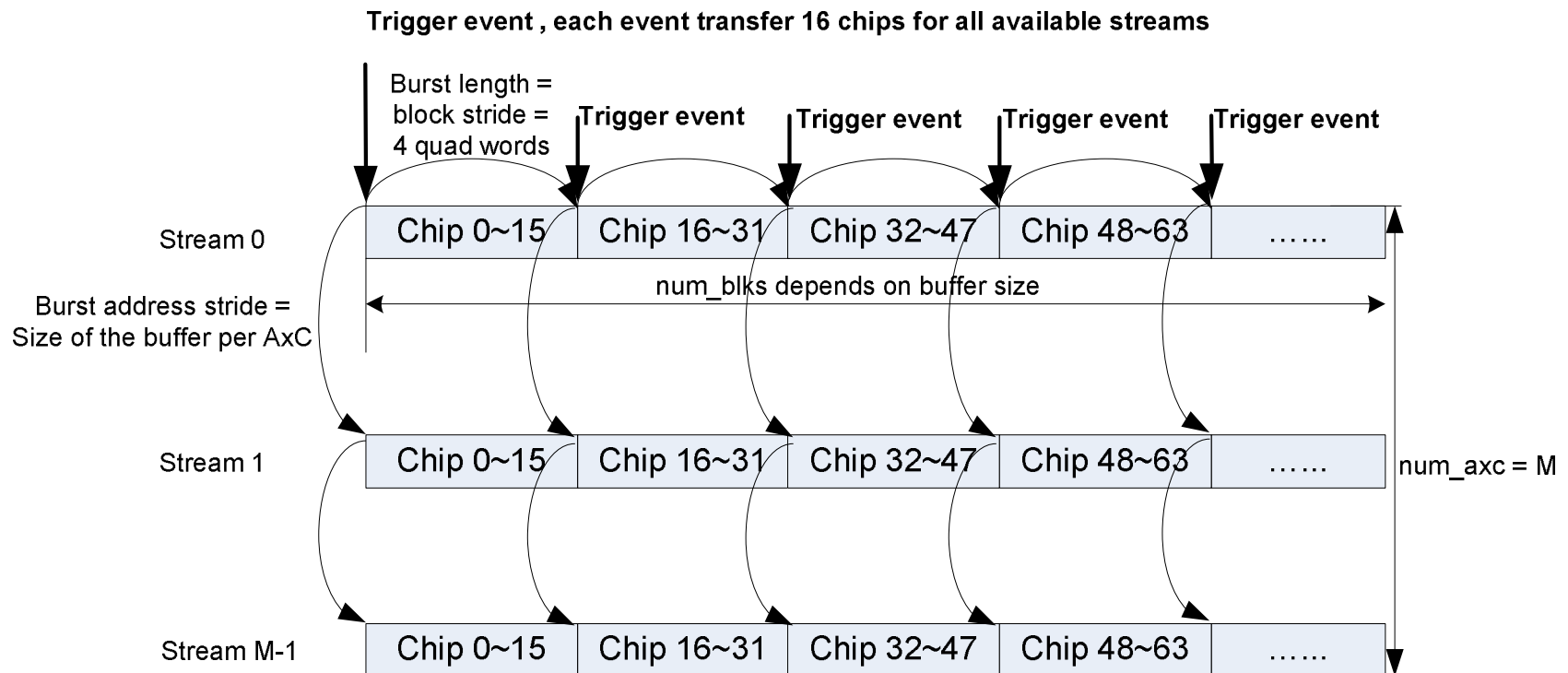
DIO configuration for TAC



Parameters	Configuration	Comments
Number of Quad word per AxC	1	Corresponding to 4 chips
Number of AxC	≤ 64	Support maximum 64 antenna streams per TAC.
DMA burst length	4 quad words	One burst include data of 4 antennas
burst address stride	4 quad words	
block address stride	0	Wrap around to the beginning after every transfer
Number of blocks	32	Since block stride =0 any value for this field should be OK. But a relative larger number may reduce average DIO overhead.

Customized antenna data buffer in DSP memory

- For antenna stream be processed by DSP core or RSA (Rake Search Accelerator), the antenna data structure in DSP memory can be freely defined by software. Above buffer structure for RAC and TAC can also be used, but those structures interleave antenna streams, which is not good for DSP core to process them efficiently. A typical structure is to collect antenna data for each stream into separate buffers.



DIO configuration for antenna buffer in DSP memory

- For this case, the period of DIO trigger event can also be freely configured. The largest period, 16 chips, can be used to improve the throughput because the largest burst size can be utilized.

Parameters	Configuration	Comments
Number of Quad word per AxC	4	Corresponding to 16 chips
Number of AxC	≤ 64	Support maximum 64 antenna streams per DIO.
Number of blocks	≤ 8192	num_blks is a 13-bit field. So, the maximum buffer size is limited to $8192 \times 16 = 131072$ chips ≈ 3.4 frames
DMA burst length	4 quad words	One burst include data of 4 antennas
burst address stride	Size of the buffer per AxC	brst_addr_stride is a 12-bit field. So the maximum buffer size is limited to $4096 \times 4 = 16384$ chips ≈ 6.4 WCDMA slots ≈ 0.43 frames
block address stride	4 quad words	

Q&A

Ten multiple choice questions from Part-2

1. Choose all true statements for AIF2 Serdes:

- A. Internal loopback is supported
- B. Scrambling is supported for 8x OBSAI link and 8x CPRI link
- C. receivers integrate 100 ohm termination and internal biasing of $0.7 \cdot V_{DDT}$
- D. Each link can use different link rate

2. With 122.88MHz reference clock input, how to configure Serdes PLL and rate scale to achieve CPRI 8x link rate

- A. $122.88 \times 10(\text{MPY}) \times 4(\text{Rate scale}) = 4915.2\text{Mbps}$
- B. $122.88 \times 20(\text{MPY}) \times 2(\text{Rate scale}) = 4915.2\text{Mbps}$
- C. $122.88 \times 25(\text{MPY}) \times 2(\text{Rate scale}) = 6144\text{Mbps}$
- D. $122.88 \times 40(\text{MPY}) \times 1(\text{Rate scale}) = 4915.2\text{Mbps}$

3. Choose all true statements for AIF2 Timer:

- A. Both PHYT and RADT can be triggered by PHYT_SYNC pulse
- B. PHYT includes 22-bit clock counter and 40-bit frame counter; RADT includes 19-bit clock counter, 8-bit symbol counter, and 40-bit frame counter
- C. The timer events for DSP core interrupt must be triggered by RADT
- D. Timer event offset can be larger than event MOD (period)

Ten multiple choice questions from Part-2

4. **AIF2 Timer clock TC LUT (Terminal Count Look up Table) is really required to generate timing events for:**
- A. WCDMA slot events
 - B. TD-SCDMA slot events
 - C. LTE normal symbol events
 - D. LTE extended symbol events
5. **Choose all true statements for AIF2 synchronization:**
- A. Synchronization pulse should be generated from the same source as the AIF2 Serdes reference clock.
 - B. Delta is downlink timing offset when TM begins transfer; PI is uplink timing offset when RM begins receiving.
 - C. Downlink AxC offset is timing offset when PE begins transfer valid antenna data and, uplink AxC offset is timing offset when PD begins receive valid antenna data.
 - D. Reference point of AxC offset is PHYT frame boundary

Ten multiple choice questions from Part-2

6. Choose all true statements for AIF2 PD/PE:

- A. Modulo rules can be used with AIF2 CPRI mode. So, one link can carrier both WCDMA streams and LTE streams.
- B. Each link uses separate DBM rules. So, one link can carrier WCDMA streams, while the other link supports LTE streams.
- C. AIF2 support up to 6 radio frame formats. So, one channel can carrier a WCDMA stream, while the other channel supports a LTE stream.
- D. Each link has a mapping table with 256 entries to map the 256 control words of a CPRI Hyper frame to 4 control data channels.

7. Choose all true statements for AIF2 DB/AD:

- A. 16KB DB RAM shared by up to 128 channels, buffer length of each channel can be different with Packet DMA mode.
- B. One AxC channel can use PacketDMA, while the other AxC channel use DIO mode.
- C. Non-AxC channel (Control channels, generic data channels) always use PktDMA, even AxC channels use DIO mode.
- D. Maximum AIF2 DMA burst size is 64 bytes.

Ten multiple choice questions from Part-2

8. How many channels supported by AIF2 packet DMA:

- A. 64
- B. 128
- C. 129
- D. 256

9. How many channels supported by one AIF2 DIO engine:

- A. 32
- B. 54
- C. 64
- D. 128

10. Choose the true statement for AIF2 DIO:

- A. DIO burst size must be same as number QW per AxC
- B. Each DIO engine is trigger by corresponding DIO events from AIF2 timer. With each trigger event, the DIO engine transfers a block of (number of quad word) x (number of AxC).
- C. The trigger event period for TAC and RAC is 8 chips.