Device Affected: KeystoneI & KeystoneII

Revisions Affected: All current revisions of silicon.

Problem Overview

If connect the DSP to PHY, after reset the PHY or unplug Ethernet cable a couple of times, though the SGMII status is OK, the packet can not be sent out from DSP. Found two possible situations in the field:

A. The Carrier Sense Errors Register (TXCARRIERSENSEERRORS) of CPSW statistics B module is increasing with the sent packet.

B. No any error register has been set on CPSW statistics B module with small TX traffic, meanwhile the RX side is OK. Increasing the TX traffic to send totally more than 68K bytes, Px_BLK_CNT (Px means the corresponding CPSW port which connect to the PHY) register value will reach Px_TX_MAX_BLKS of Px_MAX_BLKS register. Continue to output the traffic, there are some descriptors stuck in packet DMA queue No.648.

Investigation Details

1. After unplug Ethernet cable

Check SGMII STATUS register, the AN_ERROR bit of SGMII_STATUS register is 1 ,maybe with LINK bit of SGMII_STATUS register set to 0. Link Partner Advertised Ability Register (MR_LP_ADV_ABILITY) change to 0x4001 or other invalid value.

Or after reset the PHY

Continue to poll SGMII STATUS register, the AN_ERROR bit of SGMII_STATUS register is 1, maybe with LINK bit of SGMII_STATUS register set to 0. Link Partner Advertised Ability Register (MR_LP_ADV_ABILITY) change to 0x4001 or other invalid value.

2. After plug Ethernet cable again or waiting for a while after reset the PHY

The AN_ERROR bit of SGMII_STATUS register is 0, LINK bit of SGMII_STATUS register set to 1. Link Partner Advertised Ability Register (MR_LP_ADV_ABILITY) reflects to the correct value as the negotiation result of remote media.

In TI keystone I Ethernet subsystem user guide, it said
Sprugv9a: *The gigabit Ethernet (GbE) switch subsystem does not support 1000 MHz half duplex mode*

And the AN_ERROR bit means PHY issue 1000M half duplex negotiation request to CPSGMII of DSP. **TI does NOT guarantee CPSGMII/CPGMAC will work OK after receive 1000M half duplex negotiation request, even the final negotiation result is NOT 1000M half duplex. The behavior of CPSGMII/CPGMAC in this scenario is indeterminate.**

Table 3-9 Status Register (STATUS) Field Descriptions (Part 1 of 2)

Bits	Field	Description
31-5	Reserved	Reserved
4	LOCK	Lock. This is the LOCK input pin. Indicates that the SerDes PLL is locked.
3	Reserved	Reserved
2	MR_AN_COMPLETE	Auto-negotiation complete. This value is not valid until the LOCK status bit is asserted. 0 = auto-negotiation is not complete. 1 = auto-negotiation is completed.
1	AN_ERROR	Auto-negotiation error. For SGMII mode, an auto-negotiation error occurs when halfduplex gigabit is commanded. This value is not valid until the LOCK status bit is asserted. 0 = no auto-negotiation error. 1 = auto-negotiation error.
0	LINK	Link indicator. This value is not valid until the LOCK status bit is asserted. 0 = Link is not up. 1 = Link is up.
End of Table 3-9		

Workaround

Configure the PHY through MDIO interface to disable 1000M half duplex capability and do NOT negotiate 1000M half duplex on SGMII side. The target is after reset the PHY or unplug Ethernet cable, the AN_ERROR bit of SGMII_STATUS register is always 0 and the LINK bit of DSP SGMII_STATUS register is always 1 （Note, after unplug Ethernet cable or during the PHY reset, Copper Link status of PHY register 1_0.2 should be link down）. Below is the register configuration example for Marvell PHY, 88E1111, 88E1322 and 88E1512 etc.

1000BASE-T Control Register

Page 0, Register 9

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Test Mode	R/W	0x0	Retain	TX_CLK comes from the RX_CLK pin for jitter testing in test modes 2 and 3. After exiting the test mode, hardware reset or software reset (Register 0_0.15) should be issued to ensure normal operation. A restart of Auto-Negotiation will clear these bits. 000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 101, 110, 111 = Reserved
12	MASTER/SLAVE Manual Configu-ration Enable	R/W	0x0	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration
11	MASTER/SLAVE Configuration Value	R/W	See Descr.	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. Upon hardware reset this bit takes on the value of SEL_MS. 1 = Manual configure as MASTER 0 = Manual configure as SLAVE
10	Port Type	R/W	See Descr.	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. Register 9_0.10 is ignored if Register 9_0.12 is equal to 1. Upon hardware reset this bit takes on the value of SEL_MS. 1 = Prefer multi-port device (MASTER) 0 = Prefer single port device (SLAVE)
9	1000BASE-T Full-Duplex	R/W	0x1	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
8	1000BASE-T Half-Duplex	R/W	See Descr.	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. Upon hardware reset this bit takes on the value of C_ANEG[0]. 1 = Advertise 0 = Not advertised
7:0	Reserved	R/W	0x00	Retain	0

Configure the PHY register 9_0.8 to 0, which means 1000Mbps half duplex will not be advertised to the remote side which connects to the copper media of this PHY. This step will make sure that the copper side of PHY will not negotiate 1000Mbps half duplex capability with remote media. (Note, some of the PHY has hardware configure PIN to configure this function)

MAC Specific Control Register 2
Page 2, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	0x0	0
14	Copper Line Loopback	R/W	0x0	0x0	1 = Enable Loopback of MDI to MDI 0 = Normal Operation
13:12	Reserved	R/W	0x1	Update	1
11:7	Reserved	R/W	0x00	0x00	00000
6	Reserved	R/W	0x1	Update	1
5:4	Reserved	R/W	0x0	Retain	0
3	Block Carrier Extension Bit	R/W	0x0	Retain	1 = Enable Block Carrier Extension 0 = Disable Block Carrier Extension
2:0	Default MAC interface speed	R/W	0x6	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. MAC Interface Speed during Link down while Auto-Negotiation is enabled. Bit Speed 0XX = Reserved 100 = 10 Mbps 101 = 100 Mbps 110 = 1000 Mbps 111 = Reserved

Configure the PHY register 21_2.2:0 to 01, which means 100Mbps. This step will make sure when the Fiber/SGMII side of PHY status switch between link up and link down, it will not issue 1000M half duplex request to CPSGMII module of the DSP. (Note, this configuration will NEVER force the link rate to 100Mbps, the link rate depends on the final negotiation result)

If above configuration can NOT make progress for solving the problem:

1. Make sure the PHY is initialized correctly, be careful to check data sheet and release note of the PHY. For example, some Marvell PHYs have important initialization steps in the Errata part of the release note.
2. For multi-port PHY, above two registers maybe belong to different port, be careful to configure the register and issue the PHY software reset to the correct port. For example, when connect KeystoneI& KeystoneII to Marvell 88E1512 (four ports PHY), if the 88E1512 configures to *SGMII to Copper mode*, you should issue a software reset to port 0 after configure register 9_0 of port 0 and also issue a software reset to port 1 after configure register 21_2.2:0 of port 1.

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