TMS320DM36x Digital Media System-on-Chip (DMSoC)
Video Processing Front End (VPFE)

User's Guide

Literature Number: SPRUFG8C
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About This Manual

This document describes the operation of the Video Processing Front End in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM36x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the internet at www.ti.com.

SPRUFG5 — *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* This document describes the ARM Subsystem in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the components of the ARM Subsystem, the peripherals, and the external memories.

SPRUFG8 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Front End (VPFE) Users Guide* This document describes the Video Processing Front End (VPFE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFG9 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Back End (VPBE) Users Guide* This document describes the Video Processing Back End (VPBE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH0 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) 64-bit Timer Users Guide* This document describes the operation of the software-programmable 64-bit timers in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH1 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Serial Peripheral Interface (SPI) Users Guide* This document describes the serial peripheral interface (SPI) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

SPRUFH2 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Asynchronous Receiver/Transmitter (UART) Users Guide* This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

SPRUFH3 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Inter-Integrated Circuit (I2C) Peripheral Users Guide* This document describes the inter-integrated circuit (I2C) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus.

SPRUFH5 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Multimedia Card (MMC)/Secure Digital (SD) Card Controller Users Guide* This document describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH6 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Pulse-Width Modulator (PWM) Users Guide* This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH7 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Real-Time Out (RTO) Controller Users Guide* This document describes the Real Time Out (RTO) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH8 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) General-Purpose Input/Output (GPIO) Users Guide* This document describes the general-purpose input/output (GPIO) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

SPRUFH9 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Serial Bus (USB) Controller Users Guide* This document describes the universal serial bus (USB) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices and also supports host negotiation.

SPRUFI0 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Users Guide* This document describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EDMA controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DMSoC.

SPRUFI1 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Asynchronous External Memory Interface (EMIF) Users Guide* This document describes the asynchronous external memory interface (EMIF) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EMIF supports a glueless interface to a variety of external devices.

SPRUFI2 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) DDR2/Mobile DDR (DDR2/mDDR) Memory Controller Users Guide* This document describes the DDR2/mDDR memory controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM and mobile DDR devices.

SPRUFI3 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Multibuffered Serial Port Interface (McBSP) User's Guide* This document describes the operation of the multibuffered serial host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The primary audio modes that are supported by the McBSP are the AC97 and IIS modes. In addition to the primary audio modes, the McBSP supports general serial port receive and transmit operation.

SPRUFI4 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Host Port Interface (UHPI) User's Guide* This document describes the operation of the universal host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI5 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Ethernet Media Access Controller (EMAC) User's Guide* This document describes the operation of the ethernet media access controller interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI7 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Analog to Digital Converter (ADC) User's Guide* This document describes the operation of the analog to digital conversion in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI8 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Key Scan User's Guide* This document describes the key scan peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI9 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Voice Codec User's Guide* This document describes the voice codec peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). This module can access ADC/DAC data with internal FIFO (Read FIFO/Write FIFO). The CPU communicates to the voice codec module using 32-bit-wide control registers accessible via the internal peripheral bus.

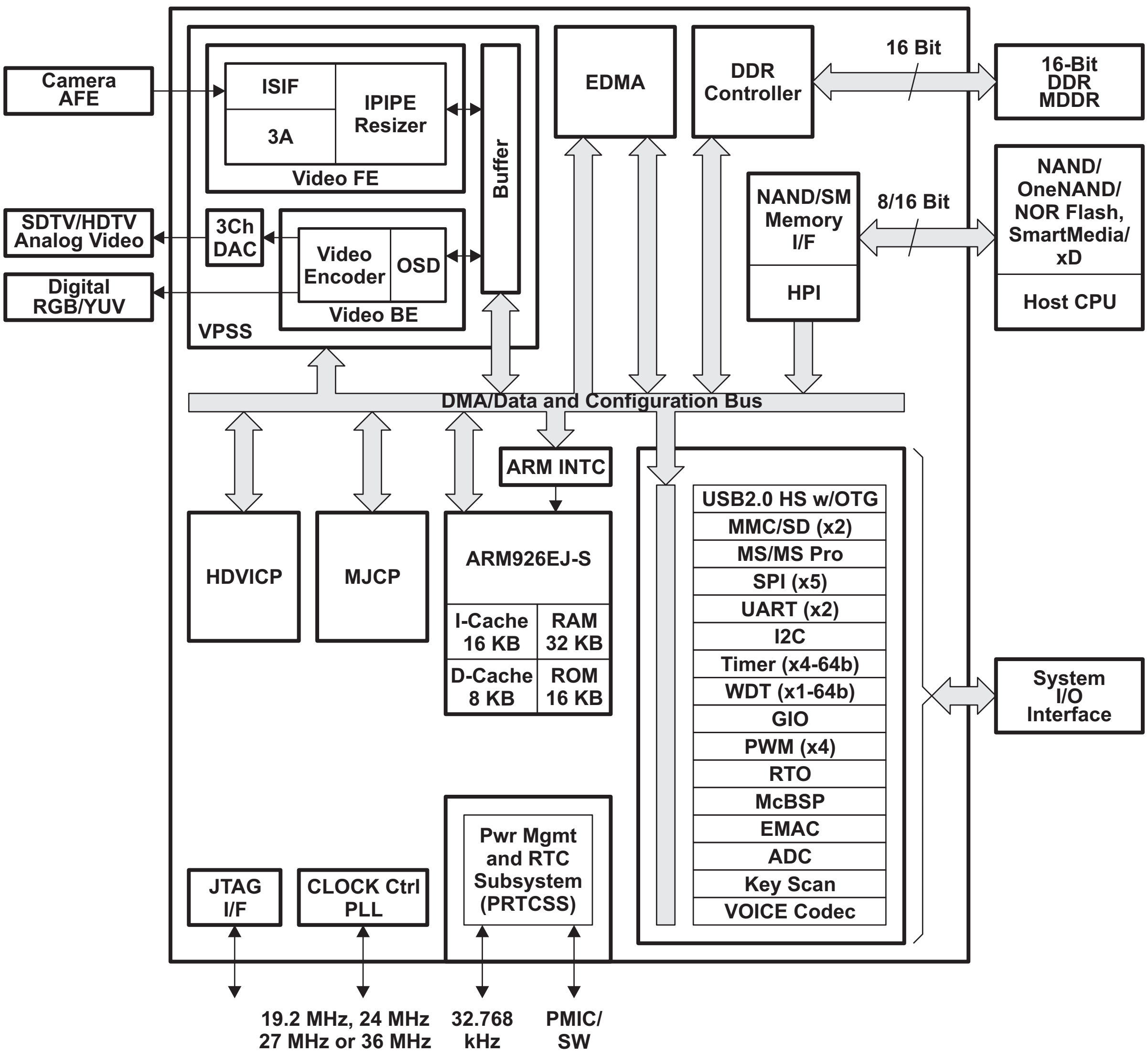
SPRUFJ0 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Power Management and Real-Time Clock Subsystem (PRTCSS) User's Guide* This document provides a functional description of the Power Management and Real-Time Clock Subsystem (PRTCSS) in the TMS320DM36x Digital Media System-on-Chip (DMSoC) and PRTC interface (PRTCIF).

SPRUGG8 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Face Detection User's Guide*This document describes the face detection capabilities for the TMS320DM36x Digital Media System-on-Chip (DMSoC).

Video Processing Front End Overview

The TMS320DM36x Digital Media System-on-Chip (DMSoC) contains video processing HW to manage video data and to free the main processor to perform other jobs. This device enables seamless interface to most additional external devices required to get video data via the Video Processing Front End Subsystem (VPFE). The interface is flexible enough to support various types of CCD and CMOS sensors, signal conditioning circuits, power management, SDRAM, SRAM, shutter, Iris and auto-focus motor controls. A block diagram of this device is shown in Figure 1-1.

Figure 1-1. Functional Block Diagram

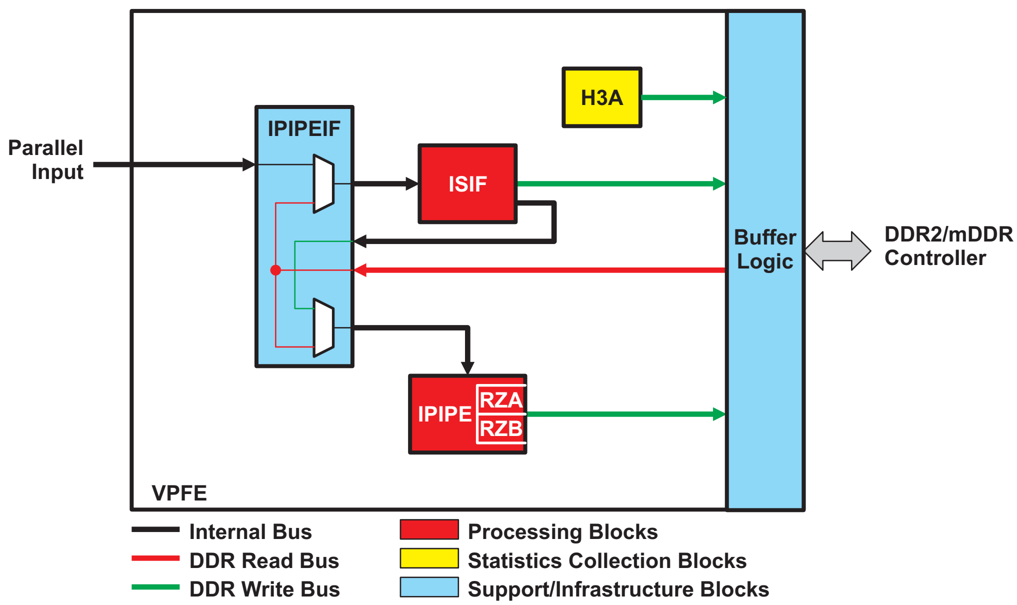


1.1 Purpose of the Video Processing Front End

The device contains a Video Processing Subsystem (VPSS), Figure 1-2, that provides an input interface (Video Processing Front End or VPFE) for external imaging peripherals such as image sensors, video decoders, etc.; and an output interface (Video Processing Back End or VPBE) for display devices, such as analog SDTV displays, digital LCD panels, and HDTV video encoders to name a few.

In addition to these peripherals, there is a set of common buffer memory and DMA controls to ensure efficient use of the DDR2/mDDR controller burst bandwidth. The buffer logic/memory is a unique block that is tailored for seamlessly integrating the VPSS into an image/video processing system. It acts as the primary source or sink to all the VPFE and VPBE modules that are either requesting or transferring data from/to DDR2/mDDR controller. In order to efficiently utilize the external DDR2/mDDR controller bandwidth, the buffer logic/memory interfaces with the DMA system via a high bandwidth bus (64-bit wide). The buffer logic/memory (divided into the read and write buffers and arbitration logic) is capable of performing the following functions. It is imperative that the VPSS utilize DDR2/mDDR controller bandwidth efficiently due to both its large bandwidth requirements and the real-time requirements of the VPSS modules.

Figure 1-2. Video Processing Subsystem (VPSS) Block Diagram



1.2 Features

The VPFE block is comprised of the Image Sensor Interface (ISIF), Image Pipe (IPIPE), Image Pipe Interface (IPIPEIF), and Hardware 3A Statistic Generator (H3A). Together, these modules provide the device with a powerful and flexible front-end interface. These modules can be broken down into three distinct types. The first type consists of major processing modules that are in the direct data flow path and affect the input image data stream. These are described below:

- The image sensor interface (ISIF) provides an interface to image sensors and digital video sources.
- The image pipe (IPIPE) is a parameterized hardwired image processing block whose image processing functions can be customized for each sensor type to realize good still image quality as well supporting video frame rates for digital still camera preview displays and video recording modes. An image resizer is also fully integrated within this module. Additionally, the IPIPE contains the following statistic collection functions: histogram, boxcar and the boundary signal calculator.

The second group of modules are support or infrastructure modules. They are in the direct data flow path and affect the input image data, but are mainly intended to extend the functionality of the aforementioned major processing modules.

- The image IPIPE interface (IPIPEIF) module is an extension to the input interface to the ISIF and IPIPE modules. It can receive data from the sensor input, ISIF, and SDRAM. It performs some additional preprocessing operations on the data, and sends the resultant data to the ISIF and IPIPE.

In addition to the modules that directly affect input image data, there is one independent module that provides statistics on the incoming images to aid designers of camera systems.

- The hardware 3A (H3A) module is designed to support the control loops for auto focus (AF), auto white balance (AWB) and auto exposure (AE) by collecting metrics on the RAW image data from the image sensor interface (ISIF).

1.2.1 Image Sensor Interface (ISIF)

The ISIF is responsible for accepting RAW (unprocessed) image/video data from a sensor (CMOS or CCD). In addition, the ISIF can accept YCbCr video data in numerous formats, typically from so-called video decoder devices. In the case of RAW inputs, the ISIF output requires additional image processing to transform the RAW input image to the final processed image. This processing can be done in the image pipe (IPIPE). The ISIF is programmed via control and parameter registers.

The ISIF module supports the following features:

- Conventional Bayer pattern, movie mode (e.g. Panasonic/Sony), and Foveon sensor formats
- Various movie mode formats is provided via a data reformatter of ISIF, which transforms any specific sensor formats to the Bayer format. The maximum line width supported by the reformatter is 4736 pixels.
- Image processing steps applicable to Foveon sensors are limited to color-dependent gain control and black level offset control
- Progressive and interlaced sensors (hardware support for up to 2 fields and firmware support for higher number of fields, typically 3-, 4-, and 5-field sensors)
- Generates HD/VD timing signals and field ID to an external timing generator, or can synchronize to the external timing generator
- Up to 32K pixels (image size) in both the horizontal and vertical direction
- Up to 120 MHz sensor clock
- ITU-R BT.656/1120 standard format
- YCbCr 422 format, either 8- or 16-bit with discrete H and VSYNC signals
- Up to 16-bit input
- Color space conversion
- Digital clamp with horizontal/vertical offset drift compensation
- Vertical Line defect correction based on a lookup table that contains defect position
- Color-dependent gain control and black level offset control
- Ability to control output to the SDRAM via an external write enable signal
- Down sampling via programmable culling patterns

- 12-bit to 8-bit DPCM compression
- 10-bit to 8-bit A-law compression
- Generating output to range 16-bits, 12-bits (12bit data pack allows for 33% saving in storage area), and 8-bits wide (8-bits wide allows for 50% saving in storage area).

1.2.2 The Image Pipe Interface (IPIPEIF)

The IPIPEIF is data and sync signals interface module for ISIF and IPIPE. Data source of this module is sensor parallel port, ISIF or SDRAM and the selected data is output to ISIF and IPIPE. This module also outputs dark frame subtraction (two-way) data which is generated by subtracting SDRAM data from sensor parallel port or ISIF data and vice versa. Depending on the functions performed, it may also readjust the HD, VD, and PCLK timing to the IPIPE and/or ISIF input.

The IPIPEIF module supports the following features:

- Up to 16-bit sensor data input
- Dark-frame subtract of raw image stored in SDRAM from image coming from sensor parallel port or ISIF
- 8-10, 8-12 DPCM decompression of 10-8, 12-8 DPCM compressed data from SDRAM
- Inverse ALAW decompression of RAW data from SDRAM
- (1,2,1) average filtering before horizontal decimation
- Horizontal decimation (downsizing) of input lines to <=2176 maximum required by the IPIPE
- Gain multiply for output data to IPIPE
- Simple defect correction to prevent a subtraction of defect pixel
- 8-bit, 12-bit unpacking of 8-bit, 12-bit packed SDRAM data

1.2.3 Image Pipe – Hardware Image Signal Processor (IPIPE)

The Image Pipe (IPIPE) is a programmable hardware image processing module that generates image data in YCbCr-4:2:2 or YCbCr-4:2:0 formats from raw CCD/CMOS data. The IPIPE can also be configured to operate in a resize-only mode, which allows YCbCr-4:2:2 or YCbCr-4:2:0 to be resized without processing every module in the IPIPE.

The following features are supported by the IPIPE:

- 12-bit RAW data image processing or 16-bit YCbCr resizing
- RGB Bayer pattern for input color filter array; does not support complementary color pattern, stripe pattern, nor Foveon sensors.
- Requires at least eight pixels for horizontal blanking and four lines for vertical blanking. In one shot mode, 16 blanking lines after processing area are required.
- Maximum horizontal and vertical offset of IPIPE processing area from synchronous signal is 65534
- Maximum input and output widths up to 2176 pixels wide (1088 for RSZ[2]).
- Raw pass-through mode for images can be wider than 2176 pixels (up to 8190 pixels)
- Automatic mirroring of pixels/lines when edge processing is performed so that the width and height is consistent throughout.
- Defect pixel correction using
  – Lookup table method that contains row and column position of the pixel to be corrected
  – On-the-fly adaptive method
- Offset and gain control for white balancing at each color component (WB).
- CFA interpolation for good quality CFA interpolation with reduced false color artifacts (CFA module). CFA module also reduces aliasing caused by under sampling by Digital Anti Aliasing (DAA).
- Programmable RGB to RGB blending matrix (9 coefficients for the 3x3 matrix). (RGB2RGB module)
- Separate lookup tables for gamma correction on each of R, G and B components for display through piece-wise linear interpolation approach.
- 4:4:4 data to 4:2:2 data conversion by chroma low-pass filtering and down sampling to Cb and Cr. (4:4:4 to 4:2:2 module)
- Programmable look-up table for luminance edge enhancement. Adjustable brightness and contrast for

Y component (Edge Enhancer module)

- Programmable down or up-sampling filter for both horizontal and vertical directions with range from 1/16x to 16x, in which the filter outputs two images with different magnification simultaneously (Resizer module)
- 4:2:2 to 4:2:0 conversion that can be done in the resizing block
- Different data formats [YCbCr (4:2:2 or 4:2:0), RGB (32bit/16bit), Raw data] are available while storing data in the SDRAM from IPIPE
- Flipping image horizontally and/or vertically
- Programmable histogram engine (4 windows, 256 bins)
- Boxcar calculation (1/8 or 1/16 size in each direction).

1.2.4 Hardware 3A (H3A)

The H3A module is designed to support the control loops for auto focus, auto white balance, and auto exposure by collecting metrics about the imaging/video data. The metrics are to adjust the various parameters for processing the imaging/video data. There are two main blocks in the H3A module:

- Auto focus engine
- Auto exposure and auto white balance engine

The AF engine extracts and filters the red, green, and blue data from the input image/video data and provides either the accumulation or peaks of the filtered output in a specified region. The specified region is a two-dimensional block of data and is referred to as a paxel when used with the auto focus engine (AF).

The AE/AWB engine accumulates the values and checks for saturated values in a sub-sampling of the video data. When used with the AE/AWB, the two-dimensional block of data is referred to as a window. Thus, other than referring them by different names, a paxel and a window are essentially the same thing. However, the number, dimensions, and starting position of the AF paxels and the AE/AWB windows are separately programmable.

1.2.4.1 Auto Focus Engine Features

The following features are supported by the AF engine:

- Peak mode in a paxel (a paxel is defined as a two dimensional block of pixels).
  - Accumulates the maximum focus value of each line in a paxel
- Accumulation/sum mode (instead of peak mode)
- Accumulates horizontal and vertical focus value in a paxel
- Focus value can be absolute value or square of the filter output
- Up to 12 paxels in the horizontal direction and up to 12 paxels in the vertical direction with vertical focus
- Up to 36 paxels in the horizontal direction and up to 128 paxels in the vertical direction with horizontal focus only
- Programmable width and height for the paxel. All paxels in the frame will be of the same size.
- Separate horizontal start for paxel and filtering
- Programmable vertical/horizontal steps within a paxel (vertical steps for vertical FV, horizontal steps for horizontal FV)

1.2.4.2 Auto Exposure and Auto White Balance Features

The following features are supported by the AE/AWB engine:

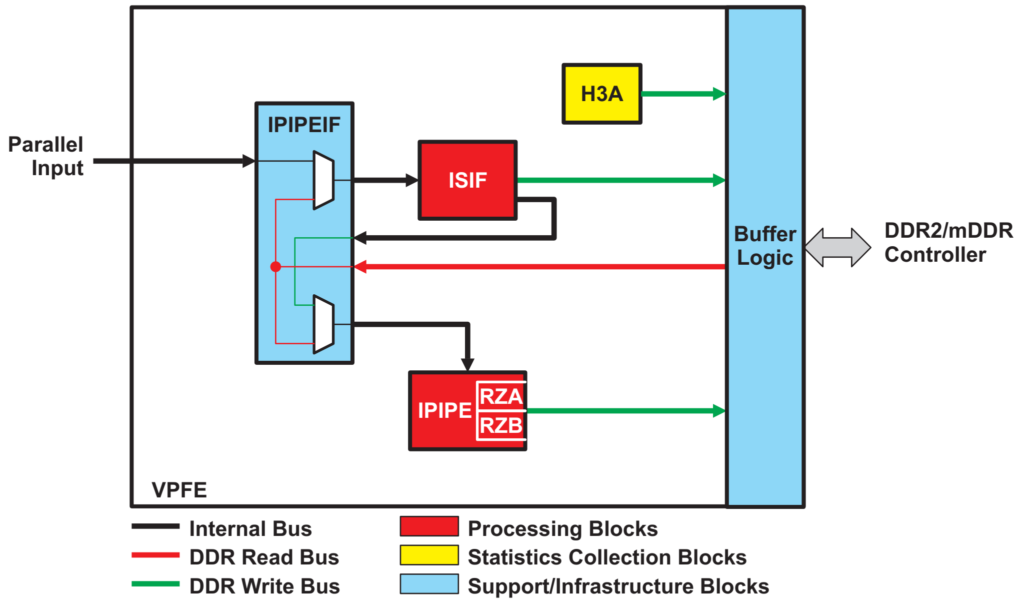
- Accumulates clipped pixels along with all non-saturated pixels in each window per color
- Accumulates the sum of squared pixels in each window per color
- Minimum and maximum pixels values in each window per color
- Up to 36 horizontal windows with sum + {sum of squares or min+max} output.
- Up to 56 horizontal windows with sum output
- Up to 128 vertical windows

- Programmable width and height for the windows. All windows in the frame will be of same size.
- Separate vertical start coordinate and height for a black row of paxels that is different than the remaining color paxels
- Programmable horizontal sampling points in a window
- Programmable vertical sampling points in a window

1.3 Functional Block Diagram

Figure 1-3 shows a high-level functional block diagram of the VPFE functional blocks, along with the different data flow paths. These data flow paths show how the various modules of the VPFE interact. The ISIF can also read the data from SDRAM via the IPIPEIF. The input to the H3A is only RAW sensor image data. The input to the IPIPE can be RAW or YCbCr video data.

Figure 1-3. Video Processing Front End (VPFE) Block Diagram and Data Flows



1.4 Supported Use Case Statement

The VPFE supports image data acquisition from sensor and digital video sources in various modes/formats. YCbCr sources have minimal image processing applied and can either be passed directly to external memory/SDRAM or passed through the IPIPE’s resizer for scaling prior to writing to the SDRAM. RAW image data modes (non-YCbCr sources) are supported by the statistics collection modules (H3A, IPIPE’s histogram, IPIPE's boundary signal calculator) as well as full image pipe processing functions, including resize.

The same processing options are supported when processing data sourced from the SDRAM. The IPIPEIF module can also perform dark frame subtraction on data from the SDRAM.

1.5 Industry Standard(s) Compliance Statement

ITU-R BT.601/656/1120

VPFE/ISP I/O Interfacing

This section addresses the configuration of any external connections that the VPFE/ISP may have at the interface of the device, including I/O signals lists, I/O pin multiplexing, and protocol/data formats for typical application(s).

The VPFE signals are shown in Table 2-1. Note that these signals can take on different meanings depending on the specific interface chosen. All of the digital input signals below are multiplexed as GIO signals at reset (not shown in Table 2-1), and some are also multiplexed as SPI3 and USB signals. Pin multiplexing is controlled from the System Module level register PINMUX0 (0x01C40000). The default value of the PINMUX0 register is 0x0, which indicates that all the VPFE-related pins in the register are used for video input purpose after reset. However, it is suggested to configure the PINMUX0 register to the value 0xXXXX0000, where X is don't care, before any video capture. The following sections describe each of the input interface scenarios supported.

Table 2-1. Interface Signals for Video Processing Front End

Pin Name	Muxed With	I/O	Description
PCLK		Input	Pixel Clock
VD	GIO94	Bidi	V sync
HD	GIO95	Bidi	H sync
YIN7	GIO103/SPI3_SCLK	Bidi	C IN signal / C_DATA [15]
YIN6	GIO102/SPI3_SDO	Bidi	C IN signal / C_DATA [14]
YIN5	GIO101/SPI3_SDENA[0	Bidi	C IN signal / C_DATA [13]
YIN4	GIO100/SPI3_SDI3/SPI3_SDENA[1]	Bidi	C IN signal / C_DATA [12]
YIN3	GIO99	Bidi	C IN signal / C_DATA [11]
YIN2	GIO98	Bidi	C IN signal / C_DATA [10]
YIN1	GIO97	Bidi	C IN signal / C_DATA [9]
YIN0	GIO96	Bidi	C IN signal / C_DATA [8]
CIN7		Input	C IN signal / C_DATA [7]
CIN6		Input	C IN signal / C_DATA [6]
CIN5		Input	C IN signal / C_DATA [5]
CIN4		Input	C IN signal / C_DATA [4]
CIN3		Input	C IN signal / C_DATA [3]
CIN2		Input	C IN signal / C_DATA [2]
CIN1		Input	C IN signal / C_DATA [1]
CIN0		Input	C IN signal / C_DATA [0]
C_WE_FIELD	GIO93/CLKOUT0/USBDRVVBUS	Bidi	CCD Write Enable/Field ID signal

2.1 Signal Interface for Different Input Data Formats

The ISIF (VPFE interfacing module with external parallel port video input) interface signals are listed in Table 2-4. The interface consists of a set of signals used to transfer raw sensor data from an imager to the ISIF. Additionally, the ISIF can be configured to operate in a mode that adheres to the ITU-R BT.601/656/1120 interface specification. The ITU-R BT.601/656/1120 specification provides a standard method to transfer YCbCr-4:2:2 formatted video data. The ISIF supports 8 to 16-bit wide RAW data signals and 8/16-bit YCbCr signals as shown in Table 2-2.

Table 2-2. Data Input Formats

Port Name	Sensor (16-bit Raw)	16-bit YCbCr	8-bit YCbCr	
YIN7	C_DATA15	Y7	Y7, Cb7, Cr7	(YCSWP = 1)
YIN6	C_DATA14	Y6	Y6, Cb6, Cr6	
YIN5	C_DATA13	Y5	Y5, Cb5, Cr5	
YIN4	C_DATA12	Y4	Y4, Cb4, Cr4	
YIN3	C_DATA11	Y3	Y3, Cb3, Cr3	
YIN2	C_DATA10	Y2	Y2, Cb1, Cr,1	
YIN1	C_DATA9	Y1	Y1,Cb1, Cr1	
YIN0	C_DATA8	Y0	Y0, Cb0, Cr0	
CIN7	C_DATA7	Cb7,Cr7	Y7,Cb7,Cr7	(YCSWP = 0)
CIN6	C_DATA6	Cb6,Cr6	Y6,Cb6,Cr6	
CIN5	C_DATA5	Cb5,Cr5	Y5,Cb5,Cr5	
CIN4	C_DATA4	Cb4,Cr4	Y4,Cb4,Cr4	
CIN3	C_DATA3	Cb3,Cr3	Y3,Cb3,Cr3	
CIN2	C_DATA2	Cb2,Cr2	Y2,Cb2,Cr2	
CIN1	C_DATA1	Cb1,Cr1	Y1,Cb1,Cr1	
CIN0	C_DATA0	Cb0,Cr0	Y0,Cb0,Cr0	

When the number of RAW data line is less than 16, data can be connected to the upper or lower lines of C_DATA[15:0]. Lines not connected should be tied low. As shown in Table 2-3, the GWDI register should be configured properly so that the MSB of the input is connected to the MSB of the 16-bit data bus in ISIF.

Table 2-3. RAW Data Connection

GWDI	16-bit data bus in ISIF
0	C_DATA[15:0]
1	C_DATA[14:0] & 0
2	C_DATA[13:0] & 00
3	C_DATA[12:0] & 000
4	C_DATA[11:0] & 0000
5	C_DATA[10:0] & 00000
6	C_DATA[9:0] & 000000
7	C_DATA[8:0] & 0000000
8	C_DATA[7:0] & 00000000

2.2 Typical ISIF Interface

The ISIF controls timing of the interface using the HD, VD, field ID, pixel clock, and write enable signals. The ISIF can either provide HD, VD, and field ID signals to the sensor or it can use the HD, VD, and field ID signals provided by the CCD imager. The pixel clock clocks data into the ISIF at a maximum rate of 120 MHz.

When the ISIF is configured to write data to SDRAM, the write enable signal allows an external device to control which data to be written to the SDRAM. To enable the filed ID input, bit-5 of the MODESET.SWEN register should be set to interlace mode. To enable the write enable signal, bit-7 of the MODESET.CCDMD register should be set.

Note: Since the field ID and the write enable signal share the same PIN, only one of them can be connected.

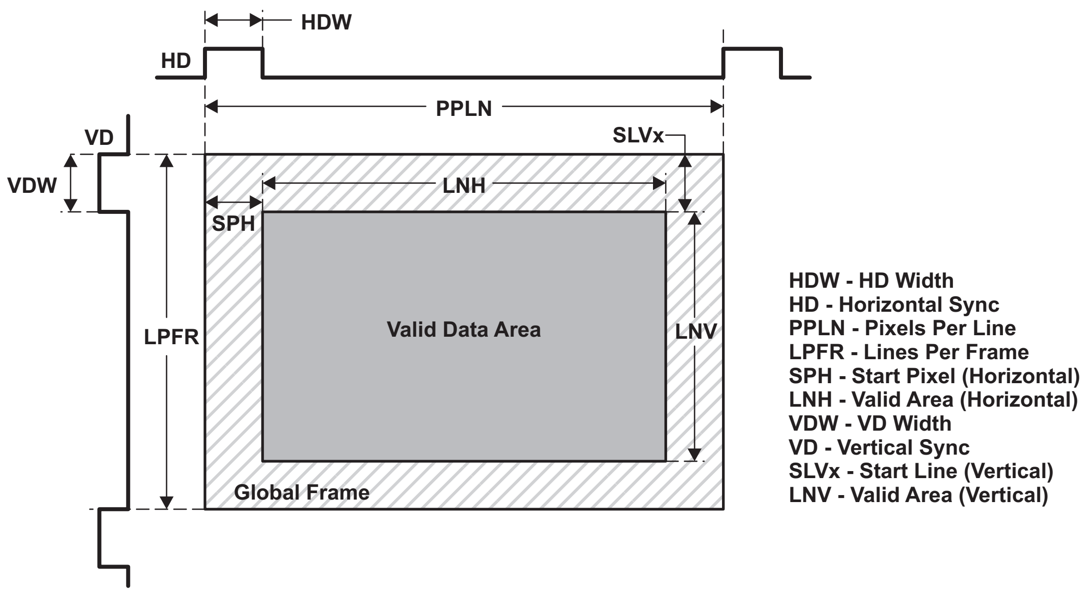
Table 2-4. ISIF Signal Interface

Name	I/O	Function
C_DATA[15:0]	I	Image data loaded from sensor. Bit width can be configured from 8 to 16 bits. The polarity of the input image data can be inversed by setting the MODESET.DPOL bit.
C_VSYNC (VD)	I/O	VSYNC. Vertical sync signal. This signal can be configured as an input or an output by setting MODESET.HDVDD bit. When configured as an input, the external sensor must supply the VD signal. When configured as an output the ISIF will supply the VD signal and VDW and LPFR registers must be configured. The polarity of VD can be inversed by setting the MODESET.VDPOL bit.
C_HSYNC (HD) INPUT	I/O	HSYNC. Horizontal sync signal. This signal can be configured as an input or an output by setting MODESET.HDVDD bit. When configured as an input, the external sensor must supply the HD signal. When configured as an output the ISIF will supply the HD signal and HDW and PPLN registers must be configured. The polarity of HD can be inversed by setting the MODESET.HDPOL bit.
C_FIELD	I/O	Field identification signal. This signal can be configured as an input or an output by setting MODESET.FIDD bit. When configured as an input, the external sensor must supply the field identification signal. When configured as an output, the ISIF will supply the field identification signal. When in input mode, the field ID can be configured to be latched by the VD signal. The polarity of the field ID can be inversed by setting the MODESET.FIPOL bit.
C_WEN	I	Write enable signal used to store valid frame data in SDRAM.
C_PCLK	I	Pixel clock. This signal is the pixel clock used to load image data into the ISIF. The Clock controller can configure to trigger on the rising or falling edge of the PCLK signal by setting the bit VPSS_CLK_CTRL.PCLK_INV in SYSTEM module registers. The maximum pixel clock rate is 120 MHz.

2.3 Timing Generator

The timing generator uses external sync signals (HD/VD) or provides internally generated timing signals to an imager. The CPU can control width, polarity, and position of the internally generated signals. Figure 2-1 shows ISIF register settings for the frame setup. The shaded area indicates the size of the physical image and the gray area indicates the valid data which can be written to the DDR/SDRAM. The vertical start position for even and odd fields can be configured separately.

Figure 2-1. Frame Image format



2.4 SDRAM RAW Data Storage

Data are stored to the lower bits of a 16-bit DDR/SDRAM word, or can be 8 bits or 12 bits packed. Raw data to be stored can be right-shifted according to the value set at CCDW.

Table 2-5 shows the format where data are stored to the lower bits of a 16-bit word and also the format that data are packed to 8 bits. The unused bits are filled with zeros.

Table 2-5. SDRAM RAW Data Format (1)

	CCDW	SDR PACK	Upper word		Lower word	
			MSB(31)	LSB(16)	MSB(15)	LSB(0)
12-bit	0	0	0	Pixel1	0	Pixel0
11-bit	1	0	0	Pixel1	0	Pixel0
10-bit	2	0	0	Pixel1	0	Pixel0
9-bit	3	0	0	Pixel1	0	Pixel0
8-bit	4	0	0	Pixel1	0	Pixel0
8-bit pack	4	2	Pixel3	Pixel2	Pixel1	Pixel0

Table 2-6 shows the format in which 12-bit data are packed.

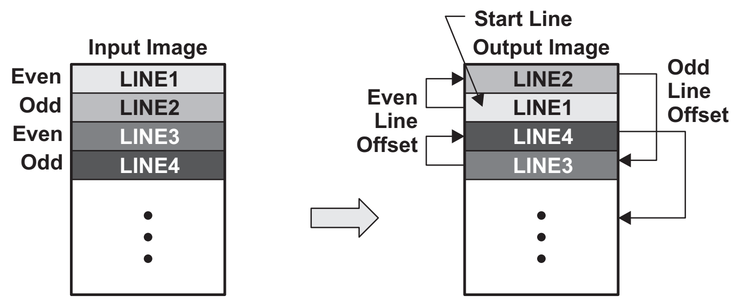
Table 2-6. SDRAM RAW Data Format (2)

	CCDW	SDR PACK	Upper word		Lower word	
12bit pack	0	1	MSB(31)	LSB(16)	MSB(15)	LSB(0)
			Pixel2[7:0]		Pixel1	Pixel0
			Pixel5[3:0]	Pixel4	Pixel3	Pixel2[11:8]
			Pixel7		Pixel6	Pixel5[11:4]

The ISIF has an internal FIFO. The processed Data are transferred from the FIFO to the buffer logic in 32-byte burst unit. The frequency of the SDRAM clock must be equal to or higher than the pixel clock. Data are written to SDRAM only if DWEN in SYNCEN is set to “1.”

The output formatter can configure to any image format by using SDRAM line offset register, and offset control registers. Figure 2-2 shows how to construct a frame format in SDRAM.

Figure 2-2. Frame Image Format Conversion



2.5 ITU-R BT.656/ 1120 4:2:2 Parallel Interface

The ITU-R BT.656 signal interface, shown in ITU-R BT.656 (sometimes referred to as REC656), is a specification that provides a method to transfer YCbCr-4:2:2 formatted, digital video data over an 8/10-bit wide interface. Data and timing codes (data along with sync signals) are transferred over the same 8/10-bit interface.

To enable ITU-R BT.656 mode, set R656ON in REC656IF register. When in ITU-R BT.656 mode, only the data lines and clock signal are connected between the external device and the ISIF. A NTSC/PAL decoder is an example of an external device that may be connected to the ITU-R BT.656 interface.

Data lines C7-C0 are used for 8-bit YCbCr data and data lines Y1-Y0, C7-C0 are used for 10-bit YCbCr data. The video timing signals, HD, VD, and FIELD, are generated internally by the ISIF.

Since the sync information is carried along with the data lines, there are no sync signal interfaces or ISIF configuration setting to make, other than the start/end pixels and the line length and vertical frame size. The signal interface is described in Table 2-7.

Table 2-7. ITU-BT.656 Interface Signals

Name	I/O	Description
C_DATA[9:0]	I	Image Data. Mode set by REC656IF.R656ON bit. • Bit width can be configured to either 8 or 10 bits (CCDCFG.BW656) bit. • The polarity of the input image data can be reversed (MODESET.DPOL) bit
PCLK	I	Pixel clock. This signal is used to load the image data into the ISIF • • The ISIF can be configured to capture on either the rising of falling edge of the PCLK signal by setting the bit VPSS_CLK_CTRL.PCLK_INV in SYSTEM module registers

At the start and end of each video data block the device sends a unique timing reference code. The start code is called the start of active video signal (SAV), and the end code is called the end of active video signal (EAV). The SAV and EAV codes proceed and follow valid data as shown in Figure 2-3. HD, VD, and FIELD are generated internally by the ISIF based on the SAV and EAV codes. The delay between the end of the HD pulse and the start of valid data can be configured by setting SPH and the length of valid data can be configured by setting LNH.

Both timing reference signals, SAV and EAV, consist of a four word sequence in the following format: FF 00 00 XY, where FF 00 00 are a set preamble and the fourth word defines the field identification, the state of vertical field blanking, the state of horizontal line blanking, and error correction codes. The bit format of the fourth word is shown in Table 2-8 and the definitions for bits, F, V, and H, are given in Figure 2-3. F, V, and H are used in place of the usual horizontal sync, vertical sync, and blank timing control signals. Bits P3, P2, P1, and P0 are error correction bits for F, V, and H. The relationship between F, V, and H and the error correction bits is given in Table 2-10. To enable error correction, set bit ECCFVH in REC656IF. The ISIF will automatically detect and apply error correction when ECCFVH is enabled.

Figure 2-3. ITU-R BT.656 Signal Interface

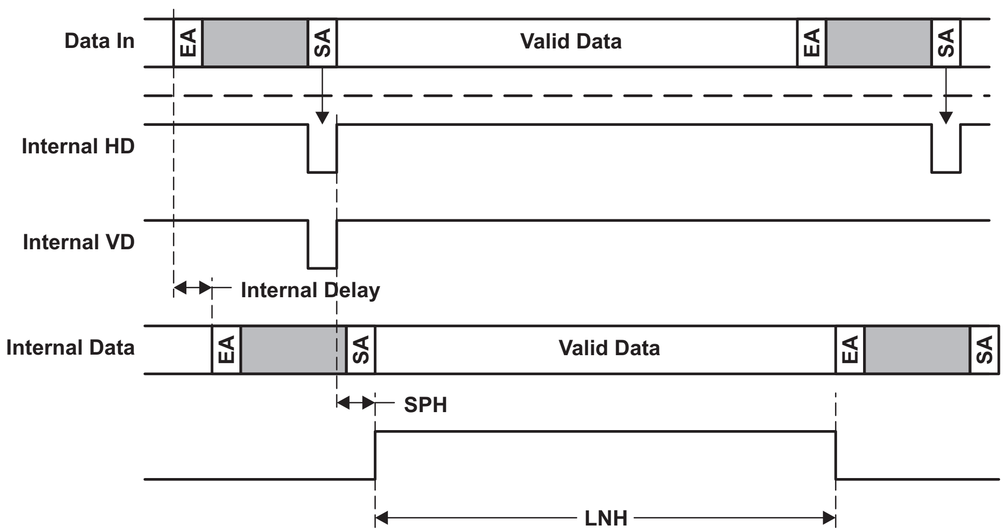


Table 2-8. Video Timing Reference Codes for SAV and EAV

Data Bit Number	First word	Second Word (00)	Third Word (00)	Fourth Word (XY)
7 (MSB)	1	0	0	1
6	1	0	0	F
5	1	0	0	V
4	1	0	0	H
3	1	0	0	P3
2	1	0	0	P2
1	1	0	0	P1
0 (LSB)	1	0	0	P0

The details of F, V, and H are given in Table 2-9 and Table 2-10. P0-P3 are the protection bits and the details are given in Table 14.

Table 2-9. F, V, H Signal Descriptions

Signal	Value	Command
F	0	Field 1
	1	Field 2
V	0	0
	1	Vertical blank
H	0	SAV
	1	EAV

Table 2-10. F, V, H Protection Bits

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

When operating in REC656 mode, data is stored in SDRAM according to the format shown in Figure 2-4.

Figure 2-4. BT.656 Mode Data Format in SDRAM

b31			b0
Pixel3 (Y1)	Pixel2 (Cr0)	Pixel1 (Y0)	Pixel0 (Cb0)

For BT.1120, Data width is 16bits and the registers would be configured as:

MODESET.INPMOD = 1 .... YCbCr16bit

REC656IF.R656ON = 1 .... ITU-R BT.656 interface mode set

CCDCFG.BW656 = 0 .... SYNC detection on C7-C0

2.6 Generic YCbCr Interface Configuration

The ISIF module can accept generic YCbCr-4:2:2 formatted digital video data over an 8/16 bit wide interface. Note that the BT.656 specification is for 525-line and 625-line, digital component video signals in compliance with BT.601.

规范

数字分量信号符合BT.601

2.6.1 Generic YCbCr Configuration Signal Interface

Table 2-11 shows the interface connections for the generic YCbCr interface.

Unlike the BT.656 mode, discrete HD, and VD signals are required. An NTSC/PAL decoder is an example of an external device that may be connected to the YCbCr interface.

In 8-bit mode, data lines YIN[7:0] and CIN[7:0] can be used for input. When using an 8-bit interface, the CIN[7:0] inputs are typically used. However, either set of data inputs can be used or, alternately, two separate imagers can be physically connected (but only one can be active at any given time). A register setting (`CCDCFG.YCINSWP`) determines which set of 8-bit inputs are active. Note that if only the lower 8 bits are used, an additional SPI can be supported in this mode without interference.

In 16-bit mode, data lines YIN[7:0] and CIN[7:0] are used for input with the Cr/Cb data multiplexed on the CIN[7:0] signals. A register setting (`CCDCFG.YCINSWP`) can be used to swap the Y and Cr/Cb data lines.

Table 2-11. Interface Signals for Generic YCbCr Mode

Pin Name	I/O	Description
PCLK	Input	Pixel Clock
VD	Bidi	V sync
HD	Bidi	H sync
CIN7	Input	C IN signal
CIN6	Input	C IN signal
CIN5	Input	C IN signal
CIN4	Input	C IN signal
CIN3	Input	C IN signal
CIN2	Input	C IN signal
CIN1	Input	C IN signal
CIN0	Input	C IN signal
YIN7	Bidi	Y IN signal
YIN6	Bidi	Y IN signal
YIN5	Bidi	Y IN signal
YIN4	Bidi	Y IN signal
YIN3	Bidi	Y IN signal
YIN2	Bidi	Y IN signal
YIN1	Bidi	Y IN signal
YIN0	Bidi	Y IN signal

2.6.2 Generic YCbCr Configuration Signal Interface Description

The digital YCbCr interface supports either 8-bit or 16-bit devices. The signal interface is described in Table 2-12.

Table 2-12. YCbCr Interface Signals

Name	I/O	Description
CCD[15:0] = YI[7:0] / CI[7:0]	I	Image data. Mode set by INPMOD (not R656ON). • Bit width can be can be configured between 8 and 16 bits BW656 • The polarity of the input image data can be reversed DPOL • When 16-bit interface is used, the Y and C inputs can be swapped (YCINSWP) • When 8-bit interface is used, either half of the bus can be connected (YCINSWP) • When 8-bit interface is used, the position of the Y data can be set to either the even or odd pixel (Y8POS)
VD	I/O	VSYNC. This vertical sync signal can be configured as an input or an output HDVDD. • When configured as an input, the signal source must supply the VD signal • When configured as an output, supplies the VD signal and the Vd width and lines per frame must be configured (VDW, LPFR) • The polarity of VD can be reversed. (VDPOL)
HD	I/O	HSYNC. This horizontal sync signal can be configured as an input or an output HDVDD. • When configured as an input, the signal source must supply the HD signal • When configured as an output, supplies the HD signal and the Hd width and pixels per line must be configured (HDW, PPLN) • The polarity of HD can be reversed (HDPOL)
C_WE_FIELD	I	Field identification signal (optional – CCDMD) • Supplied by the external signal source • Can be configured to be latched by the VD signal (FIDMD) • The polarity of the field identification signal can be reversed FIPOL
PCLK	I	Pixel clock. This signal is used to load image data into the ISIF. • The ISIF can be configured to capture on either the rising or falling edge of the PCLK signal (PCLK_INV in SYSTEM module)

2.6.3 Generic YCbCr Configuration Protocol and Data Formats

In 8-bit mode, the position on the Y data in relation to Cr/Cb data can be configured by the register setting:`CCDCFG.Y8POS`.

The byte ordering of data can be swapped by the register setting: `CCDCFG.BSWD`.

Table 2-13. DDR2/mDDR Controller Storage Format for YCbCr Processing

	Upper Word		Lower Word	
SDRAM Address	MSB(31)	LSB(16)	MSB(15)	LSB(0)
N	Y1	Cr0	Y0	Cb0
N + 1	Y3	Cr2	Y2	Cb2
N + 2	Y5	Cr4	Y4	Cb4

2.6.4 SPI and GIO Signal Multiplexing

The SPI3 peripheral and several GIOs may be made available to the system, depending on the pin usage of the particular capture mode used by the VPFE. Table 2-14 shows which pins are required by the VPFE for particular image capture modes and which pins can be made available for use by the SPI3 peripheral and/or extra GIOs. The PINMUX0 register shown in Figure 2-5 must be programmed according to the appropriate capture mode.

2.6.5 Y/C Data BUS Swap

There is an option to swap the upper and lower portion of the 16-bit YCbCr data bus (`ISIF.CCDCFG.YCINSWP`). This will swap the luma and chroma samples in 16-bit YCbCr mode. This will determine which half of the bus is used as the input source in 8-bit mode and can be used in 8-bit YCbCr mode to support two separate YCbCr input ports.

2.6.6 WEN/FIELD Signal Selection

Since the field ID and the write enable signal share the same pin, only one of these external signals can be connected. To enable the FIELD ID input, bit 7 of the ISIF.MODESET register should be set to INTERLACE MODE. To enable the write enable (WEN) signal, bit 5 of the ISIF.MODESET register should be set. These two bits should not be set concurrently or indeterminate results may occur.

2.6.7 Pin Mux 0 Register (PINMUX0)

The PINMUX0 register controls pin multiplexing for the VPFE pins. The pin mux 0 register (PINMUX0) is shown in Figure 2-5 and described in Table 2-14. The address for this register is 0x01C4:0000.

Figure 2-5. Pin Mux 0 Register (PINMUX0)

31–16
Reserved
R-0

15–14	13	12	11	10	9	8
C_WE_FIELD	VD	HD	YIN_0	YIN_1	YIN_2	YIN_3
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7–6	5–4	3–2	1–0
YIN_4	YIN_5	YIN_6	YIN_7
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 2-14. Pin Mux 0 Register (PINMUX0) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Reserved
15-14	C_WE_FIELD		C_WE_FIELD pin function
		0	C_WE_FIELD
		1	GIO093
		2	CLKOUT0
		3	USBDRVVBUS
13	VD		VD pin function
		0	VD
		1	GIO094
12	HD		HD pin function
		0	HD
		1	GIO095
11	YIN_0		YIN0 pin function
		0	YIN_0
		1	GIO096
10	YIN_1		YIN1 pin functions
		0	YIN_1
		1	GIO097

Table 2-14. Pin Mux 0 Register (PINMUX0) Field Descriptions (continued)

Bit	Field	Value	Description
9	YIN_2		YIN2 pin function
		0	YIN_2
		1	GIO098
8	YIN_3		YIN3 pin function
		0	YIN_3
		1	GIO099
7-6	YIN_4	0-3h	YIN4 pin function
		0	YIN_4
		1h	GIO100
		2h	SPI3_SDI3
		3h	SPI3_SDENA[1]
5-4	YIN_5	0-3h	YIN5 pin function
		0	YIN_5
		1h	GIO101
		2h	SPI3_SDENA[0]
		3h	Reserved
3-2	YIN_6	0-3h	YIN6 pin function
		0	YIN_6
		1h	GIO102
		2h	SPI3_SD0
		3h	Reserved
1-0	YIN_7	0-3h	YIN7 pin function
		0	YIN_7
		1h	GIO103
		2h	SPI3_SCLK
		3h	Reserved

VPFE/ISP Integration

This section describes how the VPFE/ISP subsystem is integrated into the device, including any interactions it may have with other subsystems on the device.

3.1 Clocking, Reset and Power Management Scheme

3.1.1 Clocks

There are six clock domains in the VPFE. See the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5) for more information of PLL configuration and system clock tree).

Table 3-1. Clock Domains

Name	Frequency	Description	Max Frequency
MMR	PLL0 SYSCLK4	Used for clocking the memory-mapped register (MMR) port for the control registers	121.5 MHz
DMA	PLL0 SYSCLK4	Used for clocking the DMA port for data transfers to and from the SDRAM EMIF	121.5 MHz
VPSSCLK	PLL0 SYSCLK4	Used for clocking the VPFE module internal logic. Also used to generate the IPIPEIF_PCLK	121.5 / 243 MHz
PSYNCCLK	PCLK	PCLK synchronized with the VPFE MMR clock	121.5 MHz
PCLK		The generic term PCLK in this document is an acronym for the pixel clock. There are two separate sources for the PCLKs that clock the pixels through the various VPFE modules	120 MHz
		External PCLK - if the ISIF receives data from the parallel imager input, then this is the external pixel clock (PCLK) driven by the input imager	
		IPIPEIF_PCLK - the pixel clock output of the IPIPEIF (for clocking data from SDRAM) generated from a divided down VPSSCLK according to the IPIPEIF.CLKDIV register field. Set the IPIPEIF.CFG1.CLKSEL to 1 in this case	
Crystal Clock	XTALCLK	Crystal clock	up to 48MHz

Note that there is an option to drive the VPBE module with the VPFE pixel clock (PCLK).

3.1.2 Resets

The VPFE module resets are tied to the device reset signals.

In addition, the VPSS modules can be reset by transitioning to the SyncReset state of the Power Sleep Controller (PSC). Note that the VPSS has two module domains, the VPSSmstr processing domain and the VPSSslv register interface.

3.1.3 Power Management

When powered, the VPFE modules utilize auto clock gating on a clock-by-clock basis to conserve dynamic power during periods of inactivity. When the VPSS is not required for the application, its MMR clocks (VPSSslv) and operating clocks (VPSSmstr) can be gated by the PSC to conserve dynamic power.

Additionally, when certain submodules within the VPFE are not required for the application mode, they can be disabled by software by configuring the ISP.PCCR register appropriately.

3.2 Hardware Requests

The VPSS can generate the 25 interrupts/events shown in Table 3-2. However, only nine of them can be sent to the ARM as interrupts and four of them can be sent to the EDMA as events. A mapping of which events are sent to the ARM and EDMA can be configured in the ISP.INTSEL[1:3] and ISP.EVTSEL registers respectively. The ISP.INTSTAT register can also be used to poll for events. More details on each module's events can be found in Table 3-2.

Table 3-2. VPSS Events

Event Number	Acronym	Module	Description
0	ISIF_INT0	ISIF	Triggered after a programmable number of input lines for each frame(VDINT0)
1	ISIF_INT1	ISIF	Triggered after a programmable number of input lines for each frame (VDINT1)
2	ISIF_INT2	ISIF	Triggered after a programmable number of input lines for each frame (VDINT2)
3	LSC_INT	ISIF	LSC interrupt muxed by 2DLSCIRQEN register
4	IPIPE_INT_REG	IPIPE	Triggered when IPIPE register update is allowed
5	IPIPE_INT_LAST_PIX	IPIPE	Triggered when the last pixel of a frame comes into IPIPE for each frame
6	Reserved		
7	IPIPE_INT_BSC	IPIPE	Triggered when boundary signal calculation is finished for each frame
8	IPIPE_INT_HST	IPIPE	Triggered when histogram processing is finished for each frame
9	IPIPEIF_INT	IPIPEIF	Triggered at the start position of VSYNC from parallel input- interface or ISIF (can be selected from IPIPEIF.CFG2.INTSRC bit)
10	AEW_INT	H3A	Triggered when auto exposure and auto white-balance processing is finished for each frame
11	AF_INT	H3A	Triggered when auto focus processing is finished for each frame
12	Reserved		
13	RSZ_INT_REG	Resizer	Triggered when the resizer register update is allowed
14	RSZ_INT_LAST_PIX	Resizer	Triggered when the last pixel of a frame comes into resizer for each frame
15	Reserved		
16	RSZ_INT_CYC_RZA	Resizer	Triggered when the number of lines programmed has been output of resizer-A for each frame
17	RSZ_INT_CYC_RZB	Resizer	Triggered when the number of lines programmed has been output of resizer-B for each frame
18	Reserved		
19	Reserved		
20	OSD_INT	OSD	Triggered at the end of each frame read from SDRAM (for VPBE)
21	VENC_INT	VENC	Triggered at the rising edge of VSYNC (for VPBE)
22	RSZ_INT_EOF0	Resizer	Triggered when writes to SDRAM(from both Resizer-A & Resizer-B) are finished for each frame. If both RSZ.RZA_420 and RSZ.RZB_420 are 2, then the interrupt is invalid.
23	RSZ_INT_EOF1	Resizer	Triggered when writes to SDRAM(from both Resizer-A & Resizer-B) are finished for each frame. If both RSZ.RZA_420 and RSZ.RZB_420 are 0 or 1, then the interrupt is invalid.
24	H3A_INT_EOF	H3A	Triggered at the same time as last process (AF or AEW) to finish for each frame (triggered when both AF and AEW processes are done)
25	IPIPE_INT_EOF	IPIPE	Triggered when boxcar's write to SDRAM transfer is finished for each frame
26	LDC_INT_EOF	LDC	Triggered when LDC processing is finished for each frame
27	IPIPE_INT_DPC_INI	IPIPE	This is a request to initialize both defect pixel table bank #0 and bank #1. Triggered when IPIPE.DPC_LUT_EN is 1 and the first valid pixel comes into IPIPE. If defect pixel tables are not ready, Firmware has to initialize them.
28	PIPE_INT_DPC_ RNEW0	IPIPE	This is a request to renewal defect pixel table bank #0. Triggered when the status of defect pixel table bank #0 changed to empty.
29	IPIPE_INT_DPC_ RNEW1	IPIPE	This is a request to renewal defect pixel table bank #1. Triggered when the status of defect pixel table bank #1 changed to empty.

3.2.1 Interrupt Requests

The nine interrupts selected in the ISP.INTSEL[1:3] registers are assigned to the ARM interrupt controller as shown in Table 3-3.

Table 3-3. ARM Interrupts - VPSS

INT Number	Acronym
0	VPSSINT0
1	VPSSINT1
2	VPSSINT2
3	VPSSINT3
4	VPSSINT4
5	VPSSINT5
6	VPSSINT6
7	VPSSINT7
8	VPSSINT8

VPSSINT0, VPSSINT7 and VPSSINT8 are multiplexed with the other module interrupts (NSFINT (noise filter) and IMXINT1 from IMCOP) in the system. The system level register, ARM_INTMUX, must be configured to select VPSSINT0, 7 and 8 interrupts for use. Corresponding bit fields in the ARM_INTMUX register are specified in Table 3-4.

Table 3-4. ARM_INTMUX Register (specified only VPSS interrupt mux)

Bits	Field Name	Description for ARM_INTMUX	Type	Reset
31	INT0	VPSS_INT0 or PBIST 0 = VPSS_INT0 1 = Reserved	R/W	0
26-15	Reserved		-	0
25	INT7	VPSS_INT7 or NSFINT 0 = VPSS_INT7 1 = NSFINT	R/W	0
24	INT8	VPSS_INT8 or IMXINT1 0 = VPSS_INT8 1 = IMXINT1	R/W	0

3.2.2 EDMA Requests

The four events selected in the ISP.EVTSEL register are assigned to the EDMA as shown in Table 3-5.

Table 3-5. EDMA Events - VPSS

Event Number	Binary	Event Name
4	0000100	VPSSEVT1
5	0000101	VPSSEVT2
6	0000110	VPSSEVT3
7	0000111	VPSSEVT4

There are two primary reasons for using an EDMA event from the VPSS. The first is to trigger an EDMA transfer of boundary signal vectors from the VPSS internal memory to external memory before they are overwritten by the next frame. The second is to allow for an update of the module registers by using the DMA scheme verses the direct CPU write. Normally, the ARM performs this function, but in some cases the ARM can be tied up with other activities and the interrupt latency is critical when dealing with the VPFE modules. Consider the following example: a still image is processed by the image pipe. Since an 8MP still image is too wide for a single pass through the image pipe, two passes are required. The image pipe registers need to be altered as soon as each pass is complete. Tying an IPIPE event to the EDMA allows instantaneous DMA of the new register settings for the subsequent passes.

3.3 VPSS Top-Level Register Mapping Summary

Table 3-6 provides a summary of the VPSS top-level register mapping.

Table 3-6. VPFE Module Register Map

VPSS Registers	Address Range		Size
ISP System Registers	0x01C70000	0x01C700FF	256B
VPSS System Registers	0x01C70200	0x01C702FF	256B
Resizer Registers	0x01C70400	0x01C77FF	1KB
IPIPE Registers	0x01C70800	0x01C70FFF	2KB
ISIF Registers	0x01C71000	0x01C711FF	512B
IPIPEIF Registers	0x01C71200	0x01C712FF	256B
H3A Registers	0x01C71400	0x01C714FF	256B
LDC Registers	0x01C71600	0x01C717FF	512B
OSD Registers	0x01C71C00	0x01C71CFF	256B
VENC Registers	0x01C71E00	0x01C71FFF	512B

3.4 VPSS Embedded Memory Mapping Summary

In the VPSS module, there are a few modules which *may* require their corresponding look-up tables (LUT) to be configured to the customer-specific values, and a few modules (histogram and BSC) output the results in the internal memory of the VPSS. The address map for those LUTs and internal memories is specified below.

Table 3-7. VPFE Embedded Memory Map

Embedded Memory	Module	Address Range	Size
IPIPE_HST_TB0	Histogram	0x01C72000 – 0x01C727FF	2KB
IPIPE_HST_TB1	Histogram	0x01C72800 – 0x01C72FFF	2KB
IPIPE_HST_TB2	Histogram	0x01C73000 – 0x01C737FF	2KB
IPIPE_HST_TB3	Histogram	0x01C73800 – 0x01C73FFF	2KB
IPIPE_DPC_TB0	Defect Pixel Correction	0x01C78000 – 0x01C781FF	512B
IPIPE_DPC_TB1	Defect Pixel Correction	0x01C78400 – 0x01C785FF	512B

Table 3-7. VPFE Embedded Memory Map (continued)

Embedded Memory	Module	Address Range	Size
IPIPE_YEE_TB	Edge Enhancer	0x01C78800 – 0x01C78FFF	2KB
IPIPE_GAMR_TB	Gamma Correction	0x01C7A800 – 0x01C7AFFF	2KB
IPIPE_GAMG_TB	Gamma Correction	0x01C7B000 – 0x01C7B7FF	2KB
IPIPE_GAMB_TB	Gamma Correction	0x01C7B800 – 0x01C7BFFF	2KB
OSD_CLUT	OSD (VPBE)	0x01C7F800 – 0x01C7FBFF	1KB

These embedded memories can be directly accessed by ARM through the configuration bus.

The format of the data to be filled in the look-up table memories is explained in the corresponding module functional description sub-sections (in Chapter 4).

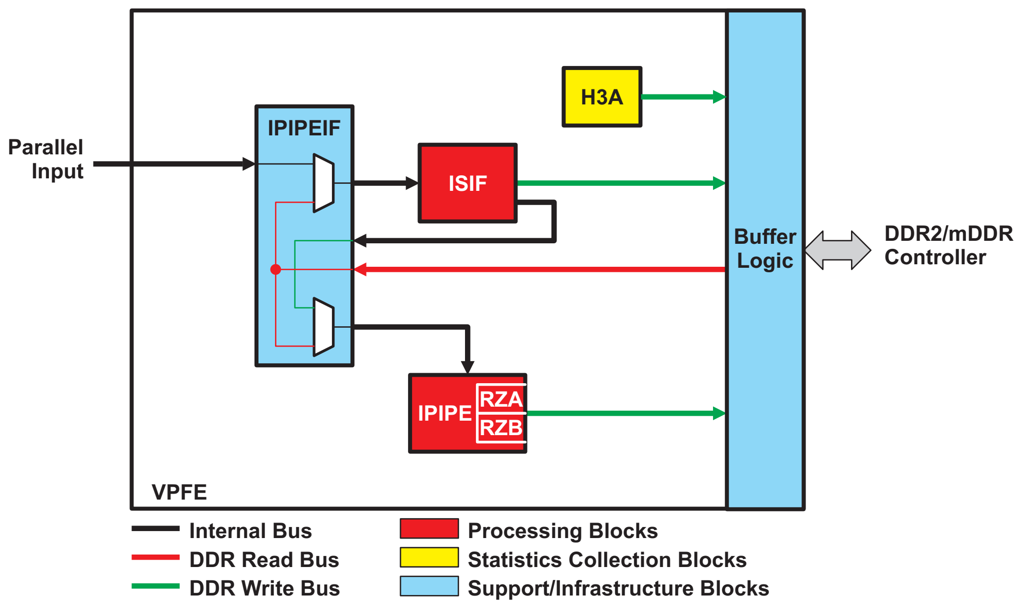
3.5 VPFE/ISP Top-Level Signal Interaction

The ISIF_VSYNC signal drives the event-trigger input signal of all four PWM modules. The PWM can configure the trigger to detect the rising or falling edge of the ISIF_VSYNC signal. This capability is provided to allow the PWM module to be used as an ISIF timer.

VPFE/ISP Functional Description

The VPFE block diagram is shown below. Additional detailed block diagrams are shown in the interface and image processing subsections.

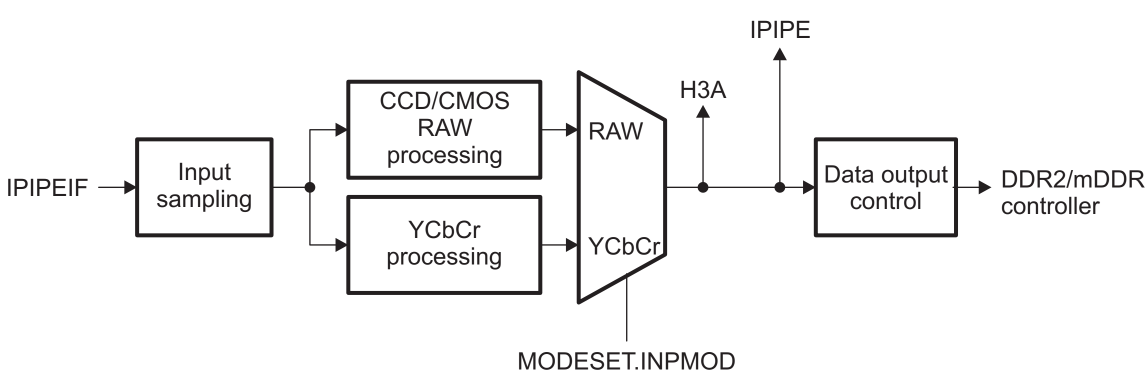
Figure 4-1. Video Processing Front End (VPFE) Block Diagram



4.1 Image Sensor Interface (ISIF)

The image sensor interface (ISIF) module interfaces with external image sources as well as CCD sensors. It supports both RAW Bayer data from CCD/CMOS sensors and processed YCbCr data from either a CMOS sensor with integrated image processing or a video decoder interface. A high-level block diagram of the ISIF module is shown in Figure 4-2 .

Figure 4-2. Image Sensor Interface (ISIF) – Top Level Block Diagram

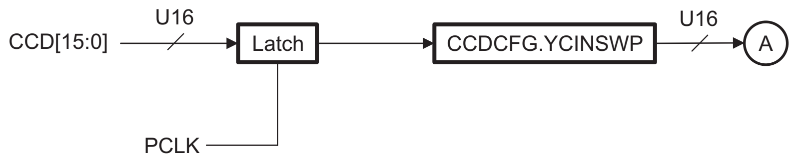


4.1.1 ISIF Input Sampling

The ISIF module input sampling and formatting are shown in Figure 4-3.

There is an option to swap the upper and lower portion of the 16-bit YUV data bus (CCDCFG.YCINSWP). This will swap the luma and chroma samples in 16-bit YUV mode and will determine which half of the bus is used as the input source in 8-bit mode, and which can be used in 8-bit YUV mode to support two separate YUV input ports. Since this bit affects both RAW and YUV input modes, CCDCFG.YCINSWP should always be set to '0' in RAW input mode (MODESET.INPMOD = 0).

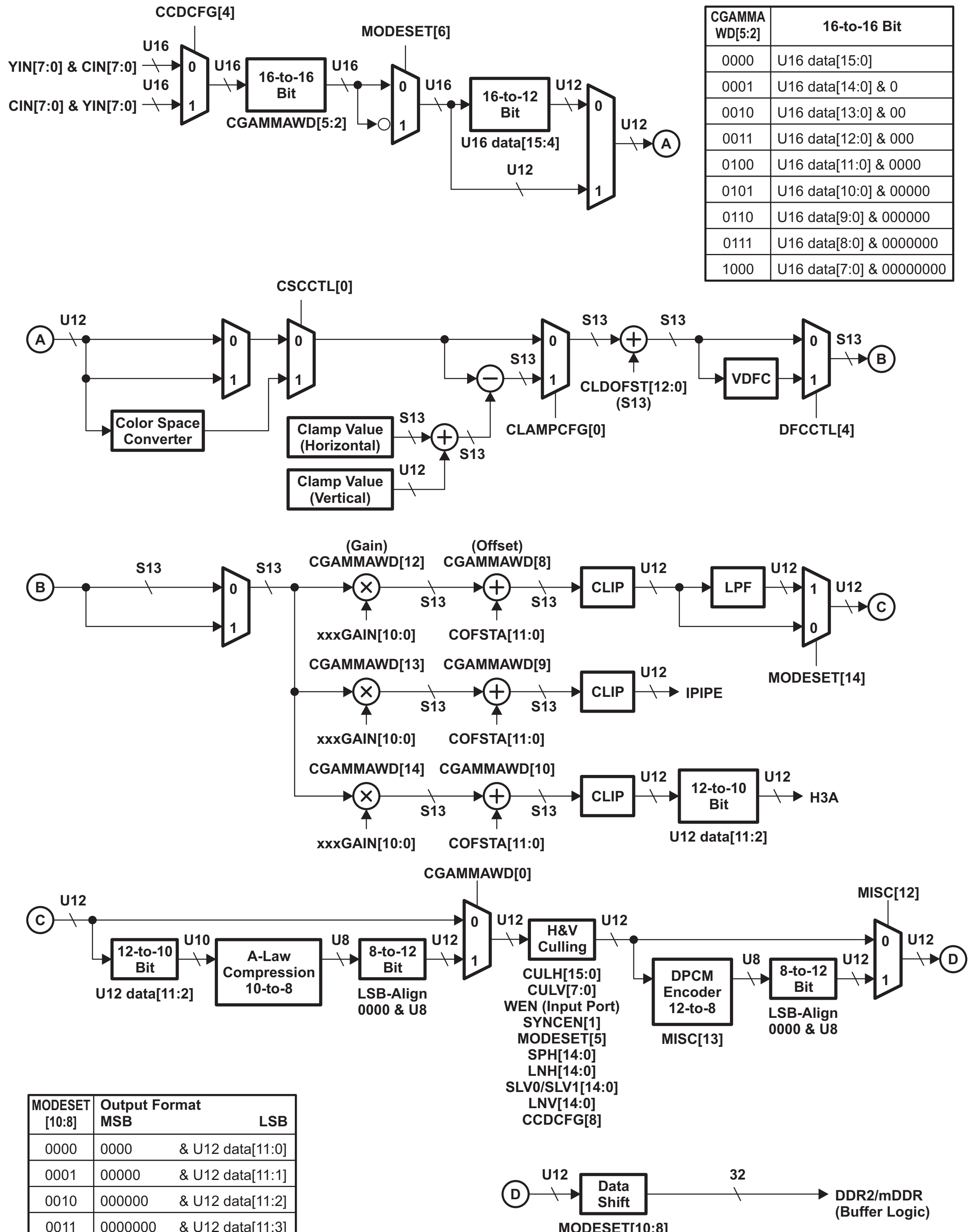
Figure 4-3. Image Sensor Interface - Input Formatting



4.1.2 ISIF Processing Data Flow

The following figure illustrates the raw data processing flow for the sensor interface.

Figure 4-4. Sensor Interface (ISIF) – RAW Data Processing Flow



CGAMMA WD[5:2]	16-to-16 Bit
0000	U16 data[15:0]
0001	U16 data[14:0] & 0
0010	U16 data[13:0] & 00
0011	U16 data[12:0] & 000
0100	U16 data[11:0] & 0000
0101	U16 data[10:0] & 00000
0110	U16 data[9:0] & 000000
0111	U16 data[8:0] & 0000000
1000	U16 data[7:0] & 00000000

MODESET [10:8]	Output Format MSB	LSB
0000	0000	& U12 data[11:0]
0001	00000	& U12 data[11:1]
0010	000000	& U12 data[11:2]
0011	0000000	& U12 data[11:3]
0100	00000000	& U12 data[11:4]

4.1.3 Input Data Formatter

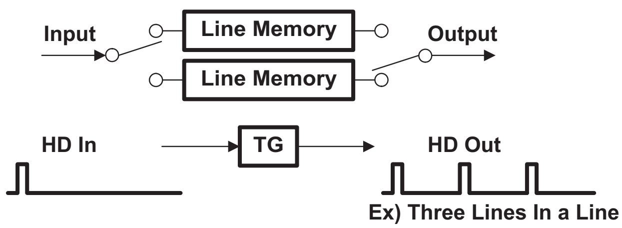
There are two functional blocks: input data formatter, and color space converter, which use two 4736 x 12 bits (corresponds to one line of maximum 4736 pixels with each pixel equal to 12 bits in size) memories. Only one of the functional blocks can be enabled in the flow at a given time as shown in .

The data formatter block allows the ISIF to handle a wide variety of current and future readout schemes other than Bayer format. Two line memories and a programmable address generator are used to translate those patterns to that of a standard Bayer pattern (or any other pattern). This allows the back end processing (noise filters, interpolation, histogram, 3A statistics) to remain unchanged.

The data formatter block also supports “divided input lines.” If an input line is divided into multiple lines and fed to the ISIF, the formatter gathers the divided lines and organizes a single line. Up to four divided lines can be supported.

The data formatter can split an input line into 1, 2, 3, or 4 output lines, or can combine the divided 1, 2, 3, or 4 input lines into a single line. Figure 4-5 shows an example generating three output lines from an input line with a new, internally generated HD signal. This HD signal then gates the downstream processing rather than the original sensor HD signal. Details of how to configure the formatter are provided in the following sections.

Figure 4-5. Splitting an Input Line Into Three Output Lines



Since the size of the line memories is 4736 x 12 bits, the following restrictions apply for the data formatter.

Split Lines

- The maximum number of pixels that can be supported in an output line if the input line is transformed into one output line is 4736.
- The maximum number of pixels that can be supported in an output line if the input line is transformed into two output lines is 2368.
- The maximum number of pixels that can be supported in an output line if the input line is transformed into three output lines is 1578.
- The maximum number of pixels that can be supported in an output line if the input line is transformed into four output lines is 1184.

Combine Lines

- The maximum number of pixels that can be supported in an output line if one input line is transformed into an output line is 4736.
- The maximum number of pixels that can be supported in an output line if two input lines are transformed into an output line is 2368.
- The maximum number of pixels that can be supported in an output line if three input lines are transformed into an output line is 1578.
- The maximum number of pixels that can be supported in an output line if four input lines are transformed into an output line is 1184.

4.1.3.1 Formatter Area Settings

As shown in Figure 4-6 FMTSPH, FMTLNH, FMTSLV, and FMTLNV registers are used for the formatter area settings.

Figure 4-6. Data Formatter Area Settings

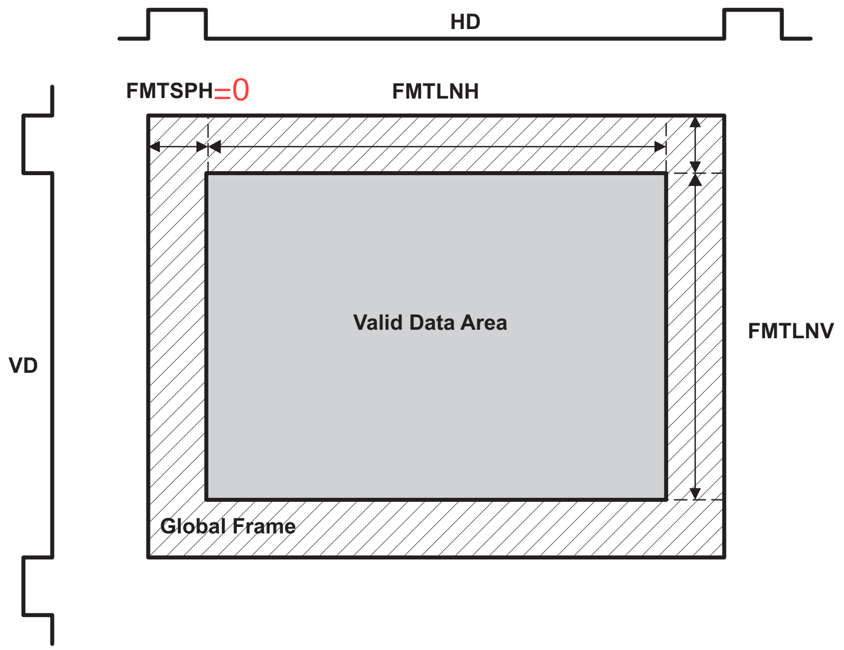


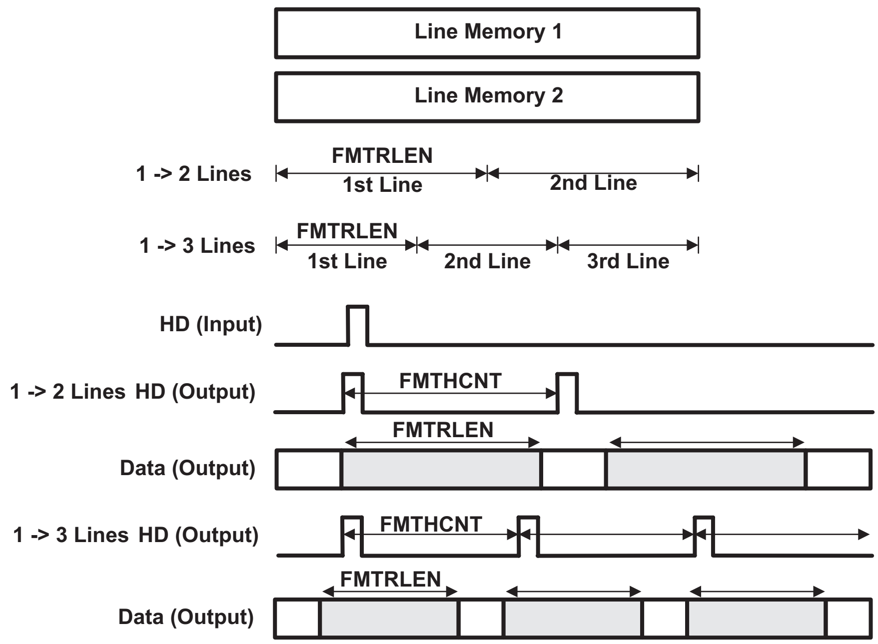
Table 4-1 explains some of the registers for the area settings. The input line is input to the formatter, and the output line is output from the formatter

Table 4-1. Formatter Area Setting Registers

Register	Description
FMTSPH	The first valid pixel of an input line
FMTLNH	Valid length of an input line = FMTLNH+1
FMTSLV	The first valid input line
FMTLNV	The number of the valid input lines = FMTLNV+1
FMTRLEN	The length of an output line
FMTHCNT	HD interval for output lines
SPH 0	The first pixel in an output line to be stored to SDRAM
LNH	Number of pixels in an output line to be stored to SDRAM = LNH+1
SLV	The line to start data storing to SDRAM. It is based on the input line count.
LNV	The number of the output lines to be stored to SDRAM = LNV+1

The number of pixels in an output line should be set to register FMTRLEN, and the HD output interval should be set to register FMTHCNT. There is no need to set FMTHCNT while combining the multiple input lines into a single line. Figure 4-7 shows the example to split an input line into two or three output lines.

Figure 4-7. Data Formatter Output Control



4.1.3.2 Color Space Converter

The color space converter (CSC) includes four 8-bit x 12-bit multipliers and one adder for the color space conversion. .

Figure 4-8. Color Space Converter Functional Block Diagram

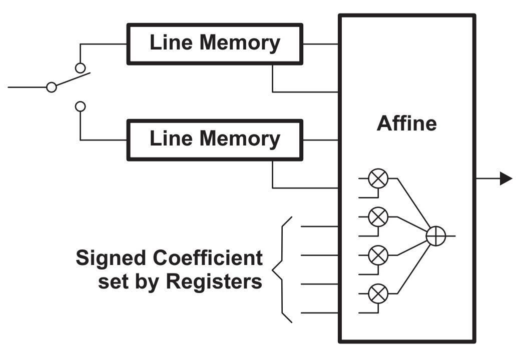
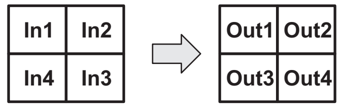


Figure 4-9. Color Space Converter Operation

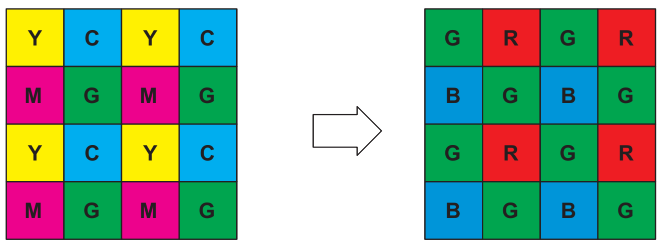


$$\begin{pmatrix} Out1 \\ Out2 \\ Out3 \\ Out4 \end{pmatrix} = \begin{pmatrix} M00 & M01 & M02 & M03 \\ M10 & M11 & M12 & M13 \\ M20 & M21 & M22 & M23 \\ M30 & M31 & M32 & M33 \end{pmatrix} \begin{pmatrix} In1 \\ In2 \\ In3 \\ In4 \end{pmatrix}$$

M00-M33 : Signed 8-Bits Data with 5-Bit Decimal
The Value Range –4 = < Mxx < 4

Coefficients are signed 8-bit (decimal is 5 bits). The CSC can convert CMYG filtered CCD data to Bayer Matrix (RGBG) data as shown in Figure 4-10.

Figure 4-10. CSC CMYG Filtered CCD Data to RGBG Data Converter Operation



$$\begin{pmatrix} G \\ R \\ B \\ G \end{pmatrix} = \begin{pmatrix} 0.5 & 0.5 & -0.5 & 0 \\ 0.5 & -0.5 & 0.5 & 0 \\ -0.5 & 0.5 & 0.5 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} Y \\ C \\ M \\ G \end{pmatrix}$$

The following figures explain which input pixels are used for the operation. There is 1 line latency between the input and the output.

Figure 4-11. CSC - Input Pixels Used

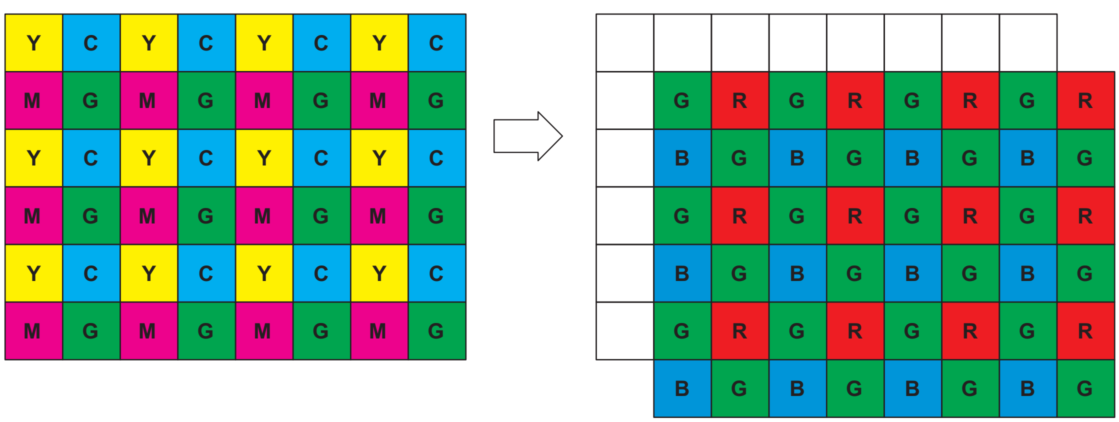


Figure 4-12. CSC - 1st Pixel / 1st Line Generation

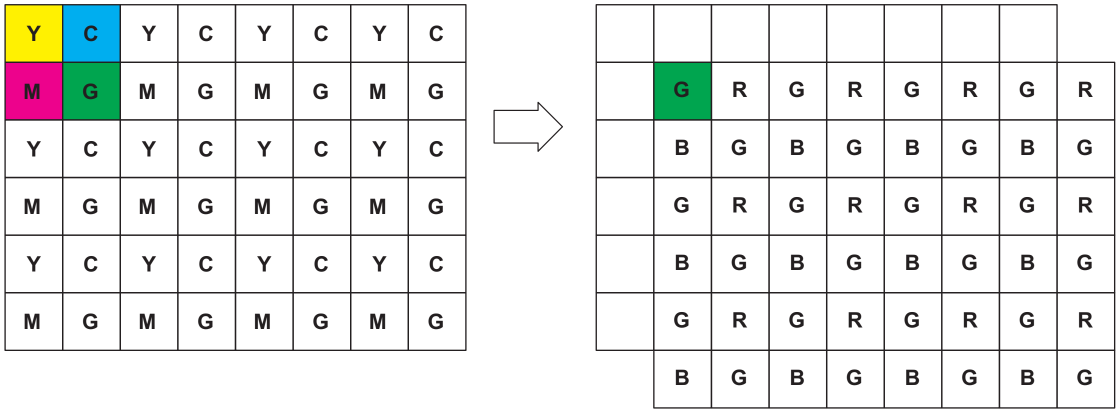


Figure 4-13. CSC - 2nd Pixel / 1st Line Generation

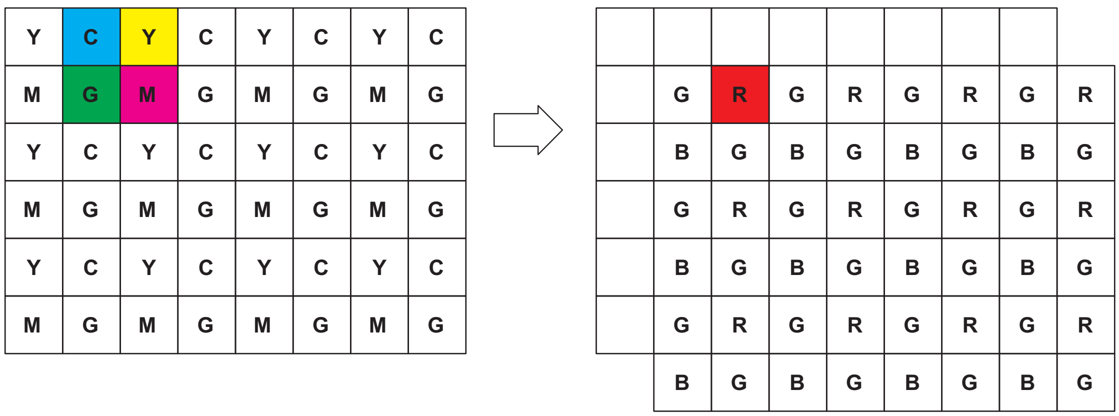


Figure 4-14. CSC - 2nd Last Pixel / 1st Line Generation

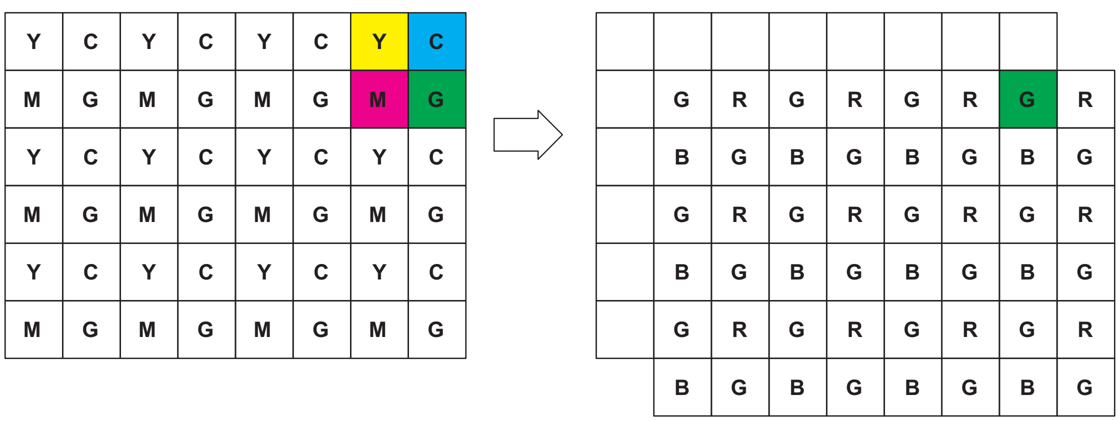
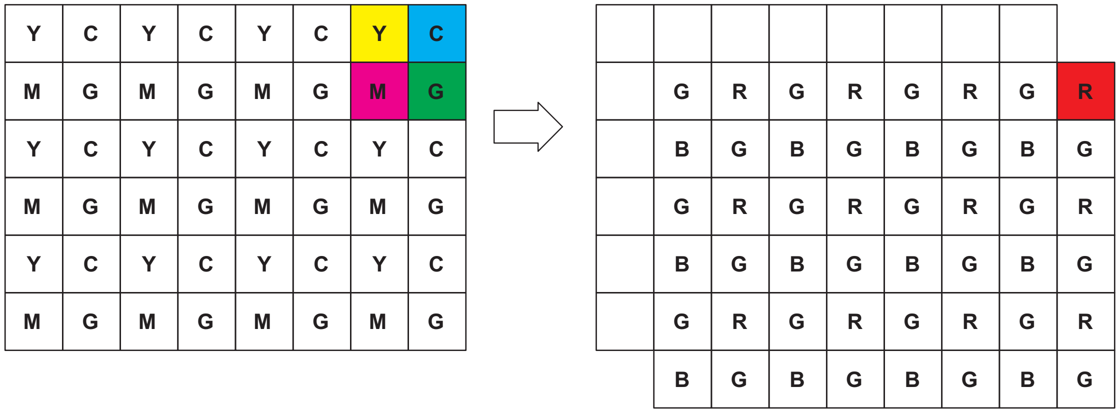


Figure 4-15. CSC - Last Pixel / 1st Line Generation



As shown in Figure 4-14 and Figure 4-15, the operation for the last pixel and the second last pixel uses the same input data.

Figure 4-16. CSC - 1st Pixel / Last Line Generation

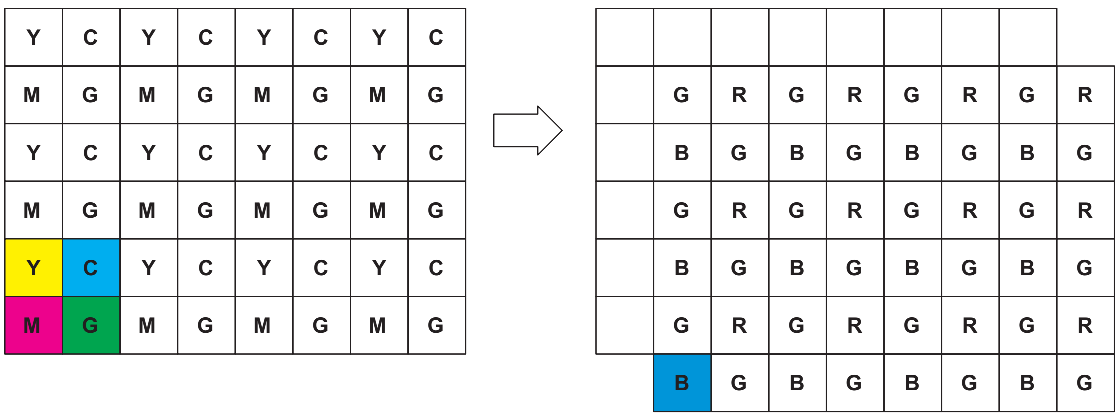


Figure 4-17. 2nd Pixel / Last Line Generation

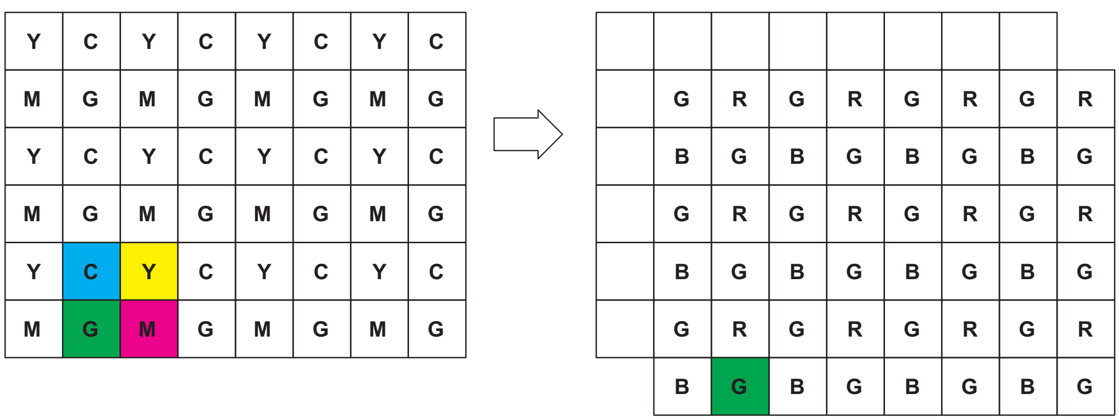


Figure 4-18. 2nd Last Pixel / Last Line Generation

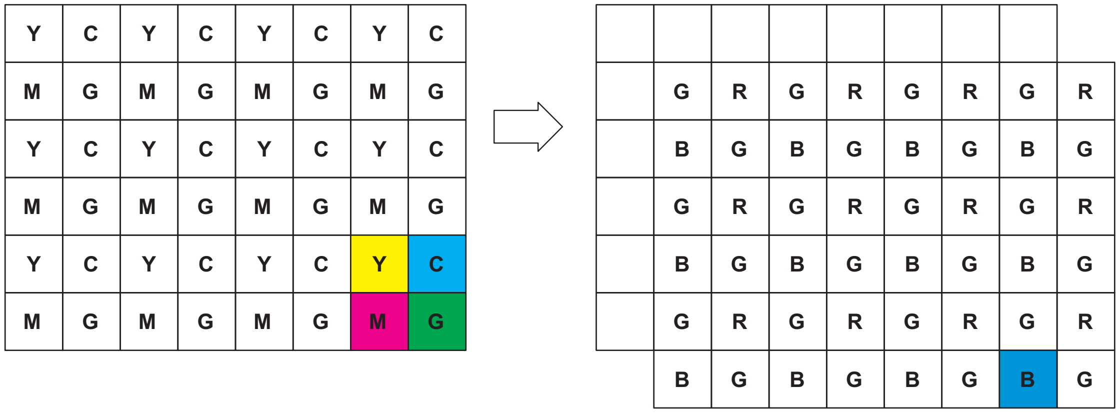
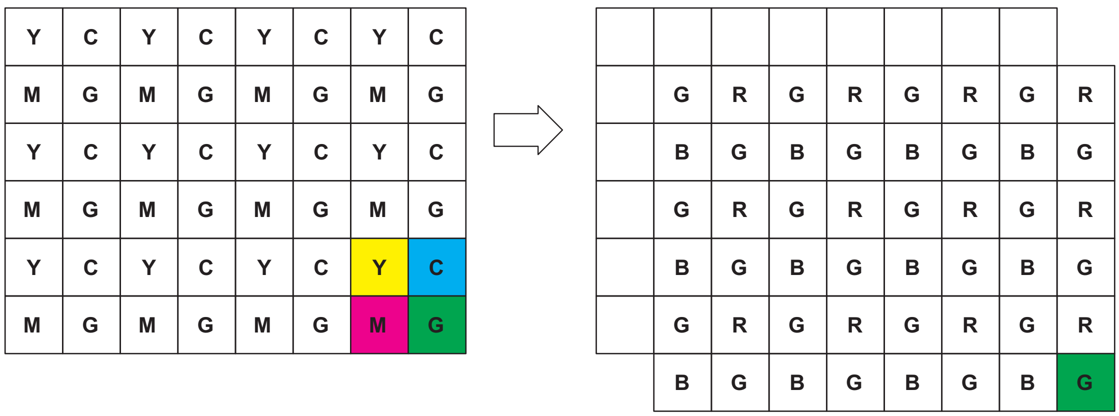


Figure 4-19. Last Pixel / Last Line Generation

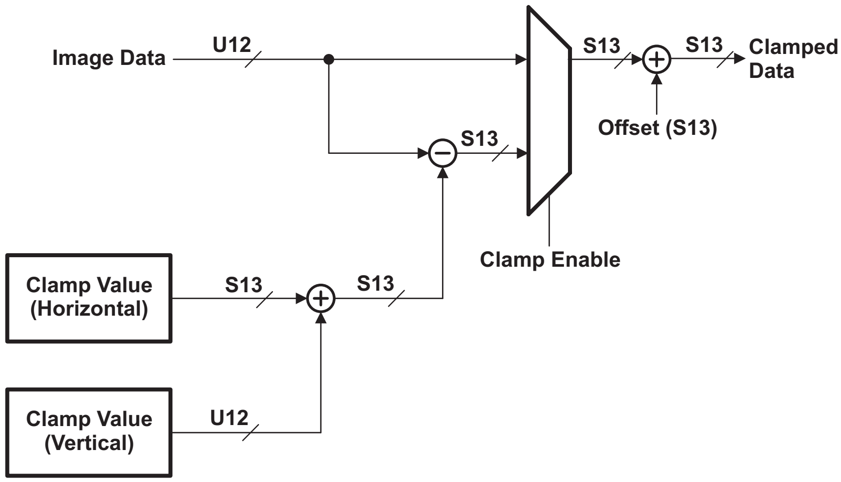


In addition to the registers specific to the color space converter, some of the registers are shared with the input data formatter to configure the valid area, which are FMTSPH, FMTLNH, FMTSLV, and FMTLNV shown in Figure 4-6. There should be at least one invalid pixel at the end of the line, and also one invalid line at the end of the frame.

4.1.3.3 Black Clamp

The next sub-module is the black clamp block. Clamp value is calculated based on the pixel value at the optical black (OB) region. Clamp value is calculated separately for horizontal and vertical directions to compensate for the offset drift in both horizontal and vertical directions. The sum of the horizontal and vertical clamp values is subtracted from the image data, and then the additional DC offset (S13) is added as shown in Figure 4-20.

Figure 4-20. Digital Clamp Block Diagram



Clamp value can be calculated regardless of the color (CLMD=0), or can be calculated separately for each four color (CLMD=1).

4.1.3.3.1 Value for Horizontal Direction

Clamp value for horizontal direction is calculated using the pixel values at the upper OB region. The maximum pixel value to be used for the clamp value calculation can be limited to 1023 if CLHLMT is set.

If CLHLMT = 1

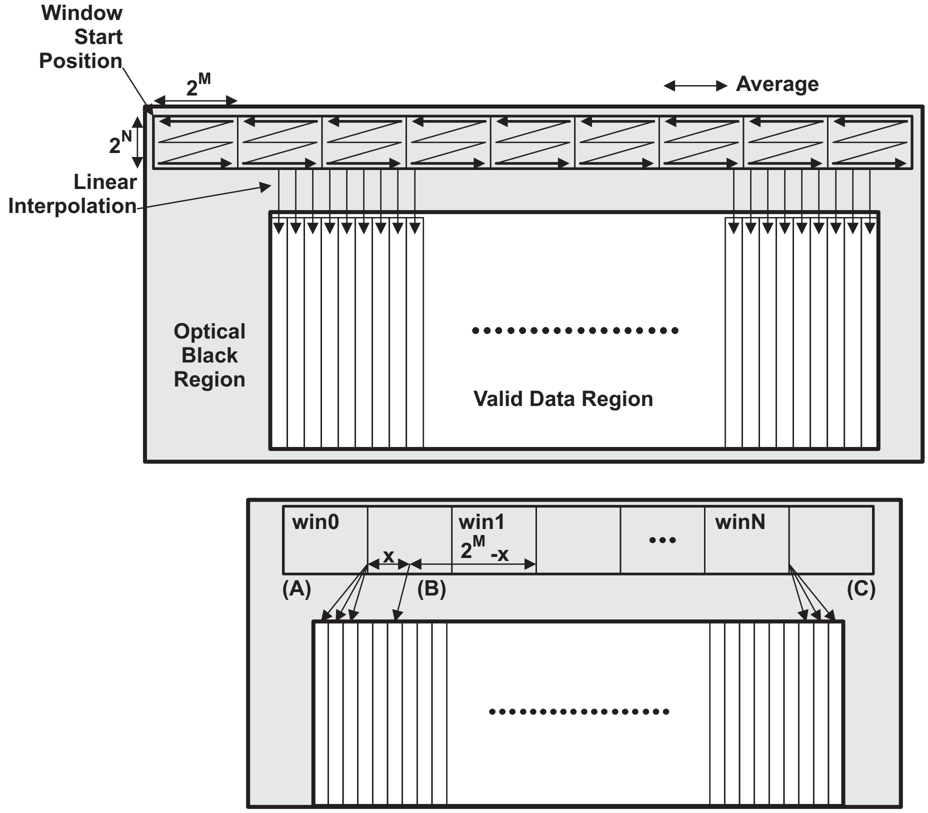
- CLMD=0: The pixel value greater than 1023 will be replaced by the last pixel value which was equal to or less than 1023
- CLMD=1: The pixel value greater than 1023 will be replaced by the last pixel value of the same color which was equal to or less than 1023

Clamp value calculation for horizontal direction could be disabled in case there is no upper OB. The operating modes are:

- Horizontal clamp value calculation is enabled. The calculated horizontal clamp value is subtracted from the Image data along with the Vertical clamp value. (CLHMD=1)
- Horizontal clamp value is not updated. The horizontal clamp value used for the previous image is subtracted from the image data along with the vertical clamp value. (CLHMD=2)
- Horizontal clamp value is not updated. Only the vertical clamp value is subtracted from the image data. (CLHMD=0)

Up to 32 windows can be set in a row for clamp value calculation. Windows are the same size in a format 2^Mx2^N (where ^ denotes an exponent).

Figure 4-21. Clamp Value for Horizontal Direction



4.1.3.3.2 Clamp Value for Vertical Direction

Clamp value for vertical direction is calculated using the pixel values at the left or right OB region. Line average is calculated for the OB H valid (2^L) period (where ^ denotes an exponent). The averages for the previous lines are also added back so as to reduce the difference between the lines.

Figure 4-22. Clamp Value for Vertical Direction (1)

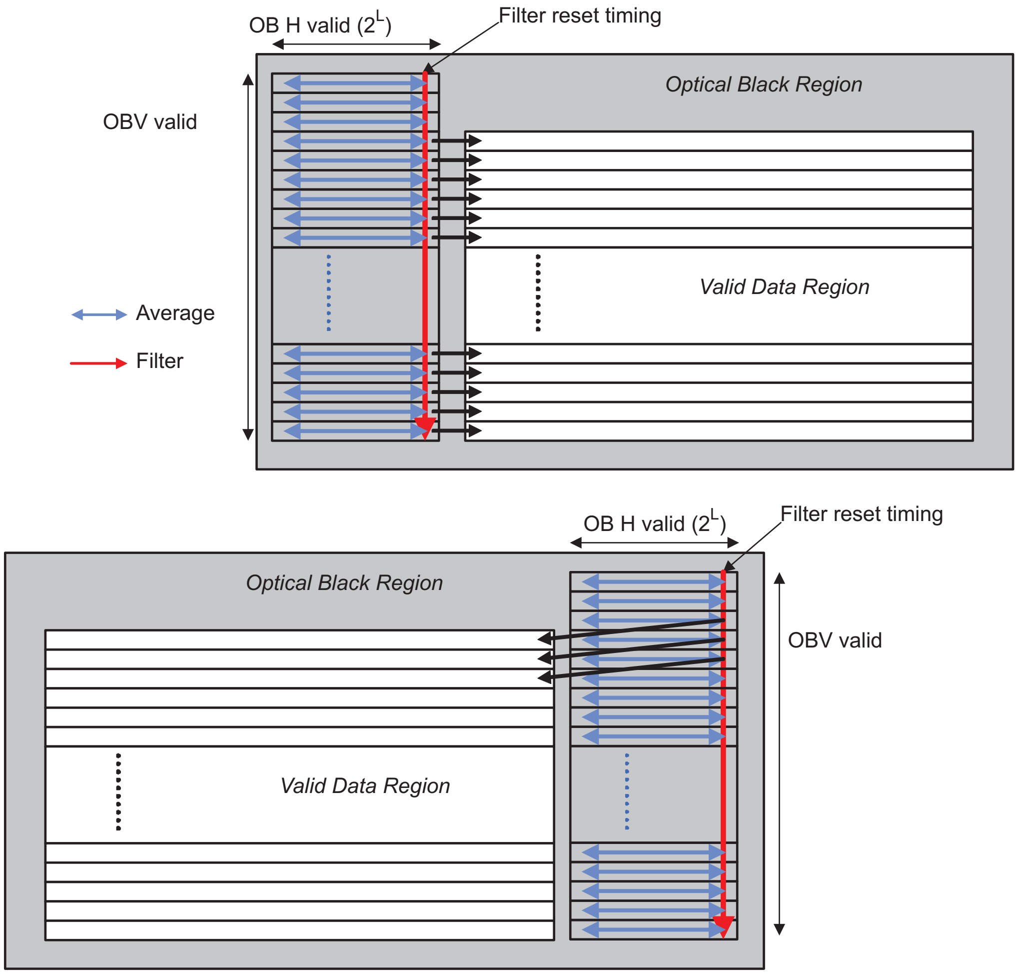
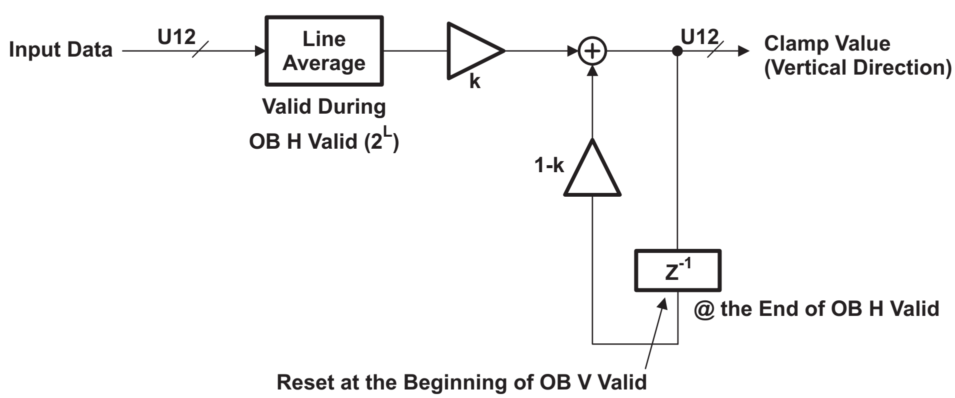


Figure 4-23. Clamp Value for Vertical Direction (2)



$$ClampValue(Vn) = LineAverage(Vn) \bullet k + ClamValue(Vn-1) \bullet (1-k)$$

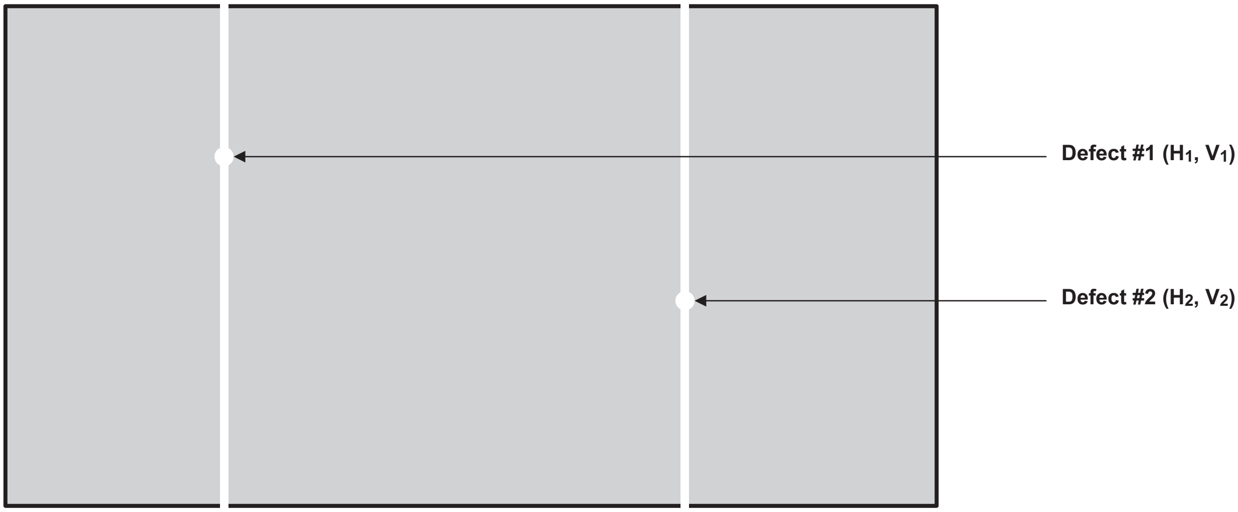
The register which holds the clamp value for the previous line is reset at the beginning of the OB V valid. The reset value can be selected from:

- Value set via the configuration register. (CLVRVSL=1)
- The base value calculated for Horizontal direction. (CLVRVSL=0)
- No update (same as the previous image). (CLVRVSL=2)

4.1.3.4 Vertical Line Defect Correction

The vertical line defect correction block can correct up to eight vertical line defects.

Figure 4-24. Vertical Line Defects



Vertical line defects are corrected by subtracting the defect level (method 1), or replaced by the average of pixel (i-2) and pixel (i+2) (method 2).

For method 1, the defect level is defined for the point of the defect, for the pixels upper than the defect, and for the pixels lower than the defect. If the data to be corrected are saturating, they are linear interpolated (replaced by the average of pixel (i-2) and pixel (i+2)) instead, or just fed through.
data_corrected(H1, V1) = data(H1, V1) – SUBH1V1
data_corrected(H1, V1upper) = data(H1, V1upper) – SUBH1V1upper (V1upper < V1)
data_corrected(H1, V1lower) = data(H1, V1lower) – SUBH1V1lower (V1lower > V1)

The coordinates of the defects and the defect level should be set to the table prior to the processing. Defect correction of the pixels upper than the defect can be disabled by the bit field DFCCTL.VDFCUDA. Other features include:

- Set the coordinates of the defects and the value to be subtracted from the data to the table (8x50) as shown in Table 4-2, prior to the processing. Up to eight defects can be set
- The coordinates are 13-bit width for horizontal and vertical direction, so image size up to 8,192 x 8,192 is supported.
- Defect level (value to be subtracted from the data) is 8-bit width, but can be up-shifted up to 4 bits by VDFLSFT.
- The defect must be set from left to right as shown in Figure 4-25.
- Defect correction of the pixels upper than the defect can be disabled by bye bit field DFCCTL.VDFCUDA.

Figure 4-25. The Order of the Vertical Line Defects

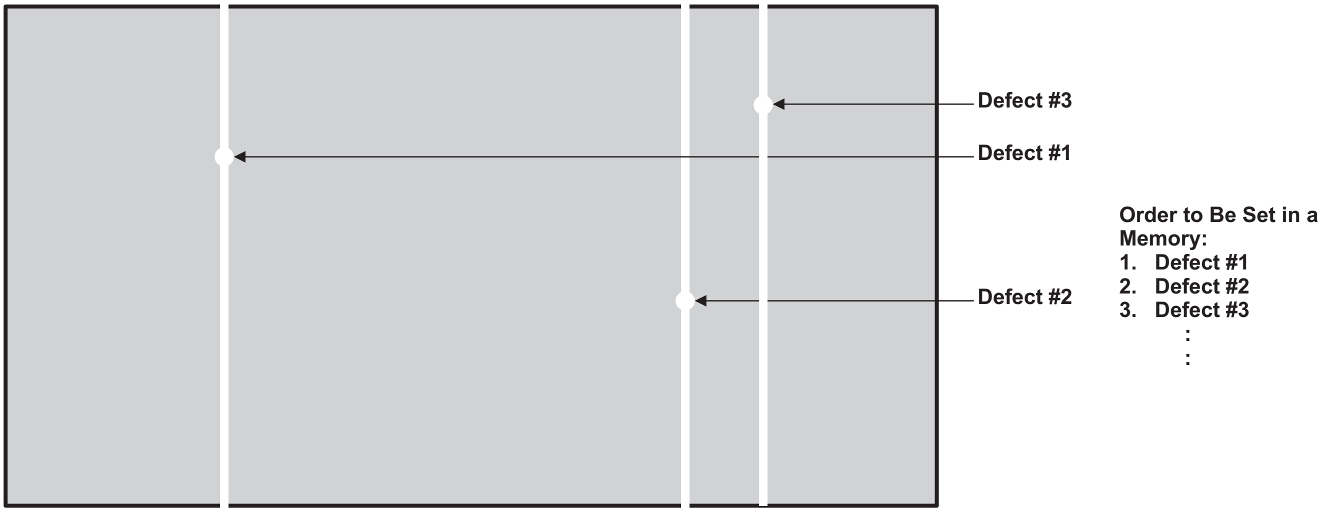


Table 4-2. Vertical Line Defect Information Table

Bit	Defect Information
12:0	Vertical position of the defects
25:13	Horizontal position of the defects
33:26	Defect level of the Vertical line defect position (V = Vdefect)
41:34	Defect level of the pixels upper than the Vertical line defect (V < Vdefect)
49:42	Defect level of the pixels lower than the Vertical line defect (V > Vdefect)

The correction method is common to all the defects, and can be selected from the following three by VDFCSL.

- Defect level subtraction. Just fed through if data are saturating
- Defect level subtraction. Horizontal interpolation ((i-2)+(i+2))/2 if data are saturating
- Horizontal interpolation ((i-2)+(i+2))/2

4.1.3.4.1 Vertical Line Defect Table Update Procedure

The following steps includes the update procedure for the vertical line defect table.

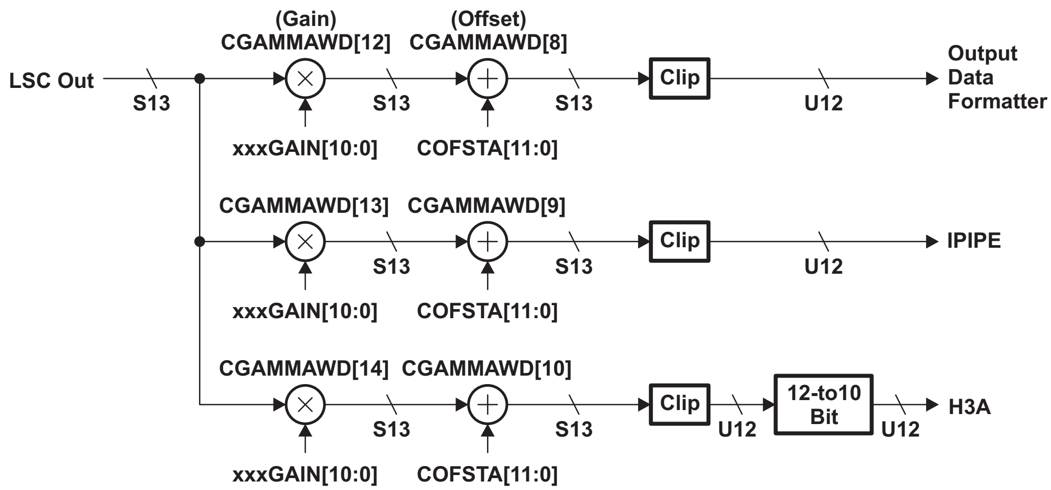
1. Make sure that VDFCEN is disabled
2. Write the V coordinate of the first defect to DFCMEM0, and the H coordinate to DFCMEM1. Also set the defect level to DFCMEM2 - DFCMEM4 if the correction method is 0 or 1
3. Set ‘1’ to DFCMWR with DFCMARST set
4. Wait until DFCMWR gets cleared, and write the next data to DFCMEM0 - DFCMEM4
5. Set ‘1’ to DFCMWR with DFCMARST cleared
6. Repeat 4~5 until all entries are written to the Vertical line Defect table.
7. In case the defect entry is less than 8, an extra write cycle is required to fill the next table location with a certain value. Clear DFCMEM0 to all '0', set DFCMEM1 to all '1', and set ‘1’ to DFCMWR with DFCMARST cleared
8. Enable Vertical line Defect Correction by setting VDFCEN

4.1.3.5 Gain and Offset

There are color-dependent gain controls for SDRAM, IPIPE, and H3A paths. Gain applied to each data is selected according to the pixel position and the color pattern settings (CCOLP). Gain factors are U12Q9 which ranges from 0 to 7+511/512, and common for all the paths. Gain control can be enabled or disabled individually for each path.

After the gain control, a single offset value can be added to each path individually. The offset value is U12 which ranges from 0 to 4,095. Data (S13) are then truncated to U12.

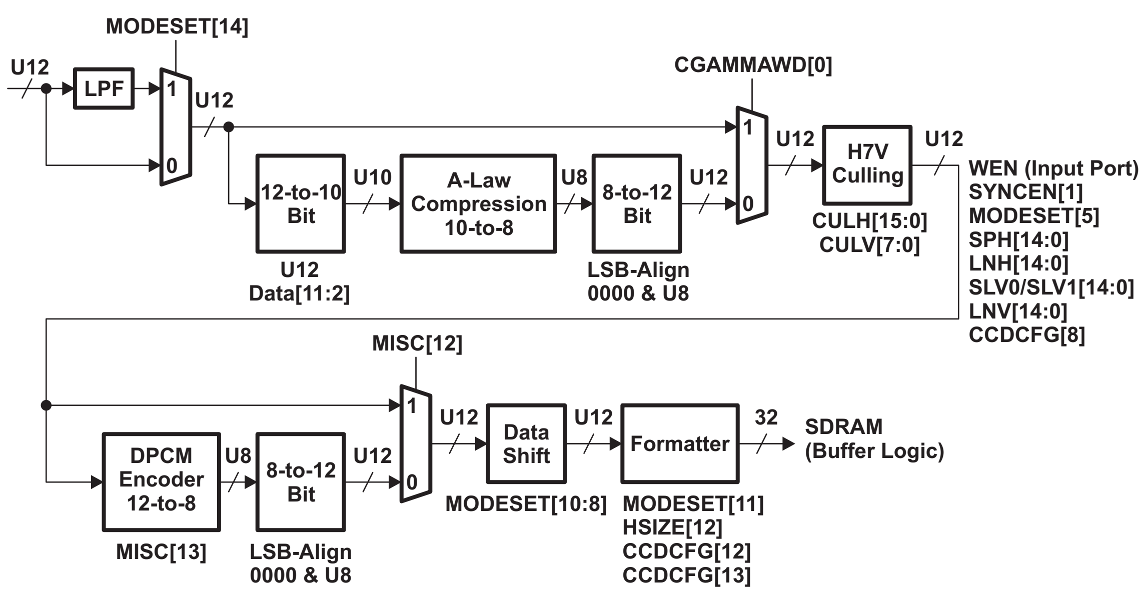
Figure 4-26. Gain and Offset



4.1.3.6 Output Formatter for SDRAM

The final stage of the RAW Data processing is the Output Formatter for DDR/SDRAM, which is shown in Figure 4-27.

Figure 4-27. Output Formatter Block Diagram



4.1.3.7 Low Pass Filter

The output formatter block provides an option for applying an anti-aliasing filter for horizontal culling. The low-pass filter consists of a simple three-tap filter.

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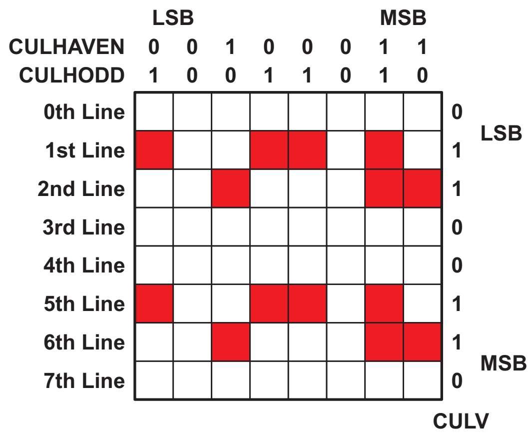
4.1.3.8 Culling

The culling block performs a programmable decimation function for both horizontal and vertical directions. The horizontal and vertical decimation of image data can be controlled by 2 registers. The 16-bit CULH register specifies the horizontal culling pattern for even and odd lines. The 8-bit CULV register specifies the pattern for the vertical direction. The LSB of CULV represent the top line of the CCD, the MSB is the 7th line. The figure below is an example showing how CULH and CULV apply a decimation pattern to the data. The pixels colored in red are transferred to DDR/SDRAM. In this case CULH = 0x59C4 and CULV = 0x0066.

Figure 4-28. Decimation Pattern



4.1.3.9 12 to 8-bit DPCM Compression

The DPCM compression block can compress 12-bit image data to 8-bit data for bandwidth reduction in transmission between the ISIF and the SDRAM. The IPIPE interface uses the 8-bit to 12-bit DPCM decoder so that data can be decompressed for processing.

The compression system uses two different predictors; one is simple and the other is complex. Predictor1 is very simple, so the processing power and the memory requirements are reduced with it (when the image quality is already high enough). Predictor2 gives a slightly better prediction for pixel value and the image quality can be improved with it.

4.1.3.10 SDRAM Data Storage

Data are stored to the lower bits of a 16-bit DDR/SDRAM word, or can be 8-bits or 12-bits packed. For raw data, data to be stored can be right-shifted according to the value set at CCDW.

Table 4-3 shows the format where data are stored to the lower bits of a 16-bit word and also the format where the data are packed to 8-bits. The unused bits are filled with zeros.

Table 4-3. SDRAM Data Format (1)

Bit	CCDW	SDR Pack	Upperword		Lowerword	
			MSB(31)	LSB(16)	MSB(15)	LSB(0)
12	0	0	0	Pixel1	0	Pixel0
11	1	0	0	Pixel1	0	Pixel0
10	2	0	0	Pixel1	0	Pixel0
9	3	0	0	Pixel1	0	Pixel0
8	4	0	0	Pixel1	0	Pixel0
8-bit pack	4	2	Pixel3	Pixel2	Pixel1	Pixel0

Table 4-4 shows the format in which 12-bit data are packed.

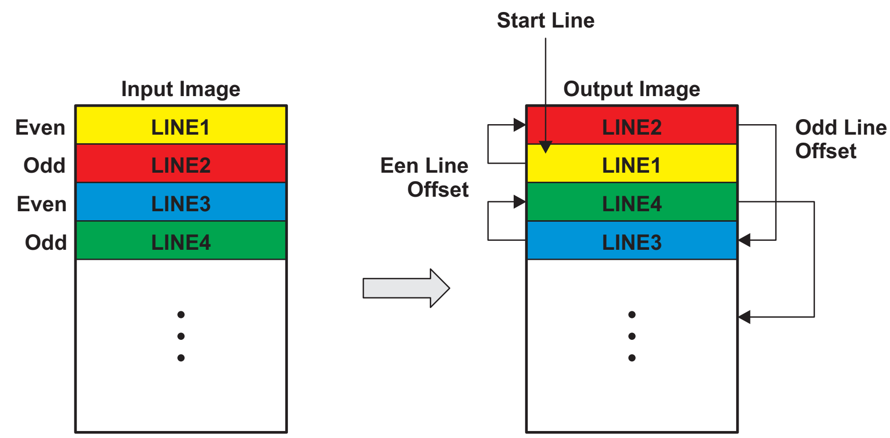
Table 4-4. SDRAM Data format (2)

Bit	CCDW	SDR Pack	Upperword		Lowerword	
			MSB(31)	LSB(16)	MSB(15)	LSB(0)
12	0	1	Pixel2[7:0]		Pixel1	Pixel0
			Pixel5[3:0]	Pixel4	Pixel3	Pixel0
				Pixel7	Pixel6	Pixel5[11:4]

The ISIF has an internal, 16-bit by 16-bytes FIFO. The processed data are transferred from the FIFO to the buffer logic in 32-byte burst unit. The frequency of the SDRAM clock must be equal to or higher than the pixel clock. Data are written to SDRAM only if DWEN in SYNCEN is set to "1."

The output formatter can configure to any image format by using SDRAM line offset register, and offset control registers. The next figure shows how to construct a frame format in SDRAM.

Figure 4-29. Frame Image Format Conversion

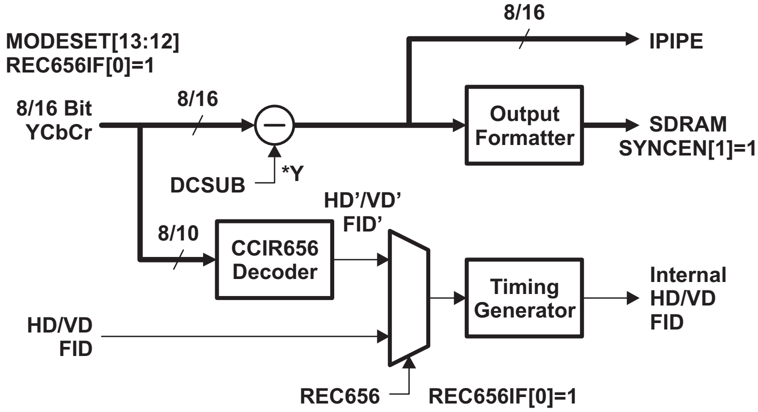


4.1.4 YCbCr Signal Processing

Figure 4-30 shows the YCbCr signal processing flow in the ISIF block. The ISIF accepts 4:2:2 sampled YCbCr input data. The luminance and chrominance are 8 bits each, scaled 0 to 255. The color difference signals are multiplexed into one 8-bit bus beginning with a Cb sample. The Y and CbCr busses may be input parallel (16-bit mode) or may be time-multiplexed and input as a single bus (8-bit mode). The single bus may also contain SAV and EAV video timing reference codes (ITU-R BT.656 mode). In ITU-R BT.656 mode, the ISIF is controlled by the start active video (SAV) time code in the 8-bit pixel data. All timing information is transmitted using a 4-byte synchronization pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace ISIF decodes SAV code and is synchronized at this timing.

The 16-bit or 8-bit YCbCr data are stored in SDRAM as 4:2:2 format. Table 4-5 shows data format in SDRAM. Y data typically has a range of 16 to 235, however, it is possible to subtract a DC value from Y signal.
减去

Figure 4-30. ISIF YCbCr Data Processing Flow



4.1.4.1 DC Subtract

An offset can optionally be subtracted from the luma (Y) component of the data by programming the CLDCOFST.CLDC register field. Note that in YCbCr processing, the CLAMPCFG.CLEN field must be disabled '0' or indeterminate results may occur.

4.1.4.2 REC656 Mode

Processing of the data in REC656 mode is identical to that of the other YCbCr modes; however, there is an additional decoder block that extracts the sync information from the data signal and generates the HD/VD/Field signals for downstream processing. If data width is 10 bits, configure ISIF to YCbCr 16-bit mode (MODESET.INPMOD=1), so that 10-bit data are stored to the lower 10 bits of a 16-bit SDRAM word.

4.1.4.3 SDRAM Data Storage

In packed YCbCr 4:2.2 mode, data are stored in SDRAM with two pixels per 32 bits, shown in Table 4-5.

Table 4-5. YCbCr Mode SDRAM Output Format

SDRAM ADDRESS	Upper Word		Lower Word	
	MSB(31)	LSB(16)	MSB(15)	LSB(0)
N	Y1	Cr0	Y0	Cb0
N+1	Y3	Cr1	Y2	Cb1
N+2	Y5	Cr2	Y4	Cb2

4.1.5 Data Output Control

Data output to SDRAM is enabled via the SYNCEN.DWEN setting. The MSB of the chroma signal can also be inverted (CCDCFG.MSBINVI). The ISIF module's final stage is the line output control, which controls how the input lines are written to SDRAM. The values CADU and CADL define the starting address where the frame should be written in SDRAM. The value, HSIZE.SDOFST, defines the distance between the beginning of output lines, in bytes. Both the starting address and line offset values are programmed in 32-byte units; i.e., either 16 or 32 pixels, depending on the HSIZE.PACK8 setting. the HSIZE.ADCR register bit can be set to decrement the addresses across each line to invert an image horizontally. The register SDOFST can be used to define additional offsets depending on the Field ID and even/odd line numbers. This provides a means to de-interlace an interlaced, two-field input and also to invert an input image vertically. See Figure 4-29 for some examples of usage.

SDOFST.FIINV — invert interpretation of the Field ID signal

SDOFST.FOFST — offset, in lines, of field = 1

SDOFST.LOFTS0 — offset, in lines, between even lines on even fields (field 0)

SDOFST.LOFTS1 — offset, in lines, between odd lines on even fields (field 0)

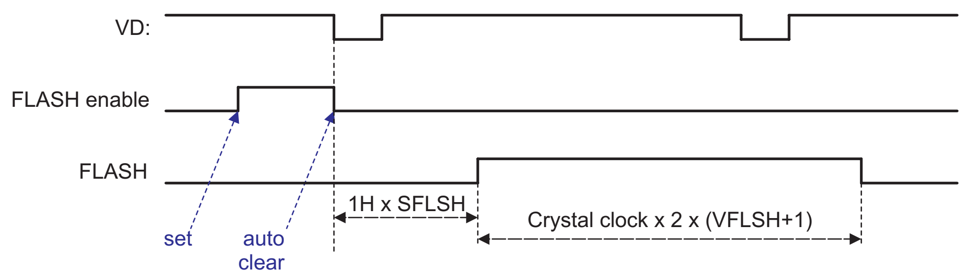
SDOFST.LOFTS2 — offset, in lines, between even lines on odd fields (field 1)

SDOFST.LOFTS3 — offset, in lines, between odd lines on odd fields (field 1)

4.1.6 Flash Timing Control

ISIF can generate a timing signal for FLASH to control the start time and the exposure period.

Figure 4-31. Flash Timing Signal



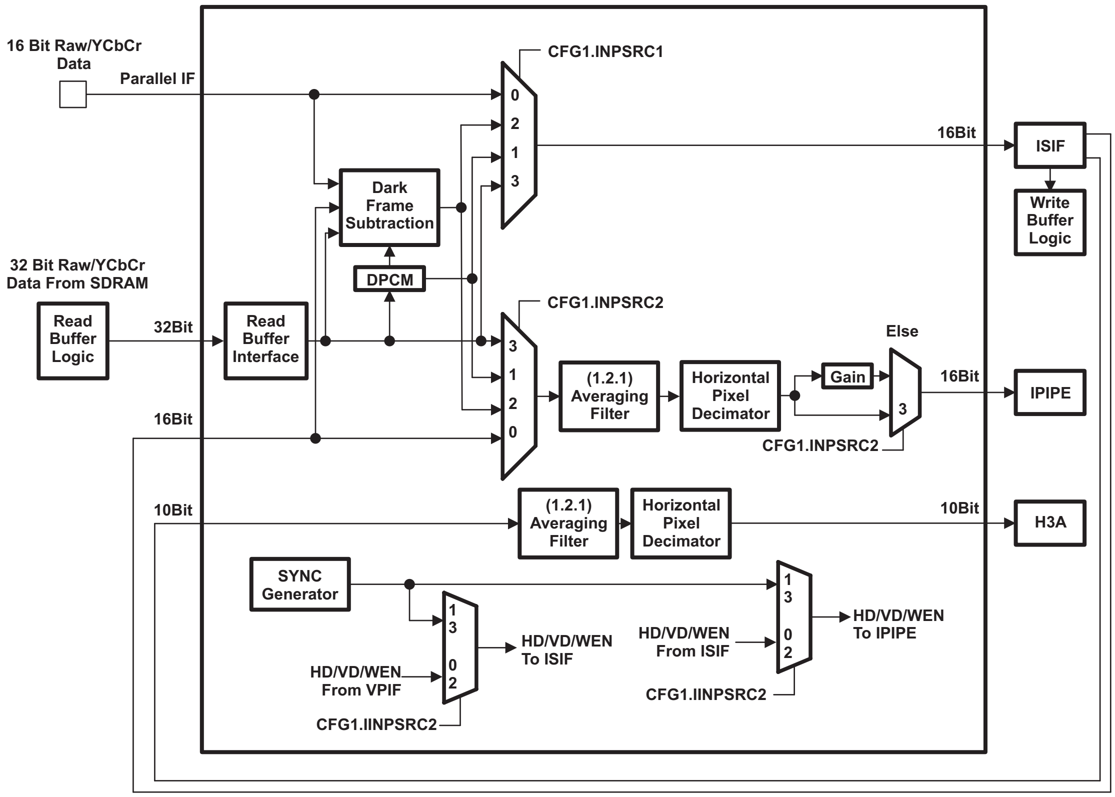
As shown in Figure 4-31, SFLSH is a configuration register that specifies the set timing of the FLASH signal, and VFLSH is a register that specifies the valid length of the FLASH signal. The FLASH signal is set at the beginning of the line specified by SFLSH, and remain high for Crystal clock x 2 x (VFLSH+1).

The VFLSH register is 16 bits wide, so if the Crystal clock is 48 MHz, the maximum length of the valid period will be 2.7 msec.

4.2 Image Pipe Interface (IPIPEIF)

The IPIPE Interface (IPIPEIF) is the data and sync signals input interface module for the IPIPE. The rest of this section describes the functionality of each sub-block in the IPIPEIF as shown in Figure 4-32.

Figure 4-32. Image Pipe Interface Processing Flow

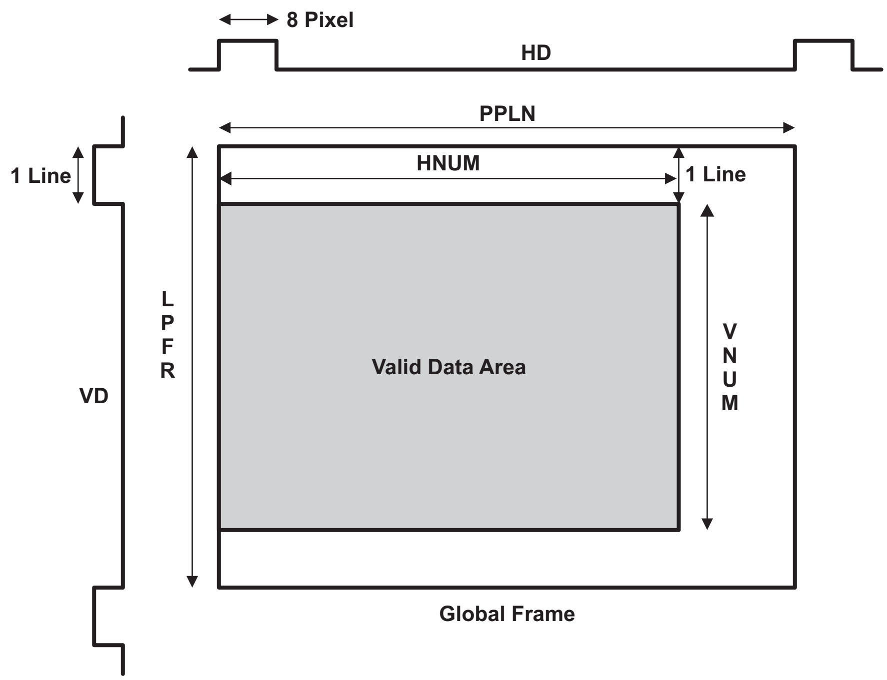


4.2.1 Input Interface and Preprocessing

The IPIPEIF consists of two major interface blocks. It can receive data from both the sensor parallel raw data via the device parallel port, and from the read buffer interface via SDRAM/DDRAM. The input sources and data type (RAW or YUV) are configured in the CFG1.INPSRC1 register field. IPIPEIF can also receive data from both the preprocessed raw data via the ISIF controller module and from the read buffer interface via SDRAM/DDRAM. The input sources and data type (RAW or YUV) are configured in the CFG1.INPSRC2 register field. The four available options for input source/type combinations and any preprocessing operations are discussed further in the following sub-sections.

When input from SDRAM/DDRAM is required, the SDRAM/DDRAM address (ADDRU, ADDRL) and line offset (ADOFS) registers must be programmed in units of 32 bytes. Additionally, the HNUM and VNUM registers define the number of pixels per line and lines per frame to read from the SDRAM as shown in Figure 4-33. For all SDRAM input modes except Darkfame subtract, the LPFR and PPLN registers define the interval of VD and HD, respectively.

Figure 4-33. Global Frame Definition in SDRAM Input Modes (except Darkframe)



4.2.2 ISIF Raw Input Mode (CFG1.INPSRC1 = CFG1.INPSRC2 = 0)

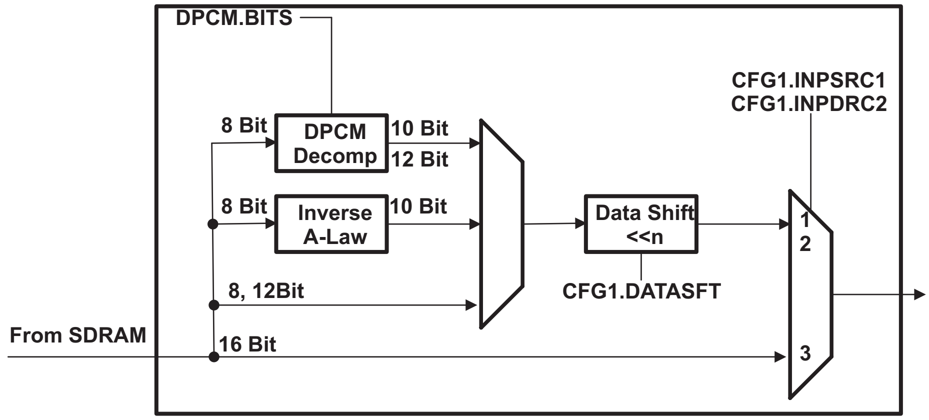
CFG1.INPSRC1
The input data is from the sensor parallel port and its data format is RAW (up to 16-bit).

CFG1.INPSRC2
The input data is from the video port interface of the ISIF and its data format is RAW (up to 12-bit)i

4.2.3 SDRAM RAW Input Mode (CFG1.INPSRC1 = CFG1.INPSRC2 = 1)

Figure 4-34 shows the DCPM sub-block that will be discussed in this section.

Figure 4-34. DPCM Sub-Block



When the input source is RAW data from the SDRAM read buffer interface, the data can either be read as 1 pixel for every 8 bits, or 16 bits in memory (CFG1.UNPACK). The 8-bit RAW data can either be linear or non-linear.

In order to save SDRAM capacity and bandwidth, the ISIF includes two options:

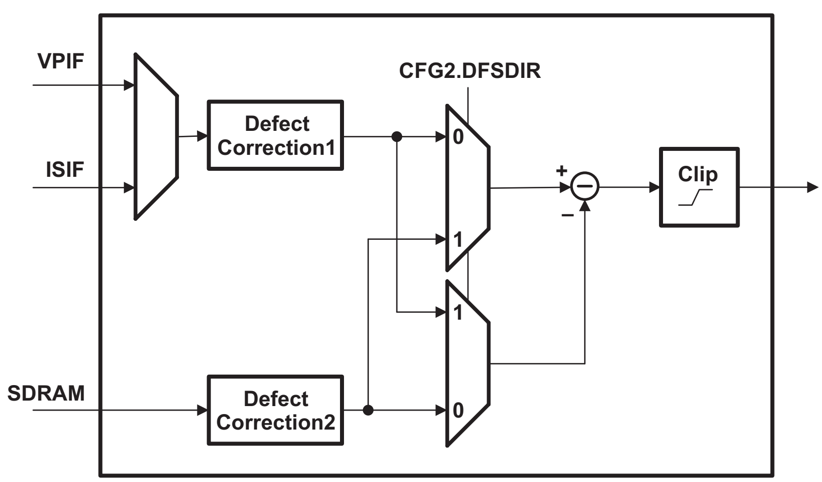
- Apply 10-bit to 8-bit A-Law compression for packing the sensor data to 1-byte per pixel. In order to process this data properly, the Inverse A-law block is provided to decompress the 8-bit non-linear data back to 10-bit linear data if enabled (CFG1.UNPACK). This 10 bit data is padded with four low zeros to form a 12-bit bus.
- Apply 12- bit to 8-bit DPCM compression for packing the sensor data to 1-byte per pixel. In order to process this data properly, the DPCM decompression block is provided to decompress the 8-bit compressed data back to 12-bit linear data if enabled (DPCM.ENA). This 12 bit data can be shifted by the CFG1.DATASFT register field to select which 12 bits to use

If the Inverse A-law and DPCM decompression are not enabled, then the data read from SDRAM can be shifted by the CFG1.DATASFT register field to select which 12 bits to use.

4.2.4 ISIF RAW Input with Dark Frame Subtract from SDRAM Mode (CFG1.INPSRC1 = CFG1.INPSRC2 = 2)

Figure 4-35 shows the DFS sub-block that will be discussed in this section.

Figure 4-35. DFS Sub-Block

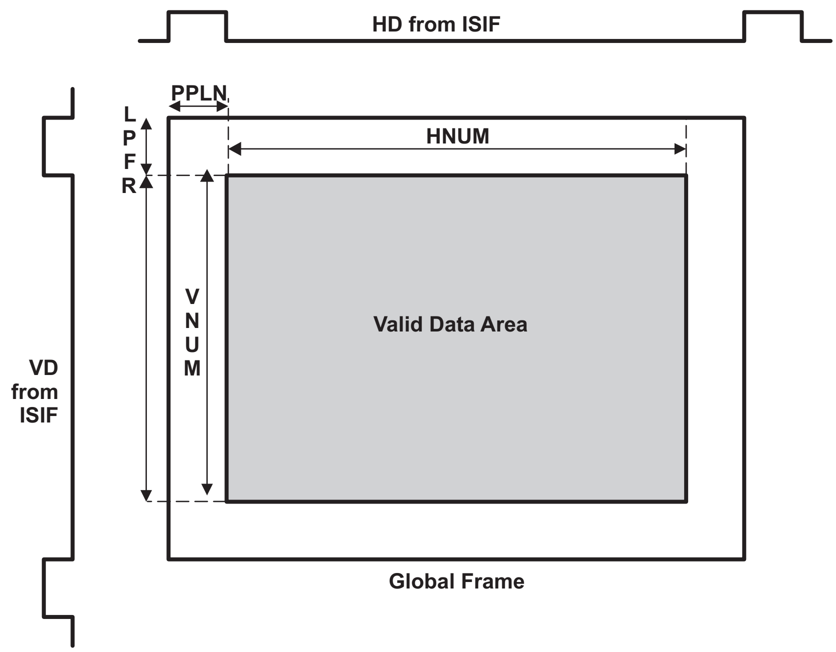


The dark frame subtract function is used to remove fixed pattern noise in the sensor. Typically, the ISIF writes a dark frame (frame captured when the shutter is closed) to SDRAM using 8 bits of linear data packed into two pixels per 16 bits. Eight bits should be enough even if the resolution of the RAW data is 12 bits, since a dark frame should not have values greater than 255 unless it is a fault pixel.

In this mode, everything from the previous two sections also applies since RAW data is used from both the ISIF and SDRAM. Data can also be read from SDRAM with CFG1.UNPACK set to ‘1’. Each pixel read from SDRAM will be subtracted from each pixel sent from the parallel I/F or the ISIF.

The output of the dark frame Subtract operation is 12-bits wide (U12Q0). There must be adequate SDRAM bandwidth if this feature is enabled. If the data fetched from memory arrives late, then there is no way of knowing. Also note that in dark frame subtract mode, the PPLN and LPFR registers should be used to indicate the horizontal and vertical start position of the subtraction from the ISIF data, as shown in Figure 4-36. The value of the LPFR must be greater than 0, since you cannot subtract the first line from the Parallel I/F or the ISIF.

Figure 4-36. Global Frame Definition in Darkframe Subtract Mode



4.2.5 SDRAM YCbCr 4:2:2 Input Mode

When the input source is YCbCr 4:2:2 data from the SDRAM read buffer interface, the data is expected to be stored as 16 bits in memory, so there is no shifting or other preprocessing done.

4.2.6 Timing Generation

When the input source is from the parallel port I/F (CFG1.INPSRC1 = 0 or 2), CFG1.CLKSEL should be set to ‘0’ so that data is latched into the IPIPE using the PCLK, HD, and VD signals from the parallel port I/F.

When the input source is from the video port interface of the ISIF (CFG1.INPSRC2 = 0 or 2), CFG1.CLKSEL should be set to ‘0’ so that data is latched into the IPIPE using the PCLK, HD, and VD signals from the ISIF.

When the input source is not from the parallel port I/F (CFG1.INPSRC1 = 1 or 3), then CFG1.CLKSEL should be set to ‘1’ so that the IPIPEIF generates the proper timing of PCLK, HD, and VD signals to the IPIPE. The CLKDIV register is then used to select a divide ratio of the SDRAM(DMA) clock for the pixel clock frequency which is used to clock the data into the PCLK.

When the input source is not from the ISIF (CFG1.INPSRC2 = 1 or 3), then CFG1.CLKSEL should be set to ‘1’ so that the IPIPEIF generates the proper timing of PCLK, HD, and VD signals to the IPIPE. The CLKDIV register is then used to select a divide ratio of the SDRAM(DMA) clock for the pixel clock frequency which is used to clock the data into the PCLK. The value of this register depends on the resize ratios of the IPIPE resizers and the available SDRAM system bandwidth.

When CFG1.INPSRC1 or CFG1.INPSRC2 is not set to ‘0’, then the IPIPE I/F SDRAM data reading and timing generation can be enabled (ENABLE.ENABLE) in either one-shot mode, or continuous mode (CFG1.ONESHOT).

The SDRAM input function (1 or 3) either CFG1.INPSRC1 or CFG1.INPSRC2 can be selected. Only one can be selected at a time.

4.2.7 Averaging Filter (1,2,1)

The averaging filter can be optionally enabled by setting the CFG1.AVGFILT register bit. It acts as an anti-aliasing filter for the horizontal pixel decimator. It typically is only needed when the pixel decimator is used (CFG1.DECM = ‘1’). It operates on every pixel (same color) in a RAW bayer input or every Y component in YCbCr data in the following equation: $output = (input[i-1] + 2 * input[i] + input[i+1]) >> 2$

4.2.8 Horizontal Pixel Decimator (Downsizer)

The image pipe input is limited to 2176 pixels per horizontal line due to line memory width restrictions in the various filtering blocks. In order to support sensors that output greater than 2176 pixels per line, a line width decimator can be enabled (CFG1.DECM) to downsample the input lines to a width equal to or less than the 2176 pixel maximum. The resize ratio can be configured by programming the RSZ register to be within the range from 16 to 112, to give a resampling range from 1x to 1/7x (16/RSZ).

4.2.9 RAW Data Gain

A gain factor ranging from 0.00195(1/512) to 1.99805(1023/512) is multiplied to the RAW output of the IPIPEIF. The gain constant is set in the GAIN register using U10Q9 format.

4.2.10 Defect Pixel Correction

A simple defect pixel correction can be applied to the ISIF input data path and SDRAM input data path respectively. DPC parameters provide threshold level to be replaced with neighborhood pixel or averaged pixel.

4.3 Image Pipe (IPIPE)

Image Signal Processing (IPIPE) is a programmable hardware image processing module that generates image data in YCbCr-4:2:2 or YCbCr-4:2:0 format from raw CCD/CMOS data. IPIPE can also be configured to operate in a resize-only mode, which allows YCbCr-4:2:2 or YCbCr-4:2:0 to be resized without applying the processing of other modules in IPIPE. In addition, IPIPE supports output of Bayer data. The data processing paths can be configured by setting the SRC_FMT.FMT field. The output of the IPIPE is typically used for both video/image compression and display.

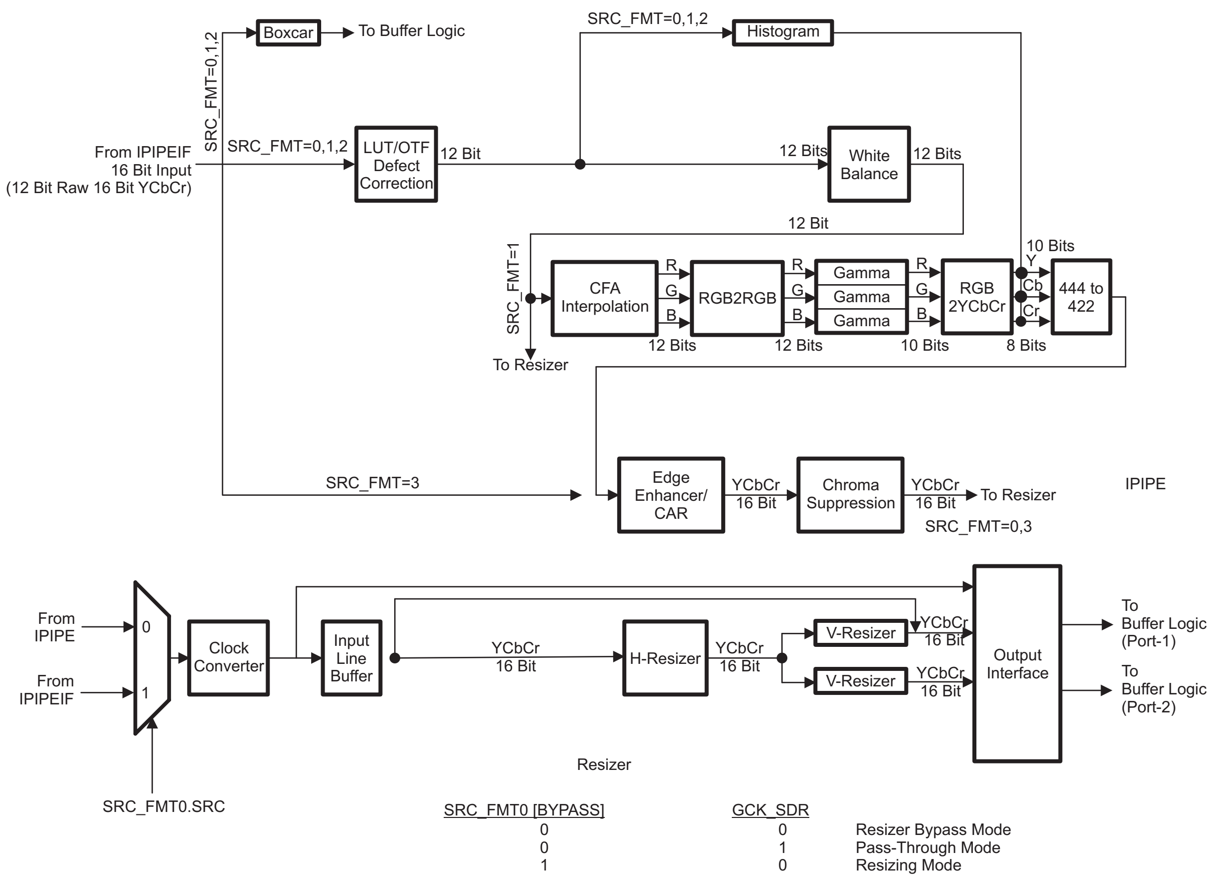
4.3.1 Data Flow in IPIPE

IPIPE has three different processing paths.

- Case 1: IPIPE reads CCD raw data and applies all IPIPE functions and stores the YCbCr (or RGB) data to SDRAM.
- Case 2: IPIPE reads CCD raw data and stores the Bayer data after white balance to SDRAM.
- Case 3: IPIPE reads YCbCr-422 data and applies edge enhancement, chroma suppression, and Resize to output YCbCr (or RG B) data to SDRAM.

IPIPE data flow is shown in Figure 4-37

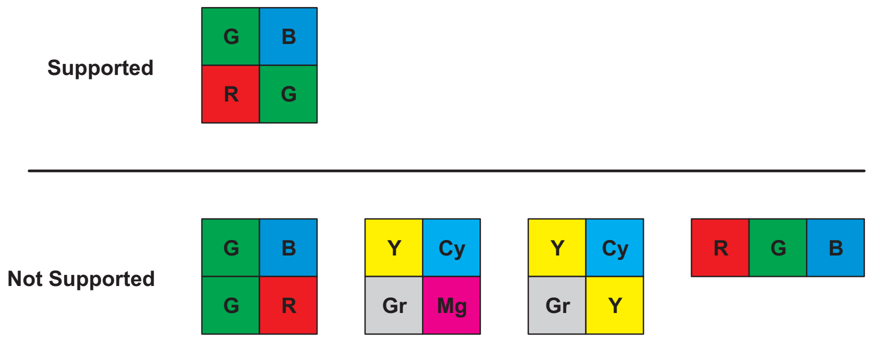
Figure 4-37. IPIPE Data Flow



4.3.2 CFA Arrangements

IPIPE supports raw data in Bayer formats as shown in Figure 4-38. Other RGB formats or complementary color formats are not supported.

Figure 4-38. Conventional 2x2 CFA Formats



4.3.3 Input Interface

The IPIPE engine receives 12-bit RAW image data or 16-bit YCbCr data via IPIPEIF. IPIPE can work with up to 2176 pixels in each horizontal line, except in RAW pass-through mode. If the image width is larger than 2176, it must be scaled down at IPIPEIF. Otherwise, the input image must be split into several blocks. If the input data is YCbCr, all RGB processing modules are skipped, and only edge enhancer, chroma artifact reduction (CAR), chroma suppression, and resizer are applied to the input data. If the input data is YCbCr-420, only Y or C may be processed at a time, and only the resizer process can be applied. In RAW pass-through mode, images up to 8190 pixels per line may be processed. In RAW pass-through mode, the input data is directly written out to SDRAM.

The input to IPIPE is in the following formats.

Table 4-6. IPIPE Input Format

IPIPE Input	RAW	LOW	LOW	LOW	LOW	RAW11	RAW10	RAW9	RAW8
	YCbCr 16 bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	Y 8 bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	CbCr 8 bit	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
IPIPE Input	RAW	RAW7	RAW6	RAW5	RAW4	RAW3	RAW2	RAW1	RAW0
	YCbCr 16 bit	Cb/Cr7	Cb/Cr6	Cb/Cr5	Cb/Cr4	Cb/Cr3	Cb/Cr2	Cb/Cr1	Cb/Cr0
	Y 8 bit	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
	CbCr 8 bit	Cb/Cr7	Cb/Cr6	Cb/Cr5	Cb/Cr4	Cb/Cr3	Cb/Cr2	Cb/Cr1	Cb/Cr0

4.3.4 LUT Defect Correction

The look-up-table (LUT) defect pixel correction is the first stage of the IPIPE image-processing pipeline. The LUT defect correction module fixes defects in input data. LUT defect correction module supports up to 256 defect point table. However, the table may be renewed as required during image processing. Therefore the maximum number of defect information is only limited by system level performance. The module uses two sets of 128x29 memories to hold defect information. The table contains the information of horizontal position (13 bits), vertical position (13 bits), and correction method (3 bits) as shown in Table 4-7. The information must be listed in the order of "from left to right" and "from the top to the bottom." The first position in defect information table and the number of defects which are actually used may be specified through register values. For correcting border pixels (top, bottom, left and right), data are properly mirrored.

Table 4-7. Defect Information Packing

Correction Method	Vertical Position	Horizontal Position
28..26	25..13	12..0

The correction methods are described in Table 4-8. The pixels in defect correction methods are numbered as shown in Figure 4-39.

Table 4-8. LUT Methods

Method	Processing
0	Replace with black dot (or a white dot) to force OTF-DPC to work on the pixel
1	Copy from left (d4)
2	Copy from right (d5)
3	Horizontal interpolation (d4+d5)/2
4	Vertical interpolation (d2+d7)/2
5	Copy from top d2
6	Copy from bottom d7
7	2D interpolation (d2+d4+d5+d7)/2

Figure 4-39. Numbering in Defect Correction Algorithm

d1		d2		d3
d4		d0		d5
d5		d7		d8

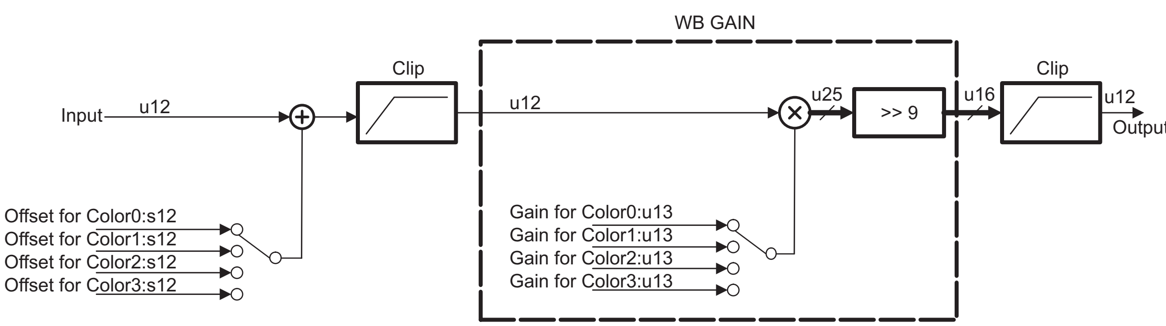
4.3.5 White Balance

The white balance module executes white balance to each color component. White balance gains adjust a ratio of each color in a CFA pattern.

Figure 4-40 shows a block diagram of this white balance module. In the white balance gain adjuster, the raw data is multiplied by a selected gain corresponding to the color. The white balance gain can be selected from four 13-bit values. Firmware can assign any combination of four pixels in the horizontal and vertical direction. The precision of each gain is as follows:

- OFFSET: -2048 to +2047
- WB GAIN: x 0 – x 15.998 (step = 1/512)

Figure 4-40. White Balancing in IPIPE



4.3.6 RGB2RGB Blending Module

The RGB2RGB blending module transforms the RGB data generated by the CFA interpolation module using a 3×3 square matrix transformation in combination with an added offset. The RGB to RGB blending is calculated using the following formula. Each gain range is from -8 to +7.996 with step 1/256 = 0.004. The offset is -4096 to 4095.

$$\begin{pmatrix} R\_out \\ G\_out \\ B\_out \end{pmatrix} = \begin{pmatrix} gain\_RR & gain\_GR & gain\_BR \\ gain\_RG & gain\_GG & gain\_BG \\ gain\_RB & gain\_GB & gain\_BB \end{pmatrix} \begin{pmatrix} R\_in \\ G\_in \\ B\_in \end{pmatrix} + \begin{pmatrix} offset\_R \\ offset\_G \\ offset\_B \end{pmatrix}$$

4.3.7 Gamma Correction Module

The gamma correction module performs a gamma correction independently for each color in the RGB color space by using a piece-wise linear interpolation. The ROM table and RAM table are selectable through a register. Each RAM table has 512 entries, and each entry accommodates a 10-bit offset and 10-bit slope (see Figure 4-43). The range of slope value is from -512 to +511. The ROM table has 1024 entries and an output of 8-bit value. As shown in Figure 4-32, this module exists independently for each color so that the independent setting is possible. Figure 4-41 shows a block diagram of the gamma correction module. It is composed of two tables and one selector. When the BYPASS bit is asserted, the input data is divided by 16. Figure 4-42 shows an example of the gamma curve.

Figure 4-41. Gamma Correction Module Block Diagram

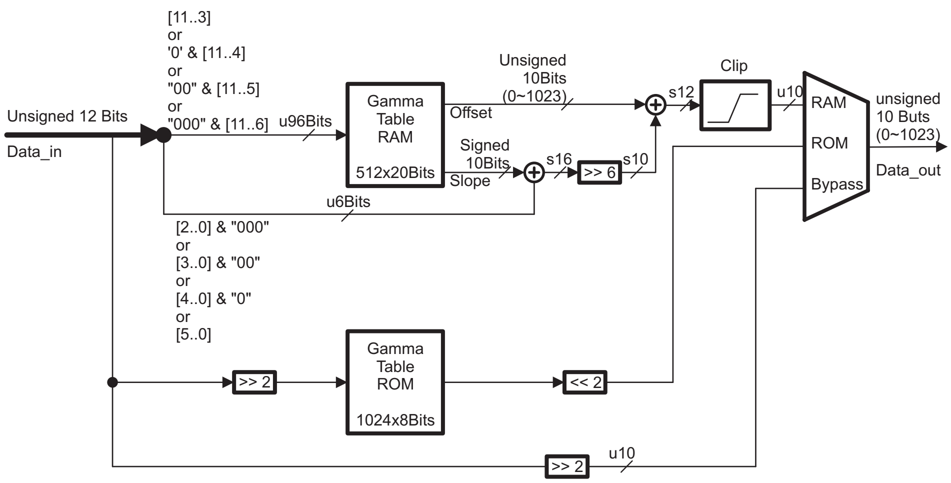


Figure 4-42. Example of Gamma Curve

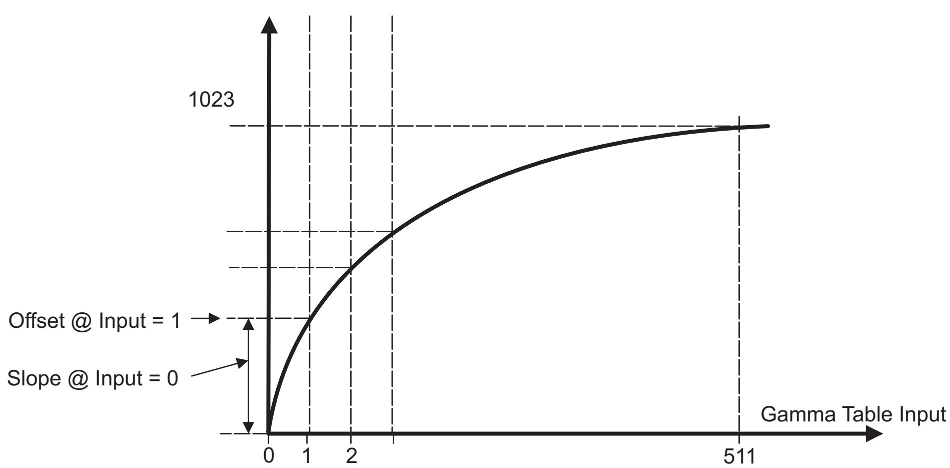


Figure 4-43. Gamma Table Offset/Slope Packing

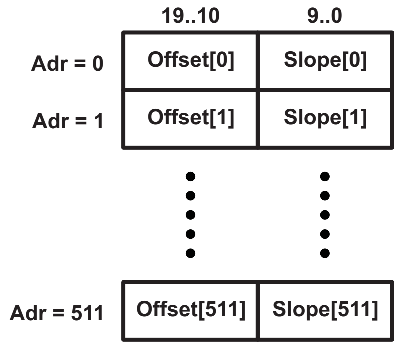


Table 4-9. LUT Memory Regions for Gamma Correction

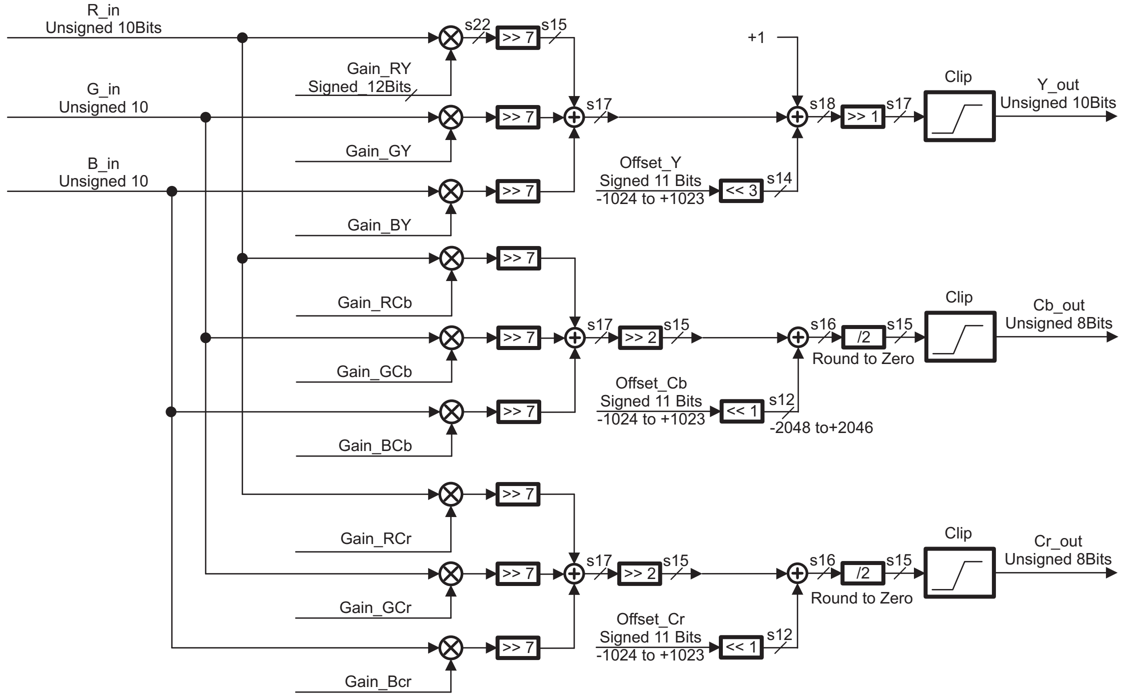
Memory Region	Address Range	Description
IPIPE_GAMR_TB	0x01C7A800 – 0x01C7AFFF	IPIPE Gamma LUT for R
IPIPE_GAMG_TB	0x01C7B000 – 0x01C7B7FF	IPIPE Gamma LUT for G
IPIPE_GAMB_TB	0x01C7B800 – 0x01C7BFFF	IPIPE Gamma LUT for B

4.3.8 RGB2YCbCr Conversion Matrix

This module transforms the RGB data to YCbCr data format using a 3x3 square matrix transformation in combination with an added offset. The transform is calculated using the following equation. Each gain range is from -8 to +7.996 with step 1/256 = 0.004. The offset is -1024 to 1023 for Y, Cb, and Cr. The block diagram of the RGB to RGB blending module is shown in the next page. The output is calculated by the following equation. The output is calculated with the following equation:

$$\begin{bmatrix} Y\_out \\ Cb\_out \\ Cr\_out \end{bmatrix} = \begin{bmatrix} gain\_RY & gain\_GY & gain\_BY \\ gain\_RCb & gain\_GCb & gain\_BCb \\ gain\_RCr & gain\_GCr & gain\_BCr \end{bmatrix} \begin{bmatrix} R\_in \\ G\_in \\ B\_in \end{bmatrix} + \begin{bmatrix} offset\_Y \\ offset\_Cb \\ offset\_Cr \end{bmatrix}$$

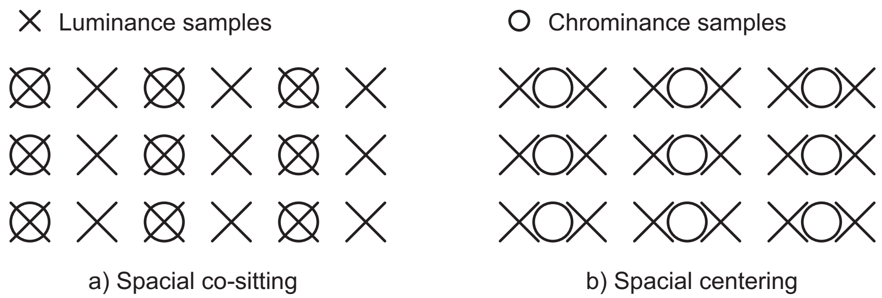
Figure 4-44. RGB2YCbCr Module Block Diagram



4.3.9 4:2:2 Conversion Module

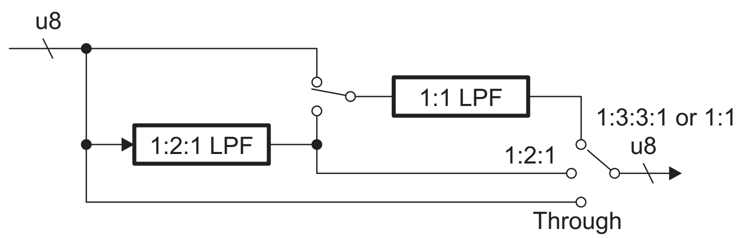
The 4:2:2 conversion module converts the image data to YCbCr-4:2:2 format by taking the average of every two Cb and Cr components. Y and Cb/Cr sampling point of either spatial co-sited or spatial centering are selectable. Horizontal 3 taps and 4 or 2 taps filters are used for spatial co-sited and spatial centering, respectively.

Figure 4-45. Chroma Sub-Sampling Position



A block diagram of 4:2:2 conversion module is shown in Figure 4-46.

Figure 4-46. 4:2:2 Conversion Functional Model



4.3.10 2D Edge Enhancer

The edge enhancer module operates on the luminance (Y data) component of images to improve the image quality. Edges in input images are detected by a 2D high-pass filter, and its sharpness is increased by the value from a non-linear table. A block diagram of the luminance non-linear edge enhancer is shown in Figure 4-47. Entry for the non-linear table is 10-bit and the output is in signed 9-bit.

In the edge enhancer, the linear filter with programmable coefficient is applied to the Y input. Here, M is 5x5 matrix with programmable coefficients.

$$HPF(h,v) = \left(\sum_{j=-2}^{2} \sum_{i=-2}^{2} M_{i,j} Y(h+i, v+j) \right) >> shf_{HPF},$$

$$M = \begin{pmatrix} M_{2,2} & M_{1,2} & M_{0,2} & M_{1,2} & M_{2,2} \\ M_{2,1} & M_{1,1} & M_{0,1} & M_{1,1} & M_{2,1} \\ M_{2,0} & M_{1,0} & M_{0,0} & M_{1,0} & M_{2.0} \\ M_{2,1} & M_{1,1} & M_{0,1} & M_{1,1} & M_{2,1} \\ M_{2,2} & M_{1,2} & M_{0,2} & M_{1,2} & M_{2,2} \end{pmatrix}$$

The HPF value is shrunk by a threshold value (u6) specified by a register, and clipped to signed 10 bits to get the index for the LUT.

$$index = clip\left(shrink\left(HPF, threshold_{HPF}\right), -512, 511\right)$$

$$shrink(x, threshold) = \begin{cases} x + threshold & x < -threshold \\ 0 & -threshold \le x \le threshold \\ x - threshold & threshold < x \end{cases}$$

$$clip(x, limit_{LOW}, limit_{HIGH}) = \begin{cases} -limit_{LOW} & x < -limit_{LOW} \\ x & -limit_{LOW} \le x \le limit_{HIGH} \\ limit_{HIGH} & limit_{HIGH} < x \end{cases}$$

The edge-enhancement intensity is looked up from the LUT.

$$E_{int} = LUT[index]$$

The mapping to the memory is shown in Table 4-10.

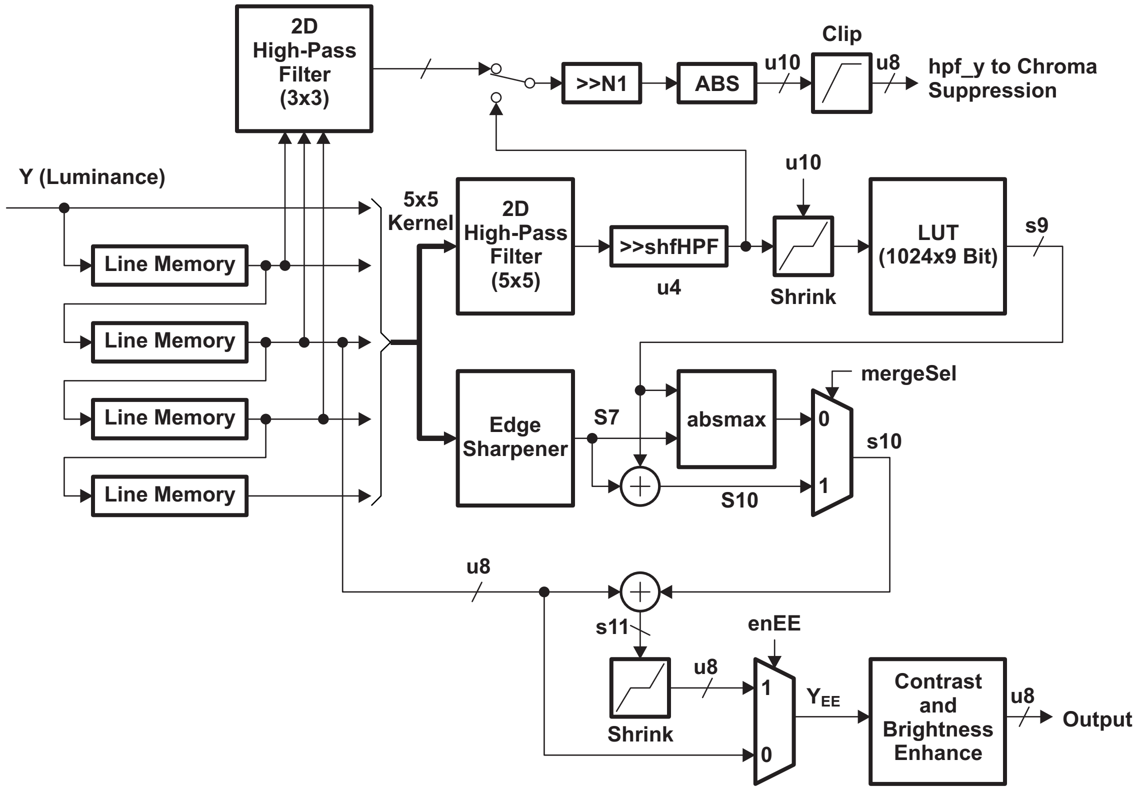
Table 4-10. Edge Enhancer LUT Mapping

Address (32-Bit Word Address)	Bit Position	LUT Index
0x00000h	8 .. 0	0
	17 ..9	1
0x00001h	8 .. 0	2
	17 .. 9	3
0x00002h	8 .. 0	4
	17 .. 9	5
0x00003h	8 .. 0	6
	17 .. 9	7
. . .	. . .	. . .
0x000FFh	8 .. 0	510
	17 .. 9	511
0x00100h	8 .. 0	-512
	17 .. 0	-511
0x00101h	8 .. 0	-510
	17 .. 9	-509
. . .	. . .	. . .
0x001FD	8 .. 0	-6
	17 .. 9	-5
0x001FE	8 .. 0	-4
	17 .. 9	-3
0x001FFh	8 .. 0	-2
	17 .. 9	-1

Table 4-11. LUT Memory Regions for Edge Enhancement Module

Memory Region	Address Range	Description
IPIPE_YEE_TB	0x01C78800 – 0x01C78FFF	IPIPE Edge Enhancement LUT

Figure 4-47. 2D Edge Enhancer Block Diagram



The edge sharpener module enhances edge clarity without producing Halo artifact. In this module, edge intensity is derived by the following 2D linear filter with fixed coefficients.

$$S_{i,j} = \begin{pmatrix} 0 & -1 & -2 & -1 & 0 \\ -1 & 0 & 2 & 0 & -1 \\ -2 & 2 & 8 & 2 & -2 \\ -1 & 0 & 2 & 0 & -1 \\ 0 & -1 & -2 & -1 & 0 \end{pmatrix}$$

$$sharpness(h,v) = clip\left(shrink\left(g \sum_{j=-2}^{2} \sum_{i=-2}^{2} S_{i,j} Y(h+i, v+j), -threshold_{LOW}, threshold_{LOW} \right) >> 6, threshold_{HIGH} \right)$$

The gain (g) and threshold values for the shrink/clip function (thresholdLOW, thresholdHIGH) are determined by register values. The bit width of g and $threshold_{HIGH}$ is in u6, and $threshold_{LOW}$ is in u6.6.

This edge intensity is then clipped by a threshold value.

$$S_{int} = \begin{cases} clip(sharpness, grad) & \text{Halo reduction on} \\ sharpness & \text{Halo reduction off} \end{cases}$$

The threshold value (grad) is a function of the activity around the target pixel, which is derived from gradient values.

Capping with gradient value prevents overly enhancing edges, and suppresses halo artifacts around edges. The output from EdgeEnhancer and EdgeSharpner are merged with the following function.

$$E_{merge} = \begin{cases} E_{int} + S_{int} & mergedsel = 1 \\ abs\,max\left(E_{int}, S_{int}\right) & mergedsel = 0 \end{cases}$$

$$abs\,max(x, y) = \begin{cases} x & abs(y) \le abs(x) \\ y & otherwise \end{cases}.$$

The E_{merge} value is added to the Y input value to make the final output.

For the chroma suppression, another 2D high pass filter (HPF) is implemented. One of the following four coefficient sets is selectable.

$$\begin{pmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{pmatrix}, \begin{pmatrix} 0 & 0 & 0 \\ 1 & -2 & 1 \\ 0 & 0 & 0 \end{pmatrix}, \begin{pmatrix} 0 & 1 & 0 \\ 0 & -2 & 0 \\ 0 & 1 & 0 \end{pmatrix}, or \begin{pmatrix} 0 & 1 & 0 \\ 1 & -4 & 1 \\ 0 & 1 & 0 \end{pmatrix}$$

At the end of the edge enhancer process, brightness and contrast adjust is applied to the Y signal. The process is described by the equation below.

$$Y_{ctr\_brt} = clip8\left(clip8\left(\left(Y_{EE} \times CTR\right) \gg 4\right) + BRT\right)$$

$$clip8(x) = \begin{cases} x & x \le 255 \\ 255 & 255 < x \end{cases}$$

Here, YEE is the output of the edge enhancer, CTR is a u4.4 contrast enhancement factor (YUV_ADJ[CTR]), BRT is a u8 brightness enhancement factor (YUV_ADJ[BRT]), and Y_{CTR_BRT} is the output as shown in Figure 4-47.

4.3.11 Horizontal and Vertical Resizer Module

The resizer module is capable of re-scaling images into various sizes ranging from x1/16 scale-down to x16 scale-up. Also, resizer uses averaging method for down scaling. The data flow diagram of the Resize module is described in Figure 4-48. After the resizing process, the processed data are transferred to the SDRAM. Table 4-12 shows the format of YCbCr image data in SDRAM.

The scaling process is carried out using interpolation with 4-tap filter. The interpolation method is either 4-tap cubic convolution, or 3-tap linear filter + 2-tap linear interpolation depending on the user's choice. The range of resizing ratio is determined by two parameters HRSZ and VRSZ, which may be set independently. The resizing ratio of the output image equals to 256/ HRSZ for horizontal process and 256/VRSZ for vertical process. The upper and lower limits of HRSZ and VRSZ are 16 and 4096, which correspond to x16 scale-up and x1/16 scale-down, respectively. This module is capable of producing two output images simultaneously (resize-1 and resize-2). The sizes of output images are limited to below 2176 pixels/line for resize-1 and below 1088 for resize-2 in normal mode. In down-scale mode, the output with is limited to below 1088 pixel/line for resize-1, and below 544 pixel/line for resize-2.

The interpolation method used in resizing is either 4-tap cubic convolution or 2-tap linear interpolation for horizontal direction. Assume input signals are,

$i_0, i_1, i_2, ..., i_n, ...$

and the output signals are

$o_0, o_1, o_2, ..., o_m, ...,$

as shown in Figure 4-49. Then, the output pixel o_m is produced by the following equation

$$0_m = h(1+d)i_{n-1} + h(d)i_n + (d-1)i_{n-1} + h(d2)i_{n-2}$$

where

$$n = \text{floor}\left(\frac{(mN+p)}{256}\right)$$

$$d = \frac{(mN+p)}{256} - n$$

Here, h(x) is an interpolation function, floor(x) is the smallest integer which does not exceed x, and p/256 is the position (or phase) of the first output pixel. The interpolation function h(x) may be selected from cubic convolution of linear interpolation function shown in . Both 4-tap cubic convolution and 2-tap linear interpolation can be used for vertical resizing.

Figure 4-48. Horizontal and Vertical Resize Module

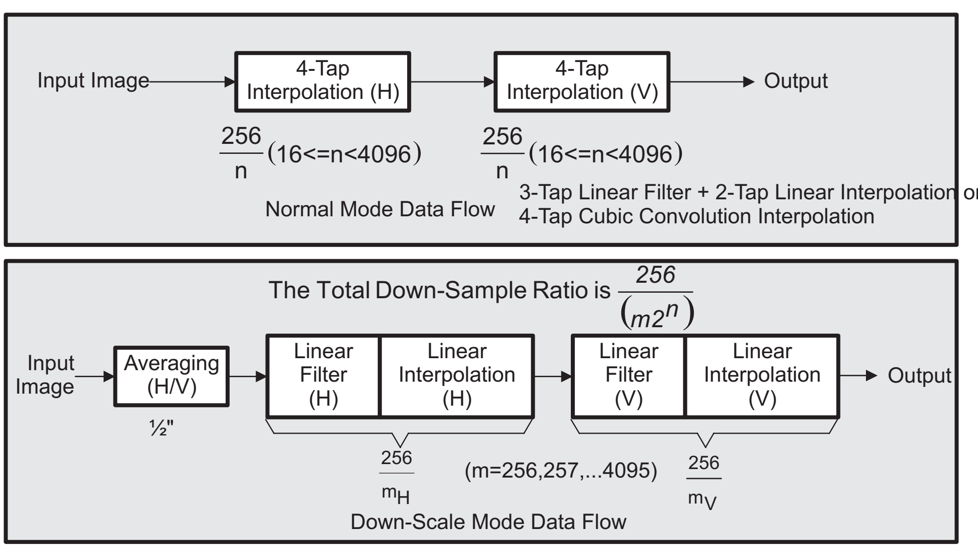
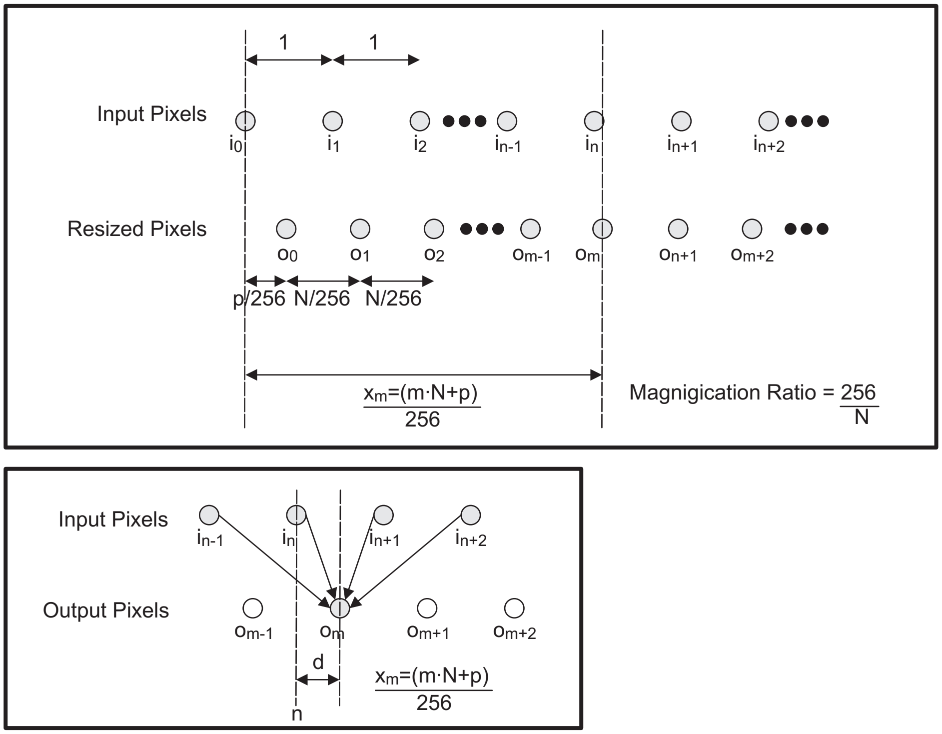


Figure 4-49. Interpolation Method



$$o_m = h(1+d)\cdot i_{n-1} + h(d)\cdot i_n + h(d-1)\cdot i_{n+1} + h(d-2)\cdot i_{n+2}$$

$$n = \text{floor}\left(\frac{mN+p}{256}\right) \qquad d = \frac{m\cdot N+p}{256} - n$$

Table 4-12. YcbCr-422 Memory Format

Byte address	4n	4n+1	4n+2	4n+3
YCbCr data	Cb0	Y0	Cr0	Y1

4.3.11.1 Resizer Performance

Scale-up performance of the module depends on the frequency ratio between the pixel clock and SDRAM clock. When the pixel and SDRAM clock are 40MHz and 200MHz respectively, the total scale-up capability is approximately (200MHz/40MHz) x 2pallaral-output = x10-scale-up, i.e. x6-scale-up for image-a and x4-scale-up for image-b. More precise measure of the performance limit is as following. The vertical resize ratio for image-a and image-b must satisfy.

$$\text{(horizontal size of input image)} \times \left(\frac{\text{SDRAM clock speed}}{\text{pixel clock speed}}\right) > ha \times ra + hb \times rb + overhead$$

where,

$$ha = \max(\text{width of input image - a, width of output image - a})$$
$$hb = \max(\text{width of input image - b, width of output image - b})$$
$$ra = \text{ceil}\left(\frac{\text{(vertical resize ration of image - a)}}{2}\right)$$
$$rb = \text{ceil}\left(\frac{\text{(vertical resize ration of image - b)}}{2}\right)$$
$$overhead = 70 \times (ra + rb) \qquad (1)$$

Here, max(a, b) is the larger of a and b, and ceil(x) is the smallest integer number that is equal to or greater than x. It is recommended that the right side value be smaller than the left side value with enough guard number.

Actual performance limit of resize output is also limited by the band-width of the attached SDRAM. Average output pixel per clock of each line must not exceed the band-width available to IPIPE module. For example, if the allowed band-width is 1 byte/clock, output pixel per clock in each line must be lower than 1 pixel per every 2 clocks with some margin for overhead. Therefore, allowed resize ratio in this case will be

image-a ratio <= x1, and image-b ratio <= x1

or

image-a ratio <= x2, and no image-b.

Bandwidth regulator (Section 4.3.11.9) must be configured to allow the required bandwidth.

4.3.11.2 Resizer Input

The resizer takes input from either IPIPE or IPIPEIF. The input is in the following formats.

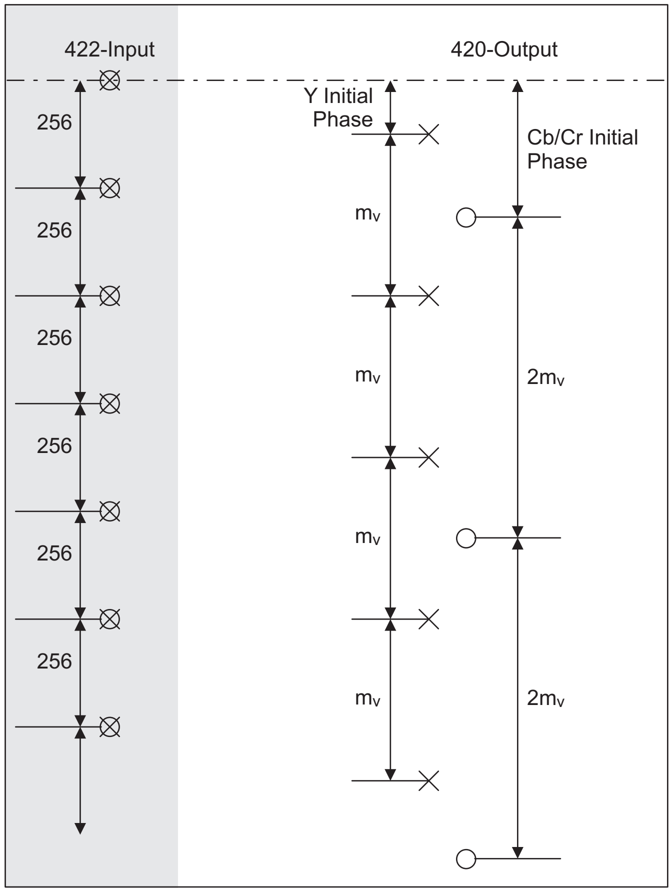
Table 4-13. Resizer Input Format

IPIPE Input	RAW	LOW	LOW	LOW	LOW	RAW11	RAW10	RAW9	RAW8
	YCbCr 16 bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	Y 8 bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	CbCr 8 bit	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
IPIPE Input	RAW	RAW7	RAW6	RAW5	RAW4	RAW3	RAW2	RAW1	RAW0
	YCbCr 16 bit	Cb/Cr7	Cb/Cr6	Cb/Cr5	Cb/Cr4	Cb/Cr3	Cb/Cr2	Cb/Cr1	Cb/Cr0
	Y 8 bit	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
	CbCr 8 bit	Cb/Cr7	Cb/Cr6	Cb/Cr5	Cb/Cr4	Cb/Cr3	Cb/Cr2	Cb/Cr1	Cb/Cr0

4.3.11.3 4:2:2 to 4:2:0 Conversion

The resizer converts 422 format to 420. In this mode, vertical scaling ratio for Cb/Cr is doubled to halves the vertical sampling points. Y data and Cb/Cr data are written to separate memory spaces.

Figure 4-50. 4:2:2 to 4:2:0 Conversion



4.3.11.4 4:2:0 Input Mode

The resizer can process 420 image data. In each frame, either Y or Cb/Cr data can be processed at a time. In order to process full 420 image with Y and Cb/Cr, IPIPE needs to run twice.

Figure 4-51. 4:2:0 Y Processing

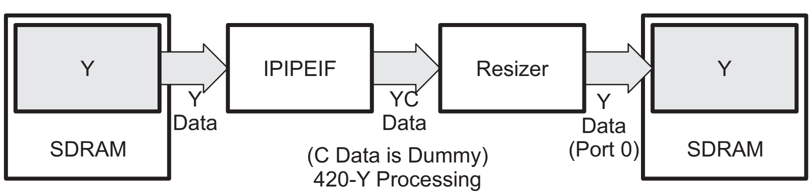
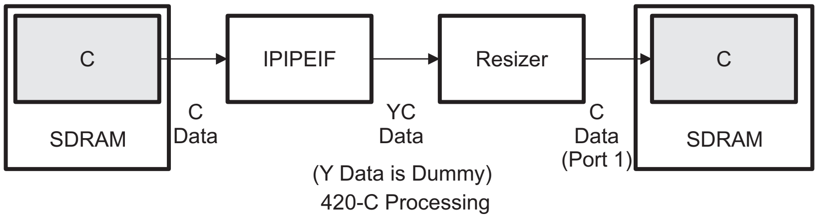


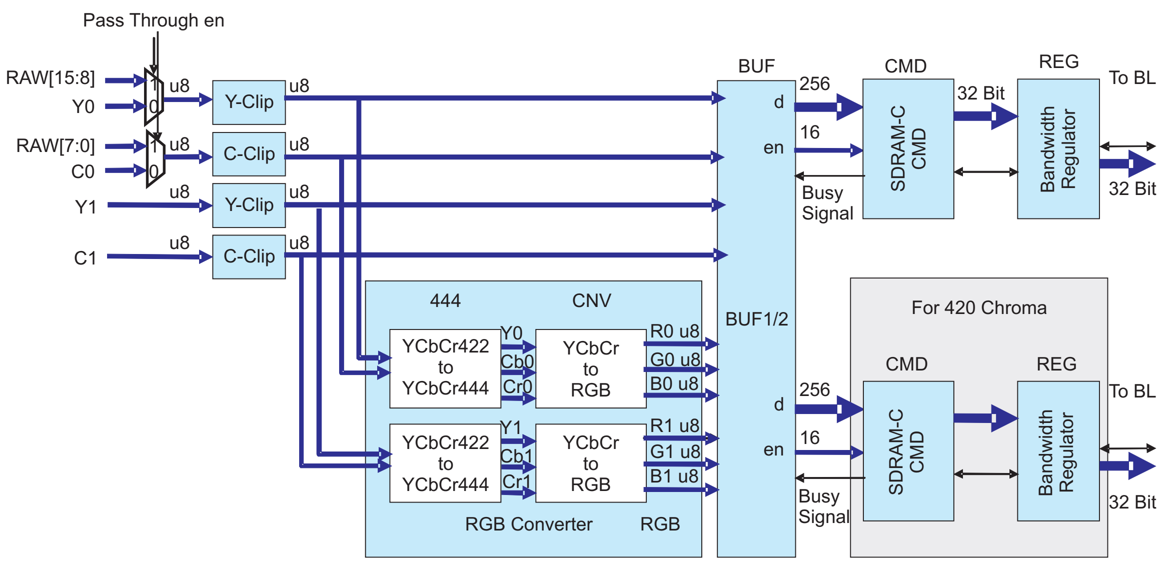
Figure 4-52. 4:2:0 C Processing



4.3.11.5 Output Interface

The block diagram of output interface module is shown in Figure 4-53. Y-Clip and C-Clip modules limit the range of image data to [ymin to ymax] or [cmin to cmax]. The values are specified in the register map. After completion the transfer of each frame, rsz_eof is sent to BufferLogic. This signal is issued at the same timing as rsz_int_dma interrupt.

Figure 4-53. Output Interface Block Diagram



4.3.11.6 RGB Converter

The IPIPE module supports output of RGB data to SDRAM. The YCbCr 4:2:2 data from the resizer module is first converted to YCbCr 4:4:4 data by linear interpolation. Since the pixels at the left and right edges are mirrored for the interpolation, two pixels at each edge are affected. To remove this effect, 2 pixels at each edge may be removed from the output. In this case, the horizontal size of the output image is 2 or 4 pixels smaller than specified in resizer register.

The YCbCr 4:4:4 data is converted to RGB using the following equation.

$$\begin{pmatrix} R \\ G \\ B \end{pmatrix} = \begin{pmatrix} 1 & 0 & 1.402 \\ 1 & -0.34414 & -0.71414 \\ 1 & 1.772 & 0 \end{pmatrix} \cdot \begin{pmatrix} Y \\ Cb-128 \\ Cr-128 \end{pmatrix}$$

This equation is realized in actual circuit using the following equations.

$$\begin{aligned} R &= (512 \cdot Y/128 + 718 \cdot Cb'/128)/4 \\ G &= (512 \cdot Y/128 - 176 \cdot Cr'/128 - 366 \cdot Cb'/128)/4 \\ B &= (512 \cdot Y/128 + 907 \cdot Cr'/128)/4 \\ Cb' &= Cb - 128 \\ Cr' &= Cr - 128 \end{aligned}$$

There are two RGB-output mode: 32-bit mode and 16-bit mode. In 32-bit mode, RGB data (8-bit each) and alpha (8-bit blending factor) are written to SDRAM. Alpha value is set through register. In 16-bit mode, R (5-bit), G (6-bit), and B (5-bit) are written.

Enabling of RGB conversion and 32-bit/16-bit selection may be independently specified to the Resize-A picture and Resize-B picture.

4.3.11.7 Resizer Output Data format

The data storage pattern in SDRAM for different resizer output formats is shown below.

4.3.11.7.1 422 Output Data

The 422 data from the resizer module are stored in the SDRAM in the following packing format.

Figure 4-54. 422 Data Packing

31–24	23–16	15–8	7–0
Y1	Cr0	Y0	Cb0

4.3.11.7.2 420 Output Data

The 420 data from the resizer module are stored in the SDRAM in the following packing format.

Figure 4-55. 420-Y Data Packing

31–24	23–16	15–8	7–0
Y3	Y2	Y1	Y0

Figure 4-56. 420-C Data Packing

31–24	23–16	15–8	7–0
Cr1	Cb1	Cr0	Cb0

4.3.11.7.3 RAW Output Data

RAW data (Bayer data) are stored in the SDRAM in the following packing format.

Figure 4-57. RAW Data Packing

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Not used	RAW1	Not used	RAW0

4.3.11.7.4 *RGB Ouput Data*

RGB data are stored in the SDRAM in the following packing format.

Figure 4-58. RGB Data Packing (32-bit)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Alpha (blending factor)	Red	Green	Blue

Figure 4-59. RGB Data Packing (16-bit)

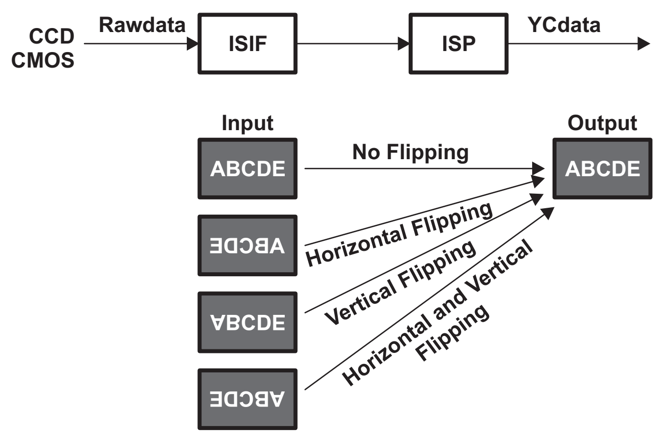
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Red-1	Green-1	Blue-1	Red-0	Green-0	Blue-0

4.3.11.8 Output Image Flipping

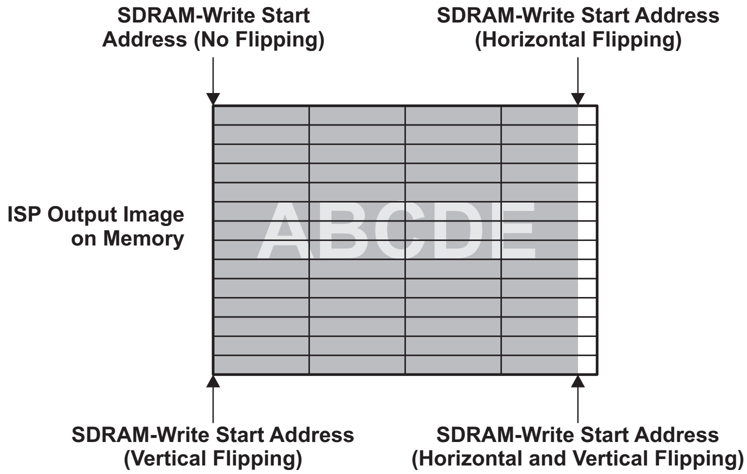
The flipping image function is implemented to support flipped raw data input. Horizontal, vertical and horizontal/vertical flipping modes are implemented as shown in Figure 4-60.

Figure 4-60. Data Flipping Mode



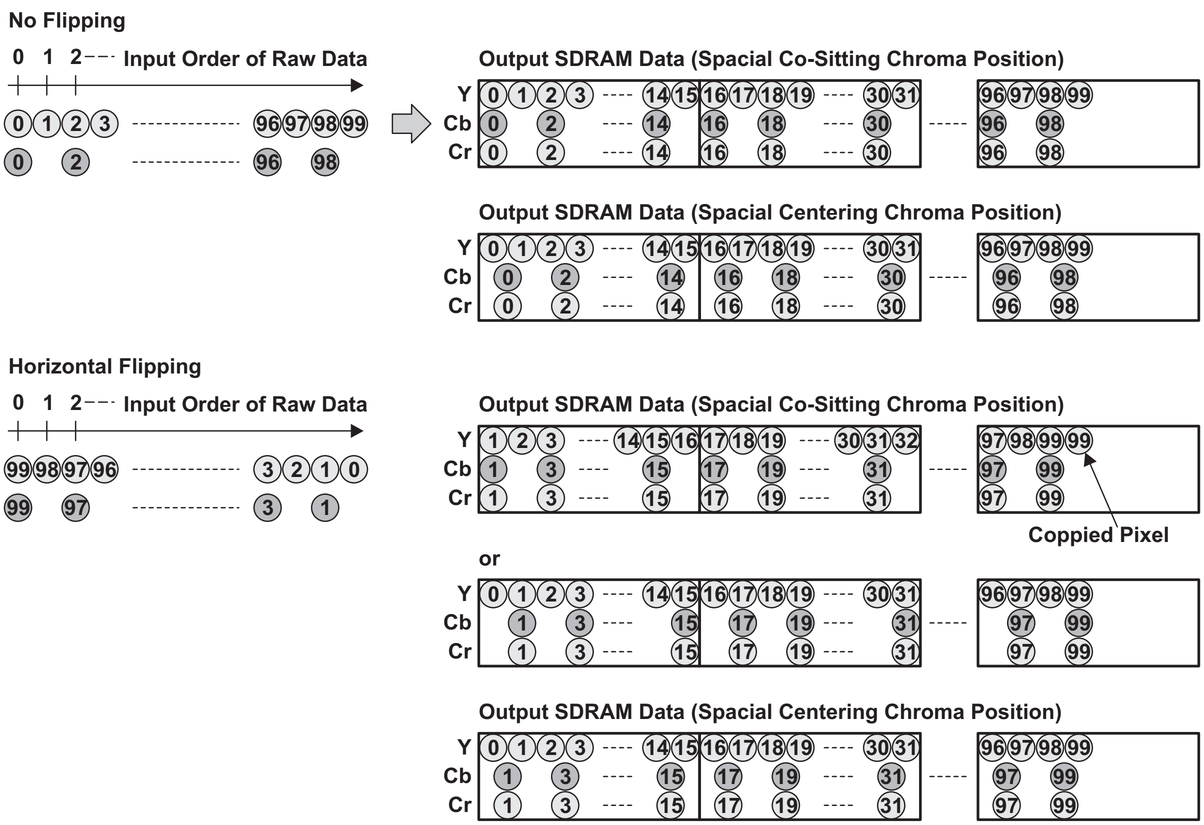
The SDRAM write-start-address is needed to be set at the register by ARM. The address at each flipping mode is illustrated in Figure 4-61.

Figure 4-61. Write Start Address at Each Flipping Mode



In the non on-the-fly operation mode, ISIF flips the data and write raw data in the SDRAM. IPIPE does not flip data in the mode. Therefore horizontal flipping mode does not support the frame division operation. Figure 4-62 illustrates output data format to SDRAM at no flipping and horizontal flipping modes.

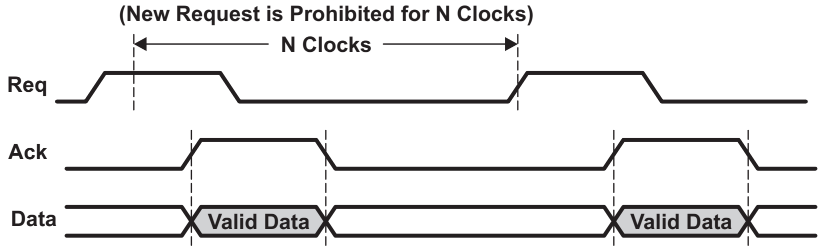
Figure 4-62. Output Data Format to SDRAM



4.3.11.9 Output Bandwidth Regulator

The bandwidth regulator module limits the maximum bandwidth used by IPIPE output. This module suppresses issuing of a new request for the desired period of time (N clocks) after each request. The period is specified by clock cycles through register values. N is between 0 and 255, and can be set independently for resize-A and resize-B. With a given N value, the maximum bandwidth used by IPIPE is 256/(N+1) bit/cycle.

Figure 4-63. SDRAM Access Request Prohibited Period



4.3.12 Histogram

Histogram and boxcar may not work at the same time, since the modules share one set of memories. The histogram module counts the number of pixels having a value in a region. Features of the histogram function are as follows:

- The data to be summed will be taken either from NF memory or from RGB2YCbCr module.
- When data are collected from NF memory, the sampled colors are R/G/B/Y. Y is derived in the following method. (HST_MUL_R, HST_MUL_GR, HST_MUL_GB, HST_MUL_B are in S4.4 format) Y=(HST_MUL_R*R+HST_MUL_GR*Gr+HST_MUL_GB*Gb+HST_MUL_B*B).
  For G histogram, either Gb, Gr, or (Gb+Gr)/2 is used
- When data are collected from RGB2YCbCr module, Cb is collected from (even, even) positions, Y from (odd, even) and (even, odd) positions and Cr from (odd, odd) positions.
- There are two banks of memory, and two sets of 512 x 20-bit memory are used for each bank.
- Two banks of memory sets are available. Tables are selected by HST_TBL.
- "The number of regions" x "the number of bins" <= 256
- The number of regions (areas) : 1, 2, 3, or 4
- The position and size of each region is specified by HST_n_HPS, HST_n_VPS, HST_n_VSZ, HST_n_HSZ (n = 0, 1, 2 or 3).
- Each region can be turned on/off counting.
- The regions have priority orders.
- Each region has its own start coordinate X/Y (12-bit) and horizontal/vertical sizes (12-bit)
- When regions are overlapped, value in the overlapped region is only accumulated in the region with the highest priority.
- The number of colors to be counted: 1, 2, 3, or 4
- Each color in all regions can be turned off counting.
- The value of each pixel is down-shifted before counting.
- The down-shift bit number: 0 ~ 11 bits
- When the value of a bin reaches to (2^{20} - 1), the value is saturated until the memory is cleared.
- The number of bins: 32, 64, 128, or 256

The histogram memory can be cleared at the VD signal. When memory is cleared, the first line of each frame can not be sampled by histogram if the width of the frame is larger than 512. If the width of the frame is smaller than 512, the first cell (512/width) lines can not be collected, where cell(x) is the smallest integer value above x. If the clearing function is not enabled, the histogram bins are accumulated over the previous values.

The histogram has two banks of memories, and they can be switched alternatively. The mapping of histogram memory is shown in Table 4-14.

Table 4-14. Histogram Memory Mapping

Memory #	Address	Histogram table	Table Address
	(32 bit word)		
Histogram memory #0	0x0000h	Histogram 0 (Bank 0)	Table address = 0x0000h
Histogram memory #0	0x0001h	Histogram 0 (Bank 0)	Table address = 0x0001h

Table 4-14. Histogram Memory Mapping (continued)

Memory #	**Address**	**Histogram table**	**Table Address**
Histogram memory #0	0x0002h	Histogram 0 (Bank 0)	Table address = 0x0002h
.	.	.	.
.	.	.	.
.	.	.	.
Histogram memory #0	0x01FEh	Histogram 0 (Bank 0)	Table address = 0x01FEh
Histogram memory #0	0x01FFh	Histogram 0 (Bank 0)	Table address = 0x01FFh
Memory #	**Address (byte)**	**Histogram table**	**Table Address**
Histogram memory #1	0x0000h	Histogram 1 (Bank 0)	Table address = 0x0000h
Histogram memory #1	0x0001h	Histogram 1 (Bank 0)	Table address = 0x0001h
Histogram memory #1	0x0002h	Histogram 1 (Bank 0)	Table address = 0x0002h
.	.	.	.
.	.	.	.
.	.	.	.
Histogram memory #1	0x01FEh	Histogram 1 (Bank 0)	Table address = 0x01FEh
Histogram memory #1	0x01FFh	Histogram 1 (Bank 0)	Table address = 0x01FFh
Memory #	**Address (byte)**	**Histogram table**	**Table Address**
Histogram memory #2	0x0000h	Histogram 0 (Bank 1)	Table address = 0x0000h
Histogram memory #2	0x0001h	Histogram 0 (Bank 1)	Table address = 0x0001h
Histogram memory #2	0x0002h	Histogram 0 (Bank 1)	Table address = 0x0002h
.	.	.	.
.	.	.	.
.	.	.	.
Histogram memory #2	0x01FEh	Histogram 0 (Bank 1)	Table address = 0x01FEh
Histogram memory #2	0x01FFh	Histogram 0 (Bank 1)	Table address = 0x01FFh
Memory #	Address (byte)	Histogram table	Table Address
Histogram memory #3	0x0000h	Histogram 1 (Bank 1)	Table address = 0x0000h
Histogram memory #3	0x0001h	Histogram 1 (Bank 1)	Table address = 0x0001h
Histogram memory #3	0x0002h	Histogram 1 (Bank 1)	Table address = 0x0002h
.	.	.	.
.	.	.	.
.	.	.	.
Histogram memory #3	0x01FEh	Histogram 1 (Bank 1)	Table address = 0x01FEh
Histogram memory #3	0x01FFh	Histogram 1 (Bank 1)	Table address = 0x01FFh

The memory map for histogram changes according to HST_PARA[BIN], (see Figure 4-64).

Figure 4-64. Histogram Memory Map Changes

(1) HST_PARA[BIN] = 0 (The Number of Bins is 32)

Histogram 0 Table Address Format									
Bit	8	7	6	5	4	3	2	1	0
Description	0	Region (0,1,2,3)		Color 0:R, 1:B	BIN Number (0-31)				

Histogram 1 Table Address Format									
Bit	8	7	6	5	4	3	2	1	0
Description	0	Region (0,1,2,3)		Color 0:G, 1:Y	BIN Number (0-31)				

(2) HST_PARA[BIN] = 1 (The Number of Bins is 64)

Histogram 0 Table Address Format									
Bit	8	7	6	5	4	3	2	1	0
Description	Region (0,1,2,3)		Color 0:R, 1:B	BIN Number (0-63)					

Histogram 1 Table Address Format									
Bit	8	7	6	5	4	3	2	1	0
Description	Region (0,1,2,3)		Color 0:G, 1:Y	BIN Number (0-63)					

(3) HST_PARA[BIN] = 2 (The Number of Bins is 128)

Histogram 0 Table Address Format									
Bit	8	7	6	5	4	3	2	1	0
Description	Region (0,1)	Color 0:R, 1:B	BIN Number (0-127)						

Histogram 1 Table Address Format									
Bit	8	7	6	5	4	3	2	1	0
Description	Region (0,1)	Color 0:G, 1:Y	BIN Number (0-127)						

(4) HST_PARA[BIN] = 3 (The Number of Bins is 255)

Histogram 0 Table Address Format									
Bit	8	7	6	5	4	3	2	1	0
Description	Color 0:R, 1:B	BIN Number (0-255)							

Histogram 1 Table Address Format									
Bit	8	7	6	5	4	3	2	1	0
Description	Color 0:G, 1:Y	BIN Number (0-255)							

Table 4-15. Histogram Memory Regions (Bins)

Memory Region	Address Range	Description
IPIPE_HST_TB0	0x01C72000 – 0x01C727FF	IPIPE Histogram Memory #0
IPIPE_HST_TB1	0x01C72800 – 0x01C72FFF	IPIPE Histogram Memory #1
IPIPE_HST_TB2	0x01C73000 – 0x01C737FF	IPIPE Histogram Memory #2
IPIPE_HST_TB3	0x01C73800 – 0x01C73FFF	IPIPE Histogram Memory #3

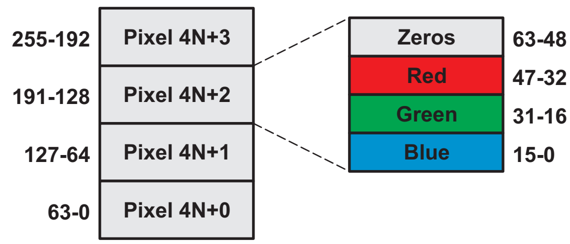
4.3.13 Boxcar

The histogram and boxcar modules may not work at the same time, since they share one set of memories.

The boxcar module generates a boxcar by taking mosaic image data and averaging the red, green, and blue pixels in an 8×8 or 16×16×16 block to produce one red, green, and blue output as shown in Figure 4-66 and in Figure 4-67.

The result from this operation is a full color image with (1/64) or (1/256) area of the original image. The maximum input horizontal width is 8190 pixels wide when 16x16 block is used. If 8×8 block is used, it is 4096 bits. Also, the image size (width and height) must be a multiple of 16 for 16×16 block, and a multiple of 8 for 8×8 block. The boxcar operation works on up to 12-bit Bayer data and output 16-bit data. The output data are 48-bit RGB data for each 8×8 or 16×16 block. The 48-bit data is aligned in 64-bit format in SDRAM as shown in Figure 4-65.

Figure 4-65. Boxcar Data Packing in SDRAM



The first address of SDRAM access is specified by IPIPE_BOX_SDR_SAD_H and IPIPE_BOX_SDR_SAD_L. The output data are written to SDRAM continuously line by line; there are no address offsets between lines. After completion of image transfer of each frame, ipipe_eof signal is sent to BufferLogic. This signal is issued at the same timing as ipipe_int_dma.

$$R_{output_{i,j}} = \left(\sum_{y=8i}^{8i+7} \sum_{x=8j}^{8j+7} R_{y,x} \right) \gg shf$$

$$B_{output_{i,j}} = \left(\sum_{y=8i}^{8i+7} \sum_{x=8j}^{8j+7} B_{y,x} \right) \gg shf$$

$$G_{output_{i,j}} = \left(\frac{\left(\sum_{y=8i}^{8i+7} \sum_{x=8j}^{8j+7} Gb_{y,x} \right)}{2} + \frac{\left(\sum_{y=8i}^{8i+7} \sum_{x=8j}^{8j+7} Gr_{y,x} \right)}{2} \right) \gg shf$$

The right-shift value is specified by a register IPIPE_BOX_SHF, which has the range of 0 to 4. (The shift down is to fit 20-bit accumulated value into 16-bit output.) For green signal processing, divide-by-two operation rounds off the LSB.

The boxcar module shares memories with histogram module; therefore they can not run simultaneously. The boxcar can run in parallel with other parts of IPIPE other than the histogram.

Figure 4-66. Boxcar Operation (8 × 8 block)

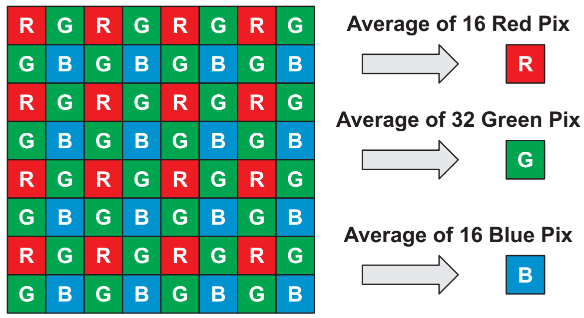
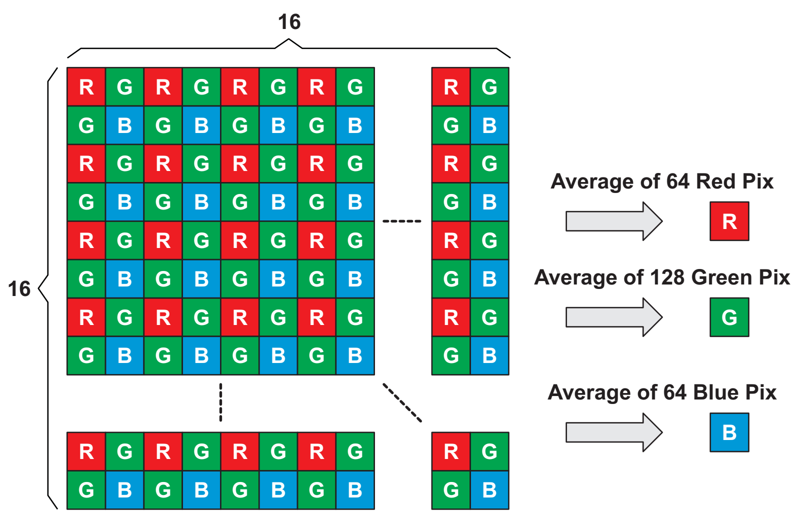


Figure 4-67. Boxcar Operation Figure (16 × 16 block)



4.4 Statistics Collection - Hardware 3A (H3A)

The H3A module is designed to support the control loops for auto focus, auto white balance, and auto exposure by collecting metrics about the imaging/video data. The metrics are to adjust the various parameters for processing the imaging/video data. There are two main blocks in the H3A module:

- Auto focus engine (AF)
- Auto exposure and auto white balance engine (AE/AWB)

The AF engine extracts and filters each green pixel from the input image/video data and provides either the accumulation or peaks of the data in a specified region. The specified region is a two-dimensional block of data and is referred to as a paxel for the case of AF.

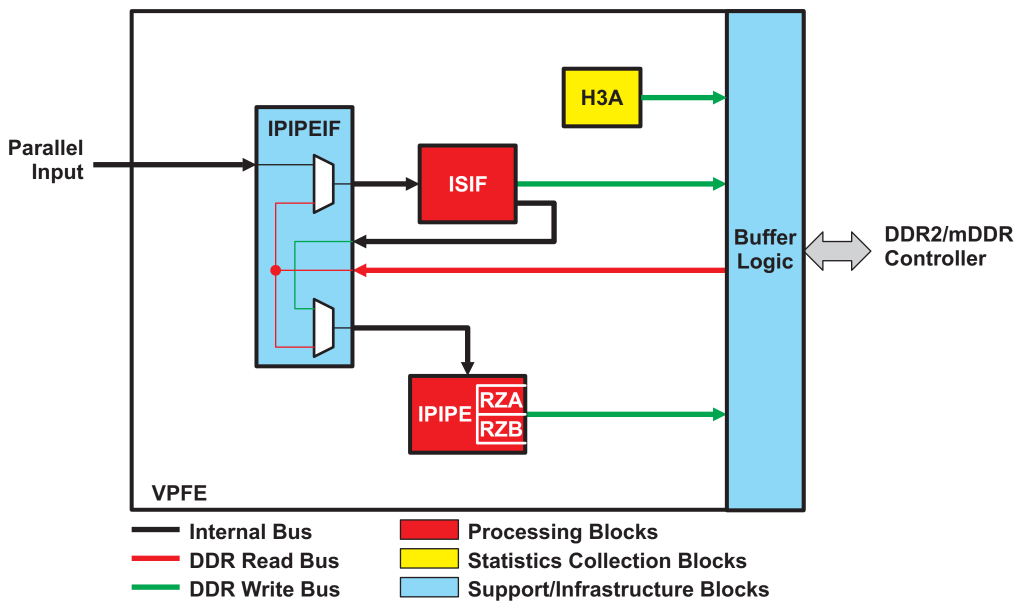
The AE/AWB engine accumulates the values and checks for saturated values in a sub-sampling of the video data. In the case of the AE/AWB, the two-dimensional block of data is referred to as a window. Thus, other than referring to them by different names, a paxel and a window are essentially the same thing. However the number, dimensions, and starting position of the AF paxels and the AE/AWB windows are separately programmable.

Programming Model

5.1 Setup for Typical Configuration

A typical configuration of the VPFE for a digital camera application includes interfacing to a CCD/CMOS sensor. In addition to programming these external devices, the VPFE is programmed in Preview mode to capture data at a 30-Hz frame rate (draft mode). The VPFE sub-module is configured to capture/read this data and format for display via the Image Pipe. Simultaneously, the H3A collects data to be used by user-defined 3A algorithms, etc. Figure 5-1 depicts the VPFE data flow diagram. The input to the Image Sensor Interface (ISIF) and IPIPE is either raw image data or YCC data. The input to the H3A is only raw image data.

Figure 5-1. DM36x Video Processing Front End Block Diagram



5.2 Resetting the Camera Subsystem

The entire VPSS subsystem (VPFE and VPBE) can be reset via the Power/Sleep Controller.

5.3 Configuring the Clocks and the Control Signals

The input pixel data clock must be provided by the external imager device. The VPFE syncs to the externally provided signals.

5.4 Programming the Image Sensor Interface (ISIF)

This section discusses the issues related to the image sensor interface software control. It lists which registers are required to be programmed in different modes, how to enable and disable the different blocks in the ISIF, and how to check the status of the ISIF. It also discusses the different register access types and provides a list of programming constraints.

5.4.1 Hardware Setup/Initialization

5.4.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the ISIF are reset to their reset values.

5.4.1.2 Register Setup

Prior to enabling the ISIF, the hardware must be properly configured via register writes. Table 5-1 identifies the register parameters that must be programmed before enabling the ISIF. Since many of these registers are latched into the hardware by the PCLK, it should be actively clocking during register configuration.

Table 5-1. ISIF Required Configuration Parameters

Function	Configuration Required
External Pin Signal Configuration	MODESET.HDVDD MODESET.FIDD MODESET.VDPOL MODESET.HDPOL MODESET.FIPOL MODESET.SWEN MODESET.CCDMD CCDCFG.VDLC CCDCFG.EXTRG
Input Mode	MODESET.INPMOD REC656IF.R656ON
YC Input Swap	CCDCFG.YCINSWP
SDRAM Output Enable	SYNCEN.DWEN
Output port MUX enable	ISP.BCR.SRC_SEL_ISIF_IPIPE

Table 5-2 identifies additional configuration requirements depending on whether the corresponding condition is met. The table can be read as:

if(**Condition** is TRUE), then **Configuration Required** parameters must be programmed.

Table 5-2. ISIF Conditional Configuration Parameters

Function	Condition	Configuration Required
VSYNC/HSYNC set as outputs	MODESET.HDVDD	HDW VDW PPLN LPFR
Interlaced Fields	MODESET.CCDMD	CCDCFG.FIDMD
External WEN	MODESET.SWEN	CCDCFG.WENLOG
External Trigger	CCDCFG.EXTRG	CCDCFG.TRGSEL
REC656 Input	REC656IF.R656ON	REC656IF.ECCFVH CCDCFG.BW656
YCC Input	MODESET.INPMOD != 0	CLDOFST.CLDC
8 bit YCC Input	MODESET.INPMOD == 2	CCDCFG.Y8POS
Raw Input	MODESET.INPMOD == 0 && !REC656IF.R656ON	MODESET.DPOL CGAMMAWD.GWDI LINCFG0.LINEN DFCCTL.VDFCEN CLAMPCFG.CLEN

Table 5-2. ISIF Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required
		FMTCFG.FMTEN CSCCTL.CSCEN CGAMMAWD.WBEN[2:0] CGAMMAWD.OFSTEN[2:0] CGAMMAWD.CFAP CCOLP CRGAIN CGRGAIN CGBGAIN CBGAIN COFSTA CLDCOFST
Vertical Line Defect Correction	DFCCTL.VDFCEN	DFCCTL.VDFCSL DFCCTL.VDFCUDA DFCCTL.VDFCSFT VDFSATLV.VDFSLV DFCMEMCTL DFCMEM[4:0] DATAHOFST DATAVOFST
Color Space Converter	CSCCTL.CSCEN	CSCM[7:0]
DPCM Enabled	MISC.DPCMEN	MISC.DPCMPRE
Black Clamp	CLAMPCFG.CLEN	CLAMPCFG CLDCOFST CLSV CLHWIN[2:0] CLVRV CLVWIN[3:0]
Flash Signal Control	FLSHCFG0.FLSHEN	FLSHCFG1 FLSHCFG2
Write to SDRAM	SYNCEN.DWEN(Common configuration required for raw and YCC modes)	CCDCFG.SDRPACK CCDCFG.BSWD CCDCFG.MSBINVI SPH LNH SLV0 SLV1 LNV CADU CADL CULH CULV HSIZE SDOFST
Write to SDRAM in Raw Mode	MODESET.SWEN && MODESET.INPMOD == 0	MODESET.HLPF MODESET.CCDW

Table 5-2. ISIF Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required
		COFSTA CGAMMAWD.CCDTBL CGAMMAWD.WBEN0 CGAMMAWD.OFSTEN0 MISC.DPCMEN
IPIPE Input	MODESET.INPMOD == 0 && IPIPE is receiving data from ISIF	CGAMMAWD.WBEN1 CGAMMAWD.OFSTEN1
H3A Input	MODESET.INPMOD == 0 && H3A is receiving data from ISIF	CGAMMAWD.WBEN2 CGAMMAWD.OFSTEN2
White Balance (Color) Gains	CGAMMAWD.WBEN0 || CGAMMAWD.WBEN1 || CGAMMAWD.WBEN2	CRGAIN CGRGAIN CGBGAIN
White Balance offset	CGAMMAWD.OFSTEN0 || CGAMMAWD.OFSTEN1 || CGAMMAWD.OFSTEN2	CBGAIN COFSTA CBGAIN
Interrupt Usage	VDINT[2:0] are enabled	VDINT0 VDINT1 VDINT2
2D LSC interrupt is enabled		2DLSCIRQEN

5.4.2 Enable/Disable Hardware

Setting the SYNCEN.SYEN bit enables the Image Sensor Interface. This should be done after all of the required registers mentioned in the previous section are programmed.

The ISIF always operates in continuous mode. In other words, after enabling the ISIF, it continues to process sequential frames until the SYNCEN.SYEN bit is cleared by software. When this happens, the frame being processed is disabled immediately, and does not continue to process the current frame.

When the ISIF is in master mode (HSYNC/VSYNC signals set to outputs), fetching and processing of the frame begins immediately upon setting the SYNCEN.SYEN bit.

When the ISIF is in slave mode (HSYNC/VSYNC signals set to inputs), processing of the frame is dependent upon the input timing of the external sensor/decoder. In order to guarantee that data from the external device is not missed, the ISIF should be enabled prior to data transmission from the external device. In this way, the ISIF waits for the data from the external device.

5.4.3 Events and Status Checking

The ISIF module can generate four different interrupts: VDINT0, VDINT1, VDINT2, and 2DLSCINT. Note that the SYNCEN.SYEN bit should be enabled to receive any of the ISIF interrupts.

5.4.3.1 VDINT0, VDINT1 and VDINT2 Interrupts

As shown in Figure 5-2 and Figure 5-3, VDINT0, VDINT1, and VDINT2 interrupts occur relative to the VSYNC pulse. The trigger timing is selected by using the MODESET.VDPOL setting. VDINT0, VDINT1, and VDINT2 occur after receiving the number of horizontal lines (HSYNC pulse signals) set in the VDINT0, VDINT1, and VDINT2 registers, respectively.

NOTE: In the case of BT.656 input mode, there is a VSYNC at the beginning of each field. Therefore, there are two interrupts for each frame (i.e., one for each field).

If MODESET.VDPOL equals 0, the VDINT0, VDINT1, and VDINT2 HSYNC counters begin counting HSYNC pulses from the rising edge of the external VSYNC.

Figure 5-2. VDINT0/1/2 Interrupt Behavior when VDPOL=0

If MODESET.VDPOL equals one, the VDINT0, VDINT1, and VDINT2 HSYNC counters begin counting HSYNC pulsed from the rising edge of the external VD.

Figure 5-3. VDINT0/1/2 Interrupt Behavior when VDPOL=1

5.4.3.2 Status Checking

The MODESET.MDFS bit is set when the field status is on an even field and it is cleared when the field status is on an odd field.

5.4.4 Register Accessibility During Frame Processing

There are two types of register access in the ISIF module.

- **Shadow registers** (event-latched registers) - These registers can be read and written at any time, but the written values only take effect (become latched) at certain times based on some event. Note that reads still return the most recent write even though the setting are not used until the specific event occurs.
- **Busy-writeable registers** - These registers/fields can be read or written even if the module is busy. Changes to the underlying setting take place instantaneously.

The registers/fields listed below are busy-writeable, all the others are shadowed. Shadowed registers can be optionally set as busy-writeable registers by setting CCDCFG.VDLC to 1.

SYNCEN.SYEN	MODESET.FIPOL	VDINT0	DFCMEMCTL
MODESET.INPMOD	MODESET.HDPOL	VDINT1	DFCMEM0
MODESET.CCDW	MODESET.VDPOL	VDINT2	DFCMEM1
MODESET.CCDMD	MODESET.FIDD	CGAMMAWD.GWDI	DFCMEM2
MODESET.DPOL	MODESET.HDVDD	REC656IF	DFCMEM3
MODESET.SWEN	CCOLP	CCDCFG	DFCMEM4

5.4.5 Inter-Frame Operations

Between frames, it may be necessary to enable/disable functions or modify the memory pointers. Since the SYNCEN.DWEN register and memory pointer registers are shadowed, these modifications can take place any time before the end of the frame and the data gets latched in for the next frame.

5.4.6 Summary of Constraints

The following is a list of register configuration constraints to adhere to when programming the ISIF module. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

- PCLK cannot be higher than 120 MHz.
- If the SDRAM output port is enabled:
  - The memory output line offset and address should be on 32-byte boundaries.

– (LNH-1) must be a multiple of 32 bytes.

- External WEN cannot be used at the same time as external FID.

5.5 Programming the Image Pipe Interface (IPIPEIF)

This section discusses issues related to the software control of the IPIPE interface. It lists which registers are required to be programmed in different modes, how to enable and disable the IPIPE interface, how to check the status the IPIPE interface, discusses the different register access types, and enumerates several programming constraints.

5.5.1 Hardware Setup/Initialization

This section discusses the configuration of the IPIPE interface required before image processing can begin.

5.5.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the IPIPE interface are reset to their reset values.

5.5.1.2 Register Setup

Prior to enabling the IPIPE interface, the hardware must be properly configured via the register writes. Table 5-3 and Table 5-4 identify the register parameters that must be programmed before enabling the IPIPE interface.

Table 5-3. IPIPE Interface Required Configuration Parameters (ISIF Enabled)

Function	Configuration Required
Input Source	CFG1.INPSRC1
Input Clock	CFG1.CLKSEL CLKDIV
DPCM Decoding	DPCM

Table 5-4. IPIPE Interface Required Configuration Parameters (IPIPE Enabled)

Function	Configuration Required
Input Source	CFG1.INPSRC2
Input Clock	CFG1.CLKSEL CLKDIV
Decimation and Anti-Aliasing Filter	CFG1.DECIM CFG1.AVGFILT

Table 5-5 identifies additional configuration requirements depending on whether the corresponding condition is met. The table can be read as:

if(**Condition** is TRUE), then **Configuration Required** parameters must be programmed.

Table 5-5. IPIPE Interface Conditional Configuration Parameters (IPIPE Enabled)

Function	Condition	Configuration Required
Decimation Value	CFG1.DECM	RSZ INIRSZ
Clock Divider	CFG1.CLKSEL	CLKDIV
ISIF input, Parallel I/F source	CFG1.INPSRC1 = 0,2	CFG2.HDPOL CFG2.VDPOL
IPIPE input, ISIF source	CFG1.INPSRC2 = 0	CFG2.YUV16
IPIPE input, raw input	(CFG1.INPSRC2 = 0 && CFG2.YUV16 = 0) ||	GAIN OCLIP

Table 5-5. IPIPE Interface Conditional Configuration Parameters (IPIPE Enabled) (continued)

Function	Condition	Configuration Required
	CFG1.INPSRC2 = 1, 2	DPC1
Input from SDRAM	CFG1.INPSRC1 != 0 || CFG1.INPSRC2 != 0	PPLN LPFR HNUM VNUM ADDRU ADDRL ADOFS DPC2
Raw input from SDRAM	CFG1.INPSRC1 = 1,2 || CFG1.INPSRC2 = 1.2	CFG1.UNPACK DPCM
Raw input from SDRAM	(CFG1.INPSRC1 = 1,2 || CFG1.INPSRC2 = 1.2)	CFG1.DATASFT
Input from SDRAM	CFG1.INPSRC1 = 1,2,3 || CFG1.INPSRC2 = 1.2,3	CFG1.ONESHOT
Dark frame subtract	CFG1.INPSRC1 = 2 || CFG1.INPSRC2 = 2	CFG2.DFSDIR
IPIPEIF Interrupt	Interrupt is used	CFG2.INTSRC

5.5.2 Enable/Disable Hardware

When CFG1.INPSRCx = 0, the IPIPEIF does not need to be enabled. It processes whatever the ISIF sends. If CFG1.INPSRDx ≠ 0, then the IPIPEIF begins to fetch data from SDRAM by setting the ENABLE.ENABLE bit. This should be done after all of the required registers in the IPIPE and IPIPEIF are programmed.

When the input source is the SDRAM, the IPIPEIF can, optionally, operate in one-slot mode or continuous mode by setting the CFG1.ONESHOT parameter. If one-shot mode is enabled, then after enabling the IPIPEIF, the ENABLE.ENABLE bit is automatically turned off (set to 0) and only a single frame is processed from memory. In this mode, fetching and processing of the frame begins immediately upon setting the ENABLE.ENABLE bit.

When the input source is the Image Sensor Interface, processing of the frame is dependent upon the timing of the ISIF. In order to guarantee that data from the ISIF is not missed, the IPIPEIF should be enabled prior to the ISIF. In this way, the IPIPEIF waits for data from the ISIF.

When the IPIPEIF is in continuous mode, it can be disabled by clearing the ENABLE.ENABLE bit after processing of the last frame. The disable takes place immediately since it is a busy-write register.

5.5.3 Events and Status Checking

The IPIPEIF generates an IPIPEIF event based on the CFG2.INTSRC bit-field setting.

5.5.4 Register Accessibility During Frame Processing

There are two types of register access in the IPIPEIF module.

- **Shadow registers** - These registers can be read and written (if the field is writeable) at any time. However, the written values take effect at the start of frame (VSYNC active edge). Note that reads still return the most recent write even though settings are not used until the next start of frame. The following are the shadow registers in the IPIPE interface:

ENABLE.SYNCOFF	HNUM	RSZ
CFG1. DECIM	VNUM	GAIN
CFG1.AVGFILT	ADDRU	RSZ3A. DECM
PPLN	ADDRL	RSZ3A.AVGFILT
LPFR	ADOFS	RSZ3A.RSZ

- **Busy-writeable registers -** These registers/fields can be read or written even if the module is busy. Changes to the underlying setting take place instantaneously. The following registers are busy-writeable:

ENABLE.ENABLE	CFG1.UNPACK	CFG2
CFG1.INPSRC1	CFG1.INPSRC2	INIRSZ
CFG1.DATASFT	CFG1.ONESHOT	OCLIP
CFG1.CLKSEL	DPCM	DPC1
		DPC2
		INIRSZ3A

5.5.5 Inter-Frame Operations

Between frames, it may be necessary to enable/disable functions or modify the memory pointers. Since several of the registers are shadowed, these modifications can take place any time before the end of the frame and the data gets latched in for the next frame. The host controller can perform these changes upon receiving an interrupt or and EDMA transfer can be programmed to make these changes upon receiving an event.

5.5.6 Summary of Constraints

The following is a list of register configuration constraints to adhere to when programming the IPIPEIF. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

- If the SDRAM output port is enabled:
  - The memory output line offset and address should be on 32-byte boundaries.
  - Data is fetched starting on the second VSYNC.
- In dark-frame subtract, LPFR must be > 0, since the first line cannot be fetched.

5.6 Programming the Image Pipe (IPIPE)

This section discusses the issues related to the IPIPE software control. It lists which registers are required to be programmed in different modes, how to enable and disable the IPIPE, discusses the different register access types, and enumerates several programming constraints.

5.6.1 Hardware Setup/Initialization

This section describes the IPIPE configuration required before image processing can begin in IPIPE module.

5.6.1.1 Reset Behavior

Upon VPSS hardware reset, all of the registers in the IPIPE are reset to their reset values. However, since the IPIPE programmable look-up tables are stored in internal RAM, their contents do not have reset values. If the reset is a chip-level power-on-reset (reset after power is applied), then the contents of these tables are unknown. If the reset is a VPSS module reset (when power remains active), then the contents of these tables remains the same as before the reset.

5.6.1.2 Register Setup

Prior to enabling the IPIPE, the hardware must be properly configured via register writes. In order to write to the IPIPE registers, the IPIPE.GCK_MMR register must first be set to 1. In order to write to the Resizer registers, the RSZ.GCK_MMR register must first be set to 1.Table 5-6 identifies the register parameters that must be programmed before enabling the IPIPE.

Table 5-6. IPIPE Required Configuration Parameters

Function	Configuration Required (IPIPE Registers)	Configuration Required (Resizer Registers)
Function Enable/Disable	SRC_MODE SRC_FMT	SRC_MODE SRC_FMT0
Input Size	SRC_VPS SRC_VSZ SRC_HPS SRC_HSZ	SRC_VPS SRC_VSZ SRC_HPS SRC_HSZ
Clocks	GCK_PIX	GCK_SDR
BOXCAR Output	BOX_SDR_SAD_H BOX_SDR_SAD_L	
SDRAM Output		RZX_SDR_Y_SAD_H RZX_SDR_Y_SAD_L
SDRAM Output for 4:2:0 mode		RZX_SDR_Y_SAD_H RZX_SDR_Y_SAD_L RZX_SDR_C_SAD_H RZX_SDR_C_SAD_L
DMA Regulator		DMA_RZX DMA_RZB
ISP configuration (output port MUX)	ISP.BCR.SRC_SEL_ISIF_IPIPE ISP.BCR.SRC_SEL_IPIPE_LDC	

Table 5-7 identifies additional configuration requirements depending on whether the corresponding condition is met.

The table can be read as: if(**Condition** is TRUE), then **Configuration Required** parameters must be programmed.

Table 5-7. Conditional Configuration Parameters

Function	Condition	Configuration Required	
		IPIPE	Resizer
IPIPE Raw Processing Path Functions	SRC_FMT = 0, 1	SRC_COL DPC_LUT_EN BOX_EN HST_EN WB2_OFT_R WB2_OFT_GR WB2_OFT_GB WB2_OFT_B WB2_WGN_R WB2_WGN_GR WB2_WGN_GB WB2_WGN_B	
IPIPE Raw-to-YCbCr Processing Path Functions	SRC_FMT = 0	CFA_MODE	

Table 5-7. Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required: IPIPE	Configuration Required: Resizer
		RGB1_MUL_RR RGB1_MUL_GR RGB1_MUL_BR RGB1_MUL_RG RGB1_MUL_GG RGB1_MUL_BG RGB1_MUL_RB RGB1_MUL_GB RGB1_MUL_BB RGB1_OFT_OR RGB1_OFT_OG RGB1_OFT_OB GMM_CFG RGB2_MUL_RR RGB2_MUL_GR RGB2_MUL_BR RGB2_MUL_RG RGB2_MUL_GG RGB2_MUL_BG RGB2_MUL_RB RGB2_MUL_GB RGB2_MUL_BB RGB2_OFT_OR RGB2_OFT_OG RGB2_OFT_OB YUV_ADJ YUV_MUL_RY YUV_MUL_GY YUV_MUL_BY YUV_MUL_RCB YUV_MUL_GCB YUV_MUL_BCB YUV_MUL_RCR YUV_MUL_GCR YUV_MUL_BCR YUV_OFT_Y YUV_OFT_CB YUV_OFT_CR YUV_PHS	
YCbCr Processing Path Functions	SRC_FMT = 0,3	YEE_EN	SRC_EN SRC_MODE SRC_FMT0 SRC_FMT1 SRC_VPS SRC_VSZ SRC_HPS

Table 5-7. Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required: IPIPE	Configuration Required: Resizer
			SRC_HSZ YUV_Y_MIN YUV_Y_MAX YUV_C_MIN YUV_C_MAX YUV_PHS SEQ RZA_EN RZB_EN
Boxcar	SRC_FMT = 0,1,2 && BOX_EN	BOX_MODE BOX_TYP BOX_SHF BOX_SDR_SAD_H BOX_SDR_SAD_L	
LUT Defect Correction	DPC_LUT_EN	DPC_LUT_SEL DPC_LUT_ADR DPC_LUT_SIZ Setup defect look-up table	
Histogram	HST_EN	HST_MODE HST_SEL HST_PARA HST_0_VPS HST_0_VSZ HST_0_HPS HST_0_HSZ HST_1_VPS HST_1_VSZ HST_1_HPS HST_1_HSZ HST_2_VPS HST_2_VSZ HST_2_HPS HST_2_HSZ HST_3_VPS HST_3_VSZ HST_3_HPS HST_3_HSZ HST_TBL HST_MUL_R HST_MUL_GR HST_MUL_GB HST_MUL_B	
Gamma Correction	GMM_CFG.BYPR=0 || GMM_CFG.BYPG=0 || GMM_CFG.BYPB=0	GMM_CFG.TBL GMM_CFG.SIZ Setup gamma table(s) if in RAM	
Edge Enhancement	YEE_EN	YEE_TYP	

Table 5-7. Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required IPIPE	Configuration Required Resizer
		YEE_SHF YEE_MUL_00 YEE_MUL_01 YEE_MUL_02 YEE_MUL_10 YEE_MUL_11 YEE_MUL_12 YEE_MUL_20 YEE_MUL_21 YEE_MUL_22 YEE_THR YEE_E_GAN YEE_E_THR_1 YEE_E_THR_2 YEE_G_GAN YEE_G_OFT Setup Edge Enhancement LUT	
Resizer Enabled	RZx_EN		RZx_MODE RZx_420 RZx_I_VPS RZx_I_HPS RZx_O_VSZ RZx_O_HSZ RZx_V_PHS_Y RZx_V_PHS_C RZx_V_DIF RZx_V_TYP RZx_V_LPF RZx_H_PHS RZx_H_PHS_ADJ RZx_H_DIF RZx_H_TYP RZx_H_LPF RZx_DWN_EN RZx_DWN_AV RZx_RGB_EN RZx_RGB_TYP RZx_RGB_BLD RZx_SDR_Y_BAD_H RZx_SDR_Y_BAD_L RZx_SDR_Y_SAD_H RZx_SDR_Y_SAD_L RZx_SDR_Y_OFT RZx_SDR_Y_PTR_S RZx_SDR_Y_PTR_E RZx_SDR_C_BAD_H

Table 5-7. Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required	
		IPIPE	Resizer
			RZx_SDR_C_BAD_L RZx_SDR_C_SAD_H RZx_SDR_C_SAD_L RZx_SDR_C_OFT RZx_SDR_C_PTR_S RZx_SDR_C_PTR_E
Resizer RGB Output Configuration	RZx_RGB_EN		RZx_RGB_TYP
Resizer RGB Alpha value in 32 bit out mode	RZx_RGB_TYP.TYP = 0		RZx_RGB_BLD
Interrupt Usage	If Resizer interrupts are required (RSZ_INT_CYC_RZx)		IRQ_RZx

In certain bypass modes, the data still passes through modules that need to be reset to their default values so that the data being passed through is not modified. The following sections identify which registers need to be set to which values in the various bypass modes.

5.6.1.2.1 Resizer Bypass Mode

Since the YCbCr data still passes through the RZA block in resizer bypass mode, the following Resizer registers must be set accordingly:

SRC_FMT1[420] = 422
RZA_EN = ENABLE
RZA_420[Y[= DISABLE
RZA_420[C] = DISABLE
RZA_I_VPS = 0
RZA_I_HPS = 0
RZA_V_PHS_Y = 0
RZA_V_PHS_C = 0
RZA_V_DIF = 256
RZA_V_LPF[Y] = 0
RZA_V_LPF[C] = 0
RZA_H_PHS = 0
RZA_H_PHS_ADJ = 0
RZA_H_DIF = 256
RZA_H_LPF[Y] = 0
RZA_H_LPF[C] = 0
RZA_DWN_EN = DISABLE
RZA_RGB_EN = DISABLE
RZB_EN = DISABLE

5.6.1.2.2 Raw Input, Raw Output Mode (IPIPE.SRC_FMT = 1)

In this mode, the raw data bypassed the raw-to-YCbCr processes, but since it still passes through the RZA processing blocks, the following registers must be set accordingly:

IPIPE.SRC_FMT = 1
SRC_FMT1[RAW] = 1
RZA_EN = ENABLE
RZA_420[Y[= DISABLE
RZA_420[C] = DISABLE
RZA_I_VPS = 0
RZA_I_HPS = 0
RZA_V_PHS_Y = 0
RZA_V_PHS_C = 0
RZA_V_DIF = 256
RZA_V_LPF[Y] = 0
RZA_V_LPF[C] = 0
RZA_H_PHS = 0
RZA_H_PHS_ADJ = 0
RZA_H_DIF = 256
RZA_H_LPF[Y] = 0
RZA_H_LPF[C] = 0
RZA_DWN_EN = DISABLE
RZA_RGB_EN = DISABLE
RZB_EN = DISABLE

5.6.1.3 Internal (Embedded) Memory Access

Internal memories that are embedded in the VPSS memories (see Section 3.4) are accessed by ARM through the configuration bus. Note that the histogram memory can be made self-cleaning by setting the register field HST_TBL.CLR to 1.

NOTE: In order to access these memories, the IPIPE.GCK_MMR register must be first set to 1 and the PCLK input to IPIPE must be enabled. If PCLK is not being driven by an external imager at the time these registers need to be accessed, the IPIPEIF can be configured to drive the PCLK input to IPIPE by setting the IPIPEIF.CFG.CLKSEL register bit to 1.

5.6.2 Enable/Disable Hardware

Setting the IPIPE.SRC_EN.EN bit enables the IPIPE. This should be done after all of the required registers and tables mentioned in the previous section are programmed.

When the IPIPE is set to one-shot mode, only a single frame is processed. When the IPIPE is in continuous mode, it can be disabled by clearing the IPIPE.SRC_EN.EN bit during the processing of the last frame. The disable is latched in at the end of the frame it was written in.

5.6.3 Events and Status Checking

IPIPE has five interrupt signals, and the Resizer also has five interrupt signals. Enabling of the interrupt signals is controlled by the interrupt controller. The same interrupt events can be used to trigger the EDMA events that are controlled by the event controller.

5.6.3.1 IPIPE Interrupt Signals

IRQ0 (IPIPE_INT_REG) is issued when the IPIPE register update is allowed.

IRQ1 (IPIPE_INT_LAST_PIX) is issued when the last pixel of a frame comes into IPIPE.

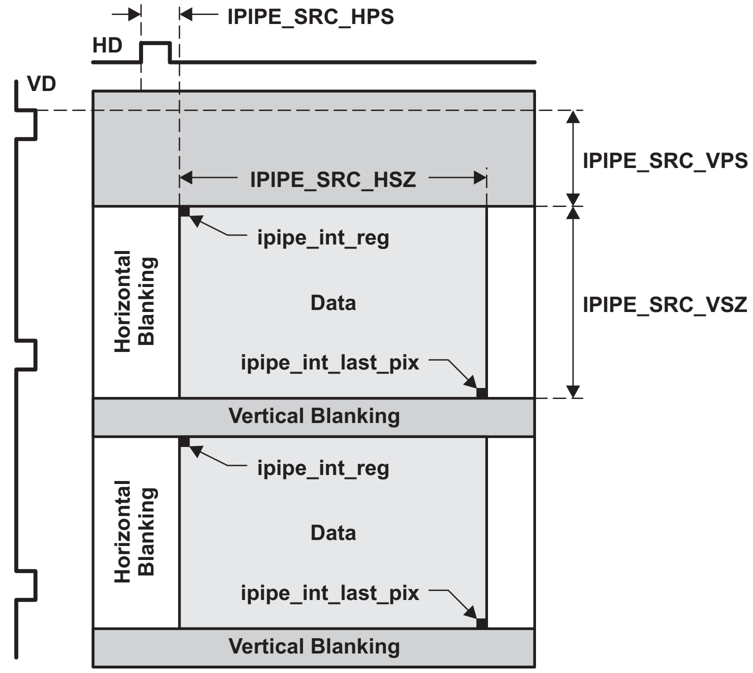
IRQ2 (IPIPE_INT_DMA) is issued when the boxcar SDRAM transfer is done. On this timing, IPIPE_EOF is sent to BL.

IRQ3 (IPIPE_INT_BSC) is issued when the boundary signal calculation is done.

IRQ4 (IPIPE_INT_HST) is issued when the histogram is done.

The interrupts IPIPE_INT_REG and IPIPE_INT_LAST_PIX are issued at the beginning and the end of the valid data area.

Figure 5-4. IPIPE_INT_REG and IPIPE_INT_LAST_PIX are Issued



5.6.3.2 Resizer Interrupt signals

RSZ_INT_REG is issued when the RSZ register update is allowed.

RSZ_INT_LAST_PIX is issued when the last pixel of a frame comes into RSZ

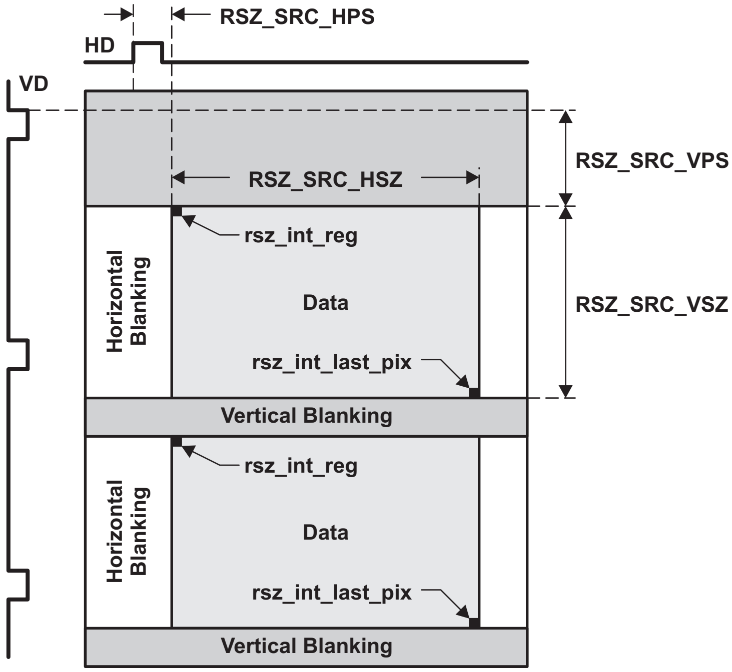
RSZ_INT_DMA is issued when the RSZ SDRAM (both resize-A and resize-B) transfer is done. On this timing, RSZ_EOF is sent to BL.

RSZ_INT_CYC_RZA is issued after every Na lines of image-a of the RSZ are written to SDRAM. (Na is specified by the register IRQ_RZA).

RSZ_INT_CYC_RZB is issued after every Na lines of image-b of the RSZ are written to SDRAM. (Na is specified by the register IRQ_RZB).

The interrupts RSZ_INT_REG and RSZ_INT_LAST_PIX are issued at the beginning and the end of the valid data area.

Figure 5-5. RSZ_INT_REG and RSZ_INT_LAST_PIX are Issued



5.6.4 Register Accessibility During Frame Processing

There are two types of register access in the IPIPE.

- **Shadow registers** - These registers can be read and written (if the field is writeable) at any time after receiving the IRQ0 event. However, the written values take effect at the start of next frame. Note that reads still return the most recent write even though settings are not used until the next start of frame. If these registers are written before receiving the IRQ0 event, the written values may apply to the current frame or the next frame. All the IPIPE registers not listed as busy-writeable registers below are included as shadow registers.
- **Busy-writeable registers** - These registers/fields can be read or written even if the module is busy. Changes to the underlying setting take place instantaneously. Therefore, to avoid unintended behavior, it is recommended that these registers only be written when the module is not busy. The following registers are busy-writeable:

IPIPE_GCK_PIX	RSZ_GCK_PIX
IPIPE_GCK_SDR	RSZ_GCK_SDR
IPIPE_HST_SEL	RSZ_SRC_MODE
IPIPE_SRC_VPS	RSZ_SRC_FMT0
IPIPE_SRC_HPS	RSZ_SRC_VPS
IPIPE_SRC_EN	RSZ_SRC_HPS
	RSZ_SRC_EN

5.6.5 Inter-Frame Operations

Between frames, it may be necessary to enable/disable functions or modify the memory pointers. Since several of the registers are shadowed, these modifications can take place any time after the IRQ0 (update register) interrupt and before the end of the frame and the data gets latched in for the next frame. The host controller can perform these changes upon receiving an interrupt or and EDMA transfer can be programmed to make these changes upon receiving an event.

Also, due to the input/output maximum width constraint of 2176 pixels (RZA), it may be necessary to process the image in vertical slices. The vertical slices processed by the IPIPE are required to overlap, due to the mirroring of image data at the edges, by internal filtering processes. The next section indicates how many edge pixels/lines are needed for edge overhead by enabling certain functions within the IPIPE.

5.7 Programming the H3A

This section discusses issues related to the software control of the H3A module. It lists which registers are required to be programmed in different modes, how to enable and disable the H3A, how to check the status of the H3A, discusses the different register access types, and enumerates several programming constraints.

5.7.1 Hardware Setup/Initialization

This section discusses the H3A configuration required before image processing can begin.

5.7.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the H3A are reset to their reset values.

5.7.1.2 Register Setup

For register configuration purposes, the H3A AF Engine and AEW Engine can be independently configured. There are separate enable bits for each engine, so this section is divided into the AF Engine and the AEW Engine.

5.7.1.2.1 AF Engine

Prior to enabling the AF Engine, the hardware must be properly configured via register writes. Table 5-8 identifies the register parameters that must be programmed before enabling the H3A AF Engine.

Table 5-8. AF Engine Required Configuration Parameters

Function	Configuration Required
AF Optional Preprocessing	PCR.AF_ALAW_EN PCR.AF_MED_EN
AF Mode Configuration	PCR.RGBPOS PCR.FVMODE
Paxel Start and Size Information	AFPAX1 AFPAX2 AFPAXSTART AFIIRSH
Memory Address	AFBUFST
Filter Coefficients	AFCOEF0[10:0] AFCOEF1[10:0]
Input Frame	LINE_START

Table 5-9 identifies additional configuration requirements depending on whether the corresponding condition is met. The table can be read as:

if(**Condition** is TRUE), then **Configuration Required** parameters must be programmed.

Table 5-9. AF Engine Conditional Configuration Parameters

Function	Condition	Configuration Required
Horizontal Median Filter	PCR.AF_MED_EN	PCR.MED_TH
Horizontal Focus Enable	PCR.AF_VF_EN = 0	HFV_THR
Both Horizontal and Vertical Focus Enable	PCR.AF_VF_EN = 1	VFV_CFG1

Table 5-9. AF Engine Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required
		VFV_CFG2 VFV_CFG3 VFV_CFG4 HFV_THR

The following references offer guidelines on how to program the filter coefficients and make use of the H3A output:

- M. Gamadia, V. Peddigari, N. Kehtarnavaz, S-Y. Lee, G. Cook, *Real-time Implementation of Auto Focus on the TI DSC Processor*, Proceedings of SPIE Real-Time Imaging Conference, Jan 2004
- N. Kehtarnavaz, H-J. Oh, *Development and real-time implementation of a rule-based auto-focus algorithm*, Journal of Real-Time Imaging, 9, 197-203, 2003

5.7.1.2.2 AEW Engine

Prior to enabling the AEW Engine, the hardware must be properly configured via register writes. Table 45 identifies the register parameters that must be programmed before enabling the H3A AEW Engine.

Table 5-10. AEW Engine Required Configuration Parameters

Function	Configuration Required
AEW Optional Preprocessing	PCR.AEW_ALAW_EN
Saturation Limit	PCR.AVE2LMT
Window Start and Size Information	AEWIN1 AEWINSTART AEWINBLK AEWSUBWIN
Memory Address	AEWBUFST
Input Frame	LINE_START

5.7.2 Enable/Disable Hardware

Setting the PCR.AF_EN bit enables the AF Engine, and the PCR.AEW_EN bit enables the AEW Engine. This should be done after all of the required registers in the previous section are programmed.

The H3A input source is the Image Sensor Interface (ISIF) and processing of the frame is dependent upon the timing of the ISIF. In order to guarantee that data from the ISIF is not missed, the H3A should be enabled prior to the ISIF. In this way, the H3A waits for the data from the ISIF. The AF Engine or AEW Engine can be disabled by clearing the PCR.AF_EN or PCR.AEW_EN bit, respectively, during the processing of the last frame. The disable is latched in at the end of the frame it was written in.

5.7.3 Events and Status Checking

The H3A module generates three interrupts (or three events to the EDMA) to the interrupt controller. They are described as follows:

1. AF_INT - This interrupt is generated after the completion of auto-focus processing per frame.
2. AEW_INT - This interrupt is generated after the completion of auto-exposure/auto-white balance processing per frame.
3. H3A_INT - This interrupt is generated at the same time as the last process to finish for each frame. This means that the interrupt comes when both the AF and AEW processes are finished.

The PCR.BUSYAF and/or PCR.BUSYAEAWB status bits are set when the start of frame occurs (if the PCR.AF_EN and/or PCR.AEW_EN bits are 1 at that time). They are automatically reset to 0 at the end of processing a frame. The PCR.BUSYAF and/or PCR.BUSYAEAWB status bits may be polled to determine the end-of-frame status.

5.7.4 Register Accessibility During Frame Processing

There are two types of register access in the H3A module.

- **Shadow registers**:
  – These registers/fields can be read and written (if the field is writeable) at any time. However, the written values take effect only at the start of a frame. Note that reads still return the most recent write even though the settings are not used until the next start of frame.
  – The following registers are shadow registers in the H3A module:

AFPAX1	AEWIN10
AFPAX2	AEWINSTART
AFPAXSTART	AEWINBLK
AFIIRSH	AEWSUBWIN
	AEWCFG

- **Busy-lock registers**:
  – Busy-lock registers cannot be written when the module is busy. Writes are allowed to occur, but no change occurs in the registers (blocked writes from the hardware perspective, but allowed writes from the software perspective). Once the busy bit in the PCR register is reset to 0, the busy-lock registers can be written.
  – All the registers EXCEPT the registers mentioned above as shadow registers, are busy-lock registers.

The ideal procedure for changing the H3A registers is:

```
IF (busy == 0) OR IF (EOF interrupt occurs) DISABLE AF or AE/AWB CHANGE REGISTERS ENABLE AF or
AE/AWB
```

5.7.5 Inter-Frame Operations

Between frames, it may be necessary to modify the memory pointers before processing the next frame. Since the PCR and memory pointer registers are shadowed, these modifications can take place any time before the end of the frame and the data gets latched in for the next frame. The host controller can perform these changes upon receiving an interrupt or an EDMA transfer can be programmed to make these changes upon receiving an event.

5.7.6 Summary of Constraints

The following is a list of register configuration constraints to adhere to when programming the H3A. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

- The H3A should not be enabled for Foveon formatted input.
- The output addresses must be on 64-byte boundaries.
- The maximum width is 4096 pixels per line.

AF Engine:

- The paxel horizontal start value must be greater than or equal to the IIR horizontal start position.
- The width and height of the paxels must be an even number.
- The minimum width of the auto focus paxel must be 8 pixels.
- Paxels cannot overlap the last pixel in a line.
- Paxels must be adjacent to one another.

AEW Engine:

- The width and height of the windows must be an even number.
- Sub-sampling windows can only start on even numbers.
- The minimum width of the AE/AWB windows must be 8 pixels.

5.8 Programming ISP/VPSS Subsystem Level Registers

This section discusses issues related to the ISP/VPSS software control subsystem level. The ISP/VPSS subsystem comprises the infrastructure data path switches, interrupt control muxing, and clock gating control within the VPSS. This section briefly lists which registers are required to be programmed in different configurations of the VPSS.

5.8.1 Hardware Setup/Initialization

This section discusses the configuration of the ISP and VPSS subsystems before image processing can begin.

5.8.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the ISP and VPSS register modules are reset to their reset values.

5.8.1.2 Register Setup

Prior to enabling the modules within the VPSS, the buffer logic hardware must be properly configured via register writes. Table 5-11 identifies the register parameters that must be programmed properly before enabling various modules. The items not bolded are optional, depending on whether the operational mode of the module requires the setting or not.

Table 5-11. ISP and VPSS Subsystem Required Configuration Parameters

Module	Configuration Required
ISIF	**ISP.PCCR.ISIF_CLK_ENABLE** ISP.BCR.SRC_SEL_ISIF_IPIPE
IPIPEIF	**ISP.PCCR.IPIPEIF_CLK_ENABLE**
IPIPE	**ISP.PCCR.IPIPE_CLK_ENABLE** ISP.BCR.SRC_SEL_ISIF_IPIPE (boxcar/ISIF) **ISP.PCCR.RSZ_CLK_ENABLE**
H3A	**ISP.PCCR.H3A_CLK_ENABLE**

5.8.2 Event and Status Checking

The ISP/VPSS subsystem controls the selection of which module interrupts are routed to the ARM ~~interrupt controller and EDMA event controllers using the ISP.INTSEL[3:1] and ISP.EVTSEL registers.~~ The ISP.INTSTAT register can also be used to poll for events. For more details, see Section 3.2.

5.8.3 Inter-Frame Operations

Since the ISP and VPSS subsystem registers are busy-writeable, care must be taken when modifying any of these registers. It is recommended that affected modules be disabled while switching modes and modifying any of these registers.

5.8.4 Summary of Constraints

None noted.

5.9 Error Identification

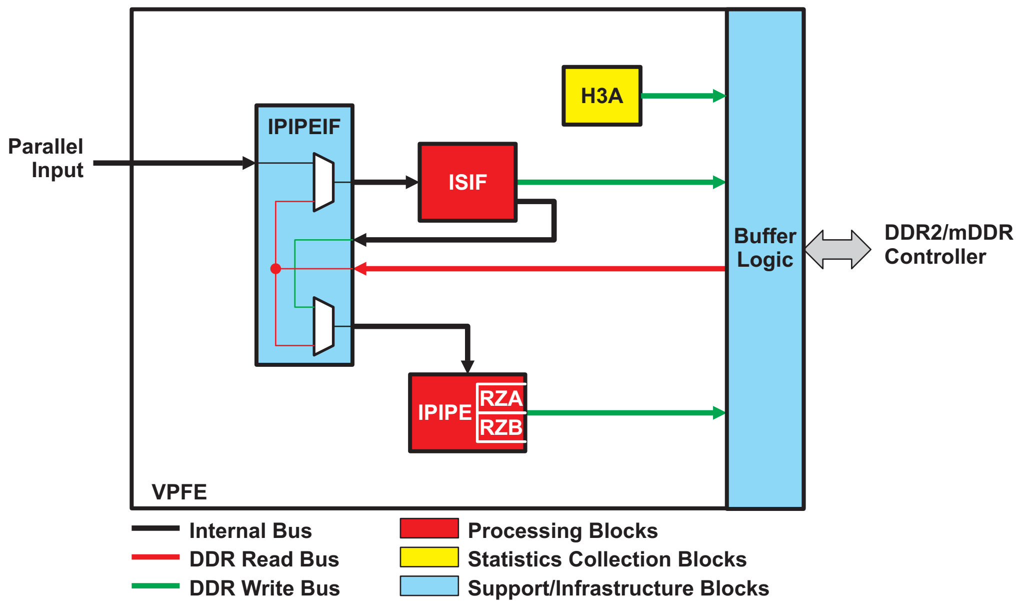
The modules that make use of hardware error identification and reporting are the ISIF (LSC) and IPIPEIF. To find more information about the error reporting registers and interrupts of these modules, see Section 5.4 and Section 5.5.

5.10 Supported Use Cases

The VPFE is designed to support a variety of video and imaging applications. For the purposes of describing the VPFE configuration for typical use cases, the application space can be divided into the following two input types: CCD/CMOS sensor data and YUV video data. This section discusses typical VPFE configurations for both of these input types separately and then discusses how both applications use the IPIPE Resizers to resize or change the aspect ration of processed video or image data.

Figure 5-6 depicts all the possible data paths through the VPFE. Each mode described in this section has a unique data path through the various modules.

Figure 5-6. Data Paths Through the VPFE



5.10.1 *CCD/CMOS Sensor Input Specific Applications*

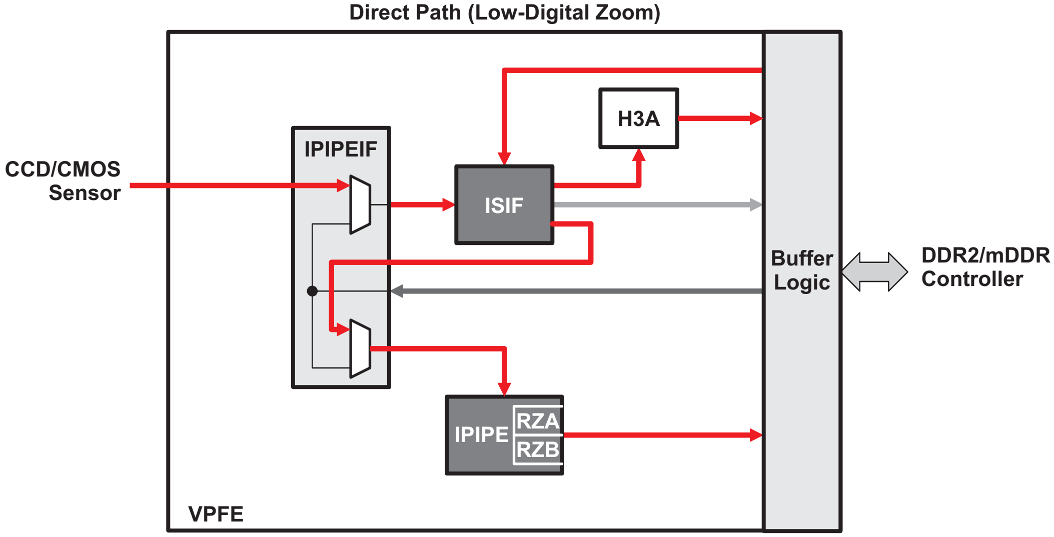
Digital still cameras and digital video cameras are the primary applications that use CCD or CMOS sensor input sources. CCD or CMOS sensors output analog data at a rate determined by a timing generator (TG). The analog front end (AFE) converts this data to a digital signal and transmits this digital raw sensor data to the input interface of the CCD controller. Depending on the sensor, this data is typically in a Bayer pattern where every pixel represents only one of the three primary colors (RGB) or their complementary colors (CYGM). The VPFE contains programmable functions that capture and digitally process this raw data into YUV-formatted video or image data that can be compressed or displayed directly on an external display.

In this application, there are three basic modes of operation that require different VPFE data paths and configurations: preview/movie capture mode, still image capture mode, and still image processing mode.

5.10.1.1 Preview/Movie Capture Mode

In a digital still camera or video camera, preview and movie capture modes are where the VPFE receives raw video data from the sensor, converts it to YUV format, and displays it on the display in real-time. There is only one distinguishing detail between preview mode and movie capture mode. In preview mode, the video data is only temporarily stored in a circular buffer in the SDRAM memory until it can be displayed and/or transmitted; in movie capture mode, the video data is additionally compressed and stored in non-volatile memory (e.g., Flash, digital video tape, DVD, hard disk, etc). Both modes have the same data path through the VPFE, as shown in Figure 5-7 , except for one potential exception: for preview mode, only one resizer output of the IPIPE is required to resize the image display size; however, in movie capture mode, if the display size is different than the encoded movie size, then both resizers can be used to output these two sizes of the video (e.g., display is VGA and MPEG encode is D1).

Figure 5-7. Preview/Movie Capture Data Paths



Register Field	Value
ISP.PCCR.ISIF_CLK_ENABLE	1
ISP.PCCR.IPIPEIF_CLK_ENABLE	1
ISP.PCCR.IPIPE_CLK_ENABLE	1
ISP.PCCR.RSZ_CLK_ENABLE	1
ISP.PCCR.H3A_CLK_ENABLE	1
ISP.PCCR.BL_CLK_ENABLE	1
ISP.BCR.SRC_SEL_ISIF_IPIPE (ISIF/boxcar)	0

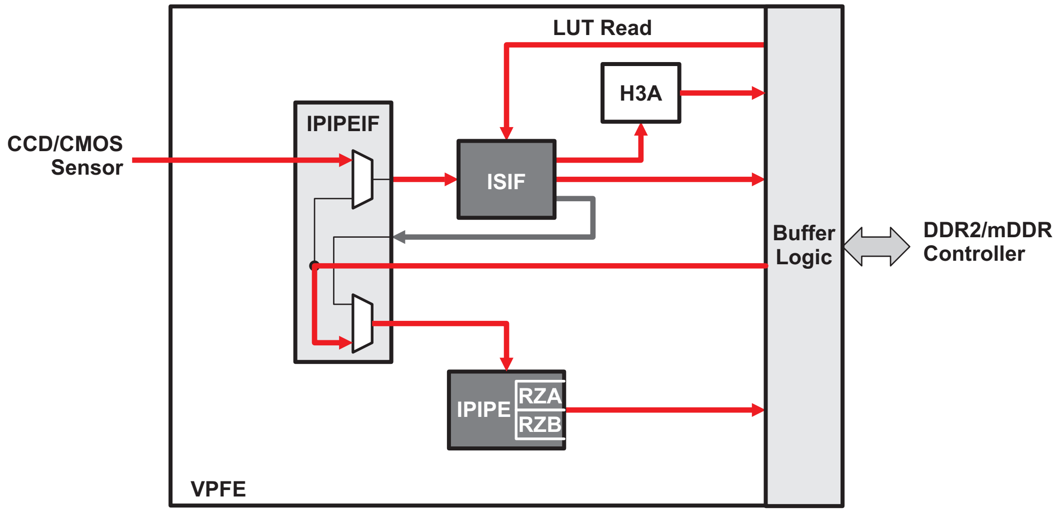
As you can see from , all of the modules may be enabled for this mode. The camera application spends the majority of its time in this mode, so the SDRAM bandwidth consumption is minimized by having a single image data path to memory (in addition to the H3A statistic data path) which is resized to the correct display size. The ARM can read the histogram information from the IPIPE memory-mapped registers after a frame has completed.

Typically in this mode, the ISIF receives the digital raw data from the sensor/AFE in a down-sampled resolution format. Different sensors may have different readout patterns in this mode (e.g., draft mode, movie mode, VGA mode, etc.). The full 16-bit raw data is output to the IPIPEIF and the upper 10-bit raw data is output to the H3A module. The IPIPE performs most of the image signal processing (e.g., CFA interpolation, white balance, noise filtering, etc.) and converts the raw data to YUV 4:2:2/4:2:0 video format. If the input is not the correct size or aspect ration for display or storage and/or if digital zoom is required, then the IPIPE can output two separately resized outputs of the image concurrently. The image(s) output from the IPIPE sent to SDRAM in a circular buffer where they are consumed for display and/or compression. End-of-frame interrupts from the IPIPE and/or other VPFE modules can trigger ARM interrupt service routines to change the address of the write buffer in the IPIPE module for each frame. The image statistics from the H3A and IPIPE-embedded histogram can be used by the ARM for implementing algorithms to modify the image processing parameters of the IPIPE and/or focus lens of the imager for subsequent frames.

5.10.1.1.1 Digital Zoom Case

As the digital zoom factors increase, there may be a threshold where the IPIPE cannot process the data fast enough as per its requirement found in Section 4.3.11. At this point, the ISIF should send the cropped output to SDRAM instead of the IPIPE. Then, the IPIPE can read this data at a slower pixel clock defined by the IPIPEIF-divided clock and PPLN value. This rate can be made as slow as possible while still meeting the required frame rate so as to keep the instantaneous SDRAM bandwidth to a minimum. Additionally, DPCM compression can be utilized on the SDRAM path so that this bandwidth is reduced even further. This buffer path is shown in Figure 5-8 .

Figure 5-8. Preview/Movie Capture Data Paths (Buffer Path)

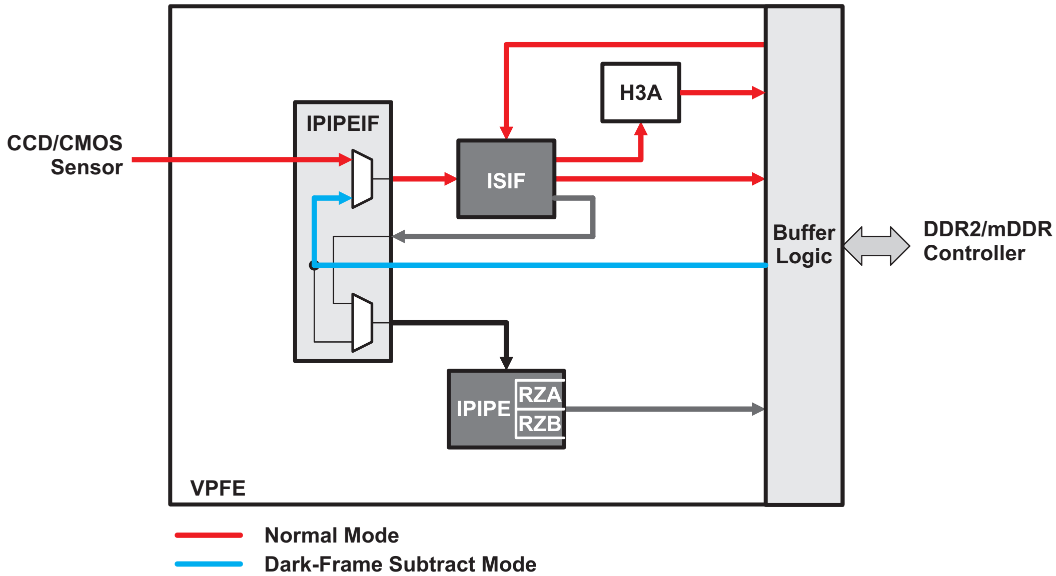


Register Field	Value
ISP.PCCR.ISIF_CLK_ENABLE	1
ISP.PCCR.IPIPEIF_CLK_ENABLE	1
ISP.PCCR.IPIPE_CLK_ENABLE	X
ISP.PCCR.RSZ_CLK_ENABLE	X
ISP.PCCR.H3A_CLK_ENABLE	1
ISP.PCCR.BL_CLK_ENABLE	1
ISP.BCR.SRC_SEL_ISIF_IPIPE (ISIF/boxcar)	1 (ISIF o/p)

5.10.1.1.2 Still Image Capture

In a digital still camera or video camera, still image capture is where the VPFE is receiving full resolution raw image data from the sensor and storing it to SDRAM to be analyzed, processed and/or later stored to non-volatile memory (e.g., flash, digital video tape, DVD, hard disk, etc.). The data path through the VPFE for still image capture is shown in Figure 5-9.

Figure 5-9. Raw Image Capture Data Path



Register Field	Value
ISP.PCCR.ISIF_CLK_ENABLE	1
ISP.PCCR.IPIPEIF_CLK_ENABLE	1
ISP.PCCR.IPIPE_CLK_ENABLE	X
ISP.PCCR.RSZ_CLK_ENABLE	X
ISP.PCCR.H3A_CLK_ENABLE	1
ISP.PCCR.BL_CLK_ENABLE	1
ISP.BCR.SRC_SEL_ISIF_IPIPE (ISIF/boxcar)	1 (ISIF o/p)

As shown in , dark-frame subtract can be optionally enabled, depending on SDRAM bandwidth usage and sensor quality. Typically, in still capture mode, the ISIF receives the full resolution of the digital raw data from the sensor/AFE. Some sensors (typically CMOS) read the data out in progressive format, whereas other (typically CCD) read the data in multiple fields.

If the format is progressive, the ISIF can perform lens shading correction on the incoming image and the H3A can extract AEW parameters.

If the input format is field based, then software should set the line offset and starting address of the ISIF outputs accordingly so that the frame is de-interleaved as it is stored into SDRAM memory. Then, the AEW parameter extraction can later be done on the data from SDRAM.

If the image is 2176 pixels wide or less, it is possible for the output of the ISIF to go directly into the IPIPE instead of SDRAM. However, the data path shown in would be used most of the time for still image capture. This is because additional processing on the raw data may be required to improve the quality of the image, such as noise filtering and/or lens distortion correction (covered in the next section). Also, if the image width is greater than 2176 pixels, then this path is required so that the IPIPE can process the image in slices from SDRAM.

5.10.1.1.3 Still Image Processing

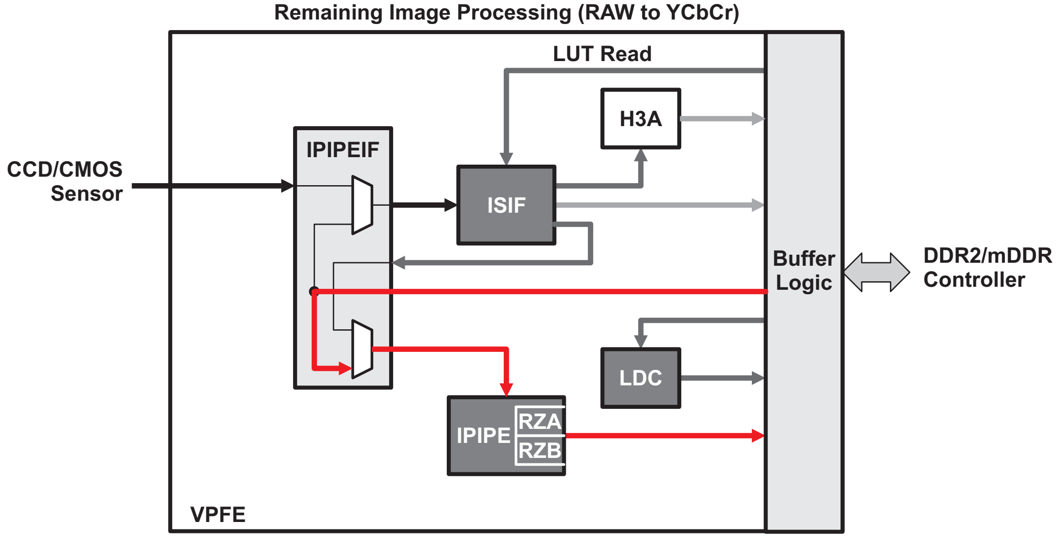
In a digital still camera or video camera, still image processing mode is when the raw image data that was captured to SDRAM during still capture mode is processed into YUV image data which can be later compressed and stored in non-volatile memory. The IPIPE performs most of the image processing steps required, including the raw-to-YUV processing, however, the VPFE in the DM36x is designed with additional raw image processing operations to further improve the quality of the final image. The next three sections describe optional steps and paths through the VPFE that can be taken to improve image quality; the fourth section describes the required final path of processing through the IPIPE.

NOTE: If the input format is progressive, then the step shown in the next section can be skipped since it should have already been done during image capture.

5.10.1.1.3.1 Image Processing (Raw to YCbCr)

Raw data captured in SDRAM can pass through the IPIPE with the raw-to-YCbCr data path enabled to perform the remaining image processing functions on the image. The data path for this step is shown in Figure 5-10 . As the figures shows, both resizer outputs are enabled. Typically, one resizer would output the full resolution still image and the other resizer may output a *thumb-nail* or *screen-nail* image to be encoded for quick display during image playback.

Figure 5-10. Remaining Image Processing Data Path



Register Field	Value
ISP.PCCR.ISIF_CLK_ENABLE	0
ISP.PCCR.IPIPEIF_CLK_ENABLE	1
ISP.PCCR.IPIPE_CLK_ENABLE	1
ISP.PCCR.RSZ_CLK_ENABLE	1
ISP.PCCR.H3A_CLK_ENABLE	0
ISP.PCCR.BL_CLK_ENABLE	1
ISP.BCR.SRC_SEL_ISIF_IPIPE (ISIF/boxcar)	X

Since the internal line memory is optimized for image resolutions of 5MP, the IPIPE can process a maximum output and input width of 2600 pixels in a single pass. Therefore, for images larger than 5MP, it required multiple passes through the IPIPE to process a full-resolution, still-captured image. This is done by partitioning the input image into multiple overlapping vertical slices and aligning the output in such a way that the processed image is seamlessly stitched together. We refer to this mode of the IPIPE as frame division mode - V.

In addition to vertical slicing, it may be required to perform horizontal slicing of the processing so that compression of the output image can be pipelined in parallel. This concept can be implemented in much the same way as the vertical slicing. We refer to this mode of the IPIPE as frame division mode - H.

5.10.2 YUV Video Input-Specific Applications

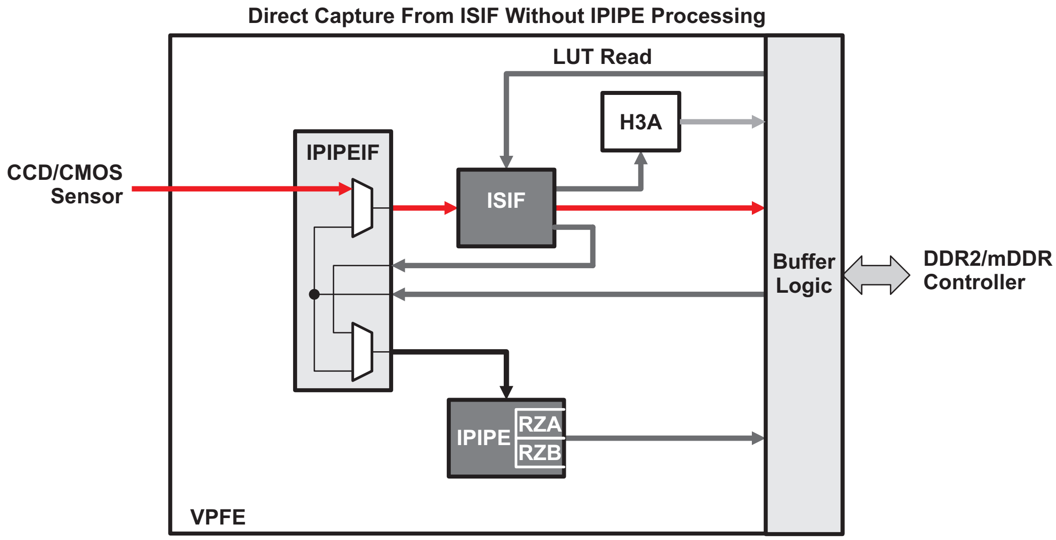
There are a variety of applications that use YUV video input sources: IP phones, video surveillance systems, and digital video recorders to name a few. Most any application that needs to capture YUV video, compress it, and transmit or store it can be included in this application category.

5.10.2.1 Video Capture Mode

Video capture mode is where the VPFE is receiving YUV video data from a digital video source and storing it to SDRAM for further processing and/or compression. On its input interface, the ISIF of the VPFE can capture BT.656-formatted video or generic 8- or 16-bit YUV digital video data from a digital video source such as an NTSC/PAL video decoder.

The possible data paths through the VPFE for video capture are shown in Figure 5-11 .

Figure 5-11. Video Capture Data Path

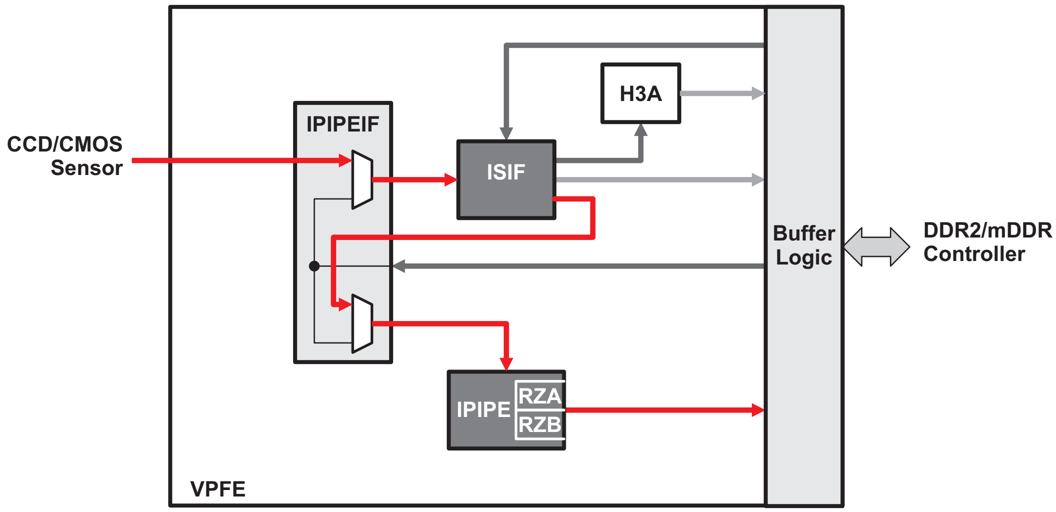


Register Field	Value
ISP.PCCR.ISIF_CLK_ENABLE	1
ISP.PCCR.IPIPEIF_CLK_ENABLE	1
ISP.PCCR.IPIPE_CLK_ENABLE	0
ISP.PCCR.RSZ_CLK_ENABLE	0
ISP.PCCR.H3A_CLK_ENABLE	0
ISP.PCCR.BL_CLK_ENABLE	1
ISP.BCR.SRC_SEL_ISIF_IPIPE (ISIF/boxcar)	1 (ISIF o/p)

As shows, the ISIF module is the only module enabled for this mode.

The YUV data captured through ISIF can be passed to IPIPE for further processing or resizing and then stored into SDRAM as shown in Figure 5-12 .

Figure 5-12. YUV Video Capture Data Path



Register Field	Value
ISP.PCCR.ISIF_CLK_ENABLE	1
ISP.PCCR.IPIPEIF_CLK_ENABLE	1
ISP.PCCR.IPIPE_CLK_ENABLE	1
ISP.PCCR.RSZ_CLK_ENABLE	1
ISP.PCCR.H3A_CLK_ENABLE	0
ISP.PCCR.BL_CLK_ENABLE	1
ISP.BCR.SRC_SEL_ISIF_IPIPE (ISIF/boxcar)	X

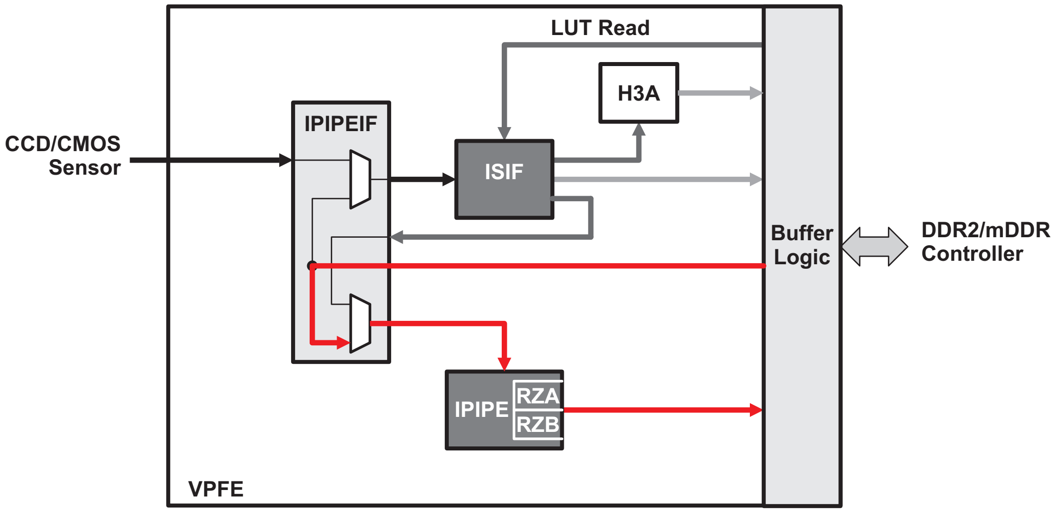
5.10.3 Video/Image Resize Applications

Application from both CCD/CMOS sensor data and YUV video data input categories use the resizers in the IPIPE to resize YUV 4:2:2-formatted video images from SDRAM.

5.10.3.1 Processed Image Resize

Processed image resize is where the resizers in the IPIPE take YUV-formatted image/video data from SDRAM and resize it back to SDRAM. Typically, the image coprocessors uncompress image or video data first and, then have the IPIPE resize the image to be displayed on a display device or recompressed again. Normally, only one resizer is required, but both can be used. The data path through the VPFE for video/image resize is shown in Figure 5-13 .

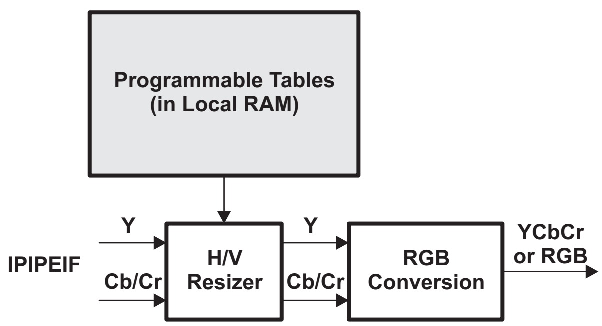
Figure 5-13. Processed Image Resize Data Path



Register Field	Value
ISP.PCCR.ISIF_CLK_ENABLE	0
ISP.PCCR.IPIPEIF_CLK_ENABLE	1
ISP.PCCR.IPIPE_CLK_ENABLE	1
ISP.PCCR.RSZ_CLK_ENABLE	1
ISP.PCCR.H3A_CLK_ENABLE	0
ISP.PCCR.BL_CLK_ENABLE	1
ISP.BCR.SRC_SEL_ISIF_IPIPE (ISIF/boxcar)	X

Within the IPIPE, the YCbCr input skips the raw data processing and enters the final stages of the IPIPE, as shown in Figure 5-14 .

Figure 5-14. YCbCr Input Resize Data Path in IPIPE



5.10.3.1.1 Multi-Pass Resize

There are two constraints in the IPIPE resizers that may require multiple passes in order to achieve a desired size:

1. Resize ratio range is limited to between 1/16x and 16x resize.
2. Maximum input/output width is 2176 pixels.

Resize ratio range: a single pass through the IPIPE can resize an image down to 1/16 or up to 16 times the input width and/or height. In order to achieve resize operations beyond this range, multiple passes through the IPIPE are required until the final sizing is achieved. For example, if a 1/20x resize is required, then a 1/10x resize and a 1/2x resize can be applied, in two passes.

Maximum output width: Since the internal line memory is optimized for video resolutions and still images up to 5MP, the IPIPE can operate on a maximum output/input width of 2176 pixels in a single pass. Therefore, it requires multiple passes through the IPIPE to resize to larger images that exceed this horizontal width requirement. This is done by partitioning the input image into multiple vertical slices and aligning the output is such a way that the processed image is seamlessly stitched together.

The basic idea is to begin subsequent slices at exactly where previous images left off. The starting phase and pixel registers can be programmed to this exact location. This location can be calculated using the algorithm details and examples in .

Registers

There are seven sub-modules associated with the VPFE subsystem, as shown in Table 6-1.

Table 6-1. Video Processing Front End Sub-Module Register Map

Address: Offset	Acronym	Register Description	Section
0x01C7:1000	ISIF	Image Sensor Interface	Section 6.1
0x01C7:1200	IPIPEIF	Image Pipe Interface	Section 6.2
0x01C7:0800	IPIPE	Image Pipe	Section 6.3
0x01C7:0400	RSZ	Resizer	Section 6.4
0x01C7:1400	H3A	Hardware 3A	Section 6.5
0x01C7:0000	ISP	ISP System Configuration	Section 6.6
0x01C7:0200	VPSS	VPSS System Configuration	Section 6.7

6.1 ISIF REGISTERS

Table 6-2 lists the memory-mapped registers for the Image Sensor Interface (ISIF). See the device-specific data manual for the memory address of these registers.

Table 6-2. Image Sensor Interface (ISIF) Registers

Offset	Acronym	Register Description	Section
0h	SYNCEN 3	Synchronization Enable	Section 6.1.1
004h	MODESET 2000	Mode Setup	Section 6.1.2
008h	HDW 0	HD pulse width	Section 6.1.3
00Ch	VDW 0	VD pulse width	Section 6.1.4
010h	PPLN 0	Pixels per line	Section 6.1.5
014h	LPFR 1	Lines per frame	Section 6.1.6
018h	SPH 0	Start pixel horizontal	Section 6.1.7
01Ch	LNH 9ff	Number of pixels in line	Section 6.1.8
020h	SLV0 1	Start line vertical - field 0	Section 6.1.9
024h	SLV1 1	Start line vertical - field 1	Section 6.1.10
028h	LNV 2df	Number of lines vertical	Section 6.1.11
02Ch	CULH ffff	Culling - horizontal	Section 6.1.12
030h	CULV ff	Culling - vertical	Section 6.1.13
034h	HSIZE 50	Horizontal size	Section 6.1.14
038h	SDOFST 0	SDRAM Line Offset	Section 6.1.15
03Ch	CADU 0x41b	SDRAM Address - high	Section 6.1.16
040h	CADL 0x 9d80	SDRAM Address - low	Section 6.1.17
04Ch	CCOLP 4e4e	CCD Color Pattern	Section 6.1.18
050h	CRGAIN 0x200	CCD Gain Adjustment - R/Ye	Section 6.1.19
054h	CGRGAIN 0x200	CCD Gain Adjustment - Gr/Cy	Section 6.1.20
058h	CGBGAIN 0x200	CCD Gain Adjustment - Gb/G	Section 6.1.21
05Ch	CBGAIN 0x200	CCD Gain Adjustment - B/Mg	Section 6.1.22
060h	COFSTA	CCD Offset Adjustment	Section 6.1.23

Table 6-2. Image Sensor Interface (ISIF) Registers (continued)

Offset	Acronym	Register Description	Section
064h	FLSHCFG0	FLSHCFG0	Section 6.1.24
068h	FLSHCFG1	FLSHCFG1	Section 6.1.25
06Ch	FLSHCFG2	FLSHCFG2	Section 6.1.26
070h	VDINT0 0x2c0	VD Interrupt #0	Section 6.1.27
074h	VDINT1 0x2c0	VD Interrupt #1	Section 6.1.28
078h	VDINT2 0x2c0	VD Interrupt #2	Section 6.1.29
080h	CGAMMAWD 0x7708	Gamma Correction settings	Section 6.1.30
084h	REC656IF 0	CCIR 656 Control	Section 6.1.31
088h	CCDCFG 0x912	CCD Configuration	Section 6.1.32
08Ch	DFCCTL	Defect Correction - Control	Section 6.1.33
090h	VDFSATLV	Defect Correction - Vertical Saturation Level	Section 6.1.34
094h	DFCMEMCTL	Defect Correction - Memory Control	Section 6.1.35
098h	DFCMEM0	Defect Correction - Set V Position	Section 6.1.36
09Ch	DFCMEM1	Defect Correction - Set H Position	Section 6.1.37
0A0h	DFCMEM2	Defect Correction - Set SUB1	Section 6.1.38
0A4h	DFCMEM3	Defect Correction - Set SUB2	Section 6.1.39
0A8h	DFCMEM4	Defect Correction - Set SUB3	Section 6.1.40
0ACh	CLAMPCFG	Black Clamp configuration	Section 6.1.41
0B0h	CLDCOFST 0x1f38	DC offset for Black Clamp	Section 6.1.42
0B4h	CLSV	Black Clamp Start position	Section 6.1.43
0B8h	CLHWIN0 0x1f	Horizontal Black Clamp configuration	Section 6.1.44
0BCh	CLHWIN1	Horizontal Black Clamp configuration	Section 6.1.45
0C0h	CLHWIN2	Horizontal Black Clamp configuration	Section 6.1.46
0C4h	CLVRV	Vertical Black Clamp configuration	Section 6.1.47
0C8h	CLVWIN0	Vertical Black Clamp configuration	Section 6.1.48
0CCh	CLVWIN1	Vertical Black Clamp configuration	Section 6.1.49
0D0h	CLVWIN2	Vertical Black Clamp configuration	Section 6.1.50
0D4h	CLVWIN3 0x1fff	Vertical Black Clamp configuration	Section 6.1.51
11Ch	FMTSPH 0	CCD Formatter - Start pixel horizontal	Section 6.1.52
120h	FMTLNH 0	CCD Formatter - number of pixels	Section 6.1.53
124h	FMTSLV 0	CCD Formatter - start line vertical	Section 6.1.54
128h	FMTLNV 0	CCD Formatter - number of lines	Section 6.1.55
12Ch	FMTRLEN 0	CCD Formatter - Read out line length	Section 6.1.56
130h	FMTHCNT 0	CCD Formatter - HD cycles	Section 6.1.57
1A4h	CSCCTL	Color Space Converter Enable	Section 6.1.58
1A8h	CSCM0	Color Space Converter - Coefficients #0	Section 6.1.59
1ACh	CSCM1	Color Space Converter - Coefficients #1	Section 6.1.60
1B0h	CSCM2	Color Space Converter - Coefficients #2	Section 6.1.61
1B4h	CSCM3	Color Space Converter - Coefficients #3	Section 6.1.62
1B8h	CSCM4	Color Space Converter - Coefficients #4	Section 6.1.63
1BCh	CSCM5	Color Space Converter - Coefficients #5	Section 6.1.64
1C0h	CSCM6	Color Space Converter - Coefficients #6	Section 6.1.65
1C4h	CSCM7	Color Space Converter - Coefficients #7	Section 6.1.66

6.1.1 Synchronization Enable (SYNCEN)

The synchronization enable (SYNCEN) register is shown in Figure 6-1 and described in Table 6-3.

Figure 6-1. Synchronization Enable (SYNCEN) Register

31–16
Reserved
R-0

15–2	1	0
Reserved	DWEN	SYEN
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-3. Synchronization Enable (SYNCEN) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	DWEN		Data Write Enable Controls whether or not CCD raw data is written to SDRAM. This bit is latched by VD.
		0	Disable
		1	Enable
0	SYEN		VD/HD Enable If VD/HD are defined as output, activates internal timing generator. If VD/HD are defined as inputs, activates internal timing generator to synchronize with VD/HD.
		0	Disable
		1	Enable

6.1.2 Mode Setup (MODESET)

The mode setup (MODESET) register is shown in Figure 6-2 and described in Table 6-4.

Figure 6-2. Mode Setup (MODESET) Register

31–16
Reserved
R-0

15	14	13–12	11	10–8
MDFS	HLPF	INPMOD	Reserved	CCDW
R-0	R/W-0	R/W-2	R-0	R/W-0

7	6	5	4	3	2	1	0
CCMD	DPOL	SWEN	FIPOL	HDPOL	VDPOL	FIDD	HDVDD
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-4. Mode Setup (MODESET) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15	MDFS		Field Status
		0	Odd field
		1	Even field
14	HLPF		3_tap Low_Pass (anti_aliasing) Filter 1/4, 1/2, 1/4 filtering applied to CCD data. This bit is latched by VD
		0	Off
		1	On
13-12	INPMOD		Data input mode
		0	CCD RAW data
		1	YCbCr 16-bit
		2	YCbCr 8-bit
		3	Reserved
11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-8	CCDW		CCD RAW Data Right Shift for Data Written to SDRAM valid only when INPMOD is set to '0'
		0	No shift
		1	1-bits
		2	2-bits
		3	3-bits
		4	4-bits
		5-7	Reserved
7	CCDMD		Sensor Field Mode. This bit should not be set if the External Write Enable bit is set.
		0	NoR-0interlaced (progressive)
		1	Interlaced
6	DPOL		CCD input Data Polarity
		0	Normal (no change)
		1	1's complement
5	SWEN		External WEN Selection When set to 1 and when ENABLE is set to 1, the external WEN signal is used as the external memory write enable (to SDRAM/DDRAM). The data is stored to memory only when the external sync (HD and VD) signals are active. This bit should not be set if the C_WE_Field bit is set.
		0	Do not use external WEN (Write Enable)
		1	Use external WEN (Write Enable)

Table 6-4. Mode Setup (MODESET) Field Descriptions (continued)

Bit	Field	Value	Description
4	FIPOL		Field Indicator Polarity
		0	Positive
		1	Negative
3	HDPOL		HD Sync Polarity
		0	Positive
		1	Negative
2	VDPOL		VD Sync Polarity
		0	Positive
		1	Negative
1	FIDD		Field ID Signal Direction
		0	Input
		1	Output
0	HDVDD		VD/HD Sync Direction
		0	Input
		1	Output

6.1.3 HD Pulse Width (HDW)

The HD pulse width (HDW) register is shown in Figure 6-3 and described in Table 6-5.

Figure 6-3. HD Pulse Width (HDW) Register

31–16
Reserved
R-0

15–12	11–0
Reserved	HDW
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-5. HD Pulse Width (HDW) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	HDW	0-FFFh	Width of HD sync pulse if output: HDW+1 pixel clocks HDWIDTH is not used when HD is input, i.e., when VDHDOUT in MODESET is cleared to '0'. This bit field is latched by VD.

6.1.4 VD Pulse Width (VDW)

The VD pulse width (VDW) register is shown in Figure 6-4 and described in Table 6-6.

Figure 6-4. VD Pulse Width (VDW) Register

31–16
Reserved
R-0

15–12	11–0
Reserved	VDW
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-6. VD Pulse Width (VDW) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VDW	0-FFFh	Width of VD sync pulse if output: VDW+1 lines VDWIDTH is not used when VD is input (i.e. when VDHDOUT in MODESET is cleared to 0). This bit field is latched by VD.

6.1.5 Pixels Per Line (PPLN)

The pixels per line(PPLN) register is shown in Figure 6-5and described in Table 6-7.

Figure 6-5. Pixels Per Line (PPLN) Register

31	16
Reserved	
R-0	

15	0
PPLN	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-7. Pixels Per Line (PPLN) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	PPLN	0-FFFFh	Pixels per line Number of pixel clock periods in one line HD period = PPLN+1 pixel clocks PPLN is not used when HD and VD are inputs(i.e., when VDHDOUT in MODESET is cleared to '0). This bit field is latched by VD.

6.1.6 Lines Per Frame (LPFR)

The lines per frame register (LPFR) is shown in Figure 6-6 and described in Table 6-8.

Figure 6-6. Lines Per Frame (LPFR) Register

31 — 16
Reserved
R-0

15 — 0
LPFR
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-8. Lines Per Frame (LPFR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	LPFR	0-FFFFh	Half lines per filed or frame Sets number of half lines per frame or field. VD period = (LPFR+1)/2 lines. LPFR is not used when HD and are inputs, i.e., when VDHDOUT in MODESET is cleared to 0. This bit field is latched by VD.

6.1.7 Start Pixel Horizontal (SPH)

The start pixel horizontal (SPH) register is shown in Figure 6-7and described in Table 6-9.

Figure 6-7. Start Pixel Horizontal (SPH) Register

31–16
Reserved
R-0

15	14–0
Reserved	SPH
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-9. Start Pixel Horizontal (SPH) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	SPH	0-7FFFh	Start pixel, horizontal. Sets pixel clock position at which data output to SDRAM begins, measured from the start of HD. This bit field is latched by VD.

6.1.8 Number of Pixels in Line (LNH)

The number of pixels in line (LNH) register is shown in Figure 6-8 and described in Table 6-10.

Figure 6-8. Number of Pixels in Line (LNH) Register

31–16
Reserved
R-0

15	14–0
Reserved	LNH
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-10. Number of Pixels in Line (LNH) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0. 2560
14-0	LNH	0-7FFFh	Number of pixels in line Sets number of horizontal pixels that will be output to SDRAM = (LNH + 1) '&' 0xFFF0, i.e. the number of horizontal output pixels is truncated to multiples of 16. This bit field is latched by VD.

9FF

6.1.9 Start Line Vertical - Field 0 (SLV0)

The start line vertical - field 0 (SLV0) register is shown in Figure 6-9and described in Table 6-11.

Figure 6-9. Start Line Vertical - Field 0 (SLV0) Register

31 – 16
Reserved
R-0

15	14 – 0
Reserved	SLV0
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-11. Start Line Vertical - Field 0 (SLV0) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	SLV0	0-7FFFh	Start Line, Vertical (Field 0) Sets line at which data output to SDRAM will begin, measured from the start of VD. This bit field is latched by VD.

6.1.10 Start Line Vertical - Field 1(SLV1)

The start line vertical - field 1 (SLV1) register is shown in Figure 6-10 and described in Table 6-12.

Figure 6-10. Start Line Vertical - Field 1 (SLV1) Register

31–16
Reserved
R-0

15	14–0
Reserved	SLV1
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-12. Start Line Vertical - Field 1 (SLV1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	SLV1	0-7FFFh	Start Line, Vertical (Field 1) Sets line at which data output to SDRAM will begin, measured from the start of VD. This bit field is latched by VD.

6.1.11 Number of Lines Vertical (LNV)

The number of lines vertical (LNV) register is shown in Figure 6-11 and described in Table 6-13.

Figure 6-11. Number of Lines Vertical (LNV) Register

31–16
Reserved
R-0

15	14–0
Reserved	LNV
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-13. Number of Lines Vertical (LNV) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	LNV	0-7FFFh	Number of vertical lines. Sets number of vertical lines that will be output to SDRAM. The number of lines output to SDRAM = (LNV + 1). This bit field is latched by VD.

2dF 736

6.1.12 Culling Horizontal (CULH)

The culling horizontal (CULH) register is shown in Figure 6-12 and described in Table 6-14.

Figure 6-12. Culling Horizontal (CULH) Register

31–16	
Reserved	
R-0	
15–8	**7–0**
CLHE	CLHO
R/W-255	R/W-255

LEGEND: R = Read only; -*n* = value after reset

Table 6-14. Culling Horizontal (CULH) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0 0	Any writes to these bit(s) must always have a value of 0.
15-8	CLHE	0-FFh	Horizontal Culling Pattern for Even Line when writing to SDRAM, 8-bit mask: 0: cull, 1:retain LSB is first pixel, MSB is 8th pixel, then pattern repeats. This bit field is latched by VD
7-0	CLHO	0-FFh	Horizontal Culling Pattern for Odd Line when writing to SDRAM, 8-bit mask: 0: cull, 1:retain LSB is first pixel, MSB is 8th pixel, then pattern repeats. This bit field is latched by VD

F7FF

6.1.13 Culling Vertical (CULV)

The culling vertical (CULV) register is shown in Figure 6-13 and described in Table 6-15.

Figure 6-13. Culling Vertical (CULV) Register

31–16
Reserved
R-0

15–8	7–0
Reserved	CULV
R-0	R/W-255

LEGEND: R = Read only; -*n* = value after reset

Table 6-15. Culling Vertical (CULV) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	CULV	0-FFh	Vertical Culling Pattern, 8-bit mask: 0: cull, 1:retain LSB is first line, MSB is 8th line, then pattern repeats. This bit field is latched by VD

FF

6.1.14 Horizontal Size (HSIZE)

The horizontal size (HSIZE) register is shown in Figure 6-14 and described in Table 6-16 .

Figure 6-14. Horizontal Size (HSIZE) Register

31–16
Reserved
R-0

15–13	12	11–0
Reserved	ADCR	HSIZE
R-0	R/W-0	

LEGEND: R = Read only; -*n* = value after reset

Table 6-16. Horizontal Size (HSIZE) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12	ADCR		SDRAM address update. By setting this bit, SDRAM address in a line is automatically decreased so that a line can be Horizontally flipped in the SDRAM.
		0	Address increment
		1	Address decrement
11-0	HSIZE	0-FFFh	Address offset for each line. Sets size of line in SDRAM, units: 32 bytes Either 16 or 32 pixels depending on setting of PACK8. This bit field is latched by VD.

2x50

6.1.15 SDRAM Line Offset (SDOFST)

The SDRAM line offset (SDOFST) register is shown in Figure 6-15 and described in Table 6-17.

Figure 6-15. SDRAM Line Offset (SDOFST) Register

31-16
Reserved
R-0

15	14	13-12	11-9	8-6	5-3	2-0
Reserved	FIINV	FOFST	LOFTS0	LOFTS1	LOFTS2	LOFTS3
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-17. SDRAM Line Offset (SDOFST) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14	FIINV		Field identification signal inverse. This field is latched by VD
		0	Non inverse
		1	Inverse
13-12	FOFST		Field line offset value of odd field (FID = 1). This field is latched by VD
		0	+1 line
		1	+2 line
		2	+3 line
		3	+4 line
11-9	LOFTS0		Line offset values of even line and even field (FID = 0). This field is latched by VD
		0	+1 line
		1	+2 lines
		2	+3 lines
		3	+4 lines
		4	-1 line
		5	-2 lines
		6	-3 lines
		7	-4 lines
8-6	LOFTS1		Line offset values of odd line and even field (FID = 0). This bit is latched by VD.
		0	+1 line
		1	+2 lines
		2	+3 lines
		3	+4 lines
		4	-1 line
		5	-2 lines
		6	-3 lines
		7	-4 lines

Table 6-17. SDRAM Line Offset (SDOFST) Field Descriptions (continued)

Bit	Field	Value	Description
5-3	LOFTS2		Line offset values of even line and odd field (FID = 1). This bit is latched by VD.
		0	+1 line
		1	+2 lines
		2	+3 lines
		3	+4 lines
		4	-1 line
		5	-2 lines
		6	-3 lines
		7	-4 lines
2-0	LOFTS3		Line offset values of odd line and odd field (FID = 1). This bit is latched by VD.
		0	+1 line
		1	+2 lines
		2	+3 lines
		3	+4 lines
		4	-1 line
		5	-2 lines
		6	-3 lines
		7	-4 lines

6.1.16 SDRAM Address - High (CADU)

The SDRAM address-high (CADU-S) register is shown in Figure 6-16and described in Table 6-18.

Figure 6-16. SDRAM Address-High (CADU) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	CADU
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-18. SDRAM Address-High (CADU) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	CADU	0-7FFh	Upper 11 bits of the SDRAM starting address for ISIF output The address is specified offset from the SDRAM base address in units of 32 bytes. This bit field is latched by VD.

6.1.17 SDRAM Address - Low (CADL)

The SDRAM address-low (CADL) register is shown in Figure 6-17 and described in Table 6-19.

Figure 6-17. SDRAM Address-Low (CADL) Register

31-16
Reserved
R-0

15-0
CADL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-19. SDRAM Address-Low (CADL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	CADL	0-FFFFh	Lower 16 bits of the SDRAM starting address for ISIF output The address is specified offset from the SDRAM base address in units of 32 bytes. This bit field is latched by VD.

6.1.18 CCD Color Pattern (CCOLP)

The CCD color pattern (CCOLP) register is shown in Figure 6-18 and described in Table 6-20.

Figure 6-18. CCD Color Pattern (CCOLP) Register

31-16
Reserved
R-0

15-14	13-12	11-10	9-8	7-6	5-4	3-2	1-0
CP17_6	CP15_4	CP13_2	CP11_0	CP07_6	CP05_4	CP03_2	CP01_0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-20. CCD Color Pattern (CCOLP) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-14	CP17_6 01		Color pattern for pixel position 0 (Field 1) Mosaic: Pixel count=0 at EVEN line Stripe: Pixel count=0.
		0	R/Ye
		1	Gr/Cy
		2	Gb/G
		3	B/Mg
13-12	CP15_4 00		Color pattern for pixel position 1 (Field 1) Mosaic: Pixel count=1 at EVEN line Stripe: Pixel count=1.
		0	R/Ye
		1	Gr/Cy
		2	Gb/G
		3	B/Mg
11-10	CP13_2 11		Color pattern for pixel position 2 (Field 1) Mosaic: Pixel count=0 at ODD line Stripe: Pixel count=2.
		0	R/Ye
		1	Gr/Cy
		2	Gb/G
		3	B/Mg
9-8	CP11_0 10		Color pattern for pixel position 3 (Field 1) Mosaic: Pixel count=1 at ODD line Stripe: Not applicable.
		0	R/Ye
		1	Gr/Cy
		2	Gb/G
		3	B/Mg
7-6	CP07_6 01		Color pattern for pixel position 0 (Field 0) Mosaic: Pixel count=0 at EVEN line Stripe: Pixel count=0.
		0	R/Ye
		1	Gr/Cy
		2	Gb/G
		3	B/Mg
5-4	CP05_4 00		Color pattern for pixel position 1 (Field 0) Mosaic: Pixel count=1 at EVEN line Stripe: Pixel count=1.
		0	R/Ye
		1	Gr/Cy
		2	Gb/G
		3	B/Mg
3-2	CP03_2 11		Color pattern for pixel position 2 (Field 0) Mosaic: Pixel count=0 at ODD line Stripe: Pixel count=2.
		0	R/Ye
		1	Gr/Cy
		2	Gb/G
		3	B/Mg

Table 6-20. CCD Color Pattern (CCOLP) Field Descriptions (continued)

Bit	Field	Value	Description
1-0	CP01_0		Color pattern for pixel position 3 (Field 0) Mosaic: Pixel count=1 at ODD line Stripe: Not applicable.
		0	R/Ye
	10	1	Gr/Cy
		2	Gb/G
		3	B/Mg

6.1.19 CCD Gain Adjustment - R/Ye (CRGAIN)

The CCD gain adjustment - R/Ye (CRGAIN) register is shown in Figure 6-19 and described in Table 6-21.

Figure 6-19. CCD Gain Adjustment - R/Ye (CRGAIN) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	CGR
R-0	R/W-512

LEGEND: R = Read only; -*n* = value after reset

Table 6-21. CRGAIN - CCD Gain Adjustment - R/Ye (CRGAIN) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	CGR	0-FFFh	R/Ye gain : Gain adjustment factor for CCD data Value is U12Q9, Range: 0 - 7+511/512. This bit is latched by VD.

6.1.20 CCD Gain Adjustment - Gr/Cy(CGRGAIN)

The CCD gain adjustment - Gr/Cy (CGRGAIN) register is shown in Figure 6-20 and described in Table 6-22.

Figure 6-20. CCD Gain Adjustment - Gr/Cy (CGRGAIN) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	CGGR
R-0	R/W-512

LEGEND: R = Read only; -*n* = value after reset

Table 6-22. CCD Gain Adjustment - Gr/Cy (CGRGAIN) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	CGGR	0-FFFh	Gr/Cy gain :Gain adjustment factor for CCD data Value is U12Q9, Range: 0 - 7+511/512. This bit is latched by VD.

6.1.21 CCD Gain Adjustment - Gb/G (CGBGAIN)

The CCD gain adjustment - Gb/G (CGBGAIN) register is shown in Figure 6-21 and described in Table 6-23.

Figure 6-21. CCD Gain Adjustment - Gb/G (CGBGAIN) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	CGGB
R-0	R/W-512

LEGEND: R = Read only; -*n* = value after reset

Table 6-23. CCD Gain Adjustment - Gb/G (CGBGAIN) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	CGGB	0-FFFh	Gb/G gain :Gain adjustment factor for CCD data Value is U12Q9, Range: 0 - 7+511/512. This bit is latched by VD.

6.1.22 CCD Gain Adjustment - B/Mg (CBGAIN)

The CCD gain adjustment - B/Mg (CBGAIN) register is shown in Figure 6-22 and described in Table 6-24.

Figure 6-22. CCD Gain Adjustment - B/Mg (CBGAIN) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	CGB
R-0	R/W-512

LEGEND: R = Read only; -*n* = value after reset

Table 6-24. CBGAIN - CCD Gain Adjustment - B/Mg (CBGAIN) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	CGB	0-FFFh	B/Mg gain :Gain adjustment factor for CCD data Value is U12Q9, Range: 0 - 7+511/512. This bit is latched by VD.

6.1.23 CCD Offset Adjustment (COFSTA)

The CCD offset adjustment (COFSTA) register is shown in Figure 6-23 and described in Table 6-25.

Figure 6-23. CCD Offset Adjustment (COFSTA) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	COFT
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-25. CCD Offset Adjustment (COFSTA) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	COFT	0-FFFh	Offset adjustment after gain adjustment Value is added to data after gain (0-4,095). This bit is latched by VD.

6.1.24 FlashCFG0 (FLSHCFG0)

The FlashCFG0 (FLSHCFG0) register is shown in Figure 6-24 and described in Table 6-26.

Figure 6-24. FlashCFG0 (FLSHCFG0) Register

31-16
Reserved
R-0

15-1	0
Reserved	FLSHEN
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-26. FlashCFG0 (FLSHCFG0) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	FLSHEN		Flash timing signal enable
		0	Disable
		1	Enable

6.1.25 FlashCFG1 (FLSHCFG1)

The FlashCFG1 (FLSHCFG1) register is shown in Figure 6-25 and described in Table 6-27.

Figure 6-25. FlashCFG1 (FLSHCFG1) Register

31-16
Reserved
R-0

15	14-0
Reserved	SFLSH
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-27. FlashCFG1 (FLSHCFG1) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	SFLSH	0-7FFFh	Start line to set the FLASH timing signal.

6.1.26 FlashCFG2 (FLSHCFG2)

The FlashCFG2 (FLSHCFG2) register is shown in Figure 6-26 and described in Table 6-28.

Figure 6-26. FlashCFG2 (FLSHCFG2) Register

31-16
Reserved
R-0

15-0
VFLSH
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-28. FlashCFG2 (FLSHCFG2) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VFLSH	0-FFFFh	Valid width of the FLASH timing signal.

6.1.27 VD Interrupt #0 (VDINT0)

The VD Interrupt #0 (VDINT0) register is shown in Figure 6-27 and described in Table 6-29.

Figure 6-27. VD Interrupt #0 (VDINT0) Register

31-16
Reserved
R-0

15	14-0
Reserved	CVD0
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-29. VD Interrupt #0 (VDINT0) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	CVD0 2C0	0-7FFFh	VD0 Interrupt Timing in a field (line number) 即 704行产生一个中断

6.1.28 VD Interrupt #1 (VDINT1)

The VD Interrupt #1 (VDINT1) register is shown in Figure 6-28 and described in Table 6-30.

Figure 6-28. VD Interrupt #1 (VDINT1) Register

31-16
Reserved
R-0

15	14-0
Reserved	CVD1
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-30. VD Interrupt #1 (VDINT1) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	CVD1	0-7FFFh	VD1 Interrupt Timing in a field (line number)

6.1.29 VD Interrupt #2 (VDINT2)

The VD Interrupt #2 (VDINT2) register is shown in Figure 6-29 and described in Table 6-31.

Figure 6-29. VD Interrupt #2 (VDINT2) Register

31-16
Reserved
R-0

15	14-0
Reserved	CVD2
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-31. VD Interrupt #2 (VDINT2) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	CVD2	0-7FFFh	VD2 Interrupt Timing in a field (line number)

6.1.30 Gamma Correction Settings (CGAMMAWD)

The gamma correction settings (CGAMMAWD) register is shown in Figure 6-30 and described in Table 6-32.

Figure 6-30. Gamma Correction Settings (CGAMMAWD) Register

31-16
Reserved
R-0

15	14	13	12	11	10	9	8	7-6	5	4-1	0
Reserved	WBEN2	WBEN1	WBEN0	Reserved	OFSTEN2	OFSTEN1	OFSTEN0	Reserved	CFAP	GWDI	CCDTBL
R-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-32. Gamma Correction Settings (CGAMMAWD) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14	WBEN2		White Balance Enable for H3A Input. This bit is latched by VD.
		0	Disable
		1	Enable
13	WBEN1		White Balance Enable for IPIPE Input. This bit is latched by VD.
		0	Disable
		1	Enable
12	WBEN0		White Balance Enable for SDRAM Capture. This bit is latched by VD.
		0	Disable
		1	Enable
11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10	OFSTEN2		Offset control Enable for H3A. This bit is latched by VD.
		0	Disable
		1	Enable
9	OFSTEN1		Offset control Enable for IPIPE. This bit is latched by VD.
		0	Disable
		1	Enable
8	OFSTEN0		Offset control Enable for SDRAM capture. This bit is latched by VD.
		0	Disable
		1	Enable
7-6	Reserved	0	Any writes to these bit(s) must always have a value of 0.
5	CFAP		CFA Pattern. This bit is latched by VD.
		0	Mosaic
		1	Stripe
4-1	GWDI		Select MSB of RAW input data 9-15: Reserved. This bit is latched by VD.
		0	bit 15
		1	bit 14
		2	bit 13
		3	bit 12
		4	bit 11
		5	bit 10
		6	bit 9
		7	bit 8
		8	bit 7

Table 6-32. Gamma Correction Settings (CGAMMAWD) Field Descriptions (continued)

Bit	Field	Value	Description
0	CCDTBL		On/Off control of Gamma (A-LAW) table to ISIF data saved to SDRAM. This bit is latched by VD.
		0	off
		1	on

6.1.31 CCIR 656 Control (REC656IF)

The CCIR 656 control (REC656IF) register is shown in Figure 6-31 and described in Table 6-33.

Figure 6-31. CCIR 656 Control (REC656IF) Register

31 … 2	1	0
Reserved	ECCFVH	R656ON
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-33. CCIR 656 Control (REC656IF) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	ECCFVH		FVH Error Correction Enable
		0	Off
		1	On
0	R656ON		REC656 Interface Enable
		0	Off
		1	On

6.1.32 CCD Configuration (CCDCFG)

The CCD configuration (CCDCFG) register is shown in Figure 6-32 and described in Table 6-34.

Figure 6-32. CCD Configuration(CCDCFG) Register

31-16
Reserved
R-0

15	14	13	12	11	10	9	8	7-6	5	4	3	2	1-0
VDLC	Reserved	MSBINVI	BSWD	Y8POS	EXTRG	TRGSEL	WENLOG	FIDMD	BW656	YCINSWP	Reserved	Reserved	SDRPACK
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-34. CCD Configuration (CCDCFG) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15	VDLC 0		Enable synchronizing function registers on VSYNC
		0	Latched on VSYNC
		1	Not latched on VSYNC
14	Reserved 0	0	Any writes to these bit(s) must always have a value of 0.
13	MSBINVI 0		MSB of Chroma input signal stored to SDRAM inverted
		0	normal
		1	MSB inverted
12	BSWD 0		Byte Swap Data stored to SDRAM
		0	normal
		1	Swap Bytes
11	Y8POS 0		Location of Y signal when YCbCr 8bit data is input
		0	even pixel
		1	odd pixel
10	EXTRG 0		External Trigger
		0	Disable
		1	Enable
9	TRGSEL 0		Signal that initializes SDRAM address when EXTRG = 1
		0	WEN bit (SYNCEN register)
		1	FID input port
8	WENLOG 1		Specifies CCD valid area
		0	Internal valid and WEN signals are ANDed logically
		1	Internal valid and WEN signals are ORed logically
7-6	FIDMD 00		Setting of FID detection function
		0	FID signal is latched at the VSYNC timing
		1	FID signal is not latched
5	BW656 1		The data width in CCIR656 input mode
		0	8-bits
		1	10-bits
4	YCINSWP 1		Y input (YIN[7:0]) and C input (CIN[7:0]) are swapped
		0	YIN[7:0] = Y signal / CIN[7:0] = C signal
		1	YIN[7:0] = C signal / CIN[7:0] = Y signal
3-2	Reserved 00	0	Any writes to these bit(s) must always have a value of 0.

Table 6-34. CCD Configuration (CCDCFG) Field Descriptions (continued)

Bit	Field	Value	Description
1-0	SDRPACK		SDRAM pack
		0	16bits/pixel
		1	12bits/pixel
	10	2	8bits/pixel
		3	Reserved

6.1.33 Defect Correction Control (DFCCTL)

The defect correction control (DFCCTL) register is shown in Figure 6-33 and described in Table 6-35.

Figure 6-33. Defect Correction Control (DFCCTL) Register

31-16
Reserved
R-0

15-11	10-8	7	6-5	4	3-0
Reserved	VDFLSFT	VDFC UDA	VDFCSL	VDFC EN	Reserved
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-35. Defect Correction Control (DFCCTL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-8	VDFLSFT	0-7h	Vertical line Defect level shift value Defect Level (value to be subtracted from the data) is 8bit width, but can be up-shifted up to 4bits by VDFLSFT. Left shift value = VDFLSFT (Range: 0-4) Setting the value greater than 4 to VDFLSFT is not allowed.
7	VDFCUDA		Vertical line Defect Correction upper pixels disable
		0	The whole line is corrected
		1	Pixels upper than the defect are not corrected
6-5	VDFCSL		Vertical line Defect Correction mode select
		0	Defect level subtraction. Just fed through if data are saturating.
		1	Defect level subtraction. Horizontal interpolation ((i-2)+(i+2))/2 if data are saturating.
		2	Horizontal interpolation ((i-2)+(i+2))/2.
		3	Reserved
4	VDFCEN		Vertical line Defect Correction enable. This bit field is latched by VD.
		0	Off
		1	On
3-0	Reserved	0	Any writes to these bit(s) must always have a value of 0.

6.1.34 Defect Correction Vertical Saturation Level (VDFSATLV)

The defect correction - vertical saturation level (VDFSATLV) register is shown in Figure 6-34 and described in Table 6-36.

Figure 6-34. Defect Correction Vertical Saturation Level (VDFSATLV) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VDFSLV
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-36. Defect Correction Vertical Saturation Level (VDFSATLV) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VDFSLV	0-FFFh	Vertical line Defect Correction saturation level. VDFSLV is U12 (Range: 0 - 4,095).

6.1.35 Defect Correction Memory Control (DFCMEMCTL)

The defect correction - memory control (DFCMEMCTL) register is shown in Figure 6-35 and described in Table 6-37.

Figure 6-35. Defect Correction Memory Control (DFCMEMCTL) Register

31-16
Reserved
R-0

15-5	4	3	2	1	0
Reserved	DFCM CLR	Reserv ed	DFCM ARST	DFCM RD	DFCM WR
R-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-37. Defect Correction Memory Control (DFCMEMCTL) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4	DFCMCLR		Memory clear Writing '1' to this bit clears the memory contents to all zero. It will be automatically cleared to '0' when the memory clear is completed.
		0	Memory clear complete
		1	Clear memory
3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	DFCMARST		Memory Address Reset Setting DFCMWR or DFCMRD with LSCMARST set starts memory access to address offset 0. DFCMARST is automatically cleared if data transfer completes. Setting DFCMWR or DFCMRD with LSCMARST cleared starts memory access to the next address.
		0	Increment the memory address
		1	Clear the memory address to offset 0
1	DFCMRD		Memory Read (for debug) Writing '1' to this bit starts reading from the memory. It will be automatically cleared when the data transfer is completed, and the data can be read from DFCMEM4-0.
		0	Memory read complete
		1	Memory read
0	DFCMWR		Memory write Writing '1' to this bit starts writing to the memory. It will be automatically cleared when the data transfer is completed. DFCMEM4-0 should be set prior to the memory access.
		0	Memory write complete
		1	Memory write

6.1.36 Defect Correction Set V Position (DFCMEM0)

The defect correction - set V position 0 (DFCMEM0) register is shown in Figure 6-36 and described in Table 6-38.

Figure 6-36. Defect Correction Set V Position 0 (DFCMEM0) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	DFCMEM0
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-38. Defect Correction Set V Position 0 (DFCMEM0) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	DFCMEM0	0-1FFFh	Memory 0 Set V position of the defects.

6.1.37 Defect Correction Set H Position 1 (DFCMEM1)

The defect correction - set H position (DFCMEM1) register is shown in Figure 6-37 and described in Table 6-39 .

Figure 6-37. Defect Correction Set H Position 1 (DFCMEM1) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	DFCMEM1
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-39. Defect Correction Set H Position 1 (DFCMEM1) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	DFCMEM1	0-1FFFh	Memory 1 Set H position of the defects.

6.1.38 Defect Correction Set SUB1 (DFCMEM2)

The defect correction - set SUB1 (DFCMEM2) register is shown in Figure 6-38 and described in Table 6-40.

Figure 6-38. Defect Correction Set SUB1 (DFCMEM2) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	DFCMEM2
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-40. Defect Correction Set SUB1 (DFCMEM2) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	DFCMEM2	0-FFh	Memory 2 Set SUB1: Defect level of the Vertical line defect position (V = Vdefect). DFCMEM2 can be up shifted according to VDFLSFT, and subtracted from the data for Vertical line defect correction.

6.1.39 Defect Correction Set SUB2 (DFCMEM3)

The defect correction - set SUB2 (DFCMEM3) register is shown in Figure 6-39 and described in Table 6-41.

Figure 6-39. Defect Correction Set SUB2 (DFCMEM3) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	DFCMEM3
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-41. Defect Correction Set SUB2 (DFCMEM3) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	DFCMEM3	0-FFh	Memory 3 Set SUB2: Defect level of the pixels upper than the Vertical line defect (V > Vdefect). DFCMEM3 can be up shifted according to VDFLSFT, and subtracted from the data for Vertical line defect correction.

6.1.40 Defect Correction Set SUB3(DFCMEM4)

The defect correction - set SUB3 (DFCMEM4) register is shown in Figure 6-40 and described in Table 6-42.

Figure 6-40. Defect Correction Set SUB3 (DFCMEM4) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	DFCMEM4
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-42. Defect Correction Set SUB3 (DFCMEM4) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	DFCMEM4	0-FFh	Memory 4 Set SUB3: Defect level of the pixels lower than the Vertical line defect (V > Vdefect). DFCMEM4 can be up shifted according to VDFLSFT, and subtracted from the data for Vertical line defect correction.

6.1.41 Black Clamp Configuration (CLAMPCFG)

The black clamp configuration (CLAMPCFG) register is shown in Figure 6-41 and described in Table 6-43.

Figure 6-41. Black Clamp Configuration (CLAMPCFG) Register

31-16
Reserved
R-0

15-5	4	3	2-1	0
Reserved	CLMD	Reserved	CLHMD	CLEN
R-0	R/W-0	R-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-43. Black Clamp Configuration (CLAMPCFG) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4	CLMD		Black Clamp Mode
		0	Clamp value calculated regardless of the color
		1	Clamp value calculated separately for each 4 color
3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2-1	CLHMD		Horizontal Clamp Mode
		0	
		1	
		2	
		3	
0	CLEN		Black Clamp Enable
		0	Disbale
		1	Enable

6.1.42 DC Offset for Black Clamp (CLDCOFST)

The DC offset for black clamp (CLDCOFST) register is shown in Figure 6-42 and described in Table 6-44.

Figure 6-42. DC Offset for Black Clamp (CLDCOFST) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	CLDC
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-44. DC Offset for Black Clamp (CLDCOFST) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	CLDC	0-1FFFh	DC offset for Black Clamp (S13)

6.1.43 Black Clamp Start Position (CLSV)

The black clamp start position (CLSV) register is shown in Figure 6-43 and described in Table 6-45.

Figure 6-43. Black Clamp Start Position (CLSV) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	CLSV
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-45. Black Clamp Start Position (CLSV) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	CLSV	0-1FFFh	Black Clamp Start position (V)

6.1.44 Horizontal Black Clamp Configuration (CLHWIN0)

The horizontal black clamp configuration 0 (CLHWIN0) register is shown in Figure 6-44 and described in Table 6-46.

Figure 6-44. Horizontal Black Clamp Configuration 0 (CLHWIN0) Register

31-16
Reserved
R-0

15-14	13-12	11-10	9-8	7	6	5	4-0
Reserved	CLHWN	Reserved	CLHWM	Reserved	CLHLMT	CLHWBS	CLHWC
R-0	R/W-0	R-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-46. Horizontal Black Clamp Configuration 0 (CLHWIN0) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-12	CLHWN		Vertical dimension of a window (2^N)
		0	
		1	
		2	
		3	
11-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-8	CLHWM		Horizontal dimension of a window (2^M)
		0	
		1	
		2	
		3	
7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6	CLHLMT		Horizontal Black clamp
		0	
		1	
5	CLHWBS		Base Window select
		0	
		1	
4-0	CLHWC	0-1Fh	Window count per color

6.1.45 Horizontal Black Clamp Configuration 1 (CLHWIN1)

The horizontal black clamp configuration 1 (CLHWIN1) register is shown in Figure 6-45 and described in Table 6-47.

Figure 6-45. Horizontal Black Clamp Configuration 1 (CLHWIN1) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	CLHSH
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-47. Horizontal Black Clamp Configuration 1 (CLHWIN1) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	CLHSH	0-1FFFh	Window Start position (H)

6.1.46 Horizontal Black Clamp Configuration 2 (CLHWIN2)

The horizontal black clamp configuration 2 (CLHWIN2) register is shown in Figure 6-46 and described in Table 6-48.

Figure 6-46. Horizontal Black Clamp Configuration 2 (CLHWIN2) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	CLHSV
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-48. Horizontal Black Clamp Configuration 2 (CLHWIN2) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	CLHSV	0-1FFFh	Window Start position (V)

6.1.47 Vertical Black Clamp Configuration (CLVRV)

The vertical black clamp configuration (CLVRV) register is shown in Figure 6-47 and described in Table 6-49.

Figure 6-47. Vertical Black Clamp Configuration (CLVRV) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	CLVRV
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-49. Vertical Black Clamp Configuration (CLVRV) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	CLVRV	0-FFFh	Reset value (U12) for the Clamp Value register

6.1.48 Vertical Black Clamp Configuration 0 (CLVWIN0)

The vertical black clamp configuration 0 (CLVWIN0) register is shown in Figure 6-48and described in Table 6-50.

Figure 6-48. Vertical Black Clamp Configuration 0 (CLVWIN0) Register

31-16
Reserved
R-0

15-8	7-6	5-4	3	2-0
CLVCOEF	Reserved	CLVRVSL	Reserved	CLVOBH
R/W-0	R-0	R/W-0	R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-50. Vertical Black Clamp Configuration 0 (CLVWIN0) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CLVCOEF	0-FFh	Line average coefficient (k)
7-6	Reserved	0	Any writes to these bit(s) must always have a value of 0.
5-4	CLVRVSL		Reset value for the Clamp value of previous line.
		0	Base value calculated for Horizontal direction
		1	Value set via the configuration register
		2	No update (same as previous image)
		3	Reserved
3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2-0	CLVOBH		Optical Black H valid (2^L)
		0	
		1	

6.1.49 Vertical Black Clamp Configuration 1 (CLVWIN1)

The vertical black clamp configuration 1 (CLVWIN1) register is shown in Figure 6-49 and described in Table 6-51 .

Figure 6-49. Vertical Black Clamp Configuration 1 (CLVWIN1) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	CLVSH
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-51. Vertical Black Clamp Configuration 1 (CLVWIN1) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	CLVSH	0-1FFFh	Optical Black Start position (H).

6.1.50 Vertical Black Clamp configuration 2 (CLVWIN2)

The vertical black clamp configuration 2 (CLVWIN2) register is shown in Figure 6-50 and described in Table 6-52.

Figure 6-50. Vertical Black Clamp Configuration 2 (CLVWIN2) Register

31-16
Reserved
R-0

L

15-13	12-0
Reserved	CLVSV
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-52. Vertical Black Clamp Configuration 2 (CLVWIN2) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	CLVSV	0-1FFFh	Optical Black Start position (V).

6.1.51 Vertical Black Clamp Configuration 3 (CLVWIN3)

The vertical black clamp configuration 3 (CLVWIN3) register is shown in Figure 6-51 and described in Table 6-53.

Figure 6-51. Vertical Black Clamp Configuration 3 (CLVWIN3) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	CLVOBV
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-53. Vertical Black Clamp Configuration 3 (CLVWIN3) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	CLVOBV	0-1FFFh	Optical Black V valid.

6.1.52 CCD Formatter Start Pixel Horiz (FMTSPH)

The CCD formatter - start pixel horiz (FMTSPH) register is shown in Figure 6-52 and described in Table 6-54.

Figure 6-52. CCD Formatter Start Pixel Horiz (FMTSPH) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	FMTSPH
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-54. CCD Formatter Start Pixel Horiz (FMTSPH) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	FMTSPH	0-1FFFh	The first pixel in a line fed into the formatter

6.1.53 CCD Formatter Number of Pixels (FMTLNH)

The CCD formatter - number of pixels (FMTLNH) register is shown in Figure 6-53 and described in Table 6-55.

Figure 6-53. CCD Formatter Number of Pixels (FMTLNH) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	FMTLNH
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-55. CCD Formatter Number of Pixels (FMTLNH) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	FMTLNH	0-1FFFh	Number of pixels in a line fed to the formatter. Number of pixels = FMTLNH + 1

6.1.54 CCD Formatter Start Line Vertical (FMTSLV)

The CCD formatter - start line vertical (FMTSLV) register is shown in Figure 6-54and described in Table 6-56.

Figure 6-54. CCD Formatter Start Line Vertical (FMTSLV) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	FMTSLV
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-56. CCD Formatter Start Line Vertical (FMTSLV) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	FMTSLV	0-1FFFh	Start line vertical

6.1.55 CCD Formatter Number of Lines (FMTLNV)

The CCD formatter - number of lines (FMTLNV) register is shown in Figure 6-55 and described in Table 6-57.

Figure 6-55. CCD Formatter Number of Lines (FMTLNV) Register

31-16
Reserved
R-0

15	14-0
Reserved	FMTLNV
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-57. CCD Formatter Number of Lines (FMTLNV) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	FMTLNV	0-7FFFh	Number of lines in vertical Number of lines = FMTLNV + 1

6.1.56 CCD Formatter Read Out Line length (FMTRLEN)

The CCD formatter - read out line length (FMTRLEN) register is shown in Figure 6-56 and described in Table 6-58.

Figure 6-56. CCD Formatter Read Out Line Length (FMTRLEN) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	FMTRLEN
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-58. CCD Formatter Read Out Line Length (FMTRLEN) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	FMTRLEN	0-1FFFh	Number of pixels in an output line Maximum value = 4480

6.1.57 CCD Formatter HD Cycles (FMTHCNT)

The CCD formatter - HD cycles (FMTHCNT) register is shown in Figure 6-57 and descried in Table 6-59.

Figure 6-57. CCD Formatter HD Cycles (FMTHCNT) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	FMTHCNT
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-59. CCD Formatter HD Cycles (FMTHCNT) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	FMTHCNT	0-1FFFh	HD interval for output lines Set all '0' to this register if combining multiple lines into a single line.

6.1.58 Color Space Converter Enable (CSCCTL)

The color space converter enable (CSCCTL) register is shown in Figure 6-58and described in Table 6-60.

Figure 6-58. Color Space Converter Enable (CSCCTL) Register

31-16
Reserved
R-0

15-1	0
Reserved	CSCEN
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-60. Color Space Converter Enable (CSCCTL) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	CSCEN		Controls ON/OFF of Color Space Converter
		0	Disable
		1	Enable

6.1.59 Color Space Converter Coefficients #0 (CSCM0)

The color space converter - coefficients #0 (CSCM0) register is shown in Figure 6-59 and described in Table 6-61.

Figure 6-59. Color Space Converter Coefficients #0 (CSCM0) Register

31-16
Reserved
R-0

15-8	7-0
CSCM01	CSCM00
R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-61. Color Space Converter Coefficients #0 (CSCM0) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CSCM01	0-FFh	Color space conversion coefficient value M01 This value is S8Q5
7-0	CSCM00	0-FFh	Color space conversion coefficient value M00 This value is S8Q5

6.1.60 Color Space Converter Coefficients #1 (CSCM1)

The color space converter - coefficients #1 (CSCM1) register is shown in Figure 6-60 and described in Table 6-62.

Figure 6-60. Color Space Converter Coefficients #1 (CSCM1) Register

31-16
Reserved
R-0

15-8	7-0
CSCM03	CSCM02
R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-62. Color Space Converter Coefficients #1 (CSCM1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CSCM03	0-FFh	Color space conversion coefficient value M03 This value is S8Q5
7-0	CSCM02	0-FFh	Color space conversion coefficient value M02 This value is S8Q5

6.1.61 Color Space Converter Coefficients #2 (CSCM2)

The color space converter - coefficients #2 (CSCM2) register is shown in Figure 6-61 and described in Figure 6-61.

Figure 6-61. Color Space Converter Coefficients #2 (CSCM2) Register

31-16
Reserved
R-0

15-8	7-0
CSCM11	CSCM10
R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-63. Color Space Converter Coefficients #2 (CSCM2) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CSCM11	0-FFh	Color space conversion coefficient value M11 This value is S8Q5
7-0	CSCM10	0-FFh	Color space conversion coefficient value M10 This value is S8Q5

6.1.62 Color Space Converter Coefficients #3 (CSCM3)

The color space converter - coefficients #3 (CSCM3) register is shown in Figure 6-62 and described in Table 6-64.

Figure 6-62. Color Space Converter Coefficients #3 (CSCM3)

31-16
Reserved
R-0

15-8	7-0
CSCM13	CSCM12
R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-64. Color Space Converter Coefficients #3 (CSCM3) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CSCM13	0-FFh	Color space conversion coefficient value M13 This value is S8Q5
7-0	CSCM12	0-FFh	Color space conversion coefficient value M12 This value is S8Q5

6.1.63 Color Space Converter Coefficients #4 (CSCM4)

The color space converter - coefficients #4 (CSCM4) register is shown in Figure 6-63 and described in Table 6-65.

Figure 6-63. CSCM4 - Color Space Converter Coefficients #4 (CSCM4)

31-16
Reserved
R-0

15-8	7-0
CSCM21	CSCM20
R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-65. Color Space Converter Coefficients #4 (CSCM4) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CSCM21	0-FFh	Color space conversion coefficient value M21 This value is S8Q5
7-0	CSCM20	0-FFh	Color space conversion coefficient value M20 This value is S8Q5

6.1.64 Color Space Converter Coefficients #5 (CSCM5)

The color space converter - coefficients #5 (CSCM5) register is shown in Figure 6-64 and described in Table 6-66.

Figure 6-64. Color Space Converter Coefficients #5 (CSCM5)

31-16	
Reserved	
R-0	
15-8	7-0
CSCM23	CSCM22
R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-66. Color Space Converter Coefficients #5 (CSCM5) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CSCM23	0-FFh	Color space conversion coefficient value M23 This value is S8Q5
7-0	CSCM22	0-FFh	Color space conversion coefficient value M22 This value is S8Q5

6.1.65 Color Space Converter Coefficients #6 (CSCM6)

The color space converter - coefficients #6 register (CSCM6)is shown in Figure 6-65 and described in Table 6-67.

Figure 6-65. Color Space Converter Coefficients #6 (CSCM6)

31-16
Reserved
R-0

15-8	7-0
CSCM31	CSCM30
R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-67. Color Space Converter Coefficients #6 (CSCM6) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CSCM31	0-FFh	Color space conversion coefficient value M31 This value is S8Q5
7-0	CSCM30	0-FFh	Color space conversion coefficient value M30 This value is S8Q5

6.1.66 Color Space Converter Coefficients #7 (CSCM7)

The color space converter - coefficients #7 (CSCM7) register is shown in Figure 6-66 and described in Table 6-68.

Figure 6-66. Color Space Converter Coefficients #7 (CSCM7)

31-16
Reserved
R-0

15-8	7-0
CSCM33	CSCM32
R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-68. Color Space Converter Coefficients #7 (CSCM7) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CSCM33	0-FFh	Color space conversion coefficient value M33 This value is S8Q5
7-0	CSCM32	0-FFh	Color space conversion coefficient value M32 This value is S8Q5

6.2 Image Pipe Input Interface Registers (IPIPEIF) Registers

The Image Pipe Input Interface registers are shown in Table 6-69.

Table 6-69. Image Pipe Input Interface Register Map (IPIPEIF)

Offset	Acronym	Register Description	Section
0h	ENABLE 1	IPIPE I/F Enable	Section 6.2.1
04h	CFG1 40d	IPIPE I/F Configuration 1	Section 6.2.2
08h	PPLN 510	IPIPE I/F Interval of HD / Start pixel in HD	Section 6.2.3
0Ch	LPFR 2f0	IPIPE I/F Interval of VD / Start line in VD	Section 6.2.4
10h	HNUM 500	IPIPE I/F Number of valid pixels per line	Section 6.2.5
14h	VNUM 2e0	IPIPE I/F Number of valid lines per frame	Section 6.2.6
18h	ADDRU 418	IPIPE I/F Memory address (upper)	Section 6.2.7
1Ch	ADDRL b80	IPIPE I/F Memory address (lower)	Section 6.2.8
20h	ADOFS 50	IPIPE I/F Address offset of each line	Section 6.2.9
24h	RSZ 10	IPIPE I/F Horizontal resizing parameter	Section 6.2.10
28h	GAIN 200	IPIPE I/F Gain parameter	Section 6.2.11
2Ch	DPCM 06	IPIPE I/F DPCM configuration	Section 6.2.12
30h	CFG2	IPIPE I/F Configuration 2	Section 6.2.13
34h	INIRSZ	IPIPE I/F Initial position of resize	Section 6.2.14
38h	OCLIP fff	IPIPE I/F Output clipping value	Section 6.2.15
3Ch	DTUDF	IPIPE I/F Data underflow error status	Section 6.2.16
40h	CLKDIV 931	IPIPE I/F Clock rate configuration	Section 6.2.17
44h	DPC1	IPIPE I/F Defect pixel correction	Section 6.2.18
48h	DPC2	IPIPE I/F Defect pixel correction	Section 6.2.19
54h	RSZ3A 10	IPIPE I/F Horizontal resizing parameter for H3A	Section 6.2.20
58h	INIRSZ3A	IPIPE I/F Initial position of resize for H3A	Section 6.2.21

6.2.1 IPIPE I/F Enable (ENABLE)

The IPIPE I/F Enable (ENABLE) register is shown in Figure 6-67 and described in Table 6-70.

Figure 6-67. IPIPE I/F Enable (ENABLE) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	SYNC OFF	ENAB LE
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-70. IPIPE I/F Enable (ENABLE) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	SYNCOFF		SYNC out mask This register masks the VSUNC output to other module.
		0	VSYNC output enable
		1	VSYNC output disable
0	ENABLE		IPIPE I/F Enable This register is used to start the operation of SDRAM buffer memory read and generates SYNC signals. This register is available when INPSRC (CFG[3:2]) = 1, 2 or 3.
		0	Disable
		1	Enable

6.2.2 IPIPE I/F Configuration 1 (CFG1)

The IPIPE I/F Configuration 1 (CFG1) register is shown in Figure 6-68 and described in Table 6-71.

Figure 6-68. IPIPE I/F Configuration 1 (CFG1) Register

31-16
Reserved
R-0

15-14	13-11	10	9-8	7	6-4	3-2	1	0
INPSRC1	DATASFT	CLKSEL	UNPACK	AVGFILT	Reserved	INPSRC2	DECM	ONESHOT
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-00	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-71. IPIPE I/F Configuration 1 (CFG1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-14	INPSRC1		Parallel Port/YCbCr Data Port Selection
		0	from Parallel Port/
		1	from SDRAM (raw data)
		2	from Parallel Port & SDRAM (Darkframe)
		3	from SDRAM (YUV data)
13-11	DATASFT		SDRAM Read Data Shift (0-7) This register is available when INPSRCx = 1 or 2.
		0	Output data (13:0) = read data(13:0)
		1	Output data (13:0) = read data(12:0) & "0"
		2	Output data (13:0) = read data(11:0) & "00"
		3	Output data (13:0) = read data(10:0) & "000"
		4	Output data (13:0) = read data(9:0) & "0000"
	100	5	Output data (13:0) = read data(8:0) & "00000"
		6	Output data (13:0) = read data(7:0) & "000000"
		7	Output data (13:0) = read data(15:2)
10	CLKSEL		IPIPEIF & IPIPE Clock Select This register is available when INPSRCx = 1 or 3. Should code "0" when INPSRCx = 0 or 2.
	0	0	pixel clock (PCLK)
		1	divided SDRAM clock as per CLKDIV
9-8	UNPACK		8/12-Bit Packed Mode When CCD raw data is stored in 8-bit packed mode or 12-bit packed mode, this register should code "1" or "3". This register is effective when INPSRCx = 1 or 2.
	00	0	16 bits / pixel
		1	8 bits / pixel
		2	8 bits / pixel+inverse Alaw(8-10)
		3	12 bits / pixel
7	AVGFILT		Averaging Filter It applies (1,2,1) filter for the RGB/YCbCr data.
	0	0	off
		1	on
6-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3-2	INPSRC2 11		ISIF/YCbCr Data Port Selection
		0	from ISIF
		1	from SDRAM (raw data)
		2	from ISIF & SDRAM (Darkframe)
		3	from SDRAM (YUV data)

Table 6-71. IPIPE I/F Configuration 1 (CFG1) Field Descriptions (continued)

Bit	Field	Value	Description
1	DECIM		Pixel Decimation rate defined by RSZ register
	0	0	no decimation 是否抽取像素
		1	decimate
0	ONESHOT		One Shot Mode This register is available when INPSRCx = 1 or 3.
		0	continuous mode
	1	1	one shot mode

6.2.3 IPIPE I/F Interval of HD / Start Pixel in HD (PPLN)

The IPIPE I/F Interval of HD / Start pixel in HD register is shown in Figure 6-69 and described in Table 6-72.

Figure 6-69. IPIPE I/F Interval of HD / Start pixel in HD (PPLN)

31-16
Reserved
R-0

15-13	12-0
Reserved	PPLN
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-72. IPIPE I/F Interval of HD / Start pixel in HD (PPLN) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	PPLN	0-1FFFh	Case-1: Interval of Horizontal Sync (HD) Specifies the interval of horizontal sync. This register is available when INPSRCx = 1 or 3. Case-2: Start Pixel in Horizontal Sync (HD) Specifies the start pixel in horizontal sync. This register is available when INPSRCx = 2

6.2.4 IPIPE I/F Interval of VD / Start Line in VD (LPFR)

The IPIPE I/F Interval of VD / Start line in VD register is shown in Figure 6-70 and described in Table 6-73.

Figure 6-70. IPIPE I/F Interval of VD / Start line in VD (LPFR) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	LPFR
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-73. IPIPE I/F Interval of VD / Start line in VD (LPFR) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	LPFR	0-1FFFh	Case-1: Interval of Vertical Sync (VD) Specifies the interval of vertical sync. This register is available when INPSRCx = 1 or 3. Case-2: Start Pixel in Vertical Sync (VD) Specifies the start line in vertical sync. This register is available when INPSRCx = 2

6.2.5 IPIPE I/F Number of Valid Pixels per Line (HNUM)

The IPIPE I/F (HNUM) register is shown in Figure 6-71 and described in Table 6-74.

Figure 6-71. IPIPE I/F Number of Valid Pixels per Line (HNUM)

31-16
Reserved
R-0

15-13	12-0
Reserved	HNUM
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-74. IPIPE I/F Number of Valid Pixels per Line (HNUM) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	HNUM 500	0-1FFFh	The Number of Valid Pixel in a Line Specifies the number of valid pixel in a horizontal line. This register is available when INPSRCx = 1, 2 or 3 即水平线上每行有效像素为1280个

6.2.6 IPIPE I/F Number of Valid Lines per Frame (VNUM)

The IPIPE I/F (VNUM) register is shown in Figure 6-72 and described in Table 6-75.

Figure 6-72. IPIPE I/F Number of valid Lines per Frame (VNUM) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VNUM
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-75. IPIPE I/F Number of Valid Lines per Frame (VNUM) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VNUM 2E0	0-1FFFh	The Number of Valid Line in a Vertical Specifies the number of valid line in a vertical. This register is available when INPSRCx = 1, 2 or 3

即垂直方向上像素点为736

6.2.7 IPIPE I/F Memory Address (Upper)(ADDRU)

The PIPE I/F memory address (Upper)(ADDRU) register is shown in Figure 6-73 and described in Table 6-76.

Figure 6-73. IPIPE I/F Memory Address (Upper)(ADDRU) Register

31-16
Reserved
R-0

15-11	10	9	8-0
Reserved	ADDR MSB	ADOF S9	ADDRMSB
R-00	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-76. IPIPE I/F Memory Address (Upper)(ADDRU) Field Descriptions

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Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10	ADDRMSB 0		Memory Address – MSB This register is available when INPSRCx = 1, 2 or 3.
9	ADOFS9 0		The Address Offset of each line - MSB bit This register is available when INPSRCx = 1, 2 or 3.
8-0	ADDRMSB 18	0-1FFh	Memory Address – Upper This register is available when INPSRCx = 1, 2 or 3.

6.2.8 IPIPE I/F Memory Address (Lower)(ADDRL)

The IPIPE I/F memory address (Lower)(ADDRL) register is shown in Figure 6-74 and described in Table 6-77.

Figure 6-74. IPIPE I/F Memory Address (Lower)(ADDRL) Register

31-16
Reserved
R-0

15-0
ADDRL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-77. IPIPE I/F Memory Address (Lower)(ADDRL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	ADDRL	0-FFFFh	Memory Address – Lower Memory address lower 16-bits are specified in units of 32-bytes. This register is available when INPSRCx = 1, 2 or 3.

6.2.9 IPIPE I/F Address Offset of Each Line (ADOFS)

The IPIPE I/F address offset of each line (ADOFS) register is shown in Figure 6-75 and described in Table 6-78.

Figure 6-75. IPIPE I/F Address Offset of Each Line (ADOFS) Register

31-16
Reserved
R-0

15-9	8-0
Reserved	ADOFS
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-78. IPIPE I/F Address offset of Each Line (ADOFS) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Any writes to these bit(s) must always have a value of 0.
8-0	ADOFS	0-1FFh	The Address Offset of each line Specifies the offset address each start line is specified in units of 32-bytes. This register is available when INPSRCx = 1, 2 or 3.

6.2.10 IPIPE I/F Horizontal Resizing Parameter (RSZ)

The IPIPE I/F horizontal resizing parameter (RSZ) register is shown in Figure 6-76 and described in Table 6-79.

Figure 6-76. IPIPE I/F Horizontal Resizing Parameter (RSZ) Register

31-16
Reserved
R-0

15-7	6-0
Reserved	RSZ
R-00	R/W-16

LEGEND: R = Read only; -*n* = value after reset

Table 6-79. IPIPE I/F Horizontal Resizing Parameter (RSZ) Field Descriptions

Bit	Field	Value	Description
31-7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6-0	RSZ	0-7Fh	The Horizontal Resizing Parameter. Specifies the horizontal resizing parameter. The RSZ register can be configured within 16 to 112 range. This resizing ratio is determined by 16/RSZ (= 1/1 to 1/7)

6.2.11 IPIPE I/F Gain Parameter (GAIN)

The IPIPE I/F gain parameter (GAIN) register is shown in Figure 6-77 and described in Table 6-80.

Figure 6-77. IPIPE I/F Gain Parameter (GAIN) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	GAIN
R-00	R/W-512

LEGEND: R = Read only; -*n* = value after reset

Table 6-80. IPIPE I/F Gain Parameter (GAIN) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	GAIN	0-3FFh	Gain Parameter. Specifies the gain parameter for IPIPE output data. The GAIN register can be configured within 0.00195(1/512) to 1.99805(1023/512) range. This gain default value is x1 gain. These bits don't influence Data of YCC.

6.2.12 IPIPE I/F DPCM Configuration (DPCM)

The IPIPE I/F DPCM configuration (DPCM) register is shown in Figure 6-78and described in Table 6-81.

Figure 6-78. IPIPE I/F DPCM Configuration (DPCM) Register

31-16
Reserved
R-0

15-3	2	1	0
Reserved	BITS	PRED	ENA
R-00	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-81. IPIPE I/F DPCM Configuration (DPCM) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	BITS 1	 0	DPCM Decompression Mode 0: 8bit to 10bit DPCM 1: 8bit to 12bit DPCM No decompression
1	PRED 1	 1	DPCM Prediction Mode 0: Simple Predictor 1: Advanced Predictor DPCM decompress predict mode 1 (simple predictor)
0	ENA 0	 2	DPCM Decompression enable 0: DPCM off(no decompress) 1: DPCM on DPCM decompress predict mode 2 (advanced predictor)

6.2.13 IPIPE I/F Configuration 2 (CFG2)

The IPIPE I/F configuration 2 (CFG2) register is shown in Figure 6-79 and described in Table 6-82.

Figure 6-79. IPIPE I/F Configuration 2 (CFG2) Register

31-16
Reserved
R-0

15-8	7	6	5	4	3	2	1	0
Reserved	YUV8P	YUV8	DFSDIR	WENE	YUV16	VDPOL	HDPOL	INTSRC
R-00	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-82. IPIPE I/F Configuration 2 (CFG2) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7	YUV8P		Y/C phase When YUV8 is selected, YUV8P specifies the Croma phase(odd or even pixel).
6	YUV8		YUV 8bit mode When INPTYP is 1YUV16bit mode and YUV8 is 1, it converts 8bit data to 16bit data and drives to IPIPE.
		0	YUV 16bit mode
		1	YUV 8bit mode
5	DFSDIR		DFS direction of subtraction
		0	
		1	
4	WENE		External WEN Selection When set to 1 and when ENABLE is set to 1, the external WEN signal is used to recognize the valid pixel for resize filter calculation.
		0	do not use external WEN (Write Enable)
		1	use external WEN (Write Enable)
3	YUV16		Input Type This register is available when CFG1.INPSRC2 = 0. Should code "0" otherwise.
		0	RAW sensor data
		1	YUV 16-bit data
2	VDPOL		VD Sync Polarity When input VD is active low SYNC pulse, should set to '1'
		0	positive
		1	negative
1	HDPOL		HD Sync Polarity When input HD is active low SYNC pulse, should set to '1'
		0	positive
		1	negative
0	INTSRC		IPIPE I/F Interrupt Source Select
		0	start position of VD from parallel port
		1	start position of VD from ISIF

6.2.14 IPIPE I/F Initial Position of Resize (INIRSZ)

The IPIPE I/F initial position of resize (INIRSZ) register is shown in Figure 6-80 and described in Table 6-83.

Figure 6-80. IPIPE I/F Initial Position of Resize (INIRSZ) Register

31-16
Reserved
R-0

15-14	13	12-0
Reserved	ALNS YNC	INIRSZ
R-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-83. IPIPE I/F Initial Position of Resize (INIRSZ) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13	ALNSYNC		Force the HD and VD align with start position. writing 1 align the HD/VD position to initial data position which is specified by INIRSZ
12-0	INIRSZ	0-1FFFh	Initial Position of Resizer Specifies the initial position from HD for resize

6.2.15 IPIPE I/F Output Clipping Value (OCLIP)

The IPIPE I/F output clipping value (OCLIP) register is shown in Figure 6-81 and described in Table 6-84 .

Figure 6-81. IPIPE I/F Output Clipping Value (OCLIP) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	OCLIP
R-00	R/W-4095

LEGEND: R = Read only; -*n* = value after reset

Table 6-84. IPIPE I/F Output Clipping Value (OCLIP) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	OCLIP	0-FFFh	Output Clipping Value after gain Control

6.2.16 IPIPE I/F Data Underflow Error Status (DTUDF)

The IPIPE I/F data underflow error status (DTUDF) register is shown in Figure 6-82 and described in Table 6-85.

Figure 6-82. IPIPE I/F Data Underflow Error Status (DTUDF) Register

31-16
Reserved
R-0

15-1	0
Reserved	DTUDF
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-85. IPIPE I/F Data Underflow Error Status (DTUDF) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	DTUDF		Data Underflow Error Status Reading '1' shows there is data under flow and at least one data is corrupted while reading from SDRAM. Writing '1' to this register clears (=0) the error (=1) status. Programmers need to configure proper read clock frequency or SDRAM priority to avoid the data underflow.

6.2.17 IPIPE I/F Clock Rate Configuration (CLKDIV)

The IPIPE I/F clock rate configuration (CLKDIV) register is shown in Figure 6-83 and described in Table 6-86.

Figure 6-83. IPIPE I/F Clock Rate Configuration (CLKDIV) Register

31-16
Reserved
R-0

15-0
CLKDIV
R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 6-86. IPIPE I/F Clock Rate Configuration(CLKDIV) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	CLKDIV	0-FFFFh	Clock rate configuration clock rate = M/N x VPSS clock rate M=CLKDIV[15:8]+1,N=CLKDIV[7:0]+1 M/N should not be greater than 1/2. This configuration is effective only when CONFIG1.CLKSEL=1

6.2.18 IPIPE I/F Defect Pixel Correction (DPC1)

The IPIPE I/F defect pixel correction (DPC1) register is shown in Figure 6-84 and described in Table 6-87.

Figure 6-84. IPIPE I/F Defect Pixel Correction (DPC1) Register

31-16
Reserved
R-0

15-13	12	11-0
Reserved	ENA	TH
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-87. IPIPE I/F Defect Pixel Correction (DPC1) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12	ENA		DPC enable applies DPC for VPIF,ISIF input path 0: off 1: on
11-0	TH	0-FFFh	DPC threshold value

6.2.19 PIPE I/F Defect Pixel Correction (DPC2)

The IPIPE I/F defect pixel correction (DPC2) register is shown inFigure 6-85 and described in Table 6-88.

Figure 6-85. IPIPE I/F Defect Pixel Correction (DPC2) Register

31-16
Reserved
R-0

15-13	12	11-0
Reserved	ENA	TH
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-88. IPIPE I/F Defect Pixel Correction (DPC2) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12	ENA		DPC enable applies DPC for SDRAM input path 0: off 1: on
11-0	TH	0-FFFh	DPC threshold value

6.2.20 IPIPE I/F Horizontal Resizing Parameter for H3A (RSZ3A)

The IPIPE I/F horizontal resizing parameter for H3A (RSZ3A) register is shown in Figure 6-86 and described in Table 6-89.

Figure 6-86. IPIPE I/F Horizontal Resizing Parameter for H3A (RSZ3A)

31-16
Reserved
R-0

15-10	9	8	7	6-0
Reserved	DECIM	AVGFILT	Reserved	RSZ
R-00	R/W-0	R/W-0	R-00	R/W-16

LEGEND: R = Read only; -*n* = value after reset

Table 6-89. IPIPE I/F Horizontal Resizing Parameter for H3A (RSZ3A) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9	DECIM		Pixel Decimation rate defined by RSZ register.
		0	no decimation
		1	decimate
8	AVGFILT		Averaging Filter It applies (1,2,1) filter for the RGB/YCbCr data.
		0	off
		1	on
7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6-0	RSZ	0-7Fh	The Horizontal Resizing Parameter Specifies the horizontal resizing parameter. The RSZ register can be configured within 16 to 112 range. This resizing ratio is determined by 16/RSZ (= 1/1 to 1/7)

6.2.21 PIPE I/F Initial Position of Resize for H3A (INIRSZ3A)

The IPIPE I/F initial position of resize for H3A (INIRSZ3A) register is shown in Figure 6-87 and described in Table 6-90.

Figure 6-87. IPIPE I/F Initial Position of Resize for H3A (INIRSZ3A)

31-16
Reserved
R-0

15-14	13	12-0
Reserved	ALSYNC	INIRSZ
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-90. IPIPE I/F Initial Position of Resize for H3A (INIRSZ3A) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13	ALSYNC		Force the HD and VD align with start position. writing 1 align the HD/VD position to initial data position which is specified by INIRSZ3A
12-0	INIRSZ	0-1FFFh	Initial Position of Resizer Specifies the initial position from HD for resize

6.3 Image Pipe (IPIPE) Registers

Table 6-91 lists the memory-mapped registers for the image pipe (IPIPE). See the device-specific data manual for the memory addresses of these registers.

Table 6-91. IPIPE Registers

Offset	Acronym	Register Description	Section
0h	SRC_EN	IPIPE Enable	Section 6.3.1
004h	SRC_MODE	One Shot Mode	Section 6.3.2
008h	SRC_FMT	Input/Output Data Paths	Section 6.3.3
00Ch	SRC_COL b1	Color Pattern	Section 6.3.4
010h	SRC_VPS	Vertical Start Position	Section 6.3.5
014h	SRC_VSZ 2df	Vertical Processing Size	Section 6.3.6
018h	SRC_HPS	Horizontal Start Position	Section 6.3.7
01Ch	SRC_HSZ 4ff	Horizontal Processing Size	Section 6.3.8
024h	DMA_STA	Status Flags (Reserved)	Section 6.3.9
028h	GCK_MMR 1	MMR Gated Clock Control	Section 6.3.10
02Ch	GCK_PIX f	PCLK Gated Clock Control	Section 6.3.11
030h	Reserved	Reserved	
034h	DPC_LUT_EN	LUTDPC (=LUT Defect Pixel Correction): Enable	Section 6.3.12
038h	DPC_LUT_SEL	LUTDPC: Processing Mode Selection	Section 6.3.13
03Ch	DPC_LUT_ADR	LUTDPC: Start Address in LUT	Section 6.3.14
040h	DPC_LUT_SIZ 3ff	LUTDPC: Number of available entries in LUT	Section 6.3.15
1D0h	WB2_OFT_R	WB2 (=White Balance): Offset	Section 6.3.16
1D4h	WB2_OFT_GR	WB2: Offset	Section 6.3.17
1D8h	WB2_OFT_GB	WB2: Offset	Section 6.3.18
1DCh	WB2_OFT_B 4	WB2: Offset	Section 6.3.19
1E0h	WB2_WGN_R a	WB2: Gain	Section 6.3.20
1E4h	WB2_WGN_GR 13	WB2: Gain	Section 6.3.21
1E8h	WB2_WGN_GB 1c	WB2: Gain	Section 6.3.22
1ECh	WB2_WGN_B 25	WB2: Gain	Section 6.3.23
22Ch	RGB1_MUL_RR 100	RGB1 (=1st RGB2RGB conv): Matrix Coefficient	Section 6.3.24
230h	RGB1_MUL_GR	RGB1: Matrix Coefficient	Section 6.3.25
234h	RGB1_MUL_BR	RGB1: Matrix Coefficient	Section 6.3.26
238h	RGB1_MUL_RG	RGB1: Matrix Coefficient	Section 6.3.27
23Ch	RGB1_MUL_GG 100	RGB1: Matrix Coefficient	Section 6.3.28
240h	RGB1_MUL_BG	RGB1: Matrix Coefficient	Section 6.3.29
244h	RGB1_MUL_RB	RGB1: Matrix Coefficient	Section 6.3.30
248h	RGB1_MUL_GB	RGB1: Matrix Coefficient	Section 6.3.31
24Ch	RGB1_MUL_BB 100	RGB1: Matrix Coefficient	Section 6.3.32
250h	RGB1_OFT_OR	RGB1: Offset	Section 6.3.33
254h	RGB1_OFT_OG	RGB1: Offset	Section 6.3.34
258h	RGB1_OFT_OB	RGB1: Offset	Section 6.3.35
25Ch	GMM_CFG 60	Gamma Correction Configuration	Section 6.3.36
294h	YUV_ADJ 10	YUV (RGB2YCbCr conv): Luminance Adjustment (Contrast and Brightness)	Section 6.3.37
298h	YUV_MUL_RY 4d	YUV: Matrix Coefficient	Section 6.3.38
29Ch	YUV_MUL_GY 96	YUV: Matrix Coefficient	Section 6.3.39
2A0h	YUV_MUL_BY 1d	YUV: Matrix Coefficient	Section 6.3.40
2A4h	YUV_MUL_RCB fd5	YUV: Matrix Coefficient	Section 6.3.41
2A8h	YUV_MUL_GCB fab	YUV: Matrix Coefficient	Section 6.3.42

048h:1
044h:1

Table 6-91. IPIPE Registers (continued)

Offset	Acronym	Register Description	Section
2ACh	YUV_MUL_BCB 80	YUV: Matrix Coefficient	Section 6.3.43
2B0h	YUV_MUL_RCR 80	YUV: Matrix Coefficient	Section 6.3.44
2B4h	YUV_MUL_GCR f95	YUV: Matrix Coefficient	Section 6.3.45
2B8h	YUV_MUL_BCR feb	YUV: Matrix Coefficient	Section 6.3.46
2BCh	YUV_OFT_Y	YUV: Offset	Section 6.3.47
2C0h	YUV_OFT_CB 80	YUV: Offset	Section 6.3.48
2C4h	YUV_OFT_CR 80	YUV: Offset	Section 6.3.49
2C8h	YUV_PHS 0	Chrominance Position (for 422 Down Sampler)	Section 6.3.50
2D4h	YEE_EN 0	YEE (=Edge Enhancer): Enable	Section 6.3.51
2D8h	YEE_TYP	YEE: Method Selection	Section 6.3.52
7DCh	YEE_SHF	YEE: HPF Shift Length	Section 6.3.53
2E0h	YEE_MUL_00	YEE: HPF Coefficient	Section 6.3.54
2E4h	YEE_MUL_01	YEE: HPF Coefficient	Section 6.3.55
2E8h	YEE_MUL_02	YEE: HPF Coefficient	Section 6.3.56
2ECh	YEE_MUL_10	YEE: HPF Coefficient	Section 6.3.57
2F0h	YEE_MUL_11	YEE: HPF Coefficient	Section 6.3.58
2F4h	YEE_MUL_12	YEE: HPF Coefficient	Section 6.3.59
2F8h	YEE_MUL_20	YEE: HPF Coefficient	Section 6.3.60
2FCh	YEE_MUL_21	YEE: HPF Coefficient	Section 6.3.61
300h	YEE_MUL_22	YEE: HPF Coefficient	Section 6.3.62
304h	YEE_THR	YEE: Lower Threshold before Referring to LUT	Section 6.3.63
308h	YEE_E_GAN	YEE: Edge Sharpener Gain	Section 6.3.64
30Ch	YEE_E_THR_1	YEE: Edge Sharpener HP Value Lower Threshold	Section 6.3.65
310h	YEE_E_THR_2	YEE: Edge Sharpener HP Value Upper Limit	Section 6.3.66
314h	YEE_G_GAN	YEE: Edge Sharpener Gain on Gradient	Section 6.3.67
318h	YEE_G_OFT	YEE: Edge Sharpener Offset on Gradient	Section 6.3.68
380h	BOX_EN 0	BOX (=Boxcar) Enable	Section 6.3.69
384h	BOX_MODE	BOX: One Shot Mode	Section 6.3.70
388h	BOX_TYP	BOX: Block Size (16x16 or 8x8)	Section 6.3.71
38Ch	BOX_SHF	BOX: Down Shift Value of Input	Section 6.3.72
390h	BOX_SDR_SAD_H	BOX: SDRAM Address MSB	Section 6.3.73
394h	BOX_SDR_SAD_L	BOX: SDRAM Address LSB	Section 6.3.74
398h	Reserved	Reserved	
39Ch	HST_EN 1	HST (=Histogram): Enable	Section 6.3.75
3A0h	HST_MODE	HST: One Shot Mode	Section 6.3.76
3A4h	HST_SEL 6	HST: Source Select	Section 6.3.77
3A8h	HST_PARA 3481	HST: Parameters Select	Section 6.3.78
3ACh	HST_0_VPS	HST: Vertical Start Position	Section 6.3.79
3B0h	HST_0_VSZ 2df	HST: Vertical Size	Section 6.3.80
3B4h	HST_0_HPS	HST: Horizontal Start Position	Section 6.3.81
3B8h	HST_0_HSZ 4ff	HST: Horizontal Size	Section 6.3.82
3BCh	HST_1_VPS	HST: Vertical Start Position	Section 6.3.83
3C0h	HST_1_VSZ	HST: Vertical Size	Section 6.3.84
3C4h	HST_1_HPS	HST: Horizontal Start Position	Section 6.3.85
3C8h	HST_1_HSZ	HST: Horizontal Size	Section 6.3.86
3CCh	HST_2_VPS	HST: Vertical Start Position	Section 6.3.87
3D0h	HST_2_VSZ	HST: Vertical Size	Section 6.3.88

Table 6-91. IPIPE Registers (continued)

Offset	Acronym	Register Description	Section
3D4h	HST_2_HPS	HST: Horizontal Start Position	Section 6.3.89
3D8h	HST_2_HSZ 1fff	HST: Horizontal Size	Section 6.3.90
3DCh	HST_3_VPS	HST: Vertical Start Position	Section 6.3.91
3E0h	HST_3_VSZ 1fff	HST: Vertical Size	Section 6.3.92
3E4h	HST_3_HPS	HST: Horizontal Start Position	Section 6.3.93
3E8h	HST_3_HSZ 1fff	HST: Horizontal Size	Section 6.3.94
3ECh	HST_TBL 3	HST: Table Select	Section 6.3.95
3F0h	HST_MUL_R	HST: Matrix Coefficient	Section 6.3.96
3F4h	HST_MUL_GR	HST: Matrix Coefficient	Section 6.3.97
3F8h	HST_MUL_GB	HST: Matrix Coefficient	Section 6.3.98
3FCh	HST_MUL_B	HST: Matrix Coefficient	Section 6.3.99

6.3.1 IPIPE Enable (SRC_EN)

The IPIPE Enable (SRC_EN) register is shown in Figure 6-88 and described in Table 6-92.

Figure 6-88. IPIPE Enable (SRC_EN) Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-92. IPIPE Enable (SRC_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		IPIPE Enable The start flag of the IPIPE module. When EN is 1, the IPIPE module starts a processing from the next rising edge of the VD. If the processing mode of the IPIPE module is "one shot", the EN is cleared to 0 after the end of the processing area.
		0	disable
		1	enable

6.3.2 One Shot Mode (SRC_MODE)

The One Shot Mode (SRC_MODE) register is shown in Figure 6-89 and described in Table 6-93.

Figure 6-89. One Shot Mode (SRC_MODE) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	WRT	OST
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-93. One Shot Mode (SRC_MODE) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	WRT		C_WE Mode Selection. The mode selection of the ipipeif_wrt which is an input port of the IPIPE module. If WRT is 0, the IPIPE module doesn't use the ipipeif_wrt. Else the IPIPE module uses it.
		0	Disable
		1	Enable
0	OST		One Shot Mode. The processing mode selection of the IPIPE module. Value 0 indicates the mode of "free run", value 1 indicates the mode of "one shot," which clears SRC_EN[EN] after each frame.
		0	Disable
		1	Enable

6.3.3 Input/Output Data Paths (SRC_FMT)

The Input/Output Data Paths (SRC_FMT) register is shown in Figure 6-90and described in Table 6-94.

Figure 6-90. Input/Output Data Paths (SRC_FMT) Register

31-16
Reserved
R-0

15-2	1-0
Reserved	FMT
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-94. Input/Output Data Paths (SRC_FMT) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1-0	FMT		Data path selection.
		0	Bayer input, YCbCr (or RGB) output
		1	Bayer input, Bayer output (Bayer output is from white balance output)
		2	Bayer input, Output disable (For histogram or Boxcar only mode)
		3	YCbCr (16bit) input, YCbCr (or RGB) output

6.3.4 Color Pattern (SRC_COL)

The Color Pattern (SRC_COL) register is shown in Figure 6-91 and described in Table 6-95.

Figure 6-91. Color Pattern (SRC_COL) Register

31-16
Reserved
R-0

15-8	7-6	5-4	3-2	1-0
Reserved	OO	OE	EO	EE
R-00	R/W-3	R/W-2	R/W-1	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-95. Color Pattern (SRC_COL) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-6	OO		Color of the odd line and odd pixel This parameter is valid when SRC_FMT[FMT] is 0, 1 ,or 2.
	10	0	Red
		1	Green (red line)
		2	Green (blue line)
		3	Blue
5-4	OE		Color of the odd line and even pixel This parameter is valid when SRC_FMT[FMT] is 0, 1, or 2.
	11	0	Red
		1	Green (red line)
		2	Green (blue line)
		3	Blue
3-2	EO		Color of the even line and odd pixel This parameter is valid when SRC_FMT[FMT] is 0, 1, or 2.
		0	Red
	00	1	Green (red line)
		2	Green (blue line)
		3	Blue
1-0	EE		Color of the even line and even pixel This parameter is valid when SRC_FMT[FMT] is 0, 1, or 2.
	01	0	Red
		1	Green (red line)
		2	Green (blue line)
		3	Blue

6.3.5 Vertical Start Position (SRC_VPS)

The Vertical Start Position (SRC_VPS) register is shown in Figure 6-92 and described in Table 6-96.

Figure 6-92. Vertical Start Position (SRC_VPS) Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-96. Vertical Start Position (SRC_VPS) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	Vertical Start Position (0 - 65534) The vertical position of the global frame from the rising edge of the VD. The IPIPE module will start an image processing from VAL'th line.

6.3.6 Vertical Processing Size (SRC_VSZ)

The Vertical Processing Size (SRC_VSZ) register is shown in Figure 6-93 and described in Table 6-97.

Figure 6-93. Vertical Processing Size (SRC_VSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-97. Vertical Processing Size (SRC_VSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical Processing Size (0-8190) The vertical size of the processing area. The IPIPE module will process (VAL+1) lines.

6.3.7 Horizontal Start Position (SRC_HPS)

The Horizontal Start Position (SRC_HPS) register is shown in Figure 6-94 and described in Table 6-98.

Figure 6-94. Horizontal Start Position (SRC_HPS) Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-98. Horizontal Start Position (SRC_HPS) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	Horizontal Start Position (0-65534) The horizontal position of the global frame from the rising edge of the HD. The IPIPE module will start an image processing from VAL'th pixel.

6.3.8 Horizontal Processing Size (SRC_HSZ)

The Horizontal Processing Size (SRC_HSZ) register is shown in Figure 6-95 and described in Table 6-99.

Figure 6-95. Horizontal Processing Size (SRC_HSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 6-99. Horizontal Processing Size (SRC_HSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal Processing Size (0-8189) The horizontal size of the processing area. VAL[0] can not be written. The IPIPE module will process (VAL+1) pixels.

6.3.9 Status Flags (Reserved) (DMA_STA)

The Status Flags (Reserved) (DMA_STA) register is shown in Figure 6-96 and described in Table 6-100 .

Figure 6-96. Status Flags (Reserved) (DMA_STA) Register

31-16
Reserved
R-0

15-5	4	3	2	1	0
Reserved	HP_STATUS	HB_STATUS	BSC_STATUS	BP_STATUS	BE_STATUS
R-00	R-0	R-0	R-0	R-0	R-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-100. Status Flags (Reserved) (DMA_STA) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4	HP_STATUS		Histogram Process Status When this bit is high, histogram module is busy
3	HB_STATUS		Histogram Bank Status This bit shows the memory bank which histogram is currently accessing
2	BSC_STATUS		Boundary Signal Calculator Process Status When this bit is high, BSC module is busy
1	BP_STATUS		Boxcar Process Status When this bit is high, Boxcar module is busy
0	BE_STATUS		Boxcar Error Status This bit shows the error status of Boxcar output

6.3.10 MMR Gated Clock Control (GCK_MMR)

The MMR Gated Clock Control (GCK_MMR) register is shown in Figure 6-97 and described in Table 6-101.

Figure 6-97. MMR Gated Clock Control (GCK_MMR) Register

31-16
Reserved
R-0

15-1	0
Reserved	REG
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-101. MMR Gated Clock Control (GCK_MMR) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	REG		IPIPE MMR Clock Enable The on/off selection of the MMR interface clock (clk_mmr_g0) which is used for MMR register accesses. When this bit is off, the registers except the following may not be written. Read access to all registers is allowed. SRC_EN GCK_MMR GCK_PIX BOX_EN HST_EN BSC_EN
		0	off
		1	on

6.3.11 PCLK Gated Clock Control (GCK_PIX)

The PCLK Gated Clock Control (GCK_PIX) register is shown in Figure 6-98 and described in Table 6-102.

Figure 6-98. PCLK Gated Clock Control (GCK_PIX) Register

31-16
Reserved
R-0

15-4	3	2	1	0
Reserved	G3	G2	G1	G0
R-00	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-102. PCLK Gated Clock Control (GCK_PIX) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved		Any writes to these bit(s) must always have a value of 0.
3	G3	0	IPIPE G3 Clock Enable The on/off selection of clk_pix_g3 which is used for the IPIPE processing of "Edge enhancer" and "Chroma artifact reduction". Data path need to be configured accordingly using SRC_FMT.
		0	off
		1	on
2	G2		IPIPE G2 Clock Enable The on/off selection of clk_pix_g2 which is used for the IPIPE processing of "CFA" to "422 conv", "Histogram (YCbCr input)", and "Boundary Signal Calculator". Data path need to be configured accordingly using SRC_FMT.
		0	off
		1	on
1	G1		IPIPE G1 Clock Enable The on/off selection of clk_pix_g1 which is used for the IPIPE processing of "Defect Pixel Correction" to "White Balance", and "Histogram (RAW input)". Data path need to be configured accordingly using SRC_FMT.
		0	off
		1	on
0	G0		IPIPE G0 Clock Enable The on/off selection of clk_pix_g0 which is used for the IPIPE processing of "Boxcar". Data path need to be configured accordingly using SRC_FMT.
		0	off
		1	on

6.3.12 LUTDPC (=LUT Defect Pixel Correction): Enable (DPC_LUT_EN)

The LUTDPC (=LUT Defect Pixel Correction): Enable (DPC_LUT_EN) register is shown in Figure 6-99 and described in Table 6-103 .

Figure 6-99. LUTDPC (=LUT Defect Pixel Correction): Enable (DPC_LUT_EN) Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-103. LUTDPC (=LUT Defect Pixel Correction): Enable (DPC_LUT_EN) Field Descriptions

Bit	Field	Value0	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		LUT Defect Pixel Correction Enable
		0	disable
		1	enable

6.3.13 LUTDPC: Processing Mode Selection (DPC_LUT_SEL)

The Processing Mode Selection (DPC_LUT_SEL) register is shown in Figure 6-100 and described in Table 6-104.

Figure 6-100. Processing Mode Selection (DPC_LUT_SEL) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	TBL	SEL
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-104. Processing Mode Selection (DPC_LUT_SEL) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	TBL		LUT type selection
		0	up to 1024 entries
		1	infinite number of entries
0	SEL		Replace dot selection on option #0 This bit indicates the correction method for option #0 in LUT entries
		0	replace with black dot
		1	replace with white dot

6.3.14 LUTDPC: Start Address in LUT (DPC_LUT_ADR)

The Start Address in LUT (DPC_LUT_ADR) register is shown in Figure 6-101 and described in Table 6-105.

Figure 6-101. Start Address in LUT (DPC_LUT_ADR) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	ADR
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-105. Start Address in LUT (DPC_LUT_ADR) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	ADR	0-3FFh	Start Address in LUT

6.3.15 LUTDPC: Number of Available Entries in LUT (DPC_LUT_ADR)

The Number of Available Entries in LUT (DPC_LUT_ADR) register is shown in Figure 6-102 and described in Table 6-106.

Figure 6-102. Number of Available Entries in LUT (DPC_LUT_ADR) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	SIZ
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-106. Number of Available Entries in LUT (DPC_LUT_ADR) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	SIZ	0-3FFh	Number of valid data in LUT (SIZ+1) of valid data in LUT. If DPC_LUT_SEL[TBL] is 1, the number is ignored.

6.3.16 WB2 (=White Balance): Offset (WB2_OFT_R)

The WB2 (=White Balance): Offset (WB2_OFT_R) register is shown in Figure 6-103 and described in Table 6-107.

Figure 6-103. WB2 (=White Balance): Offset (WB2_OFT_R) Register

31-16
Reserved
R-0

L

15-12	11-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-107. WB2 (=White Balance): Offset (WB2_OFT_R) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	White balance Offset for R (S12)

6.3.17 WB2: Offset (WB2_OFT_GR)

The Offset (WB2_OFT_GR) register is shown in Figure 6-104 and described in Table 6-108.

Figure 6-104. Offset (WB2_OFT_GR) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-108. Offset (WB2_OFT_GR) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	White balance Offset for Gr (S12)

6.3.18 WB2: Offset (WB2_OFT_GB)

The Offset (WB2_OFT_GB) register is shown in Figure 6-105 and described in Table 6-109.

Figure 6-105. Offset (WB2_OFT_GB) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-109. Offset (WB2_OFT_GB) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	White balance Offset for Gb (S12).

6.3.19 WB2: Offset (WB2_OFT_B)

The Offset (WB2_OFT_B) register is shown in Figure 6-106 and described in Table 6-110 .

Figure 6-106. Offset (WB2_OFT_B) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-110. Offset (WB2_OFT_B) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	White balance Offset for B (S12).

6.3.20 WB2: Gain (WB2_WGN_R)

The Gain (WB2_WGN_R) register is shown in Figure 6-107 and described in Table 6-111.

Figure 6-107. Gain (WB2_WGN_R) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-512

LEGEND: R = Read only; -*n* = value after reset

Table 6-111. Gain (WB2_WGN_R) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	White balance Gain for R (U4.9 = 0 - 15.998).

6.3.21 WB2: Gain (WB2_WGN_GR)

The Gain (WB2_WGN_GR) register is shown in Figure 6-108 and described in Table 6-112.

Figure 6-108. Gain (WB2_WGN_GR) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-512

LEGEND: R = Read only; -*n* = value after reset

Table 6-112. Gain (WB2_WGN_GR) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	White balance Gain for Gr (U4.9 = 0 - 15.998).

6.3.22 WB2: Gain (WB2_WGN_GB)

The Gain (WB2_WGN_GB) register is shown in Section 6.3.22 and described in Table 6-113.

Figure 6-109. Gain (WB2_WGN_GB) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-512

LEGEND: R = Read only; -*n* = value after reset

Table 6-113. Gain (WB2_WGN_GB) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	White balance Gain for Gb (U4.9 = 0 - 15.998).

6.3.23 WB2: Gain (WB2_WGN_B)

The Gain (WB2_WGN_B) register is shown in Figure 6-110 and described in Table 6-114.

Figure 6-110. Gain (WB2_WGN_B) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-512

LEGEND: R = Read only; -*n* = value after reset

Table 6-114. Gain (WB2_WGN_B) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	White balance Gain for B (U4.9 = 0 - 15.998).

6.3.24 RGB1 (=1st RGB2RGB conv): Matrix Coefficient (RGB1_MUL_RR)

The RGB1 (=1st RGB2RGB conv): Matrix Coefficient (RGB1_MUL_RR) register is shown in Figure 6-111 and described in Table 6-115.

Figure 6-111. RGB1 (=1st RGB2RGB conv): Matrix Coefficient (RGB1_MUL_RR) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-256

LEGEND: R = Read only; -*n* = value after reset

Table 6-115. RGB1 (=1st RGB2RGB conv): Matrix Coefficient (RGB1_MUL_RR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for RR (S4.8 = -8 - +7.996)

6.3.25 RGB1: Matrix Coefficient (RGB1_MUL_GR)

The Matrix Coefficient (RGB1_MUL_GR) register is shown in Figure 6-112 and described in Table 6-116.

Figure 6-112. Matrix Coefficient (RGB1_MUL_GR) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-116. Matrix Coefficient (RGB1_MUL_GR) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for GR (S4.8 = -8 - +7.996)

6.3.26 RGB1: Matrix Coefficient (RGB1_MUL_BR)

The Matrix Coefficient (RGB1_MUL_BR) register is shown in Figure 6-113 and described in Table 6-117.

Figure 6-113. Matrix Coefficient (RGB1_MUL_BR) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-117. Matrix Coefficient (RGB1_MUL_BR) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for BR (S4.8 = -8 - +7.996)

6.3.27 RGB1: Matrix Coefficient (RGB1_MUL_RG)

The Matrix Coefficient (RGB1_MUL_RG) register is shown in Figure 6-114 and described in Table 6-118.

Figure 6-114. Matrix Coefficient (RGB1_MUL_RG) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-118. Matrix Coefficient (RGB1_MUL_RG) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for RG (S4.8 = -8 - +7.996)

6.3.28 RGB1: Matrix Coefficient (RGB1_MUL_GG)

The Matrix Coefficient (RGB1_MUL_GG) register is shown in Figure 6-115 and described in Table 6-119.

Figure 6-115. Matrix Coefficient (RGB1_MUL_GG) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-256

LEGEND: R = Read only; -*n* = value after reset

Table 6-119. Matrix Coefficient (RGB1_MUL_GG) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for GG (S4.8 = -8 - +7.996).

6.3.29 RGB1: Matrix Coefficient (RGB1_MUL_BG)

The Matrix Coefficient (RGB1_MUL_BG) register is shown in Figure 6-116 and described in Table 6-120.

Figure 6-116. Matrix Coefficient (RGB1_MUL_BG) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-120. Matrix Coefficient (RGB1_MUL_BG) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for BG (S4.8 = -8 - +7.996)

6.3.30 RGB1: Matrix Coefficient (RGB1_MUL_RB)

The Matrix Coefficient (RGB1_MUL_RB) register is shown in Figure 6-117 and described in Table 6-121.

Figure 6-117. Matrix Coefficient (RGB1_MUL_RB) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-121. Matrix Coefficient (RGB1_MUL_RB) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for RB (S4.8 = -8 - +7.996)

6.3.31 RGB1: Matrix Coefficient (RGB1_MUL_GB)

The Matrix Coefficient (RGB1_MUL_GB) register is shown in Figure 6-118 and described in Table 6-122.

Figure 6-118. Matrix Coefficient (RGB1_MUL_GB) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-122. Matrix Coefficient (RGB1_MUL_GB) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for GB (S4.8 = -8 - +7.996)

6.3.32 RGB1: Matrix Coefficient (RGB1_MUL_BB)

The Matrix Coefficient (RGB1_MUL_BB) register is shown in Figure 6-119 and described in Table 6-123.

Figure 6-119. Matrix Coefficient (RGB1_MUL_BB) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-256

LEGEND: R = Read only; -*n* = value after reset

Table 6-123. Matrix Coefficient (RGB1_MUL_BB) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for BB (S4.8 = -8 - +7.996)

6.3.33 RGB1: Offset (RGB1_OFT_OR)

The Offset (RGB1_OFT_OR) register is shown in Figure 6-120 and described in Table 6-124.

Figure 6-120. Offset (RGB1_OFT_OR) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-124. Offset (RGB1_OFT_OR) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Offset for R (S13)

6.3.34 RGB1: Offset (RGB1_OFT_OG)

The Offset (RGB1_OFT_OG) register is shown in Figure 6-121 and described in Table 6-125.

Figure 6-121. Offset (RGB1_OFT_OG) Register

31-16	
Reserved	
R-0	
15-13	**12-0**
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-125. Offset (RGB1_OFT_OG) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Offset for G (S13)

6.3.35 RGB1: Offset (RGB1_OFT_OB)

The Offset (RGB1_OFT_OB) register is shown in Figure 6-122 and described in Table 6-126.

Figure 6-122. Offset (RGB1_OFT_OB) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-126. Offset (RGB1_OFT_OB) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Offset for B (S13)

6.3.36 Gamma Correction Configuration (GMM_CFG)

The gamma correction configuration (GMM_CFG) register is shown in Figure 6-123 and described in Table 6-127.

Figure 6-123. Gamma Correction Configuration (GMM_CFG) Register

31-16
Reserved
R-0

15-7	6-5	4	3	2	1	0
Reserved	SIZ	TBL	Rsv	BYPB	BYPG	BYPR
R-0	R/W-3	R/W-0	R-00	R/W-1	R/W-1	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 6-127. Gamma Correction Configuration (GMM_CFG) Field Descriptions

Bit	Field	Value	Description
31-7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6-5	SIZ		Size of Gamma Table
		0	64 words
		1	128 words
		2	256 words
		3	512 words
4	TBL		Selection of Gamma Table .
		0	RAM
		1	ROM
3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	BYPB		Gamma Correction Mode for B
		0	No bypass
		1	Bypass
1	BYPG		Gamma Correction Mode for G
		0	No bypass
		1	Bypass
0	BYPR		Gamma Correction Mode for R
		0	No bypass
		1	Bypass

6.3.37 YUV (RGB2YCbCr conv): Luminance Adjustment (Contrast and Brightness) (YUV_ADJ)

The YUV (RGB2YCbCr conv): Luminance Adjustment (Contrast and Brightness) (YUV_ADJ) register is shown in Figure 6-124 and described in Table 6-128.

Figure 6-124. YUV (RGB2YCbCr conv): Luminance Adjustment (Contrast and Brightness) (YUV_ADJ) Register

31-16
Reserved
R-0

15-8	7-0
BRT	CTR
R/W-0	R/W-16

LEGEND: R = Read only; -*n* = value after reset

Table 6-128. YUV (RGB2YCbCr conv): Luminance Adjustment (Contrast and Brightness) (YUV_ADJ) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	BRT	0-FFh	Brightness Offset value for brightness control.
7-0	CTR	0-FFh	Contrast Multiplier coefficient for contrast control (U4.4 = 0 - +15.94)

6.3.38 YUV: Matrix Coefficient (YUV_MUL_RY)

The Matrix Coefficient (YUV_MUL_RY) register is shown in Figure 6-125 and described in Table 6-129.

Figure 6-125. Matrix Coefficient (YUV_MUL_RY) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-77

LEGEND: R = Read only; -*n* = value after reset

Table 6-129. Matrix Coefficient (YUV_MUL_RY) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for RY (S4.8 = -8 - +7.996)

6.3.39 YUV: Matrix Coefficient (YUV_MUL_GY)

The Matrix Coefficient (YUV_MUL_GY) register is shown in Figure 6-126 and described in Table 6-130.

Figure 6-126. Matrix Coefficient (YUV_MUL_GY) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-150

LEGEND: R = Read only; -*n* = value after reset

Table 6-130. Matrix Coefficient (YUV_MUL_GY) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for GY (S4.8 = -8 - +7.996)

6.3.40 YUV: Matrix Coefficient (YUV_MUL_BY)

The Matrix Coefficient (YUV_MUL_BY) register is shown in Figure 6-127 and described in Table 6-131.

Figure 6-127. Matrix Coefficient (YUV_MUL_BY) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-29

LEGEND: R = Read only; -*n* = value after reset

Table 6-131. Matrix Coefficient (YUV_MUL_BY) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for BY (S4.8 = -8 - +7.996)

6.3.41 YUV: Matrix Coefficient (YUV_MUL_RCB)

The Matrix Coefficient (YUV_MUL_RCB) register is shown in Figure 6-128 and described in Table 6-132.

Figure 6-128. Matrix Coefficient (YUV_MUL_RCB) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W--43

LEGEND: R = Read only; -*n* = value after reset

Table 6-132. Matrix Coefficient (YUV_MUL_RCB) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for RCb (S4.8 = -8 - +7.996)

6.3.42 YUV: Matrix Coefficient (YUV_MUL_GCB)

The Matrix Coefficient (YUV_MUL_GCB) register is shown in Figure 6-129 and described in Table 6-133.

Figure 6-129. Matrix Coefficient (YUV_MUL_GCB) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W--85

LEGEND: R = Read only; -*n* = value after reset

Table 6-133. Matrix Coefficient (YUV_MUL_GCB) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for GCb (S4.8 = -8 - +7.996)

6.3.43 YUV: Matrix Coefficient (YUV_MUL_BCB)

The Matrix Coefficient (YUV_MUL_BCB) register is shown in Figure 6-130 and described in Table 6-134.

Figure 6-130. Matrix Coefficient (YUV_MUL_BCB) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-128

LEGEND: R = Read only; -*n* = value after reset

Table 6-134. Matrix Coefficient (YUV_MUL_BCB) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for BCb (S4.8 = -8 - +7.996)

6.3.44 YUV: Matrix Coefficient (YUV_MUL_RCR)

The Matrix Coefficient (YUV_MUL_RCR) register is shown in Figure 6-131 and described in Table 6-135 .

Figure 6-131. Matrix Coefficient (YUV_MUL_RCR) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-128

LEGEND: R = Read only; -*n* = value after reset

Table 6-135. Matrix Coefficient (YUV_MUL_RCR) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for RCr (S4.8 = -8 - +7.996)

6.3.45 YUV: Matrix Coefficient (YUV_MUL_GCR)

The Matrix Coefficient (YUV_MUL_GCR) register is shown in Figure 6-132 and described in Table 6-136.

Figure 6-132. Matrix Coefficient (YUV_MUL_GCR) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W--107

LEGEND: R = Read only; -*n* = value after reset

Table 6-136. Matrix Coefficient (YUV_MUL_GCR) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for GCr (S4.8 = -8 - +7.996)

6.3.46 YUV: Matrix Coefficient (YUV_MUL_BCR)

The Matrix Coefficient (YUV_MUL_BCR) register is shown in Figure 6-133 and described in Table 6-137.

Figure 6-133. Matrix Coefficient (YUV_MUL_BCR) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W--21

LEGEND: R = Read only; -*n* = value after reset

Table 6-137. Matrix Coefficient (YUV_MUL_BCR) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for BCr (S4.8 = -8 - +7.996)

6.3.47 YUV: Offset (YUV_OFT_Y)

The Offset (YUV_OFT_Y) register is shown in Figure 6-134 and described in Table 6-138.

Figure 6-134. Offset (YUV_OFT_Y) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-138. Offset (YUV_OFT_Y) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Y Output Offset (S11)

6.3.48 YUV: Offset (YUV_OFT_CB)

The Offset (YUV_OFT_CB) register is shown in Figure 6-135 and described in Table 6-139.

Figure 6-135. Offset (YUV_OFT_CB) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-00	R/W-128

LEGEND: R = Read only; -*n* = value after reset

Table 6-139. Offset (YUV_OFT_CB) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Cb Output Offset (S11)

6.3.49 YUV: Offset (YUV_OFT_CR)

The Offset (YUV_OFT_CR) register is shown in Figure 6-136and described in Table 6-140.

Figure 6-136. Offset (YUV_OFT_CR) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-00	R/W-128

LEGEND: R = Read only; -*n* = value after reset

Table 6-140. Offset (YUV_OFT_CR) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Cr Output Offset (S11)

6.3.50 Chrominance Position (for 422 Down Sampler) (YUV_PHS)

The Chrominance Position (for 422 Down Sampler) (YUV_PHS) register is shown in Figure 6-137 and described in Table 6-141.

Figure 6-137. Chrominance Position (for 422 Down Sampler) (YUV_PHS) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	LPF	POS
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-141. Chrominance Position (for 422 Down Sampler) (YUV_PHS) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	LPF		121-LPF Enable for Chrominance
		0	off
		1	on
0	POS		Phase position of the output of the Chrominance If SRC_FMT = 3 (YCbCr input), then the phase position of the INPUT of the Chrominance is selected by this register.
		0	same position with Luminance
		1	the middle of the Luminance

6.3.51 YEE (=Edge Enhancer): Enable (YEE_EN)

The YEE (=Edge Enhancer): Enable (YEE_EN) register is shown in Figure 6-138 and described in Table 6-142.

Figure 6-138. YEE (=Edge Enhancer): Enable (YEE_EN) Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-142. YEE (=Edge Enhancer): Enable (YEE_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Edge Enhancer Enable
		0	disable
		1	enable

6.3.52 YEE: Method Selection (YEE_TYP)

The Method Selection (YEE_TYP) register is shown in Figure 6-139 and described in Table 6-143.

Figure 6-139. Method Selection (YEE_TYP) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	HAL	SEL
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-143. Method Selection (YEE_TYP) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	HAL		Halo Reduction (in Edge Sharpener) Enable
		0	disable
		1	enable
0	SEL		Merging Method between Edge Enhancer and Edge Sharpener ABSMAX(x, y) = (|x|>|y|) ? x : y
		0	absmax(EE, ES)
		1	EE + ES

6.3.53 YEE: HPF Shift Length (YEE_SHF)

The HPF Shift Length (YEE_SHF) register is shown in Figure 6-140 and described in Table 6-144.

Figure 6-140. HPF Shift Length (YEE_SHF) Register

31-16
Reserved
R-0

15-4	3-0
Reserved	SHF
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-144. HPF Shift Length (YEE_SHF) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3-0	SHF	0-Fh	YEE_SHF Down shift length of high pass filter (HPF) in edge enhancer

6.3.54 YEE: HPF Coefficient (YEE_MUL_00)

The HPF Coefficient (YEE_MUL_00) register is shown in Figure 6-141 and described in Table 6-145.

Figure 6-141. HPF Coefficient (YEE_MUL_00) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-145. HPF Coefficient (YEE_MUL_00) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 00 (S10)

6.3.55 YEE: HPF Coefficient (YEE_MUL_01)

The HPF Coefficient (YEE_MUL_01) register is shown in Figure 6-142 and described in Table 6-146.

Figure 6-142. HPF Coefficient (YEE_MUL_01) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-146. HPF Coefficient (YEE_MUL_01) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 01 (S10)

6.3.56 YEE: HPF Coefficient (YEE_MUL_02)

The HPF Coefficient (YEE_MUL_02) register is shown in Figure 6-143 and described in Table 6-147.

Figure 6-143. HPF Coefficient (YEE_MUL_02) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-147. HPF Coefficient (YEE_MUL_02) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 02 (S10)

6.3.57 YEE: HPF Coefficient (YEE_MUL_10)

The HPF Coefficient (YEE_MUL_10) register is shown in Figure 6-144 and described in Table 6-148.

Figure 6-144. HPF Coefficient (YEE_MUL_10) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-148. HPF Coefficient (YEE_MUL_10) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 10 (S10)

6.3.58 YEE: HPF Coefficient (YEE_MUL_11)

The HPF Coefficient (YEE_MUL_11) register is shown in Figure 6-145 and described in Table 6-149.

Figure 6-145. HPF Coefficient (YEE_MUL_11) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-149. HPF Coefficient (YEE_MUL_11) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 11 (S10)

6.3.59 YEE: HPF Coefficient (YEE_MUL_12)

The HPF Coefficient (YEE_MUL_12) register is shown in Figure 6-146 and described in Table 6-150.

Figure 6-146. HPF Coefficient (YEE_MUL_12) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-150. HPF Coefficient (YEE_MUL_12) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 12 (S10)

6.3.60 YEE: HPF Coefficient (YEE_MUL_20)

The HPF Coefficient (YEE_MUL_20) register is shown in Figure 6-147 and described in Table 6-151 .

Figure 6-147. HPF Coefficient (YEE_MUL_20) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-151. HPF Coefficient (YEE_MUL_20) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 20 (S10)

6.3.61 YEE: HPF Coefficient (YEE_MUL_21)

The HPF Coefficient (YEE_MUL_21) register is shown in Figure 6-148 and described in Table 6-152.

Figure 6-148. HPF Coefficient (YEE_MUL_21) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-152. HPF Coefficient (YEE_MUL_21) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 21 (S10)

6.3.62 YEE: HPF Coefficient (YEE_MUL_22)

The HPF Coefficient (YEE_MUL_22) register is shown in Figure 6-149 and described in Table 6-153.

Figure 6-149. HPF Coefficient (YEE_MUL_22) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-153. HPF Coefficient (YEE_MUL_22) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 22 (S10)

6.3.63 YEE: Lower Threshold before Referring to LUT (YEE_THR)

The Lower Threshold before Referring to LUT (YEE_THR) register is shown in Figure 6-150 and described in Table 6-154.

Figure 6-150. Lower Threshold before Referring to LUT (YEE_THR) Register

31-16
Reserved
R-0

15-6	5-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-154. Lower Threshold before Referring to LUT (YEE_THR) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved	0	Any writes to these bit(s) must always have a value of 0.
5-0	VAL	0-3Fh	YEE_THR Lower Threshold before referring to LUT if (HPF ≤ VAL), then output = HPF+VAL. if (HPF > VAL), then output = HPF-VAL. Otherwise, output = 0.

6.3.64 YEE: Edge Sharpener Gain (YEE_E_GAN)

The Edge Sharpener Gain (YEE_E_GAN) register is shown in Figure 6-151 and described in Table 6-155.

Figure 6-151. Edge Sharpener Gain (YEE_E_GAN) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-155. Edge Sharpener Gain (YEE_E_GAN) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	YEE_E_GAN Edge Sharpener Gain

6.3.65 YEE: Edge Sharpener HP Value Lower Threshold (YEE_E_THR_1)

The Edge Sharpener HP Value Lower Threshold (YEE_E_THR_1) register is shown in Figure 6-152 and described in Table 6-156.

Figure 6-152. Edge Sharpener HP Value Lower Threshold (YEE_E_THR_1) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-156. Edge Sharpener HP Value Lower Threshold (YEE_E_THR_1) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	YEE_E_THR_1 Edge Sharpener Lower Threshold if (HPF ≤ VAL), then output = (HPF+VAL) >> 6. if (HPF > VAL), then output = (HPF-VAL) >> 6. Otherwise, output = 0.

6.3.66 YEE: Edge Sharpener HP Value Upper Limit (YEE_E_THR_2)

The Edge Sharpener HP Value Upper Limit (YEE_E_THR_2) register is shown in Figure 6-153 and described in Table 6-157.

Figure 6-153. Edge Sharpener HP Value Upper Limit (YEE_E_THR_2) Register

31-16
Reserved
R-0

15-6	5-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-157. Edge Sharpener HP Value Upper Limit (YEE_E_THR_2) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved	0	Any writes to these bit(s) must always have a value of 0.
5-0	VAL	0-3Fh	YEE_E_THR_2 Edge Sharpener HP Value Upper Limit.

6.3.67 YEE: Edge Sharpener Gain on Gradient (YEE_G_GAN)

The Edge Sharpener Gain on Gradient (YEE_G_GAN) register is shown in Figure 6-154 and described in Table 6-158.

Figure 6-154. Edge Sharpener Gain on Gradient (YEE_G_GAN) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-158. Edge Sharpener Gain on Gradient (YEE_G_GAN) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	YEE_E_G_GAN Edge Sharpener Gain on Gradient

6.3.68 YEE: Edge Sharpener Offset on Gradient (YEE_G_OFT)

The Edge Sharpener Offset on Gradient (YEE_G_OFT) register is shown in Figure 6-155 and described in Table 6-159.

Figure 6-155. Edge Sharpener Offset on Gradient (YEE_G_OFT) Register

31-16
Reserved
R-0

15-6	5-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-159. Edge Sharpener Offset on Gradient (YEE_G_OFT) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved	0	Any writes to these bit(s) must always have a value of 0.
5-0	VAL	0-3Fh	YEE_G_OFT Edge Sharpener Offset on Gradient

6.3.69 Boxcar Enable (BOX_EN)

The boxcar enable register is shown in Figure 6-156and described in Table 6-160.

Figure 6-156. Boxcar Enable (BOX_EN) Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-160. BOX_EN (BOX_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Boxcar Enable
		0	disable
		1	enable

6.3.70 BOX: BOX One Shot Mode (BOX_MODE)

The Box One Shot Mode register is shown in Figure 6-157 and described in Table 6-161.

Figure 6-157. BOX One Shot Mode (BOX_MODE) Register

31-16
Reserved
R-0

15-1	0
Reserved	OST
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-161. BOX One Shot Mode (BOX_MODE) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	OST		Boxcar One Shot Mode Enable
		0	continuous mode
		1	one shot mode

6.3.71 BOX: Block Size (16x16 or 8x8) (BOX_TYP)

The Block Size (16x16 or 8x8) (BOX_TYP) register is shown in Figure 6-158 and described in Table 6-162.

Figure 6-158. Block Size (16x16 or 8x8) (BOX_TYP) Register

31-16
Reserved
R-0

15-1	0
Reserved	SEL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-162. Block Size (16x16 or 8x8) (BOX_TYP) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	SEL		Block Size in Boxcar Sampling
		0	8x8
		1	16x16

6.3.72 BOX: Down Shift Value of Input (BOX_SHF)

The Box Down shift value of input (BOX_SHF) register is shown in Figure 6-159 and described in Table 6-163.

Figure 6-159. Down Shift Value of Input (BOX_SHF) Register

31-16
Reserved
R-0

15-3	2-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-163. Down Shift Value of Input (BOX_SHF) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2-0	VAL	0-7h	Down shift value of output data of Boxcar (0-4)

6.3.73 BOX: SDRAM Address MSB (BOX_SDR_SAD_H)

The SDRAM Address MSB (BOX_SDR_SAD_H) register is shown in Figure 6-160 and described in Table 6-164.

Figure 6-160. SDRAM Address MSB (BOX_SDR_SAD_H) Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-164. SDRAM Address MSB (BOX_SDR_SAD_H) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	Boxcar SDRAM Address (H) The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.3.74 BOX: SDRAM Address LSB (BOX_SDR_SAD_L)

The SDRAM Address LSB (BOX_SDR_SAD_L) register is shown in Figure 6-161 and described in Table 6-165.

Figure 6-161. SDRAM Address LSB (BOX_SDR_SAD_L) Register

31-16
Reserved
R-0

15-5	4-0
VAL	Reserved
R/W-0	R-00

LEGEND: R = Read only; -*n* = value after reset

Table 6-165. SDRAM Address LSB (BOX_SDR_SAD_L) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-5	VAL	0-7FFh	Boxcar SDRAM Address (L) The lower 16 bits of the first address in the allowed memory space in SDRAM.
4-0	Reserved	0	Reserved

6.3.75 HST (=Histogram): Enable (HST_EN)

The histogram enable (HST_EN) register is shown in Figure 6-162 and described in Table 6-166.

Figure 6-162. HST (=Histogram): Enable (HST_EN) Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-166. HST (=Histogram): Enable (HST_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Histogram Enable
		0	disable
		1	enable

6.3.76 HST: One Shot Mode (HST_MODE)

The One Shot Mode (HST_MODE) register is shown in Figure 6-163 and described in Table 6-167.

Figure 6-163. One Shot Mode (HST_MODE) Register

31-16
Reserved
R-0

15-1	0
Reserved	OST
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-167. One Shot Mode (HST_MODE) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	OST		Histogram One Shot Mode Enable
		0	continuous mode
		1	one shot mode

6.3.77 HST: Source Select (HST_SEL)

The Source Select (HST_SEL) register is shown in Figure 6-164 and described in Table 6-168.

Figure 6-164. Source Select (HST_SEL) Register

31-16
Reserved
R-0

15-3	2	1-0
Reserved	SEL	TYP
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-168. Source Select (HST_SEL) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	SEL		Histogram Input Selection
		0	from 1st Noise Filter (Bayer format)
		1	from RGB2YUV (YCbCr-444 format)
1-0	TYP		Histogram Green Sampling method Selection Only valid when SEL is 0.
		0	Gr is collected
		1	Gb is collected
		2	Gavg is collected

6.3.78 HST: Parameters Select (HST_PARA)

The Parameters Select (HST_PARA) register is shown in Figure 6-165 and described in Table 6-169.

Figure 6-165. Parameters Select (HST_PARA) Register

31-16
Reserved
R-0

15-14	13-12	11-8	7	6	5	4	3	2	1	0
Reserved	BIN	SHF	COL3	COL2	COL1	COL0	RGN3	RGN2	RGN1	RGN0
R-00	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-169. Parameters Select (HST_PARA) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-12	BIN		Number of bins
		0	32 bins
		1	64 bins
		2	128 bins
		3	256 bins
11-8	SHF	0-Fh	Shift Length of input data
7	COL3		Color 3 Enable Y : HST_SEL[SEL]=0 Y2: HST_SEL[SEL]=1
		0	disable
		1	enable
6	COL2		Color 2 Enable B : HST_SEL[SEL]=0 Cb: HST_SEL[SEL]=1
		0	disable
		1	enable
5	COL1		Color 1 Enable G : HST_SEL[SEL]=0 Y1: HST_SEL[SEL]=1
		0	disable
		1	enable
4	COL0		Color 0 Enable R : HST_SEL[SEL]=0 Cr: HST_SEL[SEL]=1
		0	disable
		1	enable
3	RGN3		Region 3 Enable
		0	disable
		1	enable
2	RGN2		Region 2 Enable
		0	disable
		1	enable
1	RGN1		Region 1 Enable
		0	disable
		1	enable
0	RGN0		Region 0 Enable
		0	disable
		1	enable

6.3.79 HST: Vertical Start Position (HST_0_VPS)

The Vertical Start Position (HST_0_VPS) register is shown in Figure 6-166 and described in Table 6-170.

Figure 6-166. Vertical Start Position (HST_0_VPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-170. Vertical Start Position (HST_0_VPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical start position of the region0 from the SRC_VPS The region will start the "Histogram" processing from VAL'th line. VAL[0] can not be written.

6.3.80 HST: Vertical Size (HST_0_VSZ)

The Vertical Size (HST_0_VSZ) register is shown in Figure 6-167 and described in Table 6-171.

Figure 6-167. Vertical Size (HST_0_VSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 6-171. Vertical Size (HST_0_VSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical size of the region0. The "Histogram" processing of the region will process (VAL+1) lines. VAL[0] can not be written.

6.3.81 HST: Horizontal Start Position (HST_0_HPS)

The Horizontal Start Position (HST_0_HPS) register is shown in Figure 6-168 and described in Table 6-172.

Figure 6-168. Horizontal Start Position (HST_0_HPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-172. Horizontal Start Position (HST_0_HPS) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal start position of the region0 from the SRC_VPS. The region will start the "Histogram" processing from VAL'th pixel. VAL[0] can not be written.

6.3.82 HST: Horizontal Size (HST_0_HSZ)

The Horizontal Size (HST_0_HSZ) register is shown in Figure 6-169 and described in Table 6-173.

Figure 6-169. Horizontal Size (HST_0_HSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 6-173. Horizontal Size (HST_0_HSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal size of the region0. The "Histogram" processing of the region will process (VAL+1) pixels. VAL[0] can not be written.

6.3.83 HST: Vertical Start Position (HST_1_VPS)

The Vertical Start Position (HST_1_VPS) register is shown in Figure 6-170 and described in Table 6-174.

Figure 6-170. Vertical Start Position (HST_1_VPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-174. Vertical Start Position (HST_1_VPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical start position of the region1 from the SRC_VPS The region will start the "Histogram" processing from VAL'th line. VAL[0] can not be written.

6.3.84 HST: Vertical Size (HST_1_VSZ)

The Vertical Size (HST_1_VSZ) register is shown in Figure 6-171 and described in Table 6-175.

Figure 6-171. Vertical Size (HST_1_VSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 6-175. Vertical Size (HST_1_VSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical size of the region1. The "Histogram" processing of the region will process (VAL+1) lines. VAL[0] can not be written.

6.3.85 HST: Horizontal Start Position (HST_1_HPS)

The Horizontal Start Position (HST_1_HPS) register is shown in Figure 6-172 and described in Table 6-176.

Figure 6-172. Horizontal Start Position (HST_1_HPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-176. Horizontal Start Position (HST_1_HPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal start position of the region1 from the SRC_VPS. The region will start the "Histogram" processing from VAL'th pixel. VAL[0] can not be written.

6.3.86 HST: Horizontal Size (HST_1_HSZ)

The Horizontal Size (HST_1_HSZ) register is shown in Figure 6-173 and described in Table 6-177.

Figure 6-173. Horizontal Size (HST_1_HSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 6-177. Horizontal Size (HST_1_HSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal size of the region1. The "Histogram" processing of the region will process (VAL+1) pixels. VAL[0] can not be written.

6.3.87 HST: Vertical Start Position (HST_2_VPS)

The Vertical Start Position 2 (HST_2_VPS) register is shown in Figure 6-174 and described in Table 6-178.

Figure 6-174. Vertical Start Position (HST_2_VPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-178. Vertical Start Position (HST_2_VPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical start position of the region2 from the SRC_VPS. The region will start the "Histogram" processing from VAL'th line. VAL[0] can not be written.

6.3.88 HST: Vertical Size (HST_2_VSZ)

The Vertical Size 2 (HST_2_VSZ) register is shown in Figure 6-175 and described in Table 6-179.

Figure 6-175. Vertical Size (HST_2_VSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 6-179. Vertical Size (HST_2_VSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical size of the region2 The "Histogram" processing of the region will process (VAL+1) lines. VAL[0] can not be written.

6.3.89 HST: Horizontal Start Position (HST_2_HPS)

The horizontal start position 2 (HST_2_HPS) register is shown in Figure 6-176 and described in Table 6-180.

Figure 6-176. Horizontal Start Position (HST_2_HPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-180. Horizontal Start Position (HST_2_HPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved.
12-0	VAL	0-1FFFh	Horizontal start position of the region2 from the SRC_VPS. The region will start the "Histogram" processing from VAL'th pixel. VAL[0] can not be written.

6.3.90 HST: Horizontal Size (HST_2_HSZ)

The horizontal size 2 (HST_2_HSZ) register is shown in Figure 6-177 and described in Table 6-181.

Figure 6-177. Horizontal Size (HST_2_HSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 6-181. Horizontal Size (HST_2_HSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal size of the region2. The "Histogram" processing of the region will process (VAL+1) pixels. VAL[0] can not be written.

6.3.91 HST: Vertical Start Position (HST_3_VPS)

The vertical start position 3 (HST_3_VPS) register is shown in Figure 6-178 and described in Table 6-182.

Figure 6-178. Vertical Start Position (HST_3_VPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-182. Vertical Start Position (HST_3_VPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical start position of the region3 from the SRC_VPS. The region will start the "Histogram" processing from VAL'th line. VAL[0] can not be written.

6.3.92 HST: Vertical Size (HST_3_VSZ)

The vertical size 3 (HST_3_VSZ) register is shown in Figure 6-179 and described in Table 6-183.

Figure 6-179. Vertical Size (HST_3_VSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 6-183. Vertical Size (HST_3_VSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical size of the region3. The "Histogram" processing of the region will process (VAL+1) lines. VAL[0] can not be written.

6.3.93 HST: Horizontal Start Position (HST_3_HPS)

The horizontal start position 3 (HST_3_HPS) register is shown in Figure 6-180 and described in Table 6-184.

Figure 6-180. Horizontal Start Position (HST_3_HPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-184. Horizontal Start Position (HST_3_HPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal start position of the region3 from the SRC_VPS. The region will start the "Histogram" processing from VAL'th pixel. VAL[0] can not be written.

6.3.94 HST: Horizontal Size (HST_3_HSZ)

The horizontal size 3 (HST_3_HSZ) register is shown in Figure 6-181 and described in Figure 6-181.

Figure 6-181. Horizontal Size (HST_3_HSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 6-185. Horizontal Size (HST_3_HSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal size of the region3. The "Histogram" processing of the region will process (VAL+1) pixels. VAL[0] can not be written.

6.3.95 HST: Table Select (HST_TBL)

The Table Select (HST_TBL) register is shown in Figure 6-182 and described in Table 6-186.

Figure 6-182. Table Select (HST_TBL) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	CLR	SEL
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-186. Table Select (HST_TBL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	CLR		Table Initialization When this bit is high, the table memory is cleared at VD. When high, the first line of each frame can not be sampled.
		0	disable
		1	enable
0	SEL		Output Table Select
		0	use Table 0 and 1
		1	use Table 2 and 3

6.3.96 HST: Matrix Coefficient (HST_MUL_R)

The Matrix Coefficient (HST_MUL_R) register is shown in Figure 6-183 and described in Table 6-187.

Figure 6-183. Matrix Coefficient (HST_MUL_R) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-187. Matrix Coefficient (HST_MUL_R) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Matrix Coefficient for R used for the calculation of Y sampling value (S4.4) Y=MUL_R*R+MUL_GR*Gb+MUL_GB*Gr+MUL_B*B

6.3.97 HST: Matrix Coefficient (HST_MUL_GR)

The Matrix Coefficient (HST_MUL_GR) register is shown in Figure 6-184 and described in Table 6-188.

Figure 6-184. Matrix Coefficient (HST_MUL_GR) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-188. Matrix Coefficient (HST_MUL_GR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Matrix Coefficient for Gr used for the calculation of Y sampling value (S4.4) Y=MUL_R*R+MUL_GR*Gb+MUL_GB*Gr+MUL_B*B

6.3.98 HST: Matrix Coefficient (HST_MUL_GB)

The Matrix Coefficient (HST_MUL_GB) register is shown in Figure 6-185 and described in Table 6-189.

Figure 6-185. Matrix Coefficient (HST_MUL_GB) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-189. Matrix Coefficient (HST_MUL_GB) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Matrix Coefficient for Gb used for the calculation of Y sampling value (S4.4) Y=MUL_R*R+MUL_GR*Gb+MUL_GB*Gr+MUL_B*B

6.3.99 HST: Matrix Coefficient (HST_MUL_B)

The Matrix Coefficient (HST_MUL_B) register is shown in Figure 6-186 and described in Table 6-190.

Figure 6-186. Matrix Coefficient (HST_MUL_B) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-190. Matrix Coefficient (HST_MUL_B) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Matrix Coefficient for B used for the calculation of Y sampling value (S4.4) Y=MUL_R*R+MUL_GR*Gb+MUL_GB*Gr+MUL_B*B

6.4 Resizer (RSZ) Registers

Table 6-191 lists the memory-mapped registers for the resizer registers (RSZ). See the device-specific data manual for the memory addresses of these registers.

Table 6-191. RESIZER (RSZ) Registers

Offset	Acronym	Register Description	Section
0h	SRC_EN	RSZ Enable	Section 6.4.1
004h	SRC_MODE	One Shot Mode	Section 6.4.2
008h	SRC_FMT0	Input Data Paths	Section 6.4.3
00Ch	SRC_FMT1	Source Image Format	Section 6.4.4
010h	SRC_VPS	Vertical Start Position	Section 6.4.5
014h	SRC_VSZ	Vertical Processing Size	Section 6.4.6
018h	SRC_HPS	Horizontal Start Position	Section 6.4.7
01Ch	SRC_HSZ	Horizontal Processing Size	Section 6.4.8
020h	DMA_RZA	SDRAM Request Minimum Interval for RZA	Section 6.4.9
024h	DMA_RZB	SDRAM Request Minimum Interval for RZB	Section 6.4.10
028h	DMA_STA	Status of Resizer (Reserved)	Section 6.4.11
02Ch	GCK_MMR	MMR Gated Clock Control	Section 6.4.12
030h	Reserved	Reserved	
034h	GCK_SDR	SDR Gated Clock Control	Section 6.4.13
038h	IRQ_RZA	Interval of RZA circular IRQ	Section 6.4.14
03Ch	IRQ_RZB	Interval of RZB circular IRQ	Section 6.4.15
040h	YUV_Y_MIN	Saturation (Luminance Minimum)	Section 6.4.16
044h	YUV_Y_MAX	Saturation (Luminance Maximum)	Section 6.4.17
048h	YUV_C_MIN	Saturation (Chrominance Minimum)	Section 6.4.18
04Ch	YUV_C_MAX	Saturation (Chrominance Maximum)	Section 6.4.19
050h	YUV_PHS	Chrominance Position	Section 6.4.20
054h	SEQ	Processing Mode	Section 6.4.21
058h	RZA_EN	RZA (Resizer Channel A): Enable	Section 6.4.22
05Ch	RZA_MODE	RZA: One Shot Mode	Section 6.4.23
060h	RZA_420	RZA: Output Format	Section 6.4.24
064h	RZA_I_VPS	RZA: Vertical Start Position of the Input	Section 6.4.25
068h	RZA_I_HPS	RZA: Horizontal Start Position of the Input	Section 6.4.26
06Ch	RZA_O_VSZ	RZA: Vertical Size of the Output	Section 6.4.27
070h	RZA_O_HSZ	RZA: Horizontal Size of the Output	Section 6.4.27
074h	RZA_V_PHS_Y	RZA: Initial Phase of Vertical Resizing Process for Luminance	Section 6.4.29
078h	RZA_V_PHS_C	RZA: Initial Phase of Vertical Resizing Process for Chrominance	Section 6.4.30
07Ch	RZA_V_DIF	RZA: Vertical Resize Parameter	Section 6.4.31
080h	RZA_V_TYP	RZA: Interpolation method for Vertical Rescaling	Section 6.4.32
084h	RZA_V_LPF	RZA: Vertical LPF Intensity	Section 6.4.33
088h	RZA_H_PHS	RZA: Initial Phase of Horizontal Resizing Process	Section 6.4.34
08Ch	RZA_H_PHS_ADJ	RZA: Additional Initial Phase of Vertical Resizing Process for Luminance	Section 6.4.35
090h	RZA_H_DIF	RZA: Horizontal Resize Parameter	Section 6.4.36
094h	RZA_H_TYP	RZA: Interpolation method for Horizontal Rescaling	Section 6.4.37
098h	RZA_H_LPF	RZA: Horizontal LPF Intensity	Section 6.4.38
09Ch	RZA_DWN_EN	RZA: Down Scale Mode Enable	Section 6.4.39
0A0h	RZA_DWN_AV	RZA: Down Scale Mode Averaging Size	Section 6.4.40
0A4h	RZA_RGB_EN	RZA: RGB Output Enable	Section 6.4.41
0A8h	RZA_RGB_TYP	RZA: RGB Output Bit Mode	Section 6.4.42
0ACh	RZA_RGB_BLD	RZA: YC422 to YC444 conversion method	Section 6.4.43

Table 6-191. RESIZER (RSZ) Registers (continued)

Offset	Acronym	Register Description	Section
0B0h	RZA_SDR_Y_BAD_H	RZA: SDRAM Base Address MSB	Section 6.4.44
0B4h	RZA_SDR_Y_BAD_L	RZA: SDRAM Base Address LSB	Section 6.4.45
0B8h	RZA_SDR_Y_SAD_H	RZA: SDRAM Start Address MSB	Section 6.4.46
0BCh	RZA_SDR_Y_SAD_L	RZA: SDRAM Start Address LSB	Section 6.4.47
0C0h	RZA_SDR_Y_OFT	RZA: SDRAM Line Offset	Section 6.4.48
0C4h	RZA_SDR_Y_PTR_S	RZA: Start Line of SDRAM Pointer	Section 6.4.49
0C8h	RZA_SDR_Y_PTR_E	RZA: End line of SDRAM Pointer	Section 6.4.50
0CCh	RZA_SDR_C_BAD_H	RZA: SDRAM Base Address MSB (for 420 Chroma)	Section 6.4.51
0D0h	RZA_SDR_C_BAD_L	RZA: SDRAM Base Address LSB (for 420 Chroma)	Section 6.4.52
0D4h	RZA_SDR_C_SAD_H	RZA: SDRAM Start Address MSB (for 420 Chroma)	Section 6.4.53
0D8h	RZA_SDR_C_SAD_L	RZA: SDRAM Start Address LSB (for 420 Chroma)	Section 6.4.54
0DCh	RZA_SDR_C_OFT	RZA: SDRAM Line Offset (for 420 Chroma)	Section 6.4.55
0E0h	RZA_SDR_C_PTR_S	RZA: Start Line of SDRAM Pointer (for 420 Chroma)	Section 6.4.56
0E4h	RZA_SDR_C_PTR_E	RZA: End line of SDRAM Pointer (for 420 Chroma)	Section 6.4.57
0E8h	RZB_EN	RZB (Resizer Channel B): Enable	Section 6.4.58
0ECh	RZB_MODE	RZB: One Shot Mode	Section 6.4.59
0F0h	RZB_420	RZB: Output Format	Section 6.4.60
0F4h	RZB_I_VPS	RZB: Vertical Start Position of the Input	Section 6.4.61
0F8h	RZB_I_HPS	RZB: Horizontal Start Position of the Input	Section 6.4.62
0FCh	RZB_O_VSZ	RZB: Vertical Size of the Output	Section 6.4.63
100h	RZB_O_HSZ	RZB: Horizontal Size of the Output	Section 6.4.64
104h	RZB_V_PHS_Y	RZB: Initial Phase of Vertical Resizing Process for Luminance	Section 6.4.65
108h	RZB_V_PHS_C	RZB: Initial Phase of Vertical Resizing Process for Chrominance	Section 6.4.66
10Ch	RZB_V_DIF	RZB: Vertical Resize Parameter	Section 6.4.67
110h	RZB_V_TYP	RZB: Interpolation method for Vertical Rescaling	Section 6.4.68
114h	RZB_V_LPF	RZB: Vertical LPF Intensity	Section 6.4.69
118h	RZB_H_PHS	RZB: Initial Phase of Horizontal Resizing Process	Section 6.4.70
11Ch	RZB_H_PHS_ADJ	RZB: Additional Initial Phase of Horizontal Resizing Process for Luminance	Section 6.4.71
120h	RZB_H_DIF	RZB: Horizontal Resize Parameter	Section 6.4.72
124h	RZB_H_TYP	RZB: Interpolation method for Horizontal Rescaling	Section 6.4.73
128h	RZB_H_LPF	RZB: Horizontal LPF Intensity	Section 6.4.74
12Ch	RZB_DWN_EN	RZB: Down Scale Mode Enable	Section 6.4.75
130h	RZB_DWN_AV	RZB: Down Scale Mode Averaging Size	Section 6.4.76
134h	RZB_RGB_EN	RZB: RGB Output Enable	Section 6.4.77
138h	RZB_RGB_TYP	RZB: RGB Output Bit Mode	Section 6.4.78
13Ch	RZB_RGB_BLD	RZB: YC422 to YC444 conversion method	Section 6.4.79
140h	RZB_SDR_Y_BAD_H	RZB: SDRAM Base Address MSB	Section 6.4.80
144h	RZB_SDR_Y_BAD_L	RZB: SDRAM Base Address LSB	Section 6.4.81
148h	RZB_SDR_Y_SAD_H	RZB: SDRAM Start Address MSB	Section 6.4.82
14Ch	RZB_SDR_Y_SAD_L	RZB: SDRAM Start Address LSB	Section 6.4.83
150h	RZB_SDR_Y_OFT	RZB: SDRAM Line Offset	Section 6.4.84
154h	RZB_SDR_Y_PTR_S	RZB: Start Line of SDRAM Pointer	Section 6.4.85
158h	RZB_SDR_Y_PTR_E	RZB: End line of SDRAM Pointer	Section 6.4.86
15Ch	RZB_SDR_C_BAD_H	RZB: SDRAM Base Address MSB (for 420 Chroma)	Section 6.4.87
160h	RZB_SDR_C_BAD_L	RZB: SDRAM Base Address LSB (for 420 Chroma)	Section 6.4.88
164h	RZB_SDR_C_SAD_H	RZB: SDRAM Start Address MSB (for 420 Chroma)	Section 6.4.89
168h	RZB_SDR_C_SAD_L	RZB: SDRAM Start Address LSB (for 420 Chroma)	Section 6.4.90

Table 6-191. RESIZER (RSZ) Registers (continued)

Offset	Acronym	Register Description	Section
16Ch	RZB_SDR_C_OFT	RZB: SDRAM Line Offset (for 420 Chroma)	Section 6.4.91
170h	RZB_SDR_C_PTR_S	RZB: Start Line of SDRAM Pointer (for 420 Chroma)	Section 6.4.91
174h	RZB_SDR_C_PTR_E	RZB: End line of SDRAM Pointer (for 420 Chroma)	Section 6.4.93

6.4.1 SRC_EN (SRC_EN)

The source enable (SRC_EN) register is shown in Figure 6-187 and described in Table 6-192.

Figure 6-187. SRC_EN (SRC_EN)

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-192. SRC_EN (SRC_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		RSZ Enable The start flag of the RSZ module. When EN is 1, the RSZ module starts a processing from the next rising edge of the VD. If the processing mode of the RSZ module is "one shot", the EN is cleared to 0 after the end of the processing area.
		0	disable
		1	enable

6.4.2 SRC_MODE (SRC_MODE)

The one shot mode (SRC_MODE) register is shown in Figure 6-188 and described in Table 6-193.

Figure 6-188. SRC_MODE (SRC_MODE)

31-16
Reserved
R-0

15-2	1	0
Reserved	WRT	OST
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-193. SRC_MODE (SRC_MODE) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	WRT		C_WE Mode Selection The mode selection of the ipipeif_wrt which is an input port of the IPIPE module. If WRT is 0, the IPIPE module doesn't use the ipipeif_wrt. Else the IPIPE module uses it.
		0	disable
		1	enable
0	OST		One Shot Mode The processing mode selection of the IPIPE module. Value 0 indicates the mode of "free run", value 1 indicates the mode of "one shot".
		0	disable
		1	enable

6.4.3 SRC_FMT0 (SRC_FMT0)

The SRC_FMT0 register is shown in the figure and table below.

Figure 6-189. SRC_FMT0 (SRC_FMT0)

31-16
Reserved
R-0

15-2	1	0
Reserved	BYPASS	SRC
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-194. SRC_FMT0 (SRC_FMT0) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	BYPASS		Enable Pass-through mode Enables Pass Through mode, where large raw image up to 8190 pixels per line may be processed. When enabled, all image processing is skipped. ***note*** To select BYPASS mode, following values are set. SRC_FMT1[420] = 422 RZA_EN = ENABLE RZA_420[Y] = DISABLE RZA_420[C] = DISABLE RZA_I_VPS = 0 RZA_I_HPS = 0 RZA_V_PHS_Y = 0 RZA_V_PHS_C = 0 RZA_V_DIF = 256 RZA_V_LPF[Y] = 0 RZA_V_LPF[C] = 0 RZA_H_PHS = 0 RZA_H_PHS_ADJ = 0 RZA_H_DIF = 256 RZA_H_LPF[Y] = 0 RZA_H_LPF[C] = 0 RZA_DWN_EN = DISABLE RZA_RGB_EN = DISABLE RZB_EN = DISABLE
		0	Passthrough mode off
		1	Passthrough mode on
0	SRC		Data Path through RSZ
		0	from IPIPE
		1	from IPIPEIF

6.4.4 Source Image Format1 (SRC_FMT1)

The source image format (SRC_FMT1) register is shown in Figure 6-190 and described in Table 6-195.

Figure 6-190. Source Image Format 1 (SRC_FMT1) Register

31-16
Reserved
R-0

15-3	2	1	0
Reserved	COL	420	RAW
R-00	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-195. Source Image Format 1 (SRC_FMT1) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	COL		Y/C Selection This bit is valid in 420 input mode (SRC_FMT1[420]=1)
		0	Y
		1	C
1	420		Chroma Format Selection
		0	422 image
		1	420 image
0	RAW		Pass-through mode input data format selection This bit affects the horizontal reversal (flipping) process.
		0	Flipping preserves YcbCr format
		1	Flipping preserves Raw format

6.4.5 SRC_VPS

The vertical start position register is shown and described in the figure and table below.

Figure 6-191. SRC_VPS Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-196. SRC_VPS Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	Vertical Start Position (0-65534) The vertical position of the global frame from the rising edge of the VD. The RSZ module will start an image processing from VAL'th line.

6.4.6 SRC_VSZ

The vertical processing size register is shown and described in the figure and table below.

Figure 6-192. SRC_VSZ Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-197. SRC_VSZ Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical Processing Size (0-8190) The vertical size of the processing area. The RSZ module will process (VAL+1) lines.

6.4.7 SRC_HPS

The horizontal start position register is shown and described in the figure and table below.

Figure 6-193. SRC_HPS Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-198. SRC_HPS Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	Horizontal Start Position (0-65534). The horizontal position of the global frame from the rising edge of the HD. The RSZ module will start an image processing from VAL pixel.

6.4.8 SRC_HSZ

The horizontal processing size register is shown and described in the figure and table below.

Figure 6-194. SRC_HSZ Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 6-199. SRC_HSZ Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal Processing Size (0-8189) The horizontal size of the processing area. VAL[0] can not be written. The RSZ module will process (VAL+1) pixels.

6.4.9 DMA_RZA

The SDRAM request minimum interval for RZA register is shown and described in the figure and table below.

Figure 6-195. DMA_RZA Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-200. DMA_RZA Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Minimum interval between two consecutive SDRAM requests for resize-A Specified in number of VPSS clock cycles

6.4.10 DMA_RZB

The SDRAM request minimum interval for RZB register is shown and described in the figure and table below.

Figure 6-196. DMA_RZB Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-201. DMA_RZB Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Minimum interval between two consecutive SDRAM requests for resize-B Specified in number of VPSS clock cycles.

6.4.11 DMA_STA

The status of resizer (Reserved) register is shown and described in the figure and table below.

Figure 6-197. DMA_STA Register

31-16
Reserved
R-0

15-1	0
Reserved	STATUS
R-00	R-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-202. DMA_STA Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	STATUS		Resize Process Status

6.4.12 GCK_MMR

The MMR gated clock control register is shown and described in the figure and table below.

Figure 6-198. GCK_MMR Register

31-16
Reserved
R-0

15-1	0
Reserved	REG
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-203. GCK_MMR Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	REG		RSZ MMR Clock Enable The on/off selection of the MMR interface clock (clk_mmr_g0) which is used for MMR register accesses. When this bit is off, the registers except the following may not be written. Read access is allowed. SRC_EN GCK_MMR GCK_SDR RZA_EN RZB_EN
		0	off
		1	on

6.4.13 GCK_SDR

The SDR gated clock control register is shown and described in the figure and table below.

Figure 6-199. GCK_SDR Register

31-16
Reserved
R-0

15-1	0
Reserved	CORE
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-204. GCK_SDR Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	CORE		RSZ Core Clock Enable The on/off selection of clk_vpss_g0 which is used for "Resizer Core". When this bit is off, Resizer core (interpolator) is automatically bypassed (resizer-bypass mode of pass-through mode depending on SRC_FMT0 value). In resizer-bypass mode or pass-through mode, no up-scaling or down scaling process is operated. Rescaling : GCK_SDR=1, SRC_FMT0[BYPASSS]=0 Resizer bypass : GCK_SDR=0, SRC_FMT0[BYPASSS]=0 Pass-through : GCK_SDR=0, SRC_FMT0[BYPASSS]=1
		0	off
		1	on

6.4.14 IRQ_RZA

The Interval of RZA circular IRQ register is shown and described in the figure and table below.

Figure 6-200. IRQ_RZA Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-8191

LEGEND: R = Read only; -*n* = value after reset

Table 6-205. IRQ_RZA Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Interval of RZA circular IRQ Interrupt signal at every (VAL+1) lines of Resize and RGB output

6.4.15 IRQ_RZB

The Interval of RZB circular IRQ register is shown and described in the figure and table below.

Figure 6-201. IRQ_RZB Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-8191

LEGEND: R = Read only; -*n* = value after reset

Table 6-206. IRQ_RZB Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Interval of RZB circular IRQ Interrupt signal at every (VAL+1) lines of Resize and RGB output

6.4.16 YUV_Y_MIN

The saturation (luminance minimum) register is shown and described in the figure and table below.

Figure 6-202. YUV_Y_MIN Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-207. YUV_Y_MIN Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Minimum Luminance Value In RAW data processing, this value should be 0

6.4.17 YUV_Y_MAX

The saturation (luminance maximum) register is shown and described in the figure and table below.

Figure 6-203. YUV_Y_MAX Register

31-16	
Reserved	
R-0	
15-8	7-0
Reserved	VAL
R-00	R/W-255

LEGEND: R = Read only; -*n* = value after reset

Table 6-208. YUV_Y_MAX Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Maximum Luminance Value In RAW data processing, this value should be 255

6.4.18 YUV_C_MIN

The saturation (chrominance minimum) register is shown and described in the figure and table below.

Figure 6-204. YUV_C_MIN Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-209. YUV_C_MIN Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Minimum Chrominance Value In RAW data processing, this value should be 0

6.4.19 YUV_C_MAX

The saturation (chrominance maximum) register is shown and described in the figure and table below.

Figure 6-205. YUV_C_MAX Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-00	R/W-255

LEGEND: R = Read only; -*n* = value after reset

Table 6-210. YUV_C_MAX Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Maximum Chrominance Value In RAW data processing, this value should be 255

6.4.20 YUV_PHS

The chrominance position register is shown and described in the figure and table below.

Figure 6-206. YUV_PHS Register

31-16
Reserved
R-0

15-1	0
Reserved	POS
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-211. YUV_PHS Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	POS		Phase position of the output of the Chrominance
		0	same position with Luminance
		1	the middle of the Luminance

6.4.21 Processing Mode (SEQ)

The processing Mode (SEQ) register is shown in Figure 6-207 and described in Table 6-212.

Figure 6-207. SEQ Register

31-16
Reserved
R-0

15-5	4	3	2	1	0
Reserved	CRV	VRVB	HRVB	VRVA	HRVA
R-00	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-212. SEQ Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4	CRV		Chroma sampling point change If CRV is 1, chroma sampling point is changed from odd-numbered pixels to even R-0 number pixels. The pixel the left end is removed and the pixel at the right end is duplicated. If CRV is 0, chroma sampling point is not changed.
		0	Flipping disable
		1	Flipping enable
3	VRVB		Vertical reversal of output image for RZB If VRVB is 1, the order of output data from RZB is flipped top to bottom. If VRVB is 0, processed pixels of RZB are output in the order of input (normal operation) in vertical direction.
		0	Flipping disable
		1	Flipping enable
2	HRVB		Horizontal reversal of output image for RZB If HRVB is 1, the order of output data from RZB is flipped left to right. If HRVB is 0, processed pixels of RZB are output in the order of input (normal operation) in horizontal direction.
		0	Flipping disable
		1	Flipping enable
1	VRVA		Vertical reversal of output image for RZA If VRVA is 1, the order of output data from RZA is flipped top to bottom. If VRVA is 0, processed pixels of RZA are output in the order of input (normal operation) in vertical direction.
		0	Flipping disable
		1	Flipping enable
0	HRVA		Horizontal reversal of output image for RZA If HRVA is 1, the order of output data from RZA is flipped left to right. If HRVA is 0, processed pixels of RZA are output in the order of input (normal operation) in horizontal direction.
		0	Flipping disable
		1	Flipping enable

6.4.22 RZA_EN

The RZA (=Resizer Channel A): Enable (RZA_EN) register is shown in Figure 6-208 and described in Table 6-213.

Figure 6-208. RZA_EN Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-213. RZA_EN Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Resizer Enable In one-shot mode, this bit is negated on VD. In pass-through mode, RZA_EN enables the output
		0	disable
		1	enable

6.4.23 RZA_MODE (RZA_MODE)

The one shot mode (RZA_MODE) register is shown in Figure 6-209 and described in Table 6-214.

Figure 6-209. RZA_MODE Register

31-16
Reserved
R-0

15-1	0
Reserved	OST
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-214. RZA_MODE Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	OST		One Shot Mode Enable
		0	continuous mode
		1	one shot mode

6.4.24 RZA_420 Output Format (RZA_420)

The RZA 420 output format register is shown in Figure 6-210 and described in Table 6-215.

Figure 6-210. RZA_420 (RZA_420)

31-16
Reserved
R-0

15-2	1	0
Reserved	CEN	YEN
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-215. RZA_420 Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	CEN		Output Enable for Chrominance This bit is valid in 422 input mode. When CEN=0 and YEN=0, output is 422
		0	C output disable
		1	C output enable and 422to420 conversion enabled
0	YEN		Output Enable for Luminance This bit is valid in 422 input mode. When CEN=0 and YEN=0, output is 422
		0	Y output disable
		1	Y output enable and 422to420 conversion enabled

6.4.25 RZA Vertical Start Position (RZA_I_VPS)

The RZA vertical start position of the input is shown in Figure 6-211 and described in Table 6-216.

Figure 6-211. RZA Vertical Start Position Input (RZA_I_VPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-216. RZA Vertical Start Position Input (RZA_I_VPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical start position of image processing After SRC_VPS, the VAL'th line is processed as the first line in each image.

6.4.26 RZA Horizontal Start Postion Input (RZA_I_HPS)

The RZA horizontal start position of the input is shown in Figure 6-212 and described in Table 6-217.

Figure 6-212. RZA_I_HPS Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-217. RZA Horizontal Start Postion Input (RZA_I_HPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0
12-0	VAL	0-1FFFh	Horizontal start position of image processing After SRC_HPS, the VAL'th pixel is processed as the first pixel. VAL[0] can not be written.

6.4.27 Vertical Size Output (RZA_O_VSZ)

The vertical size of the output (RZA_O_VSZ) register is shown in Figure 6-213 and described in Table 6-218.

Figure 6-213. Vertical Size Output (RZA_O_VSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-218. Vertical Size Output (RZA_O_VSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical size of the output image The number of output lines is (VAL+1).

6.4.28 RZA_O_HSZ (RZA_O_HSZ)

The horizontal size of the output register is shown in Figure 6-214 and described in Table 6-219.

Figure 6-214. Horizontal Size Output (RZA_O_HSZ)

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 6-219. Horizontal Size Output (RZA_O_HSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal size of output image The number of pixel in each line is (VAL+1). VAL[0] can not be written. RZA_O_HSZ ≤ 2176 in normal mode, RZA_O_HSZ ≤ 1088 in down scale mode

6.4.29 RZA_V_PHS_Y (RZA_V_PHS_Y)

The RZA initial phase of vertical resizing process for luminance register is shown in Figure 6-215and described in Table 6-220.

Figure 6-215. RZA Vertical Resizing Process (RZA_V_PHS_Y) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-220. RZA Vertical Resizing Process (RZA_V_PHS_Y) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Initial value for the phase value in vertical resizing process for Luminance (0-10000) Usually this values is zero except in Frame Division Operation - V.

6.4.30 RZA_V_PHS_C

RZA: Initial Phase of Vertical Resizing Process for Chrominance (RZA_V_PHS_C) register is shown in Figure 6-216 and described in Table 6-221.

Figure 6-216. RZA_V_PHS_C Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-221. RZA_V_PHS_C Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Initial value for the phase value in vertical resizing process for Chrominance (0-10000) Usually this values is zero except in Frame Division Operation - V.

6.4.31 RZA Vertical Resize Parameter(RZA_V_DIF)

RZA vertical resize parameter (RZA_V_DIF) register is shown in Figure 6-217 and described in RSZ_RZA_V_DIF_tbl.

Figure 6-217. RZA Vertical Size Parameter (RZA_V_DIF) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-00	R/W-256

LEGEND: R = Read only; -*n* = value after reset

Table 6-222. RZA Vertical Size Parameter (RZA_V_DIF) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Vertical Resize Parameter The actual resizing ratio is 256/VAL. ***note*** 16 ≤ VAL ≤ 4096 : Normal Mode, 256 ≤ VAL ≤ 4096 : Down Scale Mode

6.4.32 RZA_V_TYP

The RZA: Interpolation method for Vertical Rescaling (RZA_V_TYP) register is shown in Figure 6-218 and described in Table 6-223.

Figure 6-218. RZA_V_TYP Register

31-16
Reserved
R-0

15-2	1	0
Reserved	C	Y
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-223. RZA_V_TYP Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	C		Selection of resizing method for Chrominance in vertical direction
		0	4-tap cubic convolution
		1	2-tap linear interpolation
0	Y		Selection of resizing method for Luminance in vertical direction
		0	4-tap cubic convolution
		1	2-tap linear interpolation

6.4.33 RZA_V_LPF

The RZA: Vertical LPF Intensity (RZA_V_LPF) register is shown in Figure 6-219and described in Table 6-224.

Figure 6-219. RZA_V_LPF Register

31-16
Reserved
R-0

15-12	11-6	5-0
Reserved	C	Y
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-224. RZA_V_LPF Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-6	C	0-3Fh	Vertical LPF Intensity for Chrominance (0-32)
5-0	Y	0-3Fh	Vertical LPF Intensity for Luminance (0-32)

6.4.34 RZA_H_PHS

The RZA_H_PHS register is shown in Figure 6-220 and described in Table 6-225.

Figure 6-220. RZA_H_PHS Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-225. RZA_H_PHS Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Initial value for the phase value in horizontal resizing process (0-8704) Should be set to zero except in Frame Division Mode-H.

6.4.35 RZA_H_PHS_ADJ

The RZA_H_PHS_ADJ register is shown in Figure 6-221 and described in Table 6-226.

Figure 6-221. RZA_H_PHS_ADJ Register

31-16
Reserved
R-0

15-9	8-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-226. RZA_H_PHS_ADJ Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Any writes to these bit(s) must always have a value of 0.
8-0	VAL	0-1FFh	Additional Initial Phase of Horizontal Resizing Process for Luminance This value is added to Horizontal Y phase

6.4.36 RZA_H_DIF

The RZA_H_DIF register is shown in Figure 6-222 and described in Table 6-227.

Figure 6-222. RZA_H_DIF Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-00	R/W-256

LEGEND: R = Read only; -*n* = value after reset

Table 6-227. RZA_H_DIF Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Horizontal Resize Parameter The actual resizing ratio is 256/VAL. ***note*** 16 ≤ VAL ≤ 4096 : Normal Mode, 256 ≤ VAL ≤ 4096 : Down Scale Mode

6.4.37 RZA_H_TYP

The: interpolation method for horizontal rescaling (RZA_H_TYP) register is shown in Figure 6-223 and described in Table 6-228.

Figure 6-223. RZA_H_TYP Register

31-16
Reserved

15-2	1	0
Reserved	C	Y
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-228. RZA_H_TYP Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	C		Selection of resizing method for Chrominance in horizontal direction
		0	4-tap cubic convolution
		1	2-tap linear interpolation
0	Y		Selection of resizing method for Luminance in horizontal direction
		0	4-tap cubic convolution
		1	2-tap linear interpolation

6.4.38 RZA_H_LPF

The RZA: Horizontal LPF Intensity. The RZA_H_LPF register is shown in Figure 6-224 and described in Table 6-229.

Figure 6-224. RZA_H_LPF Register

31-16		
Reserved		
R-0		
15-12	11-6	5-0
Reserved	C	Y
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-229. RZA_H_LPF Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-6	C	0-3Fh	Horizontal LPF Intensity for Chrominance (0-32)
5-0	Y	0-3Fh	Horizontal LPF Intensity for Luminance (0-32)

6.4.39 RZA_DWN_EN

The RZA: Down Scale Mode Enable. The RZA_DWN_EN register is shown in Figure 6-225 and described in Table 6-230.

Figure 6-225. RZA_DWN_EN Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-230. RZA_DWN_EN Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Down Scale Mode Enable
		0	down scale mode off
		1	down scale mode on

6.4.40 RZA_DWN_AV

RZA: Down Scale Mode Averaging Size. The RZA_DWN_AV register is shown in Figure 6-226 and described in Table 6-231.

Figure 6-226. RZA_DWN_AV Register

31-16
Reserved
R-0

15-6	5-3	2-0
Reserved	V	H
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-231. RZA_DWN_AV Field Descriptions

Bit	Field	Value	Description
31-6	Reserved	0	Any writes to these bit(s) must always have a value of 0.
5-3	V		Down Scale Mode Averaging Size in vertical direction
		0	1/2 down scale
		1	1/4 down scale
		2	1/8 down scale
		3	1/16 down scale
		4	1/32 down scale
		5	1/64 down scale
		6	1/128 down scale
		7	1/256 down scale
2-0	H		Down Scale Mode Averaging Size in horizontal direction
		0	1/2 down scale
		1	1/4 down scale
		2	1/8 down scale
		3	1/16 down scale
		4	1/32 down scale
		5	1/64 down scale
		6	1/128 down scale
		7	1/256 down scale

6.4.41 RZA_RGB_EN

The RZA: RGB Output Enable (RZA_RGB_EN) register is shown in Figure 6-227 and described in Table 6-232.

Figure 6-227. RZA_RGB_EN Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-232. RZA_RGB_EN Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		RGB Output Enable
		0	YCbCr output
		1	RGB output

6.4.42 RZA_RGB_TYP

The RZA: RGB Output Bit Mode (RZA_RGB_TYP) register is shown in Figure 6-228 and described in Table 6-233.

Figure 6-228. RZA_RGB_TYP Register

31-16
Reserved
R-0

15-3	2	1	0
Reserved	MSK1	MSK0	TYP
R-00	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-233. RZA_RGB_TYP Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	MSK1		Enable masking of the last 2 pixels This bit is used to mask the 2 pixels at the boundary which are affected by 422 to 444 conversion
		0	output the last 2 pixels
		1	mask the last 2 pixels (do not output)
1	MSK0		Enable masking of the first 2 pixels This bit is used to mask the 2 pixels at the boundary which are affected by 422 to 444 conversion
		0	output the first 2 pixels
		1	mask the first 2 pixels (do not output)
0	TYP		16bit/32bit output selection
		0	32 bit output; alpha + R + G + B (8 bit each)
		1	16 bit output; R(5bit) + G(6bit) + B(5bit)

6.4.43 RZA_RGB_BLD

The RZA_RGB_BLD register is shown in Figure 6-229 and described in Table 6-234.

Figure 6-229. RZA_RGB_BLD Register

31-16	
Reserved	
R-0	
15-8	7-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-234. RZA_RGB_BLD Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	The alpha value used in 32-bit output mode

6.4.44 RZA_SDR_Y_BAD_H

The RZA: SDRAM Base Address MSB (RZA_SDR_Y_BAD_H) register is shown in Figure 6-230 and described in Table 6-235.

Figure 6-230. RZA_SDR_Y_BAD_H Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-235. RZA_SDR_Y_BAD_H Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Base Address The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.4.45 RZA_SDR_Y_BAD_L

The RZA: SDRAM Base Address LSB (RZA_SDR_Y_BAD_L) register is shown in Figure 6-231 and described in Table 6-236.

Figure 6-231. RZA_SDR_Y_BAD_L Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-236. RZA_SDR_Y_BAD_L Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Base Address The lower 16 bits of the first address in the allowed memory space in SDRAM. In Resize mode, the lowest 2 bits should be "00" when horizontal reversal mode is off (SEQ[HRV] = NOFLIP). These 2 bits should be "11" when horizontal reversal mode is on (SEQ[HRV] = FLIP). In RGB-32 bit output mode, the lowest 3 bits must be "000"

6.4.46 RZA_SDR_Y_SAD_H

The RZA: SDRAM Start Address MSB (RZA_SDR_Y_SAD_H) register is shown in Figure 6-232 and described in Table 6-237.

Figure 6-232. RZA_SDR_Y_SAD_H Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-237. RZA_SDR_Y_SAD_H Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Start Address The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.4.47 RZA_SDR_Y_SAD_L

The RZA: SDRAM Start Address LSB (RZA_SDR_Y_SAD_L) register is shown in Figure 6-233 and described in Table 6-238.

Figure 6-233. RZA_SDR_Y_SAD_L Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-238. RZA_SDR_Y_SAD_L Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Start Address The lower 16 bits of the first address in the allowed memory space in SDRAM. In Resize mode, the lowest 2 bits should be "00" when horizontal reversal mode is off (SEQ[HRV] = NOFLIP). These 2 bits should be "11" when horizontal reversal mode is on (SEQ[HRV] = FLIP). In RGB-32 bit output mode, the lowest 3 bits must be "000"

6.4.48 RZA_SDR_Y_OFT

The RZA: SDRAM Line Offset (RZA_SDR_Y_OFT) register is shown in Figure 6-234 and described in Table 6-239.

Figure 6-234. RZA_SDR_Y_OFT Register

31-16
Reserved
R-0

15-0
OFT
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-239. RZA_SDR_Y_OFT Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	OFT	0-FFFFh	The size of the memory space for each line (in bytes) The first address of each output line should be SAD+(line+OFT). Example: line 0: address = SAD + (0*OFT) line 1: address = SAD + (1*OFT) line 2: address = SAD + (2*OFT) line 3: address = SAD + (3*OFT) This register value is neglected in RGB output mode. The lower 5 bits are held low, so this value should be a multiple of 32 bytes.

6.4.49 RZA_SDR_Y_PTR_S

The RZA: Start Line of SDRAM Pointer (RZA_SDR_Y_PTR_S) register is shown in Figure 6-235 and described in Table 6-240.

Figure 6-235. RZA_SDR_Y_PTR_S Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-240. RZA_SDR_Y_PTR_S Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	The vertical position of the first output line in the output memory space. This value should be 0, when SAD=BAD In RGB output mode, this value should be multiple of 4 (the lowest two bits be "00").

6.4.50 RZA_SDR_Y_PTR_E

The RZA: End line of SDRAM Pointer (RZA_SDR_Y_PTR_E) register is shown in Figure 6-236 and described in Table 6-241.

Figure 6-236. RZA_SDR_Y_PTR_E Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-8191

LEGEND: R = Read only; -*n* = value after reset

Table 6-241. RZA_SDR_Y_PTR_E Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	SDRAM Available Capacity: The maximum number of lines to be stored in the memory space in Buffer Memory or DRAM. When the number output lines exceeds this value, the address restarts from the first address in the memory space. Example: VAL=0x0003h line 0: address = SAD + (0*OFT) line 1: address = SAD + (1*OFT) line 2: address = SAD + (2*OFT) line 3: address = SAD + (3*OFT) line 4: address = SAD + (0*OFT) ≤ (Returned to the first address) line 5: address = SAD + (1*OFT) line 6: address = SAD + (2*OFT) line 7: address = SAD + (3*OFT) line 8: address = SAD + (0*OFT) ≤ (Returned to the first address) line 9: address = SAD + (1*OFT) line 10: address = SAD + (2*OFT) line 11: address = SAD + (3*OFT) In RGB output mode, this value should be multiple of 4 (the lowest two bits be "00") to ensure that the end of SDRAM region is aligned with line size.

6.4.51 RZA_SDR_C_BAD_H (RZA_SDR_C_BAD_H)

The RZA: SDRAM Base Address MSB (RZA_SDR_C_BAD_H) register is shown in Figure 6-237 and described in Table 6-242.

Figure 6-237. RZA_SDR_C_BAD_H (RZA_SDR_C_BAD_H)

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-242. RZA_SDR_C_BAD_H Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Base Address The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.4.52 RZA_SDR_C_BAD_L

The RZA: SDRAM Base Address LSB (for 420 Chroma) (RZA_SDR_C_BAD_L) register is shown in Figure 6-238 and described in Table 6-243.

Figure 6-238. RZA_SDR_C_BAD_L Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-243. RZA_SDR_C_BAD_L Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Base Address The lower 16 bits of the first address in the allowed memory space in SDRAM. In Resize mode, the lowest 2 bits should be "00" when horizontal reversal mode is off (SEQ[HRV] = NOFLIP). These 2 bits should be "11" when horizontal reversal mode is on (SEQ[HRV] = FLIP). In RGB-32bit output mode, the lowest 3 bits must be "000"

6.4.53 RZA_SDR_C_SAD_H

The RZA: SDRAM Start Address MSB (for 420 Chroma) (RZA_SDR_C_SAD_H) register is shown in Figure 6-239 and described in Table 6-244.

Figure 6-239. RZA_SDR_C_SAD_H Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-244. RZA_SDR_C_SAD_H Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Start Address The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.4.54 RZA_SDR_C_SAD_L

The RZA: SDRAM Start Address LSB (for 420 Chroma) (RZA_SDR_C_SAD_L) register is shown in Figure 6-240 and described in Table 6-245.

Figure 6-240. RZA_SDR_C_SAD_L Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-245. RZA_SDR_C_SAD_L Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Start Address The lower 16 bits of the first address in the allowed memory space in SDRAM. In Resize mode, the lowest 2 bits should be "00" when horizontal reversal mode is off (SEQ[HRV] = NOFLIP). These 2 bits should be "11" when horizontal reversal mode is on (SEQ[HRV] = FLIP). In RGB-32bit output mode, the lowest 3 bits must be "000"

6.4.55 RZA_SDR_C_OFT

The RZA: SDRAM Line Offset (for 420 Chroma) (RZA_SDR_C_OFT) register is shown in Figure 6-241 and described in Table 6-246.

Figure 6-241. RZA_SDR_C_OFT Register

31-16
Reserved
R-0

15-0
OFT
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-246. RZA_SDR_C_OFT Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	OFT	0-FFFFh	The size of the memory space for each line (in bytes) The first address of each output line should be SAD+(line+OFT). Example: line 0: address = SAD + (0*OFT) line 1: address = SAD + (1*OFT) line 2: address = SAD + (2*OFT) line 3: address = SAD + (3*OFT) This register value is neglected in RGB output mode. The lower 5 bits are held low, so this value should be a multiple of 32 bytes.

6.4.56 RZA_SDR_C_PTR_S

RZA: Start Line of SDRAM Pointer (for 420 Chroma). The RZA_SDR_C_PTR_S register is shown in Figure 6-242 and described in Table 6-247.

Figure 6-242. RZA_SDR_C_PTR_S Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-247. RZA_SDR_C_PTR_S Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	The vertical position of the first output line in the output memory space. This value should be 0, when SAD=BAD In RGB output mode, this value should be multiple of 4 (the lowest two bits be "00").

6.4.57 RZA_SDR_C_PTR_E

The RZA: End line of SDRAM Pointer (RZA_SDR_C_PTR_E) register is shown in Figure 6-243 and described in Table 6-248.

Figure 6-243. RZA_SDR_C_PTR_E Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-8191

LEGEND: R = Read only; -*n* = value after reset

Table 6-248. RZA_SDR_C_PTR_E Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	SDRAM Available Capacity: The maximum number of lines to be stored in the memory space in Buffer Memory or DRAM. When the number output lines exceeds this value, the address restarts from the first address in the memory space. Example: VAL=0x0003h line 0: address = SAD + (0*OFT) line 1: address = SAD + (1*OFT) line 2: address = SAD + (2*OFT) line 3: address = SAD + (3*OFT) line 4: address = SAD + (0*OFT) ≤ (Returned to the first address) line 5: address = SAD + (1*OFT) line 6: address = SAD + (2*OFT) line 7: address = SAD + (3*OFT) line 8: address = SAD + (0*OFT) ≤ (Returned to the first address) line 9: address = SAD + (1*OFT) line 10: address = SAD + (2*OFT) line 11: address = SAD + (3*OFT) In RGB output mode, this value should be multiple of 4 (the lowest two bits be "00") to ensure that the end of SDRAM region is aligned with line size.

6.4.58 Resizer Channel B Enable (RZB_EN)

The resizer channel B enable register (RZB_EN) is shown in Figure 6-244 and described in Table 6-249.

Figure 6-244. Resizer Channel B Enable (RZB_EN) Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-249. Resizer Channel B Enable (RZB_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Resizer Enable In one-shot mode, this bit is negated on VD.
		0	disable
		1	enable

6.4.59 RZB_MODE

The RZB: One Shot Mode (RZB_MODE) register is shown in Figure 6-245 and described in Table 6-250.

Figure 6-245. RZB_MODE Register

31-16
Reserved
R-0

15-1	0
Reserved	OST
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-250. RZB_MODE Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	OST		One Shot Mode Enable
		0	continuous mode
		1	one shot mode

6.4.60 RZB_420 Output

The RZB_420 output register is shown in Figure 6-246 and described in Table 6-251.

Figure 6-246. RZB_420 Register

31-16
Reserved
R-0

15-2	1	0
Reserved	CEN	YEN
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-251. RZB_420 Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	CEN		Output Enable for Chrominance This bit is valid in 422 input mode. When CEN=0 and YEN=0, output is 422
		0	C output disable
		1	C output enable and 422 to 420 conversion enabled
0	YEN		Output Enable for Luminance This bit is valid in 422 input mode. When CEN=0 and YEN=0, output is 422
		0	Y output disable
		1	Y output enable and 422 to 420 conversion enabled

6.4.61 Vertical Start Position of the Input (RZB_I_VPS)

The vertical start position of the input (RZB_I_VPS) register is shown in Figure 6-247 and described in Table 6-252.

Figure 6-247. Vertical Start Position of Input (RZB_I_VPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-252. Vertical Start Position of Input (RZB_I_VPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical start position of image processing After SRC_VPS, the VAL'th line is processed as the first line in each image.

6.4.62 Horizontal Start Position of the Input (RZB_I_HPS)

The horizontal start position of the input (RZB_I_HPS) register is shown in Figure 6-248 and described in Table 6-253.

Figure 6-248. Horizontal Start Position of the Input (RZB_I_HPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-253. Horizontal Start Position of the Input (RZB_I_HPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal start position of image processing After SRC_HPS, the VAL'th pixel is processed as the first pixel. VAL[0] can not be written.

6.4.63 Vertical Size of the Output (RZB_O_VSZ)

The Vertical Size of the Output (RZB_O_VSZ) register is shown in Figure 6-249 and described in Table 6-254.

Figure 6-249. Vertical Size of the Output (RZB_O_VSZ)

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-254. Vertical Size of the Output RZB_O_VSZ Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical size of the output image The number of output lines is (VAL+1).

6.4.64 Horizontal Size of Output (RZB_O_HSZ)

The horizontal size of the output (RZB_O_HSZ) register is shown in Figure 6-250 and described in Table 6-255.

Figure 6-250. Horizontal Size of Output (RZB_O_HSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 6-255. Horizontal Size of Output (RZB_O_HSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal size of output image The number of pixels in each line is (VAL+1). VAL[0] can not be written. RZB_O_HSZ ≤ 1088 in normal mode RZB_O_HSZ ≤ 544 in down scale mode

6.4.65 Vertical Resizing Process for Luminance (RZB_V_PHS_Y)

The initial phase of vertical resizing process for luminance (RZB_V_PHS_Y) register is shown in Figure 6-251 and described in Table 6-256.

Figure 6-251. Vertical Resizing Process for Luminance (RZB_V_PHS_Y)

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-256. Vertical Resizing Process for Luminance (RZB_V_PHS_Y) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Initial value for the phase value in vertical resizing process for Luminance (0-10000) Usually, this value is zero except in Frame Division Mode - V.

6.4.66 Vertical Resizing Process for Chrominance (RZB_V_PHS_C)

The initial phase of vertical resizing process for chrominance (RZB_V_PHS_C) register is shown in Figure 6-252and described in Table 6-257.

Figure 6-252. Vertical Resizing Process for Chrominance (RZB_V_PHS_C) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-257. Vertical Resizing Process for Chrominance (RZB_V_PHS_C) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Initial value for the phase value in vertical resizing process for Chrominance (0-10000) Usually this values is zero except in Frame Division Operation - V.

6.4.67 Vertical Resize Parameter (RZB_V_DIF)

The Vertical Resize Parameter (RZB_V_DIF) register is shown in Figure 6-253and described in Table 6-258.

Figure 6-253. Vertical Resize Parameter (RZB_V_DIF) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-00	R/W-256

LEGEND: R = Read only; -*n* = value after reset

Table 6-258. Vertical Resize Parameter (RZB_V_DIF) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Vertical Resize Parameter The actual resizing ratio is 256/VAL. ***note*** 16 ≤ VAL ≤ 4096 : Normal Mode, 256 ≤ VAL ≤ 4096 : Down Scale Mode

6.4.68 Vertical Rescaling Interpolation (RZB_V_TYP)

The vertical rescaling interpolation method register is shown in Figure 6-254 and described in Table 6-259.

Figure 6-254. Vertical Rescaling Interpolation (RZB_V_TYP)

31-16
Reserved
R-0

15-2	1	0
Reserved	C	Y
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-259. Vertical Rescaling Interpolation (RZB_V_TYP) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	C		Selection of resizing method for Chrominance in vertical direction
		0	4-tap cubic convolution
		1	2-tap linear interpolation
0	Y		Selection of resizing method for Luminance in vertical direction
		0	4-tap cubic convolution
		1	2-tap linear interpolation

6.4.69 Vertical LPF Intensity (RZB_V_LPF)

The vertical LPF intensity (RZB_V_LPF) register is shown in Figure 6-255 and described in Table 6-260.

Figure 6-255. Vertical LPF Intensity (RZB_V_LPF) Register

31-16
Reserved
R-0

15-12	11-6	5-0
Reserved	C	Y
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-260. Vertical LPF Intensity (RZB_V_LPF) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-6	C	0-3Fh	Vertical LPF Intensity for Chrominance (0-32)
5-0	Y	0-3Fh	Vertical LPF Intensity for Luminance (0-32)

6.4.70 Initial Phase of Horizontal Resizing Process (RZB_H_PHS)

The initial phase of horizontal resizing process (RZB_H_PHS) register is shown in Figure 6-256and described in Table 6-261.

Figure 6-256. Horizontal Resizing Process (RZB_H_PHS) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-261. Horizontal Resizing Process (RZB_H_PHS) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Initial value for the phase value in horizontal resizing process (0-8704) Should be set to zero except in Frame Division Mode-H.

6.4.71 Horizontal Resizing Process for Luminance (RZB_H_PHS_ADJ)

The additional initial phase of Horizontal resizing process for luminance (RZB_H_PHS_ADJ) register is shown in Section 6.4.71 and described in Table 6-262.

Figure 6-257. Horizontal Resizing Process for Luminance (RZB_H_PHS_ADJ) Register

31-16
Reserved
R-0

15-9	8-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-262. Horizontal Resizing Process for Luminance (RZB_H_PHS_ADJ) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
8-0	VAL	0-1FFh	Additional Initial Phase of Horizontal Resizing Process for Luminance This value is added to Horizontal Y phase

6.4.72 Horizontal Resize Parameter (RZB_H_DIF)

The horizontal resize parameter (RZB_H_DIF) register is shown in Figure 6-258 and described in Table 6-263.

Figure 6-258. Horizontal Resize Parameter (RZB_H_DIF) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-00	R/W-256

LEGEND: R = Read only; -*n* = value after reset

Table 6-263. Horizontal Resize Parameter (RZB_H_DIF) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Horizontal Resize Parameter The actual resizing ratio is 256/VAL. ***note*** 16 ≤ VAL ≤ 4096 : Normal Mode, 256 ≤ VAL ≤ 4096 : Down Scale Mode

6.4.73 Interpolation Method for Horizontal Rescaling (RZB_H_TYP)

The interpolation method for horizontal rescaling (RZB_H_TYP) register is shown in Figure 6-259 and described in Table 6-264.

Figure 6-259. Horizontal Rescaling (RZB_H_TYP) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	C	Y
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-264. Horizontal Rescaling (RZB_H_TYP) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	C		Selection of resizing method for Chrominance in horizontal direction
		0	4-tap cubic convolution
		1	2-tap linear interpolation
0	Y		Selection of resizing method for Luminance in horizontal direction
		0	4-tap cubic convolution
		1	2-tap linear interpolation

6.4.74 Horizontal LPF Intensity (RZB_H_LPF)

The horizontal LPF intensity (RZB_H_LPF) register is shown in Figure 6-260 and described in Table 6-265.

Figure 6-260. Horizontal LPF Intensity (RZB_H_LPF) Register

31-16
Reserved
R-0

15-12	11-6	5-0
Reserved	C	Y
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-265. Horizontal LPF Intensity (RZB_H_LPF) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-6	C	0-3Fh	Horizontal LPF Intensity for Chrominance (0-32)
5-0	Y	0-3Fh	Horizontal LPF Intensity for Luminance (0-32)

6.4.75 Down Scale Mode Enable (RZB_DWN_EN)

The down scale mode enable (RZB_DWN_EN) register is shown in Figure 6-261 and described in Table 6-266.

Figure 6-261. Down Scale Mode Enable (RZB_DWN_EN) Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-266. Down Scale Mode Enable (RZB_DWN_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved		Any writes to these bit(s) must always have a value of 0.
0	EN		Down Scale Mode Enable
		0	down scale mode off
		1	down scale mode on

6.4.76 Down Scale Mode Averaging Size (RZB_DWN_AV)

The Down Scale Mode Averaging Size (RZB_DWN_AV) register is shown in Figure 6-262 and described in Table 6-267.

Figure 6-262. Down Scale Mode Averaging Size (RZB_DWN_AV) Register

31-16
Reserved
R-0

15-6	5-3	2-0
Reserved	V	H
R-00	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-267. Down Scale Mode Averaging Size (RZB_DWN_AV) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved	0	Any writes to these bit(s) must always have a value of 0.
5-3	V		Down Scale Mode Averaging Size in Horizontal direction If RZB_DWN_AV[H]=0, RZB_DWN_AV[V] must be either 0, 1, or 2.
		0	1/2 down scale
		1	1/4 down scale
		2	1/8 down scale
		3	1/16 down scale
		4	1/32 down scale
		5	1/64 down scale
		6	1/128 down scale
		7	1/256 down scale
2-0	H		Down Scale Mode Averaging Size in horizontal direction
		0	1/2 down scale
		1	1/4 down scale
		2	1/8 down scale
		3	1/16 down scale
		4	1/32 down scale
		5	1/64 down scale
		6	1/128 down scale
		7	1/256 down scale

6.4.77 RGB Output Enable (RZB_RGB_EN)

The RGB output enable (RZB_RGB_EN) register is shown in Figure 6-263 and described in Table 6-268.

Figure 6-263. RGB Output Enable (RZB_RGB_EN) Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-268. RGB Output Enable (RZB_RGB_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		RGB Output Enable
		0	YCbCr output
		1	RGB output

6.4.78 RZB_RGB_TYP

The RZB: RGB Output Bit Mode (RZB_RGB_TYP) register is shown in Figure 6-264 and described in Table 6-269.

Figure 6-264. RZB_RGB_TYP Register

31-16
Reserved
R-0

15-3	2	1	0
Reserved	MSK1	MSK0	TYP
R-00	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-269. RZB_RGB_TYP Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	MSK1		Enable masking of the last 2 pixels This bit is used to mask the 2 pixels at the boundary which are affected by 422 to 444 conversion
		0	output the last 2 pixels
		1	mask the last 2 pixels (do not output)
1	MSK0		Enable masking of the first 2 pixels This bit is used to mask the 2 pixels at the boundary which are affected by 422 to 444 conversion
		0	output the first 2 pixels
		1	mask the first 2 pixels (do not output)
0	TYP		16bit/32bit output selection
		0	32 bit output; alpha + R + G + B (8 bit each)
		1	16 bit output; R(5bit) + G(6bit) + B(5bit)

6.4.79 RZB_RGB_BLD

The RZB_RGB_BLD register is shown in Figure 6-265 and described in Table 6-270.

Figure 6-265. RZB_RGB_BLD Register

31-16	
Reserved	
R-0	
15-8	7-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-270. RZB_RGB_BLD Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	The alpha value used in 32-bit output mode

6.4.80 RZB_SDR_Y_BAD_H

The RZB: SDRAM Base Address MSB (RZB_SDR_Y_BAD_H) register is shown in Figure 6-266 and described in Table 6-271.

Figure 6-266. RZB_SDR_Y_BAD_H Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-271. RZB_SDR_Y_BAD_H Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Base Address The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.4.81 RZB_SDR_Y_BAD_L

The RZB: SDRAM Base Address LSB (RZB_SDR_Y_BAD_L) register is shown in Figure 6-267 and described in Table 6-272.

Figure 6-267. RZB_SDR_Y_BAD_L Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-272. RZB_SDR_Y_BAD_L Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Base Address The lower 16 bits of the first address in the allowed memory space in SDRAM. In Resize mode, the lowest 2 bits should be "00" when horizontal reversal mode is off (SEQ[HRV] = NOFLIP). These 2 bits should be "11" when horizontal reversal mode is on (SEQ[HRV] = FLIP). In RGB-32 bit output mode, the lowest 3 bits must be "000"

6.4.82 RZB_SDR_Y_SAD_H

The RZB: SDRAM Start Address MSB (RZB_SDR_Y_SAD_H) register is shown in Figure 6-268 and described in Table 6-273.

Figure 6-268. RZB_SDR_Y_SAD_H Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-273. RZB_SDR_Y_SAD_H Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Start Address The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.4.83 RZB_SDR_Y_SAD_L (RZB_SDR_Y_SAD_L)

The RZB: SDRAM Start Address LSB (RZB_SDR_Y_SAD_L) register is shown in Figure 6-269 and described in Table 6-274.

Figure 6-269. RZB_SDR_Y_SAD_L Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-274. RZB_SDR_Y_SAD_L Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Start Address The lower 16 bits of the first address in the allowed memory space in SDRAM. In Resize mode, the lowest 2 bits should be "00" when horizontal reversal mode is off (SEQ[HRV] = NOFLIP). These 2 bits should be "11" when horizontal reversal mode is on (SEQ[HRV] = FLIP). In RGB-32 bit output mode, the lowest 3 bits must be "000"

6.4.84 RZB_SDR_Y_OFT

The RZB: SDRAM Line Offset register is shown in Figure 6-270 and described in Table 6-275.

Figure 6-270. RZB_SDR_Y_OFT

31-16
Reserved
R-0

15-0
OFT
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-275. RZB_SDR_Y_OFT Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	OFT	0-FFFFh	The size of the memory space for each line (in bytes) The first address of each output line should be SAD+(line+OFT). Example: line 0: address = SAD + (0*OFT) line 1: address = SAD + (1*OFT) line 2: address = SAD + (2*OFT) line 3: address = SAD + (3*OFT) This register value is neglected in RGB output mode. The lower 5 bits are held low, so this value should be a multiple of 32 bytes.

6.4.85 RZB_SDR_Y_PTR_S

The RZB: Start Line of SDRAM Pointer (RZB_SDR_Y_PTR_S) register is shown in Figure 6-271 and described in Table 6-276.

Figure 6-271. RZB_SDR_Y_PTR_S Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-276. RZB_SDR_Y_PTR_S Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	The vertical position of the first output line in the output memory space. This value should be 0, when SAD=BAD In RGB output mode, this value should be multiple of 4 (the lowest two bits be "00").

6.4.86 RZB_SDR_Y_PTR_E

The RZB: End line of SDRAM Pointer (RZB_SDR_Y_PTR_E) register is shown in Figure 6-272 and described in Table 6-277.

Figure 6-272. RZB_SDR_Y_PTR_E Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-8191

LEGEND: R = Read only; -*n* = value after reset

Table 6-277. RZB_SDR_Y_PTR_E Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	SDRAM Available Capacity: The maximum number of lines to be stored in the memory space in Buffer Memory or DRAM. When the number output lines exceeds this value, the address restarts from the first address in the memory space. Example: VAL=0x0003h line 0: address = SAD + (0*OFT) line 1: address = SAD + (1*OFT) line 2: address = SAD + (2*OFT) line 3: address = SAD + (3*OFT) line 4: address = SAD + (0*OFT) ≤ (Returned to the first address) line 5: address = SAD + (1*OFT) line 6: address = SAD + (2*OFT) line 7: address = SAD + (3*OFT) line 8: address = SAD + (0*OFT) ≤ (Returned to the first address) line 9: address = SAD + (1*OFT) line 10: address = SAD + (2*OFT) line 11: address = SAD + (3*OFT) In RGB output mode, this value should be multiple of 4 (the lowest two bits be "00") to ensure that the end of SDRAM region is aligned with line size.

6.4.87 RZB_SDR_C_BAD_H

The RZB: SDRAM Base Address MSB (RZB_SDR_C_BAD_H) register is shown in Figure 6-273 and described in Table 6-278.

Figure 6-273. RZB_SDR_C_BAD_H Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-278. RZB_SDR_C_BAD_H Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Base Address The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.4.88 RZB_SDR_C_BAD_L

The RZB: SDRAM Base Address LSB (RZB_SDR_C_BAD_L) register is shown in Figure 6-274 and described in Table 6-279.

Figure 6-274. RZB_SDR_C_BAD_L Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-279. RZB_SDR_C_BAD_L Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Base Address The lower 16 bits of the first address in the allowed memory space in SDRAM. In Resize mode, the lowest 2 bits should be "00" when horizontal reversal mode is off (SEQ[HRV] = NOFLIP). These 2 bits should be "11" when horizontal reversal mode is on (SEQ[HRV] = FLIP). In RGB-32bit output mode, the lowest 3 bits must be "000"

6.4.89 RZB_SDR_C_SAD_H

The RZB: SDRAM Start Address MSB (RZB_SDR_C_SAD_H) register is shown in Figure 6-275 and described in Table 6-280.

Figure 6-275. RZB_SDR_C_SAD_H Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-280. RZB_SDR_C_SAD_H Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Start Address The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.4.90 RZB_SDR_C_SAD_L

The RZB: SDRAM Start Address LSB (RZB_SDR_C_SAD_L) register is shown in Figure 6-276 and described in Table 6-281.

Figure 6-276. RZB_SDR_C_SAD_L Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-281. RZB_SDR_C_SAD_L Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Start Address The lower 16 bits of the first address in the allowed memory space in SDRAM. In Resize mode, the lowest 2 bits should be "00" when horizontal reversal mode is off (SEQ[HRV] = NOFLIP). These 2 bits should be "11" when horizontal reversal mode is on (SEQ[HRV] = FLIP). In RGB-32bit output mode, the lowest 3 bits must be "000"

6.4.91 RZB_SDR_C_OFT

The RZB: SDRAM Line Offset (RZB_SDR_C_OFT) register is shown in Figure 6-277 and described in Table 6-282.

Figure 6-277. RZB_SDR_C_OFT Register

31-16
Reserved
R-0

15-0
OFT
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-282. RZB_SDR_C_OFT Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	OFT	0-FFFFh	The size of the memory space for each line (in bytes) The first address of each output line should be SAD+(line+OFT). Example: line 0: address = SAD + (0*OFT) line 1: address = SAD + (1*OFT) line 2: address = SAD + (2*OFT) line 3: address = SAD + (3*OFT) This register value is neglected in RGB output mode. The lower 5 bits are held low, so this value should be a multiple of 32 bytes.

6.4.92 RZB_SDR_C_PTR_S

The RZB: Start Line of SDRAM Pointer (RZB_SDR_C_PTR_S) register is shown in Figure 6-278 and described in Table 6-283.

Figure 6-278. RZB_SDR_C_PTR_S Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-283. RZB_SDR_C_PTR_S Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	The vertical position of the first output line in the output memory space. This value should be 0, when SAD=BAD In RGB output mode, this value should be multiple of 4 (the lowest two bits be "00").

6.4.93 RZB_SDR_C_PTR_E

The RZB: End line of SDRAM Pointer (RZB_SDR_C_PTR_E) register is shown in Figure 6-279and described in Table 6-284.

Figure 6-279. RZB_SDR_C_PTR_E Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-00	R/W-8191

LEGEND: R = Read only; -*n* = value after reset

Table 6-284. RZB_SDR_C_PTR_E Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	SDRAM Available Capacity: The maximum number of lines to be stored in the memory space in Buffer Memory or DRAM. When the number output lines exceeds this value, the address restarts from the first address in the memory space. Example: VAL=0x0003h line 0: address = SAD + (0*OFT) line 1: address = SAD + (1*OFT) line 2: address = SAD + (2*OFT) line 3: address = SAD + (3*OFT) line 4: address = SAD + (0*OFT) ≤ (Returned to the first address) line 5: address = SAD + (1*OFT) line 6: address = SAD + (2*OFT) line 7: address = SAD + (3*OFT) line 8: address = SAD + (0*OFT) ≤ (Returned to the first address) line 9: address = SAD + (1*OFT) line 10: address = SAD + (2*OFT) line 11: address = SAD + (3*OFT) In RGB output mode, this value should be multiple of 4 (the lowest two bits be "00") to ensure that the end of SDRAM region is aligned with line size.

6.5 Hardware 3A (H3A) Registers

Table 6-285 lists the memory-mapped registers for the Hardware 3A Statistics Generation (AE, AF, AWB) (H3A). See the device-specific data manual for the memory address of these registers.

Table 6-285. Hardware 3A Statistics Generation (AE, AF, AWB) (H3A) Registers

Offset	Acronym	Register Description	Section
0h	PID	Peripheral Revision and Class Information	Section 6.5.1
04h	PCR	Peripheral Control Register	Section 6.5.2
08h	AFPAX1	Setup for the AF Engine Paxel Configuration	Section 6.5.3
0Ch	AFPAX2	Setup for the AF Engine Paxel Configuration	Section 6.5.4
10h	AFPAXSTART	Start Position for AF Engine Paxels	Section 6.5.5
18h	AFBUFST	SDRAM/DDRAM Start address for AF Engine	Section 6.5.6
4Ch	AEWWIN1	Configuration for AE/AWB Windows	Section 6.5.7
50h	AEWINSTART	Start position for AE/AWB Windows	Section 6.5.8
54h	AEWINBLK	Start position and height for black line of AE/AWB Windows	Section 6.5.9
58h	AEWSUBWIN	Configuration for subsample data in AE/AWB window	Section 6.5.10
5Ch	AEWBUFST	SDRAM/DDRAM Start address for AE/AWB Engine Output Data	Section 6.5.11
60h	RSDR_ADDR	AE/AWB Engine Configuration	Section 6.5.12
64h	LINE_START	Line start position for ISIF interface	Section 6.5.13
68h	VFV_CFG1	AF Vertical Focus Configuration 1 Register	Section 6.5.14
6Ch	VFV_CFG2	AF Vertical Focus Configuration 2 Register	Section 6.5.15
70h	VFV_CFG3	AF Vertical Focus Configuration 3 Register	Section 6.5.16
74h	VFV_CFG4	AF Vertical Focus Configuration 4 Register	Section 6.5.17
78h	HFV_THR	Configures the Horizontal Thresholds for the AF IIR filters	Section 6.5.18

6.5.1 Peripheral Revision and Class Information (PID)

The peripheral revision and class information (PID) register is shown in Figure 6-280 and described in Table 6-286.

Figure 6-280. PID - Peripheral Revision and Class Information (PID)

31-30	29-28	27-16
SCHEME	Reserved	FUNC
R-1	R-00	R-3329

15-11	10-8	7-6	7-0
RTL	MAJOR	Reserved	MINOR
R-0	R-0	R-00	R-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-286. PID - Peripheral Revision and Class Information (PID) Field Descriptions

Bit	Field	Value	Description
31-30	SCHEME	0-3h	Scheme used is PDR3.5
29-28	Reserved	0-3h	Any writes to these bit(s) must always have a value of 0.
27-16	FUNC	0-FFFh	Function h3A (AF, AE, and AWB)
15-11	RTL	0-1Fh	RTL Revision
10-8	MAJOR	0-7h	Major Version
7-6	Reserved	0-3h	Any writes to these bit(s) must always have a value of 0.
7-0	MINOR	0-FFh	Peripheral Revision Number Initial Revision

6.5.2 Peripheral Control Register (PCR)

The peripheral control register (PCR) is shown in Figure 6-281 and described in Table 6-287.

Figure 6-281. Peripheral Control Register (PCR) Register

31-22	21	20	19	18	17	16
AVE2LMT	Reserved	AF_VF_EN	AEW_MED_EN	BUSYAEAWB	AEW_ALAW_EN	AEW_EN
R/W-1023	R-00	R/W-0	R/W-0	R-0	R/W-0	R/W-0

15	14	13-11	10-3	2	1	0
BUSYAF	FVMODE	RGBPOS	MED_TH	AF_MED_EN	AF_ALAW_EN	AF_EN
R-0	R/W-0	R/W-0	R/W-255	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-287. Peripheral Control Register (PCR) Field Descriptions

Bit	Field	Value	Description
31-22	AVE2LMT	0-3FFh	AE/AWB Saturation Limit This is the value that all sub sampled pixels in the AE/AWB engine are compared to. If the data is greater or equal to this data then the block is considered saturated.
21	Reserved	0	Any writes to these bit(s) must always have a value of 0.
20	AF_VF_EN		AF Vertical Focus Enable
		0	4 Color Horizontal Only FV operation
		1	1 Color Horizontal and Vertical FV operation
19	AEW_MED_EN		AE/AWB Median filter Enable If the median filter is enabled, then the 1st 2 and last 2 pixels in the frame are not filtered.
		0	Disable AE/AWB median filter
		1	Enable AE/AWB median filter
18	BUSYAEAWB		Busy bit for AE/AWB
17	AEW_ALAW_EN		AE/AWB A-law Enable
		0	Disable AE/AWB A-law table
		1	Enable AE/AWB A-law table
16	AEW_EN		AE/AWB Enable
		0	Disable AE/AWB Engine
		1	Enable AE/AWB Engine
15	BUSYAF		Busy bit for AF
14	FVMODE		Focus Value Accumulation Mode
		0	Sum Mode
		1	Peak Mode
13-11	RGBPOS		Red, Green, and Blue pixel location in the AF windows
		0	GR and GB as Bayer pattern
		1	RG and GB as Bayer pattern
		2	GR and BG as Bayer pattern
		3	RG and BG as Bayer pattern
		4	GG and RB as custom pattern
		5	RB and GG as custom pattern
10-3	MED_TH		Median filter threshold
2	AF_MED_EN		Auto Focus Median filter Enable If the median filter is enabled, then the 1st 2 and last 2 pixels in the frame are not filtered.
		0	Disable Auto Focus median filter
		1	Enable Auto Focus median filter

Table 6-287. Peripheral Control Register (PCR) Field Descriptions (continued)

Bit	Field	Value	Description
1	AF_ALAW_EN		Auto Focus A-law table Enable
		0	Disable Auto Focus A-law table
		1	Enable Auto Focus A-law table
0	AF_EN		Auto Focus Enable
		0	Disable Auto Focus Engine
		1	Enable Auto Focus Engine

6.5.3 Setup for the AF Engine Paxel Configuration (AFPAX1)

The setup for the AF engine paxel configuration (AFPAX1) register is shown in Figure 6-282 and described in Table 6-288.

Figure 6-282. Setup for the AF Engine Paxel Configuration (AFPAX1) Register

31-24	23-16
Reserved	PAXW
R-00	R/W-0

15-8	7-0
Reserved	PAXH
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-288. Setup for the AF Engine Paxel Configuration (AFPAX1) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Any writes to these bit(s) must always have a value of 0.
23-16	PAXW	0-FFh	AF Engine Paxel Width The width of the paxel is the value of this register plus 1 multiplied by 2. The minimum width is expected to be 8 pixels.
15-8	Reserved	0-FFh	Any writes to these bit(s) must always have a value of 0.
7-0	PAXH	0-FFh	AF Engine Paxel Height The height of the paxel is the value of this register plus 1 multiplied by 2 with a final value of 2-256 (even).

6.5.4 Setup for the AF Engine Paxel Configuration (AFPAX2)

The setup for the AF engine paxel configuration (AFPAX2) register is shown in and described in .

Figure 6-283. Setup for the AF Engine Paxel Configuration (AFPAX2) Register

31-17	20-17
Reserved	AFINCH
R-00	R/W-0

15-13	12-6	5-0
AFINCV	PAXVC	PAXHC
R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-289. Setup for the AF Engine Paxel Configuration (AFPAX2) Field Descriptions

Bit	Field	Value	Description
31-17	Reserved	0	Any writes to these bit(s) must always have a value of 0.
20-17	AFINCH	0-Fh	AF Engine Column Increments Number of columns to increment in a Paxel plus 1 multiplied by 2. Thus, the number of columns that can be skipped between two processed line pairs is 0-30 (even). The starting two columns in a paxel are first processed before this field is applied. This must be set so that there are at least 4 samples on a line when combined with the number of horizontal paxels. * This registered is shadowed and latched on the rising edge of VSYNC
16-13	AFINCV	0-Fh	AF Engine Line Increments Number of lines to increment in a Paxel plus 1 multiplied by 2. Incrementing the line in a paxel is always done on a line pair due to the fact that the RGB pattern falls in two lines. If all the lines are to be processed, this field should be set to zero, and thus line count is incremented by 2 following a line pair. Thus, the number of lines that can be skipped between two processed line pairs is 0-30 (even). The starting two lines in a paxel are first processed before this field is applied.
12-6	PAXVC	0-7Fh	AF Engine Vertical Paxel Count The number of paxels in the vertical direction plus 1. The maximum number of vertical paxels in a frame should not exceed 128. The value should be set to ensure that the bandwidth requirements and buffer size are not exceeded.
5-0	PAXHC	0-3Fh	AF Engine Horizontal Paxel Count The number of paxels in the horizontal direction plus 1. It is illegal to set a number that is greater than 35 (total of 36 paxels in the horizontal direction).

6.5.5 Start Position for AF Engine Paxels (AFPAXSTART)

The start position for AF engine paxels (AFPAXSTART) register is shown in Figure 6-284 and described in Table 6-290.

Figure 6-284. Start Position for AF Engine Paxels (AFPAXSTART) Register

31-28	27-16
Reserved	PAXSH
R-00	R/W-0

15-12	11-0
Reserved	PAXSV
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-290. Start Position for AF Engine Paxels (AFPAXSTART) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Any writes to these bit(s) must always have a value of 0.
27-16	PAXSH	0-FFFh	AF Engine Paxel Horizontal start position Range: 2-4094 PAXSH must be equal to or greater than (IIRSH + 2) This value must be even
15-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	PAXSV	0-FFFh	AF Engine Paxel Vertical start position Range: 0-4095 Sets the vertical line for the first paxel.

6.5.6 SDRAM/DDRAM Start address for AF Engine (AFBUFST)

The SDRAM/DDRAM start address for AF engine (AFBUFST) is shown in Figure 6-285 and described in Table 6-291.

Figure 6-285. SDRAM/DDRAM Start Address for AF Engine (AFBUFST)

31-16
AFBUFST
R/W-0

15-0
AFBUFST
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-291. SDRAM/DDRAM Start Address for AF Engine (AFBUFST) Field Descriptions

Bit	Field	Value	Description
31-0	AFBUFST	0-FFFF FFFFh	AF Engine SDRAM/DDRAM Start Address The starting location in the SDRAM/DDRAM. The 6 LSB are ignored, address should be on a 64-byte boundary. * This field can be altered even when the AF is busy. Change will take place only for the next frame. However, note that reading this register will always give the latest value.

6.5.7 Configuration for AE/AWB Windows (AEWWIN1)

The configuration for AE/AWB windows (AEWWIN1) register is shown in Figure 6-286 and described in Table 6-292.

Figure 6-286. Configuration for AE/AWB Windows (AEWWIN1)

31-24	23-21	20-16
WINH	Reserved	WINW
R/W-0	R-00	R/W-0

15-13	12-6	5-0
WINW	WINVC	WINHC
R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-292. AEWWIN1 - Configuration for AE/AWB Windows (AEWWIN1) Field Descriptions

Bit	Field	Value	Description
31-24	WINH	0-FFh	AE/AWB Engine Window Height. This specifies the window height in an even number of pixels, the window height is the value plus 1 multiplied by 2. The final value can be from 2-512 (even).
23-21	Reserved	0	Any writes to these bit(s) must always have a value of 0.
20-13	WINW	0-FFh	AE/AWB Engine Window Width. This specifies the window width in an even number of pixels, the window width is the value plus 1 multiplied by 2. The minimum width is expected to be 8 pixels.
12-6	WINVC	0-7Fh	AE/AWB Engine Vertical Window Count. The number of windows in the vertical direction plus 1. The maximum number of vertical windows in a frame should not exceed 128. The value should be set to ensure that the bandwidth requirements and buffer size are not exceeded.
5-0	WINHC	0-3Fh	AE/AWB Engine Horizontal Window Count. The number of horizontal windows plus 1. The maximum number of horizontal windows is 35 plus 1 (36). The minimum number of windows should be 2 (valid range for the field is 1-35).

6.5.8 Start Position for AE/AWB Windows (AEWINSTART)

The start position for AE/AWB Windows (AEWINSTART) register is shown in Figure 6-287 and described in Table 6-293.

Figure 6-287. Start Position for AE/AWB Windows (AEWINSTART) Register

31-28	27-16
Reserved	WINSV
R-00	R/W-0

15-12	11-0
Reserved	WINSH
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-293. Start Position for AE/AWB Windows (AEWINSTART) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Any writes to these bit(s) must always have a value of 0.
27-16	WINSV	0-FFFh	AE/AWB Engine Vertical Window Start Position. Sets the first line for the first window. Range 0-4095.
15-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	WINSH	0-FFFh	AE/AWB Engine Horizontal Window Start Position. Sets the horizontal position for the first window on each line. Range 0-4095.

6.5.9 Black Line of AE/AWB Windows (AEWINBLK)

The start position and height for black line of AE/AWB Windows (AEWINBLK) register is shown in Figure 6-288and described in Table 6-294.

Figure 6-288. Black Line of AE/AWB Windows (AEWINBLK) Register

31-28	27-16
Reserved	WINSV
R-00	R/W-0

15-7	6-0
Reserved	WINH
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-294. Black Line of AE/AWB Windows (AEWINBLK) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Any writes to these bit(s) must always have a value of 0.
27-16	WINSV	0-FFFh	AE/AWB Engine Vertical Window Start Position for single black line of windows. Sets the first line for the single black line of windows. Range 0-4095 Note that the horizontal start and the horizontal number of windows will be similar to the regular windows.
15-7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6-0	WINH	0-7Fh	AE/AWB Engine Window Height for the single black line of windows. This specifies the window height in an even number of pixels, the window height is the value plus 1 multiplied by 2. The final value can be from 2-256 (even).

6.5.10 Configuration for Subsample Data in AE/AWB Window(AEWSUBWIN)

The configuration for subsample data in AE/AWB window (AEWSUBWIN) register is shown in Figure 6-289 and described in Table 6-295.

Figure 6-289. Configuration for Subsample Data in AE/AWB Window (AEWSUBWIN)

31-16
Reserved
R-00

15-12	11-8	7-4	3-0
Reserved	AEWINCV	Reserved	AEWINCH
R-00	R/W-0	R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-295. Configuration for Subsample Data in AE/AWB Window (AEWSUBWIN) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-8	AEWINCV	0-Fh	AE/AWB Engine Vertical Sampling Point Increment. Sets vertical distance between sub-samples within a window plus 1 multiplied by 2. The final range is 2-32.
7-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3-0	AEWINCH	0-Fh	AE/AWB Engine Horizontal Sampling Point Increment. Sets horizontal distance between sub-samples within a window plus 1 multiplied by 2. The final range is 2-32.

6.5.11 SDRAM/DDRAM Start address for AE/AWB Engine Output Data (AEWBUFST)

The SDRAM/DDRAM start address for AE/AWB engine output data (AEWBUFST) register is shown in Figure 6-290 and described in Table 6-296.

Figure 6-290. SDRAM/DDRAM Start Address for AE/AWB Engine Output Data (AEWBUFST) Register

31-16
AEWBUFST
R/W-0

15-0
AEWBUFST
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-296. SDRAM/DDRAM Start Address for AE/AWB Engine Output Data (AEWBUFST) Field Descriptions

Bit	Field	Value	Description
31-0	AEWBUFST	0-FFFF FFFFh	AE/AWB Engine SDRAM/DDRAM Start Address The starting location in the SDRAM/DDRAM for the AE/AWB data. The 6 LSB are ignored, address should be on a 64-byte boundary. * This field can be altered even when the AE/AWB is busy. Change will take place only for the next frame. However, note that reading this register will always give the latest value.

6.5.12 AEW_CFG - AE/AWB Engine Configuration Register (RSDR_ADDR)

The AE/AWB engine configuration (RSDR_ADDR) register is shown in Figure 6-291 and described in Table 6-297.

Figure 6-291. AEW_CFG - AE/AWB Engine Configuration Register (RSDR_ADDR)

31-16
Reserved
R-00

15-10	9-8	7-4	3-0
Reserved	AEFMT	Reserved	SUMSFT
R-00	R/W-0	R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-297. AEW_CFG - AE/AWB Engine Configuration Register (RSDR_ADDR) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-8	AEFMT		AE/AWB OUTPUT Format.
		0	Sum of squares data along with accumulated data.
		1	Min and max values of each color of each window.
		2	Only send the accumulator values.
7-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3-0	SUMSFT	0-Fh	AE/AWB Engine Shift Value for the sum of pixel values. The right shift value for the accumulated pixel values to avoid overflow when built into a packet. SUMSFT = right shift value. Range: 0 -15 * This registered is shadowed and latched on the rising edge of VSYNC

6.5.13 Line Start Position (LINE_START)

The line start position for ISIF interface (LINE_START) register is shown in Figure 6-292 and described in Table 6-298.

Figure 6-292. Line Start Position (LINE_START) Register

31-16
SLV
W-0

15-0
LINE_START
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-298. Line Start Position (LINE_START) Field Descriptions

Bit	Field	Value	Description
31-16	SLV	0-FFFFh	Start Line Vertical Specifies how many lines after the VD rising edge the real frame starts.
15-0	LINE_START	0-FFFFh	Line Start Specifies the start pixel of the ISIF interface module into the line buffer.

6.5.14 Vertical Focus Configuration 1 (VFV_CFG1)

AF vertical focus configuration 1 (VFV_CFG1) register is shown in Figure 6-293 and described in Table 6-299.

Figure 6-293. VFV_CFG1 (VFV_CFG1) Register

31-24	23-16
VCOEF1_3	VCOEF1_2
R/W-0	R/W-0

15-8	7-0
VCOEF1_1	VCOEF1_0
R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-299. Vertical Focus Configuration 1 (VFV_CFG1) Field Descriptions

Bit	Field	Value	Description
31-24	VCOEF1_3	0-FFh	Vertical FV FIR 1 coefficient 3.
23-16	VCOEF1_2	0-FFh	Vertical FV FIR 1 coefficient 2.
15-8	VCOEF1_1	0-FFh	Vertical FV FIR 1 coefficient 1.
7-0	VCOEF1_0	0-FFh	Vertical FV FIR 1 coefficient 0.

6.5.15 Vertical Focus Configuration 2 (VFV_CFG2)

The AF vertical focus configuration 2 (VFV_CFG2) register is shown in Figure 6-294 and described in Table 6-300.

Figure 6-294. Vertical Focus Configuration 2 (VFV_CFG2) Register

31-16
VTHR1
R/W-0

15-8	7-0
Reserved	VCOEF1_4
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-300. Vertical Focus Configuration 2 (VFV_CFG2) Field Descriptions

Bit	Field	Value	Description
31-16	VTHR1	0-FFFFh	Threshold for Vertical FV FIR 1.
15-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VCOEF1_4	0-FFh	Vertical FV FIR 1 coefficient 4.

6.5.16 Vertical Focus Configuration 3 (VFV_CFG3)

The AF vertical focus configuration 3 (VFV_CFG3) register is shown in Figure 6-295 and described in Table 6-301.

Figure 6-295. Vertical Focus Configuration 3 (VFV_CFG3) Register

31-24	23-16
VCOEF2_3	VCOEF2_2
R/W-0	R/W-0

15-8	7-0
VCOEF2_1	VCOEF2_0
R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-301. Vertical Focus Configuration 3 (VFV_CFG3) Field Descriptions

Bit	Field	Value	Description
31-24	VCOEF2_3	0-FFh	Vertical FV FIR 2 coefficient 3.
23-16	VCOEF2_2	0-FFh	Vertical FV FIR 2 coefficient 2.
15-8	VCOEF2_1	0-FFh	Vertical FV FIR 2 coefficient 1.
7-0	VCOEF2_0	0-FFh	Vertical FV FIR 2 coefficient 0.

6.5.17 Vertical Focus Configuration 4 (VFV_CFG4)

The AF vertical focus configuration 4 (VFV_CFG4) register is shown in Figure 6-296 and described in Table 6-302.

Figure 6-296. Vertical Focus Configuration 4 (VFV_CFG4) Register

31-16
VTHR2
R/W-0

15-8	7-0
Reserved	VCOEF2_4
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-302. Vertical Focus Configuration 4 (VFV_CFG4) Field Descriptions

Bit	Field	Value	Description
31-16	VTHR2	0-FFFFh	Threshold for Vertical FV FIR 2.
15-8	Reserved	0	Reserved
7-0	VCOEF2_4	0-FFh	Vertical FV FIR 2 coefficient 4.

6.5.18 Horizontal Threshold (HFV_THR)

The horizontal threshold (HFV_THR) register is shown in Figure 6-297 and described in Table 6-303.

Figure 6-297. Horizontal Threshold (HFV_THR) Register

31-16
HTHR2
R/W-0

15-0
HTHR1
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-303. Horizontal Threshold (HFV_THR) Field Descriptions

Bit	Field	Value	Description
31-16	HTHR2	0-FFFFh	Threshold for Horizontal FV IIR 2.
15-0	HTHR1	0-FFFFh	Threshold for Horizontal FV IIR 1.

6.6 ISP System Configuration (ISP) Registers

The ISP system configuration registers are listed here and described in the following sections.

Table 6-304. ISP System Configuration Registers

Offset	Acronym	Register Description	Section
0h	PID 4c180800	Peripheral Revision and Class Information(NA)	Section 6.6.1
04h	PCCR ff	Peripheral Clock Control Register	Section 6.6.2
08h	BCR 2	Buffer logic Control Register	Section 6.6.3
0Ch	INTSTAT 1f0fe07	Interrupt Status Register	Section 6.6.4
10h	INTSEL1 120f0100	Interrupt Selection Register1	Section 6.6.5
14h	INTSEL2 14060713	Interrupt Selection Register2	Section 6.6.6
18h	INTSEL3 15	Interrupt Selection Register3	Section 6.6.7
1Ch	EVTSEL 1e1d0807	Event Selection Register	Section 6.6.8
2Ch	MPSR 0	Memory Priority Select Register	Section 6.6.9

6.6.1 Peripheral Revision and Class Information (PID) Register

The peripheral revision and class Information(PID) register is shown in Figure 6-298 and described in Table 6-305.

Figure 6-298. PID - Peripheral Revision and Class Information (PID)

31-16
PREV
R-1276643328

15-0
PREV
R-1276643328

LEGEND: R = Read only; -*n* = value after reset

Table 6-305. PID - Peripheral Revision and Class Information (PID) Field Descriptions

Bit	Field	Value	Description
31-0	PREV	0-FFFF FFFFh	Peripheral Revision Number Initial Revision

6.6.2 *Peripheral Clock Control Register (PCCR)*

The peripheral clock control register (PCCR) is shown in Figure 6-299 and described in Table 6-306.

Figure 6-299. Peripheral Clock Control Register (PCCR)

31-16
Reserved
R-00

15-8	7	6	5	4	3	2	1	0
Reserved	PSYNC_CLK_SEL	SYNC_ENABLE	IPIPEIF_CLK_ENABLE	IPIPE_CLK_ENABLE	RSZ_CLK_ENABLE	H3A_CLK_ENABLE	ISIF_CLK_ENABLE	BL_CLK_ENABLE
R-00	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 6-306. Peripheral Clock Control Register (PCCR) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7	Reserved	0	Reserved
6	Reserved	0	Reserved. This bit should be set to 1 always.
5	IPIPEIF_CLK_ENABLE	1	IPIPEIF clock enable 0: Disable 1:Enable
4	IPIPE_CLK_ENABLE	1	IPIPE clock enable 0: Disable 1:Enable
3	RSZ_CLK_ENABLE	1	RSZ clock enable 0: Disable 1:Enable
2	H3A_CLK_ENABLE	1	H3A clock enable 0: Disable 1:Enable
1	ISIF_CLK_ENABLE	1	ISIF clock enable 0: Disable 1:Enable
0	BL_CLK_ENABLE	1	BL clock enable 0: Disable 1:Enable (should be set to 1 for DDR R/W access)

6.6.3 Buffer logic Control Register (BCR)

The buffer logic control (BCR) register is shown in Figure 6-300 and described in Table 6-307.

Figure 6-300. Buffer Logic Control Register (BCR)

31-16
Reserved
R-00

15-8	7-5	4-2	1	0
Reserved	CPRIORITY_W	CPRIORITY_R	SRC_SEL_ISIF_IPIPE	SRC_SEL_IPIPE_LDC
R-00	R/W-0	R/W-0	R/W-1	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-307. Buffer logic Control Register (BCR) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-5	CPRIORITY_W	0-7h 0	Sets Priority of VPSS Should be set to highest priority (0) for best performance
4-2	CPRIORITY_R	0-7h 0	Sets Priority of VPSS Should be set to highest priority (0) for best performance
1	SRC_SEL_ISIF_IPIPE		BL_WBL select (DDR write port mux b/w IPIPE boxcar output and ISIF output)
		0 1	IPIPE BOXCAR OUT
		1	ISIF OUT
0	SRC_SEL_IPIPE_LDC		BL_WBL select (DDR write port mux b/w IPIPE boxcar output and LDC output)
		0 0	~~LDC OUT~~
		1	IPIPE BOXCAR OUT

6.6.4 Interrupt Status (INTSTAT) Register

The interrupt status (INTSTAT) register is shown in Figure 6-301 and described in Table 6-308.

Figure 6-301. Interrupt Status (INTSTAT)Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	Reserved	IPIPE_INT_DPC_RNEW1	IPIPE_INT_DPC_RNEW0	IPIPE_INT_DPC_INI	LDC_INT_EOF	IPIPE_INT_EOF	H3A_INT_EOF	RSZ_INT_EOF1	RSZ_INT_EOF0	VENC_INT	OSD_INT	Reserved	Reserved	Reserved	Reserved
R-00	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSZ_INT_DMA	RSZ_INT_LAST_PIX	RSZ_INT_REG	Reserved	AF_INT	AEW_INT	IPIPEIF_INT	IPIPE_INT_HST	IPIPE_INT_BSC	Reserved	IPIPE_INT_LAST_PIX	IPIPE_INT_REG	ISIF_INT3	ISIF_INT2	ISIF_INT1	ISIF_INT0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-308. Interrupt Status (INTSTAT) Field Descriptions

Bit	Field	Value	Description
30-31	Reserved	0	Any writes to these bit(s) must always have a value of 0.
29	IPIPE_INT_DPC_RNEW1	0 1	Set when IPIPE_INT_DPC_RNEW1 is triggered, clear by writing 1. Clear bit
28	IPIPE_INT_DPC_RNEW0	0 1	Set when IPIPE_INT_DPC_RNEW0 is triggered, clear by writing 1. Clear bit
27	IPIPE_INT_DPC_INI	0 1	Set when IPIPE_INT_DPC_INI is triggered, clear by writing 1. Clear bit
26	LDC_INT_EOF	 1 0	Set when LDC_INT_EOF is triggered, clear by writing 1. Clear bit
25	IPIPE_INT_EOF	 1 0	Set when IPIPE_INT_EOF is triggered, clear by writing 1. Clear bit
24	H3A_INT_EOF	1 1	Set when H3A_INT_EOF is triggered, clear by writing 1. Clear bit
23	RSZ_INT_EOF1	 1 1	Set when RSZ_INT_EOF1 is triggered, clear by writing 1. Clear bit
22	RSZ_INT_EOF0	 1 1	Set when RSZ_INT_EOF0 is triggered, clear by writing 1. Clear bit
21	VENC_INT	1 1	Set when VENC_INT is triggered, clear by writing 1. Clear bit
20	OSD_INT	1 1	Set when OSD_INT is triggered, clear by writing 1. Clear bit
19	Reserved	0 1	Reserved. Clear bit
18	Reserved	 1 0	Reserved Clear bit
17	RSZ_INT_CYC_RZB	 1 0	Set when RSZ_INT_CYC_RZB is triggered, clear by writing 1. Clear bit
16	RSZ_INT_CYC_RZA	 1 0	Set when RSZ_INT_CYC_RZA is triggered, clear by writing 1. Clear bit
15	Reserved	 1	Reserved Clear bit

Table 6-308. Interrupt Status (INTSTAT) Field Descriptions (continued)

Bit	Field	Value	Description
14	RSZ_INT_LAST_PIX		Set when RSZ_INT_LAST_PIX is triggered, clear by writing 1.
		1	Clear bit
13	RSZ_INT_REG		Set when RSZ_INT_REG is triggered, clear by writing 1.
		1	Clear bit
12	Reserved		Reserved
		1	Clear bit
11	AF_INT		Set when AF_INT is triggered, clear by writing 1.
		1	Clear bit
10	AEW_INT		Set when AEW_INT is triggered, clear by writing 1.
		1	Clear bit
9	IPIPEIF_INT		Set when IPIPEIF_INT is triggered, clear by writing 1.
		1	Clear bit
8	IPIPE_INT_HST		Set when IPIPE_INT_HST is triggered, clear by writing 1.
		1 0	Clear bit
7	IPIPE_INT_BSC		Set when IPIPE_INT_BSC is triggered, clear by writing 1.
		1 0	Clear bit
6	Reserved		Reserved
		1 0	Clear bit
5	IPIPE_INT_LAST_PIX		Set when IPIPE_INT_LAST_PIX is triggered, clear by writing 1.
		1 0	Clear bit
4	IPIPE_INT_REG		Set when IPIPE_INT_REG is triggered, clear by writing 1.
		1 0	Clear bit
3	ISIF_INT3		Set when ISIF_INT3 is triggered, clear by writing 1.
		1 0	Clear bit
2	ISIF_INT2		Set when ISIF_INT2 is triggered, clear by writing 1.
		1	Clear bit
1	ISIF_INT1		Set when ISIF_INT1 is triggered, clear by writing 1.
		1	Clear bit
0	ISIF_INT0		Set when ISIF_INT0 is triggered, clear by writing 1.
		1	Clear bit

6.6.5 IInterrupt Selection (INTSEL1) Register

The interrupt selection (INTSEL1) register is shown in Figure 6-302 and described in Table 6-309.

Figure 6-302. Interrupt Selection (INTSEL1) Register

31-29	28-24	23-21	20-16
Reserved	INTSEL3	Reserved	INTSEL2
R-00	R/W-0	R-00	R/W-0

15-13	12-8	7-5	4-0
Reserved	INTSEL1	Reserved	INTSEL0
R-00	R/W-0	R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-309. Interrupt Selection (INTSEL1) Field Descriptions

Bit	Field	Value	Description
31-29	Reserved	0	Any writes to these bit(s) must always have a value of 0.
28-24	INTSEL3		Selects the interrupt for vpss_int[3]
		0	ISIF_INT0
		1	ISIF_INT1
		2	ISIF_INT2
		3	ISIF_INT3
		4	IPIPE_INT_REG
		5	IPIPE_INT_LAST_PIX
		6	Reserved
		7	IPIPE_INT_BSC
		8	IPIPE_INT_HST
		9	IPIPEIF_INT
		10	AEW_INT
		11	AF_INT
		12	Reserved
		13	RSZ_INT_REG
		14	RSZ_INT_LAST_PIX
		15	Reserved
		16	RSZ_INT_CYC_RZA
		17	RSZ_INT_CYC_RZB
		18	Reserved
		19	Reserved
		20	OSD_INT
		21	VENC_INT
		22	RSZ_INT_EOF0
		23	RSZ_INT_EOF1
		24	H3A_INT_EOF
		25	IPIPE_INT_EOF
		26	LDC_INT_EOF
		27	IPIPE_INT_DPC_INI
		28	IPIPE_INT_DPC_RNEW0
		29	IPIPE_INT_DPC_RNEW1
23-21	Reserved	0	Any writes to these bit(s) must always have a value of 0.
20-16	INTSEL2	0-1Fh	Selects the interrupt for vpss_int[2]
15-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-8	INTSEL1	0-1Fh	Selects the interrupt for vpss_int[1]

Table 6-309. Interrupt Selection (INTSEL1) Field Descriptions (continued)

Bit	Field	Value	Description
7-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4-0	INTSEL0	0-1Fh	Selects the interrupt for vpss_int[0]

6.6.6 Interrupt Selection (INTSEL2) Register

The interrupt selection register2 (INTSEL2) register is shown in Figure 6-303 and described in Table 6-310.

Figure 6-303. Interrupt Selection (INTSEL2) Register

31-29	28-24	23-21	20-16
Reserved	INTSEL7	Reserved	INTSEL6
R-00	R/W-0	R-00	R/W-0

15-13	12-8	7-5	4-0
Reserved	INTSEL5	Reserved	INTSEL4
R-00	R/W-0	R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-310. Interrupt Selection (INTSEL2) Field Descriptions

Bit	Field	Value	Description
31-29	Reserved	0	Any writes to these bit(s) must always have a value of 0.
28-24	INTSEL7	0-1Fh	Selects the interrupt for vpss_int[7]
23-21	Reserved	0	Any writes to these bit(s) must always have a value of 0.
20-16	INTSEL6	0-1Fh	Selects the interrupt for vpss_int[6]
15-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-8	INTSEL5	0-1Fh	Selects the interrupt for vpss_int[5]
7-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4-0	INTSEL4	0-1Fh	Selects the interrupt for vpss_int[4]

6.6.7 Interrupt Selection (INTSEL3) Register

The interrupt selection register3 (INTSEL3) register is shown in Figure 6-304 and described in Table 6-311.

Figure 6-304. Interrupt Selection Register (INTSEL3) Register

31-16
Reserved
R-00

15-5	4-0
Reserved	INTSEL8
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-311. Interrupt Selection Register (INTSEL3) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4-0	INTSEL8	0-1Fh	Selects the interrupt for vpss_int[8]

6.6.8 Event Selection (EVTSEL) Register

The event selection register is shown in Figure 6-305 and described in Table 6-312.

Figure 6-305. Event Selection (EVTSEL) Register

31-29	28-24	23-21	20-16
Reserved	EVTSEL3	Reserved	EVTSEL2
R-00	R/W-0	R-00	R/W-0

15-13	12-8	7-5	4-0
Reserved	EVTSEL1	Reserved	EVTSEL0
R-00	R/W-0	R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 6-312. Event Selection (EVTSEL) Field Descriptions

Bit	Field	Value	Description
31-29	Reserved	0	Any writes to these bit(s) must always have a value of 0.
28-24	EVTSEL3 11110		Selects the event for vpss_evt[3]
		0	ISIF_INT0
		1	ISIF_INT1
		2	ISIF_INT2
		3	ISIF_INT3
		4	IPIPE_INT_REG
		5	IPIPE_INT_LAST_PIX
		6	Reserved
		7	IPIPE_INT_BSC
		8	IPIPE_INT_HST
		9	IPIPEIF_INT
		10	AEW_INT
		11	AF_INT
		12	Reserved
		13	RSZ_INT_REG
		14	RSZ_INT_LAST_PIX
		15	Reserved
		16	RSZ_INT_CYC_RZA
		17	RSZ_INT_CYC_RZB
		18	Reserved
		19	Reserved
		20	OSD_INT
		21	VENC_INT
		22	RSZ_INT_EOF0
		23	RSZ_INT_EOF1
		24	H3A_INT_EOF
		25	IPIPE_INT_EOF
		26	LDC_INT_EOF
		27	IPIPE_INT_DPC_INI
		28	IPIPE_INT_DPC_RNEW0
		29	IPIPE_INT_DPC_RNEW1
23-21	Reserved 000	0	Any writes to these bit(s) must always have a value of 0.
20-16	EVTSEL2 11101	0-1Fh	Selects the event for vpss_evt[2]
15-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-8	EVTSEL1 0000	0-1Fh	Selects the event for vpss_evt[1]

Table 6-312. Event Selection (EVTSEL) Field Descriptions (continued)

Bit	Field	Value	Description
7-5	Reserved 000	0	Any writes to these bit(s) must always have a value of 0.
4-0	EVTSEL0 0111	0-1Fh	Selects the event for vpss_evt[0]

6.6.9 Memory Priority Select (MPSR) Register

The memory priority select register (MPSR) is shown in Figure 6-306 and described in Table 6-313.

Figure 6-306. Memory Priority Select (MPSR) Register

31-25	24	23-21	20	19	18	17	16
Reserved	RGBCOPY	Reserved	BSC_TB1	BSC_TB0	HST_TB3	HST_TB2	HST_TB1
R-00	R/W-0	R-00	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HST_TB0	D3L_TB3	D3L_TB2	D3L_TB1	D3L_TB0	GBC_TB	YEE_TB	GMM_TBR	GMM_TBG	GMM_TBB	DPC_TB	DCLAMP	LS_TB1	LS_TB0	LIN_TB	Reserved
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-00

LEGEND: R = Read only; -*n* = value after reset

Table 6-313. Memory Priority Select (MPSR) Field Descriptions

Bit	Field	Value	Description
31-25	Reserved	0	Any writes to these bit(s) must always have a value of 0.
24	RGBCOPY		RGB memory table copy enable 0: Disable 1:Enable
23-21	Reserved	0	Reserved
20	BSC_TB1		BSC_TB1 memory access priority
19	BSC_TB0		BSC_TB0 memory access priority
18	HST_TB3		HST_TB3 memory access priority
17	HST_TB2		HST_TB2 memory access priority
16	HST_TB1		HST_TB1 memory access priority
15	HST_TB0		HST_TB0 memory access priority
14	D3L_TB3		D3L_TB3 memory access priority
13	D3L_TB2		D3L_TB2 memory access priority
12	D3L_TB1		D3L_TB1 memory access priority
11	D3L_TB0		D3L_TB0 memory access priority
10	GBC_TB		GBC_TB memory access priority
9	YEE_TB		YEE_TB memory access priority
8	GMM_TBR		GMM_TBR memory access priority
7	GMM_TBG		GMM_TBG memory access priority
6	GMM_TBB		GMM_TBB memory access priority
5	DPC_TB		DPC_TB memory access priority
4	DCLAMP		DCLAMP memory access priority
3	LS_TB1		LS_TB1 memory access select
2	LS_TB0		LS_TB0 memory access select
1	LIN_TB		LIN_TB memory access priority
0	Reserved		Reserved

6.7 VPSS System Configuration (VPSS) Registers

This section contains information about the VPSS system configuration (VPSS) register.
0x1d

Table 6-314. VPSS System Configuration (VPSS) Registers

Offset	Acronym	Register Description	Section
0h	VPBE_CLK_CTRL	VPBE Clock Control Register	Section 6.7.1

6.7.1 VPBE Clock Control (VPBE_CLK_CTRL) Register

The peripheral clock control register is shown in Figure 6-307 and described in Table 6-315.

Figure 6-307. VPBE Clock Control (VPBE_CLK_CTRL) Register

31–8
Reserved
R-0

7	6	5	4	3	2	1	0
LDC_CLK_SEL	OSD_CLK_SEL	Reserved	Reserved	LDC_CLK_ENABLE	CLKSEL_VENC	Reserved	VPBE_CLK_ENABLE
R/W-0	R/W-0	R-0	R/W-1	R/W-1	R/W-0	R-0	R/W-1
			1	1	1	0	1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-315. VPBE Clock Control (VPBE_CLK_CTRL) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0
7	LDC_CLK_SEL		LDC memory clock select
		0	OSD module has access to memory
		1	ARM has access to memory
6	OSD_CLK_SEL		OSD memory clock select
		0	OSD module has access to memory
		1	ARM has access to memory
5	Reserved	0	Reserved
4	Reserved	0	Reserved
3	LDC_CLK_ENABLE		LDC clock enable
		0	Disable
		1	Enable
2	CLKSEL_VENC		VENC clock select
		0	ENC_CLOCK 1
		1	ENC_CLOCK/2
1	Reserved	0	Any writes to these bit(s) must always have a value of 0
0	VPBE_CLK_ENABLE		OSD, VENC clock enable
		0	Disable
		1	Enable

Revision History (Revision C)

This section highlights the technical changes made to the SPRUFG8B device-specific user's guide to make it a SPRUFG8**C** revision.

Table 7-1. Revision C Updates

Location	Additions/Deletions/Edits
Figure 4-4	Updated figure.
Section 4.3.11	Changed 5th sentence, 2nd paragraph.
Section 4.3.11.1	Corrected equation.
Table 5-2	Removed 2DLSCCFG.ENABLE from table.
Section 6.1	Exposed registers from Offset 11Ch to 130h.

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