


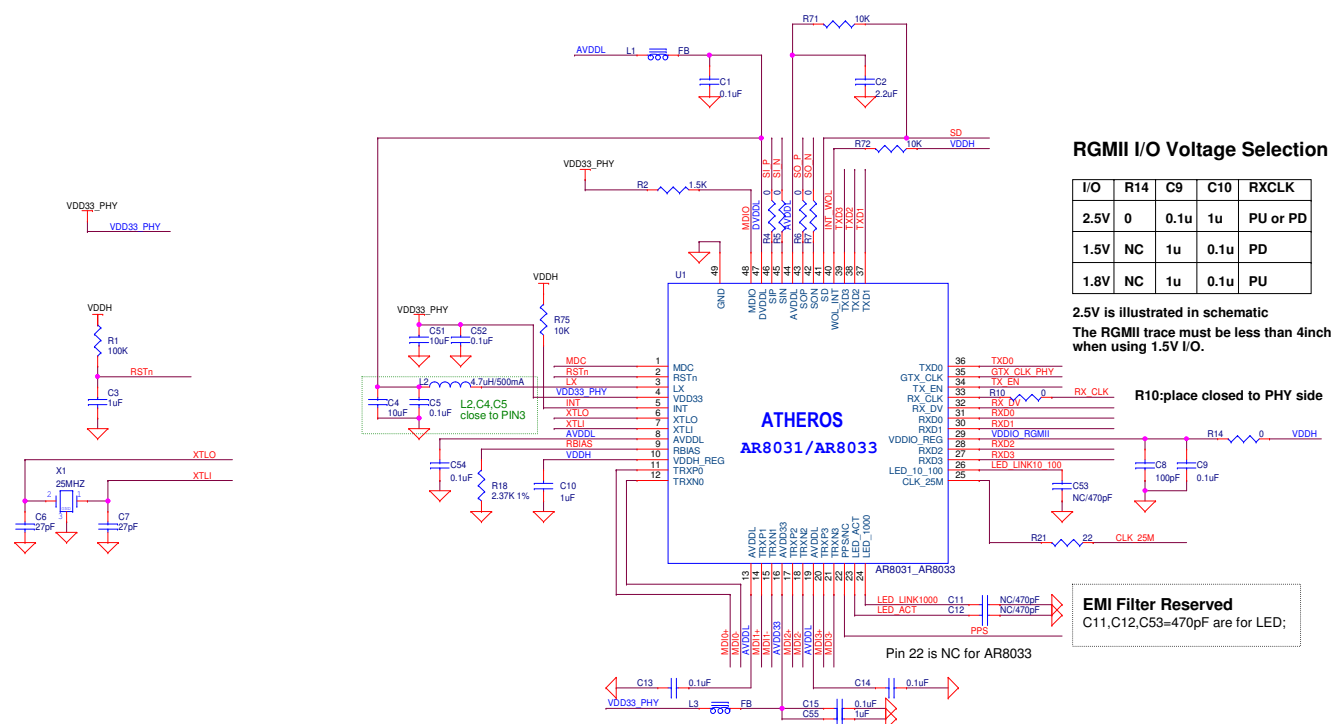
DATE	REVISION NUMBER	INITIALS	DESCRIPTION
02/09/2011	AR8031/33 Reference Design V1.0	Izhou	INITIAL REVISION
08/30/2011	AR8031/33 Reference Design V1.1	nyin	Update pin44 decoupling capacitor C2 from 0.1uF to 2.2uF

# AR8031/33 Reference Design V1.1

## AR8031/33: GbE PHY Transceiver

**ATHEROS CONFIDENTIAL  
PRELIMINARY**

 <b>Atheros Communications, Inc.</b> <small>5480 Great America Parkway Santa Clara, CA 95054</small>		Title <b>Title and Rev</b>	
Date	Tuesday, August 30, 2011	Size	C
Rev	1.0	Sheet	1 of 3
DWG NO <b>AR8031/33 Reference Design V1.1</b>			



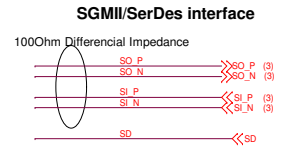
**RGMI I/O Voltage Selection**

I/O	R14	C9	C10	RXCLK
2.5V	0	0.1u	1u	PU or PD
1.5V	NC	1u	0.1u	PD
1.8V	NC	1u	0.1u	PU

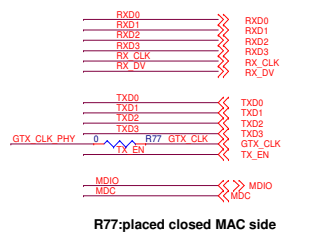
2.5V is illustrated in schematic  
The RGMI trace must be less than 4inch when using 1.5V I/O.

R10: place closed to PHY side

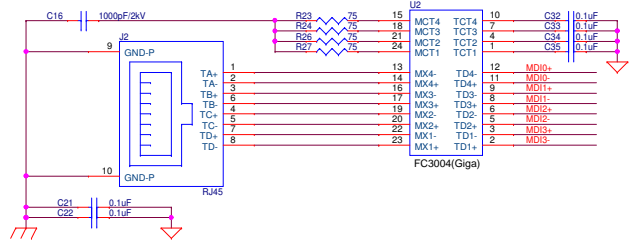
**EMI Filter Reserved**  
C11, C12, C53=470pF are for LED;



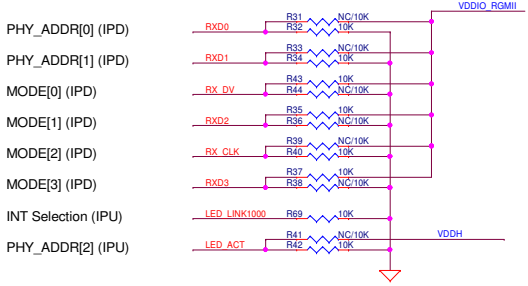
**To RGMI&SMI interface at MAC side**



**Other Signals to control host**



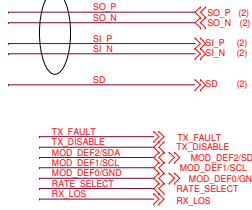
**Power-on Strapping Pins**



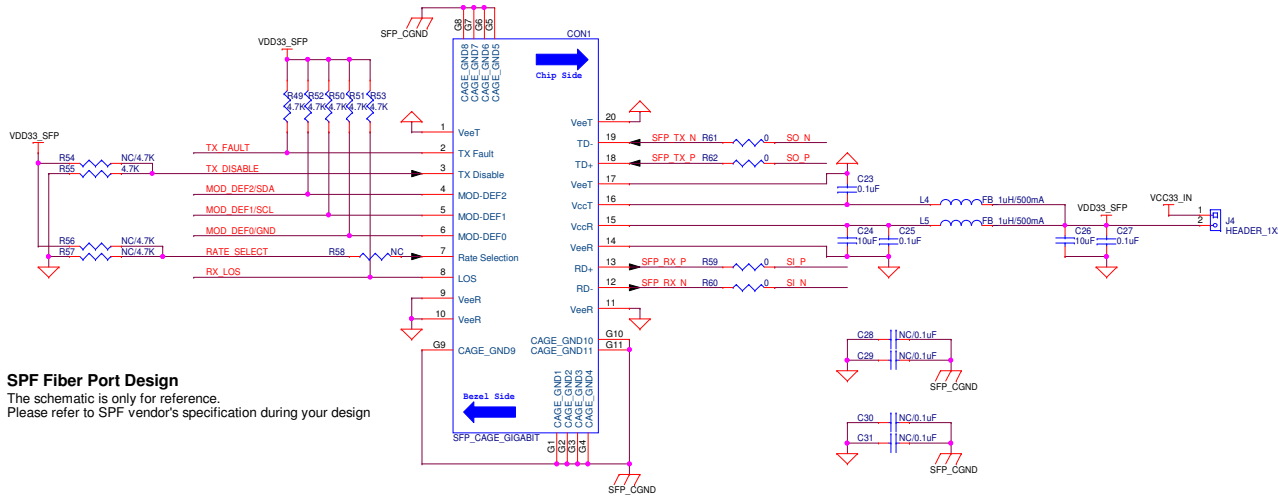
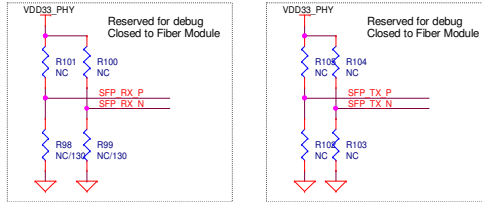
**MODE[3:0]**  
1011 Auto-Media Selection (In schematic)  
0000 1000BASE-T, RGMII;  
0001 1000BASE-T, SGMII;  
0010 1000BASE-X, RGMII, 50Ω;  
0011 1000BASE-X, RGMII, 75Ω;  
0100 1000M Converter, 50Ω;  
0101 1000M Converter, 75Ω;  
0110 100BASE-FX, RGMII, 50Ω;  
0111 100M Converter, 50Ω;  
1110 100BASE-FX, RGMII, 75Ω;  
1111 100M Converter, 75Ω;

PHY Address: 5b'00000

100Ohm Differential Impedance



## SGMII/SerDes Interface



**SFP Fiber Port Design**  
The schematic is only for reference.  
Please refer to SFP vendor's specification during your design