Powering the AM335x With the TPS650250

This document details a power solution for the AM335x application processor with a TPS650250 Power Management Unit (PMU) or Power Management IC (PMIC).

Portable application solution size demands a high level of integration and the AM335x requires at least three different voltage rails with specific power-on and power-off sequencing requirements. The TPS650250 is a highly integrated power solution that provides the 1.8-, 3.3-, and 1.1-V rail signals required by the AM335x. The TPS650250 has three step-down converters, three low-dropout (LDO) regulators, and a voltage supervisor.

This document can be used as a reference for connectivity between the TPS650250 and the AM335x.

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1 Power Requirements

Figure 1 shows a block diagram of the TPS650250-AM335x interface. A detailed circuit schematic detailing the power solution (TPS650250 and sequencing circuit) is found in Figure 2

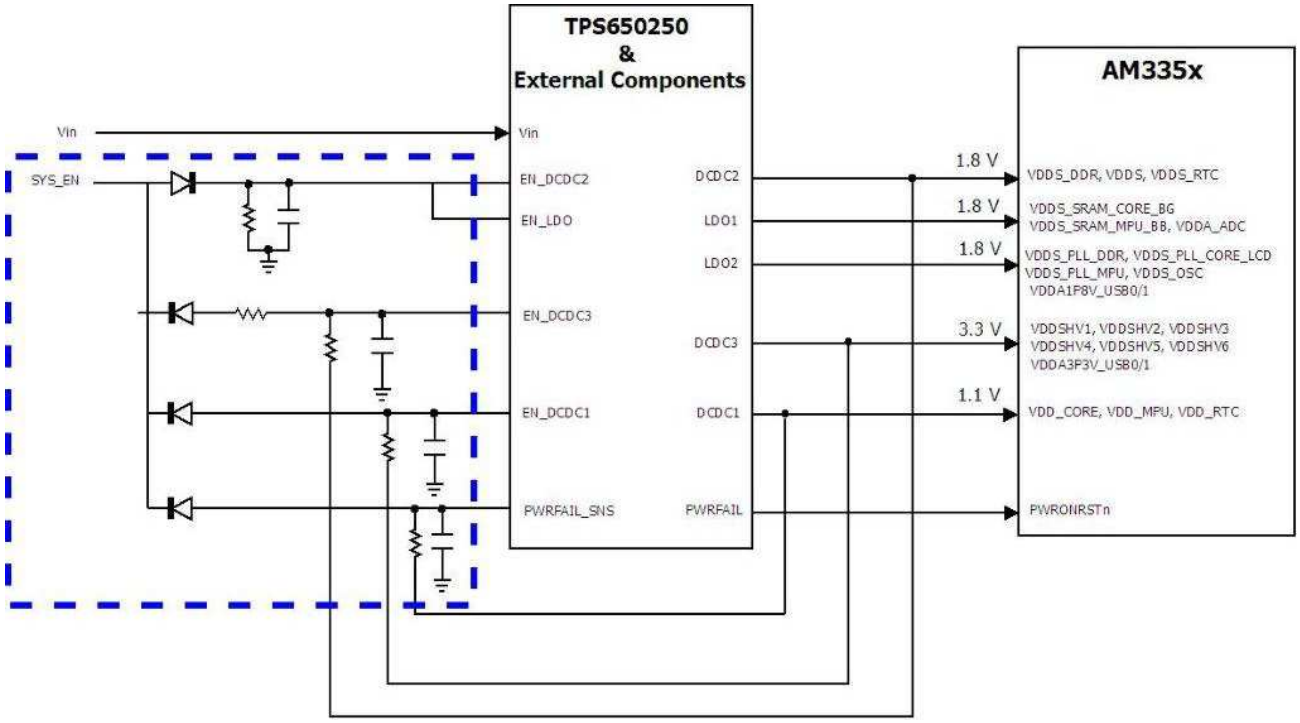


Figure 1. TPS650250 with Sequencing Circuit and AM335x Functional Block Diagram

The AM335x power requirements are listed on Table 1.

Table 1. AM335x Power Requirements

TPS650250						AM335x			
Power-Up Sequence	Power-Down Sequence	Power Supply	Vout [V]	Iout [mA]	Output Voltage [V]	Power Supply	Nominal Rating	Grouping	Max Current [mA]
3	1	DCDC1	2.8, 3.3, Adjustable	1600	1.1	VDD_CORE, VDD_MPU, VDD_RTC	1.1 V ±4%	1.1-V Core	902
1	3	DCDC2	1.8, 2.5, Adjustable	800	1.8	VDDS_DDR, VDDS, VDDS_RTC, VDDSHVx	1.8 V ±5%	1.8-V IO	605
2	2	DCDC3	Adjustable	800	3.3	VDDA3P3V_USB0, VDDA3P3V_USB1, VDDSHVx	3.3 V ±5%	3.3-V Analog and IO	370
1	3	VLDO1	1-3.3	200	1.8	VDDS_SRAM_MPU_BB, VDDS_SRAM_CORE_BG, VDDA_ADC	1.8 V ±5%	1.8-V Analog	30
1	3	VLDO2	1-3.3	200	1.8	VDDS_PLL_DDR, VDDS_PLL_MPU, VDDS_PLL_CORE_LCD, VDDS_OSC, VDDA1P8V_USB0, VDDA1P8V_USB1	1.8 V ±5%	1.8-V Analog	125
		VLDO3	1.0	30	1.0	n/a	n/a	n/a	n/a

The TPS650250 meets these power requirements with its three step-down converters and three LDO regulators. A simple sequencing circuit is needed to meet power-sequence requirements. This document details a power-sequencing solution for the RTC feature disable as described in the AM335x data sheet (SPRS717) and timing diagram *Figure 4-5. Power Supply Sequencing with RTC Feature Disabled*.

1.1 Power-On Sequence

According to the excerpt from the AM335x datasheet, the device must be powered on in the following order:

1. 1.8-V Analog and I/O
2. 3.3-V Analog and I/O
3. 1.1-V Core

An external system enable signal, SYS_EN, is enabled HIGH for power up. Diodes D2, D3, and D4 are reversed biased. Diode D1 is forward biased and EN1.8 is HIGH. This turns ON the 1.8-V rails DCDC2, LDO1, and LDO2. The output voltage of the DCDC2 converter, VO_1.8, is filtered into the enable of the DCDC3 converter EN3.3 and creates an RC (R7 and C12) delay before turning ON the 3.3-V rail. When EN3.3 reaches the turn-on threshold of the converter, VO_3.3 ramps up to nominal voltage. The output voltage of the DCDC3 converter, VO_3.3, is filtered into the enable of the DCDC1 converter EN1.1 and creates an RC (R16 and C15) delay before turning ON the 1.1 V rail. When EN1.1 reaches the turn-on threshold of the converter, VO_1.1 ramps up to nominal voltage. Lastly, the output voltage of the DCDC1 converter VO_1.1 is filtered into the power sense fail pin of the TPS650250 PWRRAIL_SNS and creates an RC (R17 and C16) delay between the last rail turning on and the Power On Reset signal, PWRONRSTn, pulling HIGH. The PWRFAIL_SNS signal is sensed through an internal comparator in the TPS650250 and triggers the PWRONRSTn signal HIGH when PWRRAIL_SNS reaches 1 V.

Power-on sequence is complete. The proper connections for this power-on sequencing are shown in Figure 2.

1.2 Power-Off Sequence

As shown in the excerpt from the AM335x data sheet, the device must be powered off in reverse order as power-on.

1. 1.1-V Core
2. 3.3-V Analog and I/O
3. 1.8-V Analog and I/O

SYS_EN is LOW for power down. D2, D3, and D4 are forward biased. PWRFAIL_SNS becomes LOW to pull PWRONRSTn LOW. EN1.1 becomes LOW and VO_1.1 ramps down. EN3.3 signal is filtered to create an RC (R3 and C12) delay between VO_1.1 ramping down and VO_3.3 ramping down. Lastly, D1 is reversed biased and capacitor C11 discharges through resistor R2 with a delay longer than the ramping down of VO1.1 and VO3.3. After VO1.1 and VO3.3 are off, the 1.8-V rail ramps down.

Power-off sequence is complete.

The proper connections for this power-off sequencing are shown in Figure 2.

2 Schematic

Figure 2 shows the circuit schematic detailing the external components required by the TPS650250 to achieve the 1.8-, 3.3-, and 1.1-V power rails required by the AM335x. In addition, Figure 2 shows the sequencing circuit that achieves the proper power-on, power-off, and PWRONRSTn sequencing required by the AM335x.

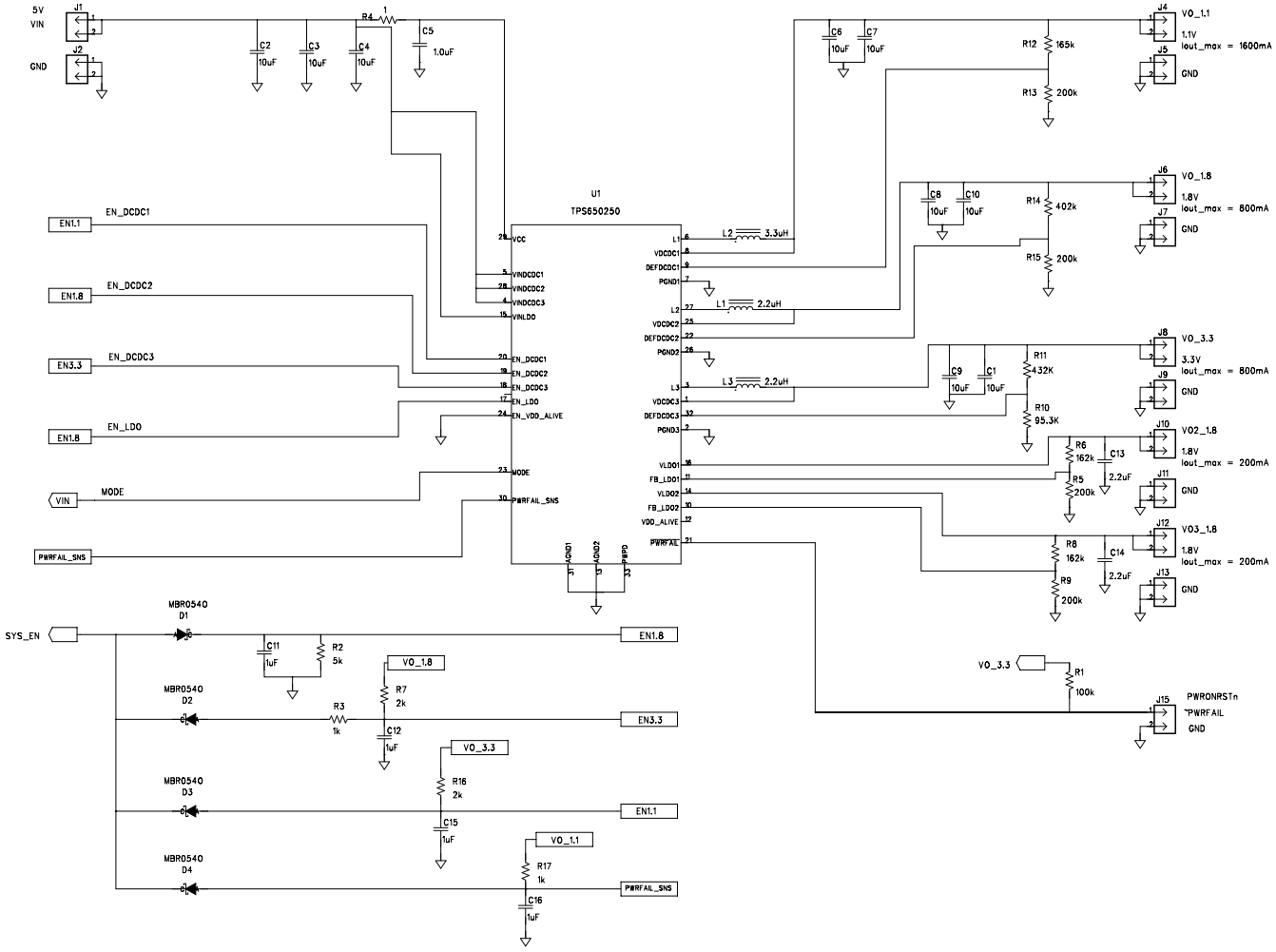
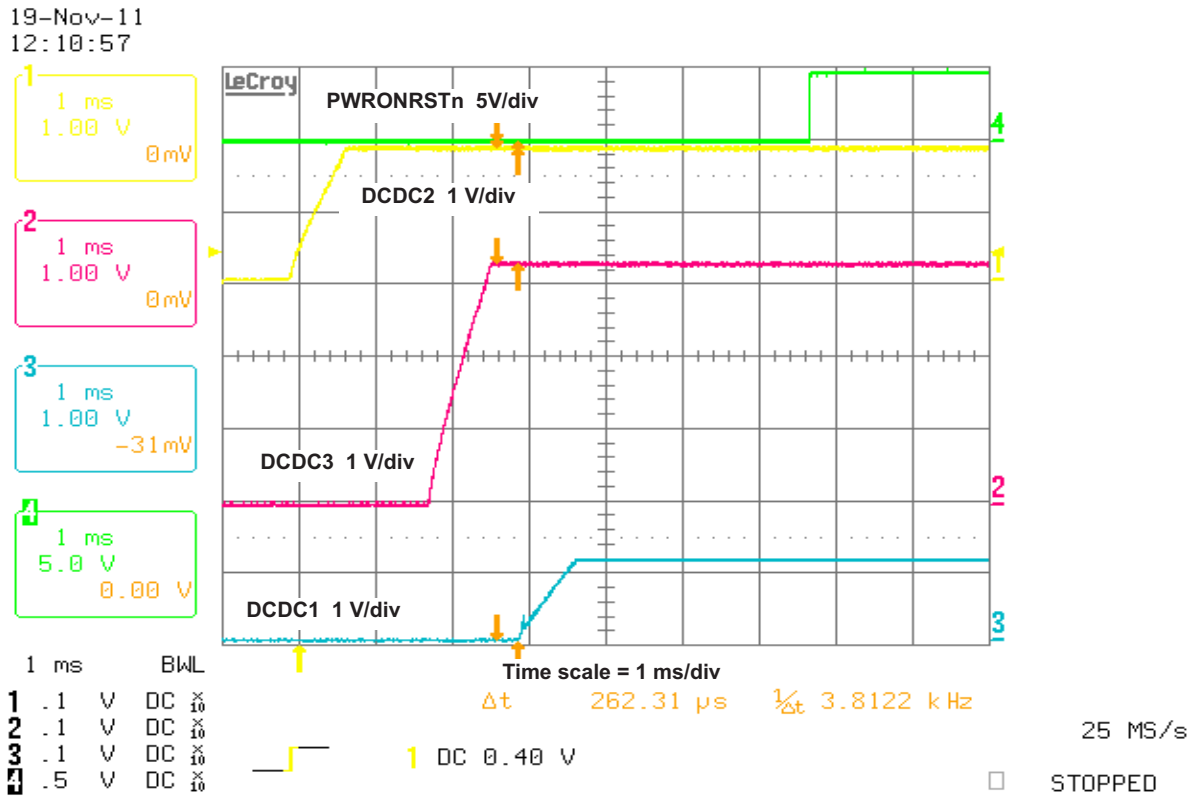


Figure 2. TPS650250 Powering and Sequencing Circuit for the AM335x Powering Requirements

3 Waveforms

The following waveforms demonstrate the power-on and power-off sequence of the TPS650250 as required by the AM335x.

Figure 3 shows the power-on sequence for each of the output voltage rails and the PWRONRSTn signal. The 1.8-, 3.3-, and 1.1-V rails turn on sequentially and the PWRONRSTn signal goes HIGH after all rails are ON.



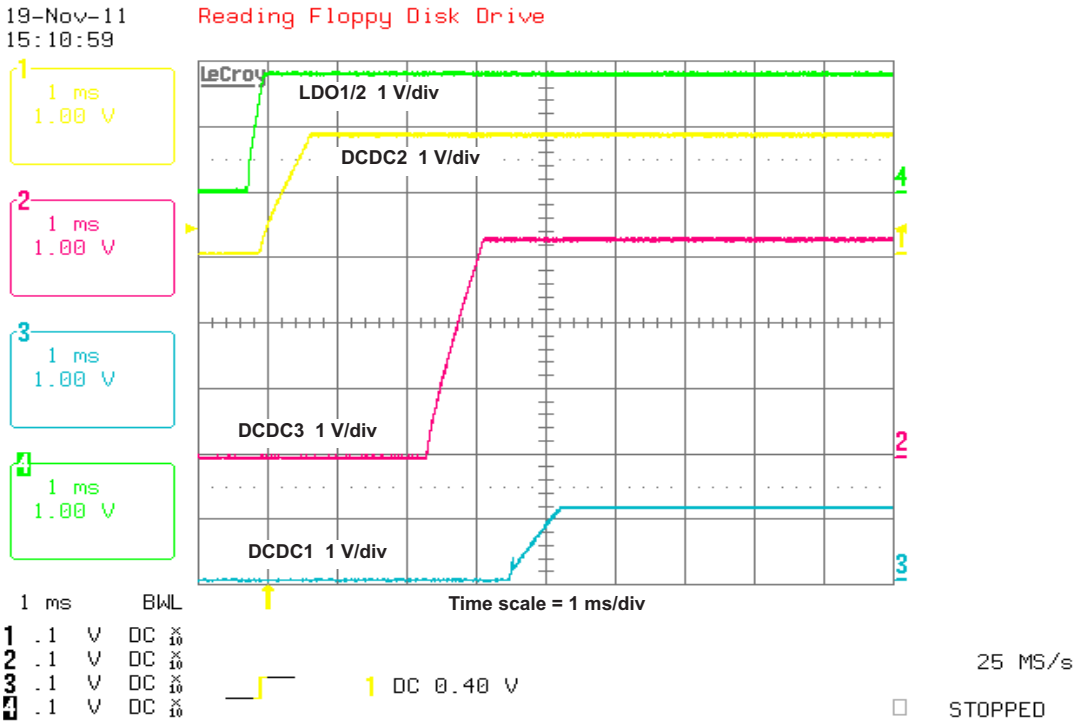
1.8-V (DCDC2), 3.3-V (DCDC3), and 1.1-V (DCDC1) Rails

Figure 3. Power-on Sequence With PWRONRSTn

Figure 4 shows the power-on sequence for each of the output voltages of the TPS650250. DCDC2 (1.8 V) and the LDOs (1.8 V) of the TPS650250 turn on before DCDC3 (3.3 V) and DCDC1 (1.1 V).

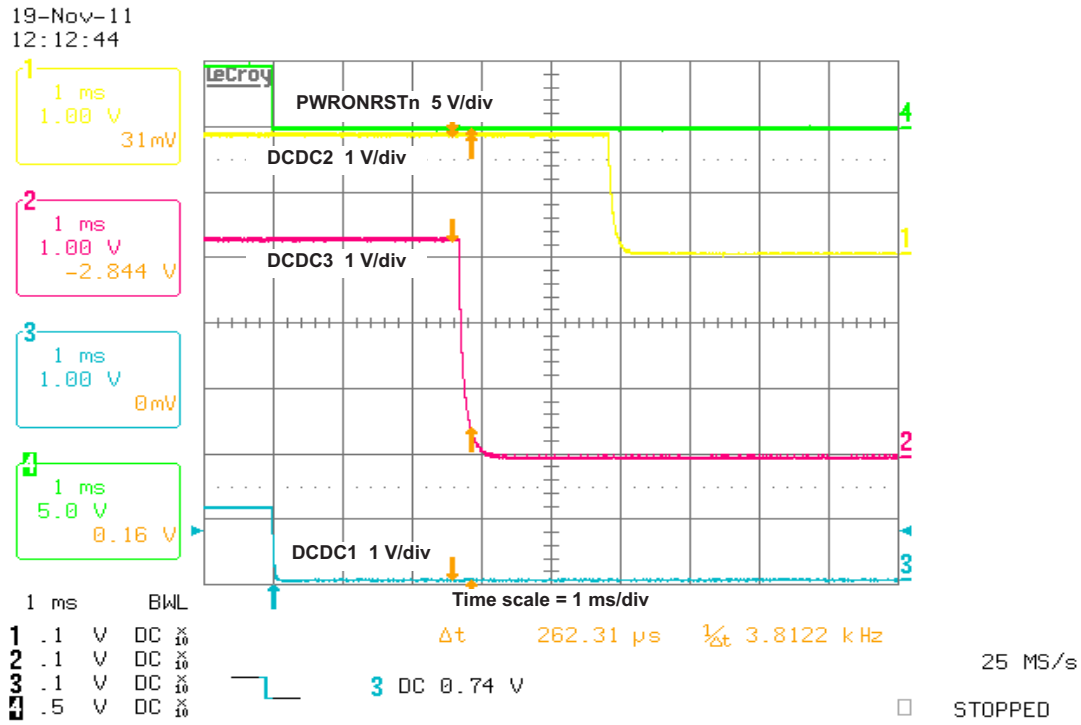
Figure 5 shows the power-off sequence for each of the output voltage rails and the PWRONRSTn signal. The 1.8-, 3.3-, and 1.1-V rails turn off sequentially and the PWRONRSTn signal goes LOW when the 1.1-V rail begins to ramp down.

Figure 6 shows the power-off sequence for each of the output voltages of the TPS650250. DCDC2 (1.8 V) and the LDOs (1.8 V) of the TPS650250 turn off after DCDC1 (1.1 V) and DCDC3 (3.3 V) have ramped down.



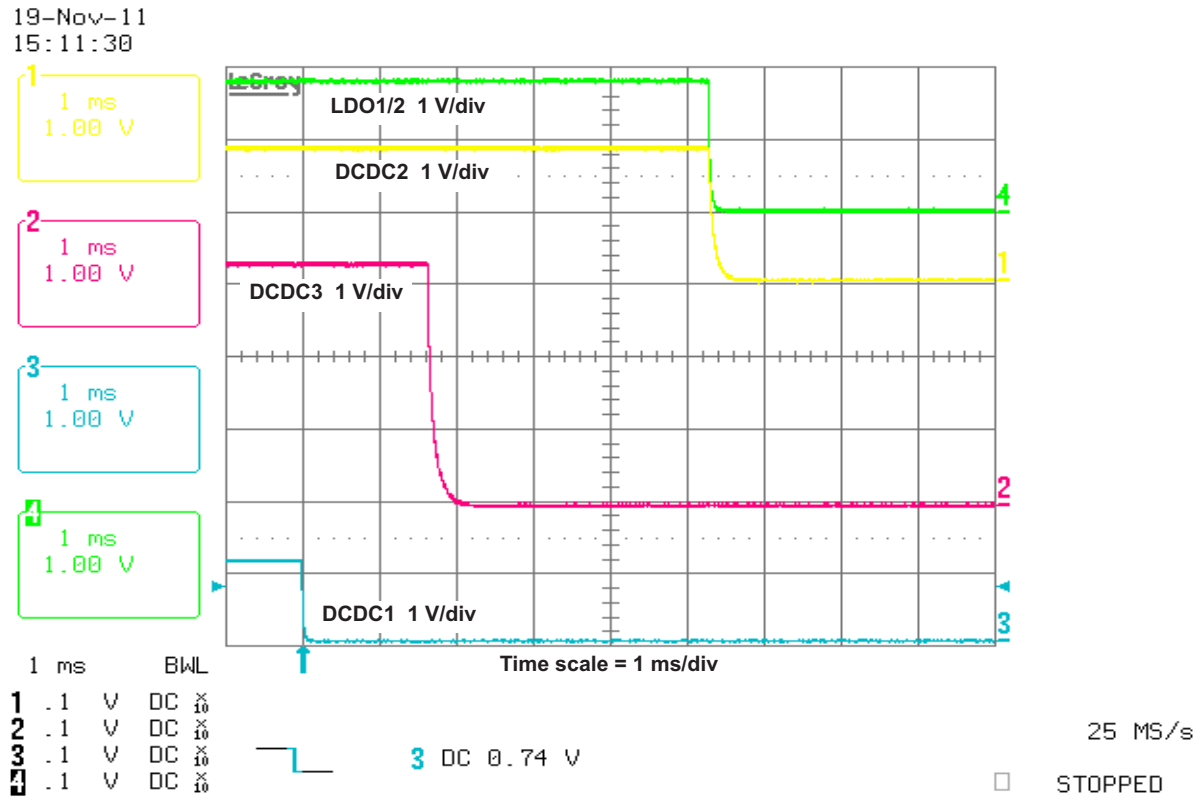
1.8-V (DCDC2,LDO1/2), 3.3-V (DCDC3), and 1.1-V (DCDC1) Rails

Figure 4. Power-on Sequence for the TPS650250 Converter Rails



1.8-V (DCDC2), 3.3-V (DCDC3), and 1.1-V (DCDC1) Rails

Figure 5. Power-off Sequence With PWRONRSTn



1.8-V (DCDC2,LDO1/2), 3.3-V (DCDC3), and 1.1-V (DCDC1) Rails

Figure 6. Power-off Sequence for the TPS650250 Converter Rails

4 Bill of Materials

The bill of materials is displayed in Table 2.

Table 2. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C2	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C3	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C4	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C5	1.0 µF	Capacitor, ceramic, 6.3 V, X5R,10%	0603	Std	Std
1	C6	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C7	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C8	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C9	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C10	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C11	1 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C12	1 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C13	2.2 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0603	Std	Std
1	C14	2.2 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0603	Std	Std
1	C15	1 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	C16	1 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	Std	Std
1	D1	MBR054O	Diode, Schottky, 0.5 A, x0V	SOD-123	MBR054O	MCC Semi
1	D2	MBR054O	Diode, Schottky, 0.5 A, x0V	SOD-123	MBR054O	MCC Semi
1	D3	MBR054O	Diode, Schottky, 0.5 A, x0V	SOD-123	MBR054O	MCC Semi
1	D4	MBR054O	Diode, Schottky, 0.5 A, x0V	SOD-123	MBR054O	MCC Semi
1	L1	2.2 µH	Inductor, SMT, 1.72 A, 59 mΩ	0.157 × 0.157 inch	VLCF4020T-2R2N1R7	TDK
1	L2	3.3 µH	Inductor, SMT, 1.52 A, 78 mΩ	0.157 × 0.157 inch	VLCF4020T-3R3N1R5	TDK
1	L3	2.2 µH	Inductor, SMT, 1.72 A, 59 mΩ	0.157 × 0.157 inch	VLCF4020T-2R2N1R7	TDK
1	R1	100 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R2	5 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	R3	1 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	R4	1 Ω	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	R5	200 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R6	162 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R7	2 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	R8	162 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R9	200 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R10	95.3 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R11	432 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R12	165 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R13	200 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R14	402 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R15	200 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R16	2 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	R17	1 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	U1	TPS650250	IC, Power Management ICs for Li-Ion Powered Systems	QFN-32	TI	

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG components.

5 Using the TPS650250 to Support DDR3

The TPS650250 provides the power required by the AM335x and is capable of supporting external DDR3 memory applications. However, the 1.8-V I/O output current capabilities are reduced from what was presented in Section 1. Table 3 shows the power requirements for powering the AM335x with DDR3 support.

Table 3. AM335x Power Requirements for Supporting DDR3

TPS650250						AM335x			
Power-Up Sequence	Power-Down Sequence	Power Supply	Vout [V]	Iout [mA]	Output Voltage [V]	Power Supply	Nominal Rating	Grouping	Max Current [mA]
4	1	DCDC1	2.8, 3.3, Adjustable	1600	1.1	VDD_CORE, VDD_MPU, VDD_RTC	1.1 V ± 4%	1.1-V Core	902
2	3	DCDC2	1.8, 2.5, Adjustable	800	1.5	VDDS_DDR	1.5 V ± 5%	1.5-V DDR3	300
3	2	DCDC3	Adjustable	800	3.3	VDDA3P3V_USB0, VDDA3P3V_USB1, VDDSHVx	3.3 V ±5%	3.3-V Analog and IO	370
1	4	VLDO1	1–3.3	200	1.8	VDDS_SRAM_MPU_BB, VDDS_SRAM_CORE_BG, VDDA_ADC, VDDSHVx,VDDS_PLL_DDR, VDDS_PLL_MPU, VDDS_PLL_CORE_LCD, VDDS_OSC, VDDA1P8V_USB0, VDDA1P8V_USB1	1.8 V ± 5%	1.8-V Analog	155
1	4	VLDO2	1–3.3	200	1.8	VDDS, VDDS_RTC, VDDSHVx	1.8 V ± 5%	1.8-V IO	55
		VLDO3	1.0	30	1.0	n/a	n/a	n/a	n/a

On the TPS650250, DCDC2 is dedicated to 1.5 V to support external DDR3 applications. The AM335x DDR3 I/O domain (VDDS_DDR) must be 1.5 V, leaving 500 mA of available current for external DDR3 memory.

The 1.8-V I/O domains (VDDSHVx) are now powered through the 1.8-V rails, VLDO1 and VLDO2, of the TPS650250. The added loads cause current constraints on LDO1 and LDO2 so as not to go over the rated current of 200 mA. Therefore, the AM335x must be operated such that VDDSHVx does not cause each LDO current to exceed 200 mA on VLDO1 or VLDO2.

5.1 Adjusting DCDC2 to 1.5 V

A 1.5-V rail is required to power DDR3. If R15 is 200 kΩ, change R14 to 301 kΩ to adjust the output voltage of DCDC2 to 1.5 V. Figure 7 shows this change of the resistor divider for DCDC2.

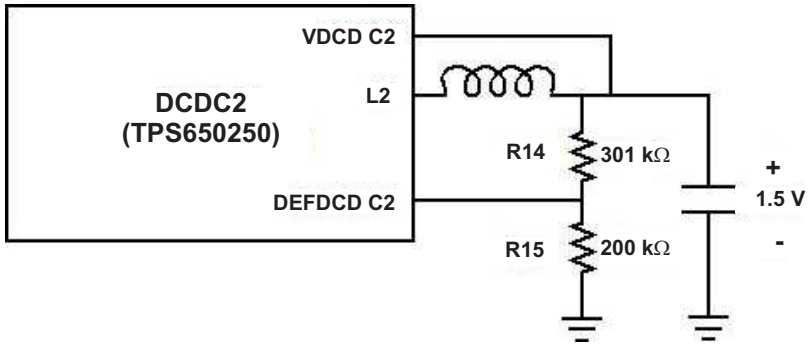


Figure 7. DCDC2 Resistor Change (R14) to Achieve 1.5 V

6 Use of a Clamping Circuit for Simultaneous Ramp Down

Reading the datasheet for the AM335x, (SPRS717), and the challenge when ramping down VDDS and VDDSHVx [1–6] simultaneously is obvious. “If it is desired to ramp down VDDS and VDDSHVx [1–6] simultaneously, it should always be ensured that the difference between VDDS and VDDSHVx [1–6] during the entire power-down sequence is < 2 V. If this is violated it can result in reliability risks for the device.” This only refers to 1.8-V VDDS and 3.3-V VDDSHVx rails. The worst-case scenario of this issue is the 3.3-V rail remains high possibly because of large output capacitance or no load being present on the output while, the 1.8-V rail ramps down quickly such as if it were fully loaded.

A solution to this issue is the use of a clamping circuit between the 1.8-V VDDS and 3.3-V VDDSHVx rails, ensuring proper shutdown when V_{IN} is removed. As illustrated in Figure 8, the clamping circuit suggested is only five additional components, 3 of which are resistors. The TLVH431 is regulated at 1.5 V through resistor divider R1 and R2. Before the rails ramp down, Q1 is off. When the 1.8-V rail drops, Vbase drops and Q1 turns ON. The 3.3-V rail discharges through Q1 and the 1.8-V rail. This technique ensures that the difference between the 3.3-V VDDSHVx rails and the 1.8-V VDDS rail never exceeds 2 V.

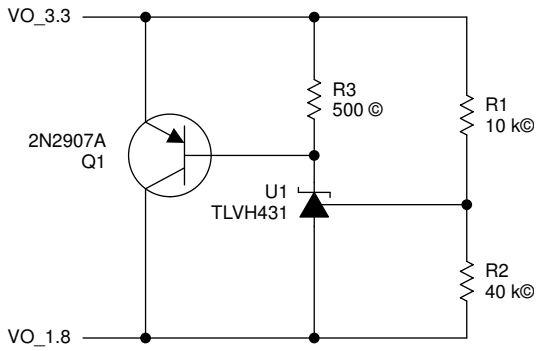


Figure 8. Clamping Circuit

Figure 9 shows the power-down sequence for the DCDCs, LDOs and PWRONRSTn outputs and signals of the TPS650250 without the clamping circuit. This is the worst-case scenario since the VDDSHVx 3.3-V rail is not loaded at all while the VDDS 1.8-V rail is fully loaded. Notice that the difference between DCDC3 and DCDC2 (VDDSHVx and VDDS) exceeds 2 V. See Table 4 for more testing details.

Figure 10 shows the power-down sequence for the DCDCs, LDOs and PWRONRSTn output voltages of the TPS650250 with the clamping circuit. With the same load conditions, the clamp circuit test results show the difference between DCDC3 and DCDC2 is kept below 2 V. Notice how the 3.3-V rail tracks the 1.8-V rail. Refer to Table 4 for more testing details.

Table 4. Clamp Circuit Testing

Rail	Current Load
DCDC1 1.1 V	1000 mA
DCDC2 1.8 V	600 mA
DCDC3 3.3 V	0.01 mA
LDOs 1.8 V	200 mA

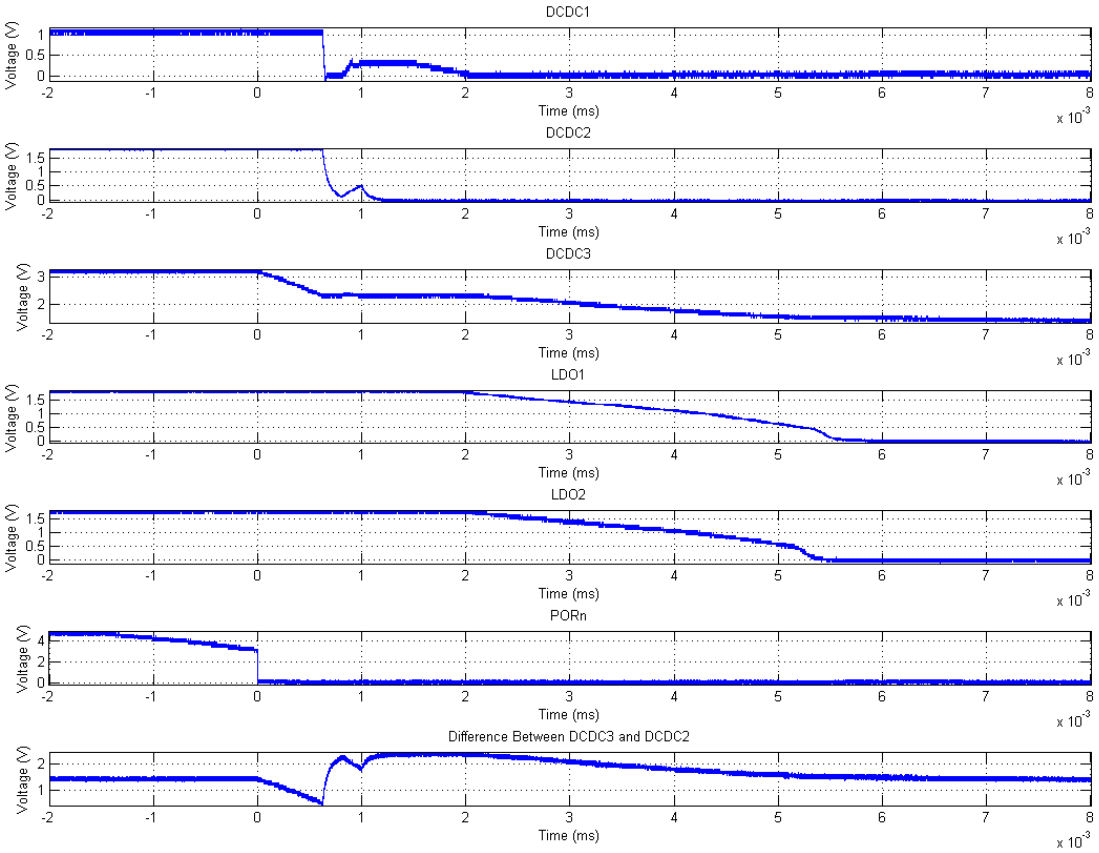


Figure 9. TPS650250 Shutdown without Clamping Circuit

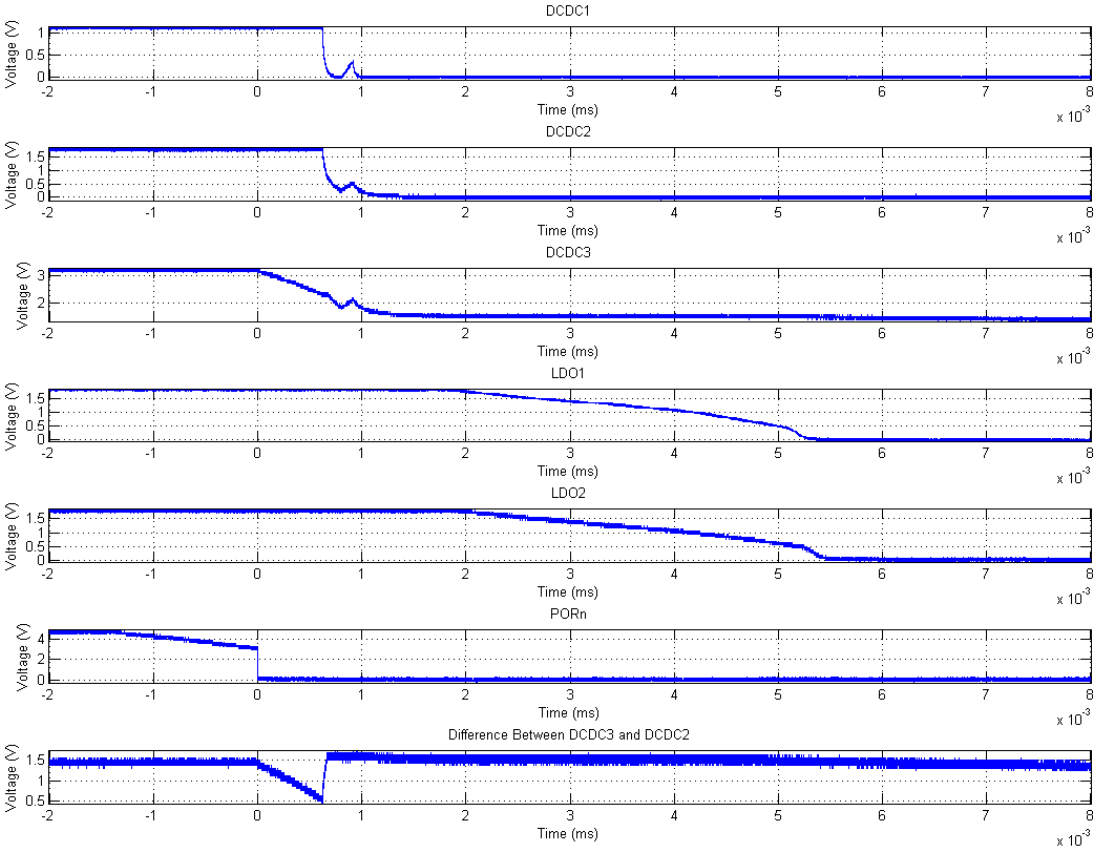


Figure 10. TPS650250 Shutdown with Clamping Circuit

7 Conclusion

The TPS650250 provides a low-cost, comprehensive power solution for the AM335x. This reference design demonstrates the external components of the TPS650250 to provide the required voltage rails and a simple sequencing circuit that meets power-on and power-off sequencing required by the AM335x. For external DDR3 applications, the output voltage of DCDC2 for the TPS650250 can be easily adjusted to accommodate a 1.5-V rail. However, this limits the output-current capabilities of the 1.8-V I/O Domains (VDDSHVx) in the AM335x. If simultaneous ramp down of the VDDSHVx and VDDS rail is desired a clamping circuit may be required.

8 References

1. *TPS650250, Power Management IC for Li-Ion Powered Systems* data sheet (SLVS843)
2. *AM335x, AM335x ARM® Cortex™-A8 Microprocessors (MPUs)* data sheet (SPRS717)

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This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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