GENERAL NOTES, UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES IN OHMS.
2. CAPACITANCE VALUES IN MICROFARADS.
3. REFERENCE DESIGNATORS USED:
   - A. JTAG HEADERS:
   - B. INTEGRATED CIRCUTS:
   - C. CERAMIC CAPS:
   - D. ELECTROLYTIC CAPS:
   - E. RESISTORS:
   - F. CONNECTORS/HEADERS:
   - G. CRYSTALS:
   - H. JUMPERS:
   - I. EMI FILTERS:
   - J. FERRITE BEADS:
   - K. FUSES:
   - L. DIODES:
   - M. SWITCHES:
   - N. TEST POINTS:
4. THE FOLLOWING INTEGRATED CIRCUITS ARE SOCKETED: U23 & U40
5. OBSERVE THE FOLLOWING SPECIFIC NOTES:

   FORMAT: PAGENUMBER.NOTENUMBER

   3.1-3.7, 4.1-4.3, 5.1-5.3, 6.1-6.8, 7.1-7.3, 8.1-8.3, 9.1-9.4, 10.1-10.4, 11.1-11.2, 12.1, 13.1-13.4, 14.1-14.2, 15.1-15.7, 16.1-16.6, 17.1-17.3, 18.1-18.3, 19.1-19.3, 20.1-20.3, 21.1, 22.1, 23.1-23.4, 24.1-24.4

6. ALL 0.1 uF CAPACITORS ARE BYPASS CAPS UNLESS OTHERWISE NOTED. THEY ARE SHOWN ON THE PAGE WITH THE INTEGRATED CIRCUITS THEY SHOULD BE PLACED NEAR.
7. PRINTED CIRCUIT BOARD PROPERITES:
   - A. ROUTE TO WITHIN 10% OF MANHATTAN DISTANCE
   - B. 100 OHM DIFFERENITAL IMPEDANCE. SINGLE ENDED IMPEDANCE APPROXIMATELY 60 OHMS, CONTROLLED BY DIFFERENTIAL IMPEDANCE.
   - C. FR4 BOARD MATERIAL
   - D. PCB TO PCI 2.1 SIZE SPECIFICATIONS. EXCESS HEIGHT ALLOWED FOR TOP CONNECTORS.
   - E. THERMAL RELIEFS ONLY TO BE USED ON VIAS FOR THROUGH HOLE PARTS. VIAS FOR SURFACE MOUNT PARTS AND ROUTING SHALL NOT USE THERMAL RELIEFS.

SCHEMATIC CONTENTS:

Primary I2C Address Table

ADDRESS HEX	ADDRESS BINARY	DEVICE	FUNCTION
0x18	0011000B	AIC33	Analog Audio I/O CH1 and CH2
0x19	0011001B	AIC33	Analog Audio I/O CH3 and CH4
0x1A	0011010B	AIC33	Analog Audio I/O CH5 and CH6
0x1B	0011011B	AIC33	Analog Audio I/O CH7 and CH8
0x20	0100000B	THS8200	HD Video Encoder
0x44	1000100B	SAA7015H	SD Video Encoder
0x5C	1011100B	TVP7000	HD Video Decoder
0x5E	1011110B	TVP5154	SD Video Decoder CH5-CH8
0x5F	1011111B	TVP5154	SD Video Decoder CH1-CH4
0xXX	xxxxxxxB	MSP430	EVM Supervisor Software Programmable
0xXX	xxxxxxxB	DM648	DM648 DSP Software Programmable

Secondary I2C Address Table

ADDRESS HEX	ADDRESS BINARY	DEVICE	FUNCTION
0x21	0100001B	PCA9535W	MSP430 I2C IO Expander
0x22	0100010B	PCA9535W	MSP430 I2C IO Expander for Bootmodes
0x23	0100011B	PCA9535W	MSP430 I2C IO Expander for Reset & Power
0x69	1101001B	CDCE906	Clock Generator Control via SMBus
0xXX	xxxxxxxB	MSP430	EVM Supervisor Software Programmable

Title	DM648 EVM - Title Page	
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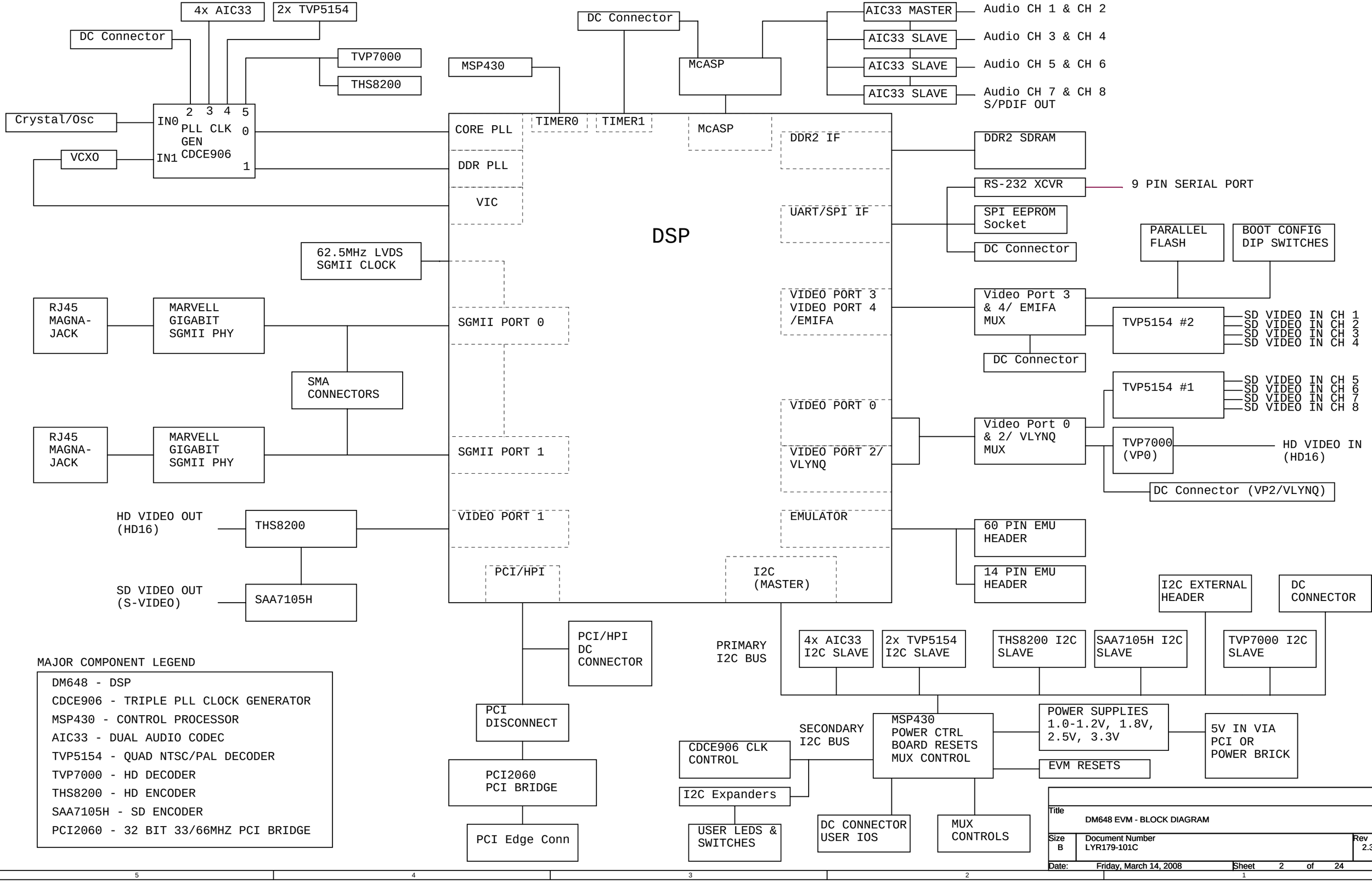

MAJOR COMPONENT LEGEND

- DM648 - DSP
- CDCE906 - TRIPLE PLL CLOCK GENERATOR
- MSP430 - CONTROL PROCESSOR
- AIC33 - DUAL AUDIO CODEC
- TVP5154 - QUAD NTSC/PAL DECODER
- TVP7000 - HD DECODER
- THS8200 - HD ENCODER
- SAA7105H - SD ENCODER
- PCI2060 - 32 BIT 33/66MHZ PCI BRIDGE

Title: DM648 EVM - BLOCK DIAGRAM		
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NOTE 3.2: PLACE R25, R26, AND R27 CLOSE TO U26.
NOTE 3.3: PLACE R21-R23, R105-R108 CLOSE TO U26.
NOTE 3.4: PLACE R109 CLOSE TO U27.
NOTE 3.5: PLACE R110 CLOSE TO U23.
NOTE 3.6: PLACE R112 AND R111 CLOSE TO U28.
NOTE 3.7: PLACE BYPASS CAPS ON THIS PAGE (0.1uF) NEAR THE ASSOCIATED DEVICES.

VCC_3V3
C568 0.1uF
C120 0.1uF
C183 0.1uF
C182 0.1uF
C181 0.1uF
U27 OSC 27 MHz
R109 33
U26 CDCE906PW
24 PLL_BYPASSn
24 CLOCK_STOPn
R314 5.6K
R315 5.6K
U62 SN74CB3T3306DCUR
24 SMB_DAT_CLK
24 SMBDAT
24 SMBCLK
R21 33 HDOUT_CLKIN 11
R22 33 HDIN_CLKIN 10
R23 33 TVP5154_CLKIN1 9
R24 33 TVP5154_CLKIN2 13
R108 33 AIC33_CLKIN1 15
R107 33 AIC33_CLKIN2 15
R106 33 AIC33_CLKIN3 15
R105 33 AIC33_CLKIN4 15
DC_CLK R25 33 TDC_CLK 4
DM648_CORE_CLKIN R26 33 TDM648_CORE_CLKIN
DM648_DDR2_CLKIN R27 33 TDM648_DDR2_CLKIN
U23L TMS320DM648
DC_SYSCLK4 4
R110 33
24 DM648_PORn
24 DM648_RESETn
24 DM648_NMI
DM648_RESET_STATn 4
TOUT1 24
DC_TOUT0 4
DC_TINP0 4
TINP1 24
STCLK 14
C180 NO-POP
C186 NO-POP
Y1 27MHz
C185 0.1uF
C622 0.1uF
R101 1K
R104 2.21K
R103 100K
TP21 TP-30
U29 PI6CX100-27W
R102 22.1K 1%
Q1 2N3904
C179 0.1uF
C178 100pF
C184 10pF
U28 SN74LVC2G34DBVR
R112 33
R111 33
VCTL

NOTE 3.1: THESE COMPONENTS TO BE PLACED CLOSE TOGETHER.

Title: DM648 EVM Reset and Clock Source		
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NOTE 4.1: PLACE BYPASS CAPS ON THIS PAGE (0.1uF) NEAR THE ASSOCIATED DEVICES.

NOTE 4.2: PLACE R503-R512, R516,R517 CLOSE TO U45.

NOTE 4.3: ALL PINS ON J15 AND J16 MAY BE SWIZZLED EXCEPT FOR GROUNDS.

J15 — 45X2

U45 — S29GL256N11FFI010

SW2 DIP_SWITCH-10 TDA10H0SK1

SW3 DIP_SWITCH-10 TDA10H0SK1

RN20 RPACK8-1.0K

RN22 RPACK8-1.0K

RN21 RPACK8-22K

RN23 RPACK8-22K

J16 — 45X2

Title	DM648 EVM Flash and Daughter Card Connectors	
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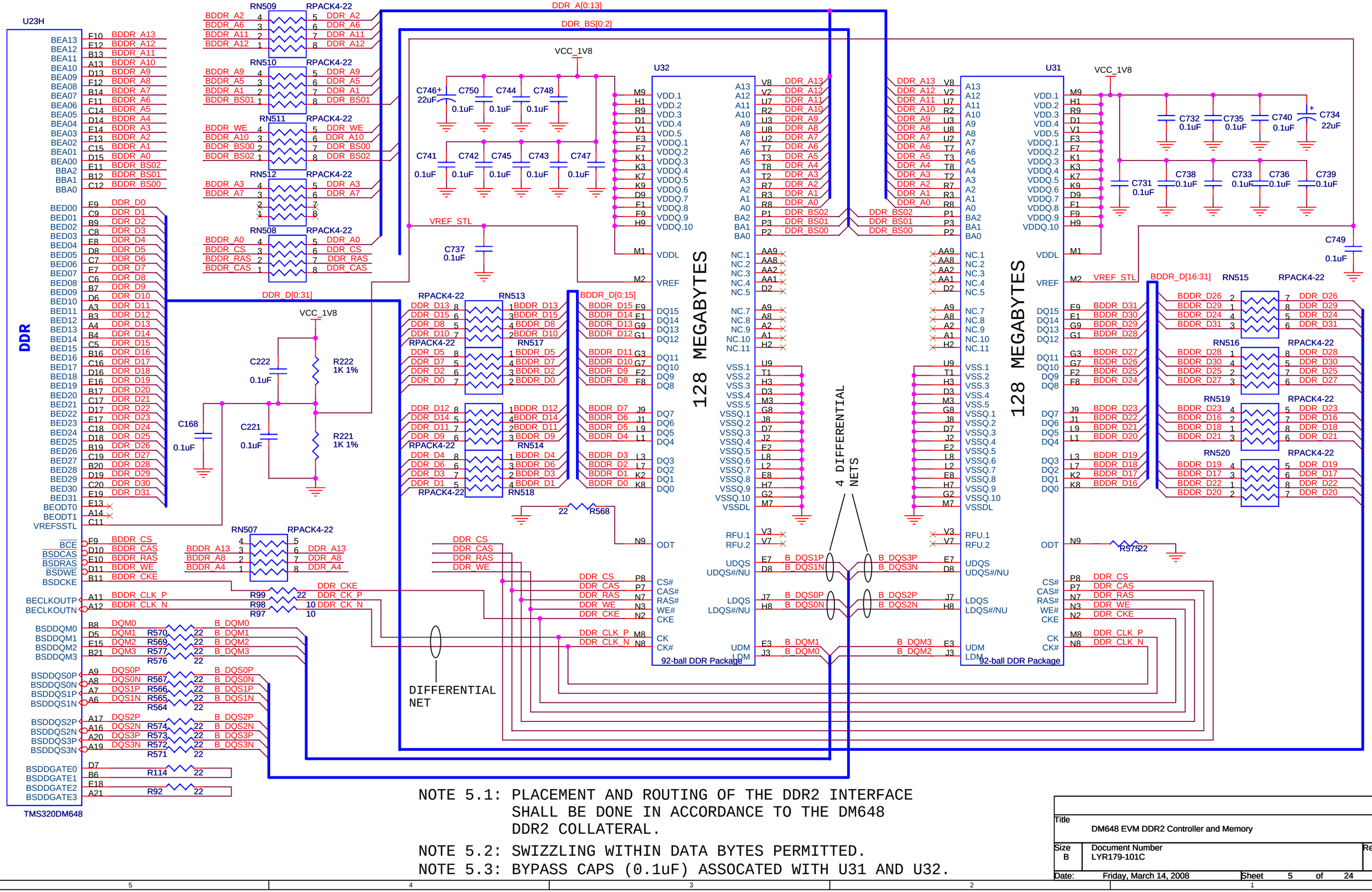

NOTE 5.1: PLACEMENT AND ROUTING OF THE DDR2 INTERFACE SHALL BE DONE IN ACCORDANCE TO THE DM648 DDR2 COLLATERAL.

NOTE 5.2: SWIZZLING WITHIN DATA BYTES PERMITTED.

NOTE 5.3: BYPASS CAPS (0.1uF) ASSOCATED WITH U31 AND U32.

Title	DM648 EVM DDR2 Controller and Memory	
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NOTE 6.7: BYPASS CAPS ON THIS PAGE (0.1uF) ASSOCIATED WITH U38.

NOTE 6.8: PCI LAYOUT TO FOLLOW PCI SPECIFICATION 2.2.

U38

PCI2060

P8

NP

SOURCE WHILE IN PCI SLOT

See Note 6.1

NOTE 6.4: LENGTH TO CAP NO GREATER THAN 0.25".
NOTE 6.5: TRACE SIZE TO CAP 0.020".
NOTE 6.6: ANY NUMBER OF PIN SHARES AS LONG AS DOES NOT EXCEED LENGTH.

Note 6.1: TRACE LENGTH OF P_CLK MUST BE 2.5" +/- 0.1".
Note 6.2: TRACE LENGTH OF ALL OTHER PRIMARY PCI SIGNALS EXCEPT INTAn AND PCI_PLUG ARE LIMITED TO 1.5".
Note 6.3: PRIMARY PCI TRACE LENGTH MEASURED FROM TOP OF THE FINGERS OF P8 OF THE PCI2060.

Title	DM648 EVM PCI Interface and Bridge
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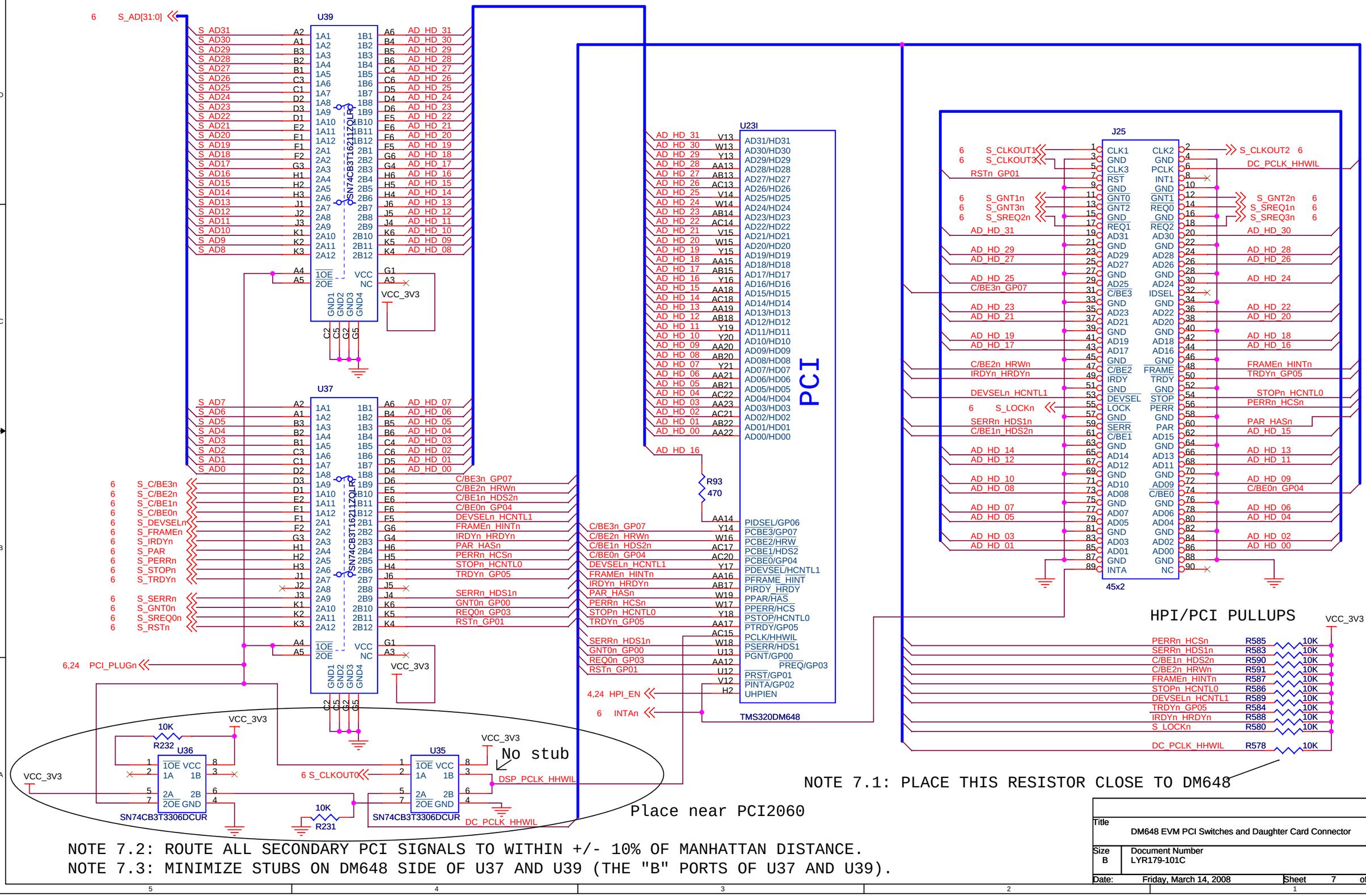

Title	DM648 EVM PCI Switches and Daughter Card Connector		
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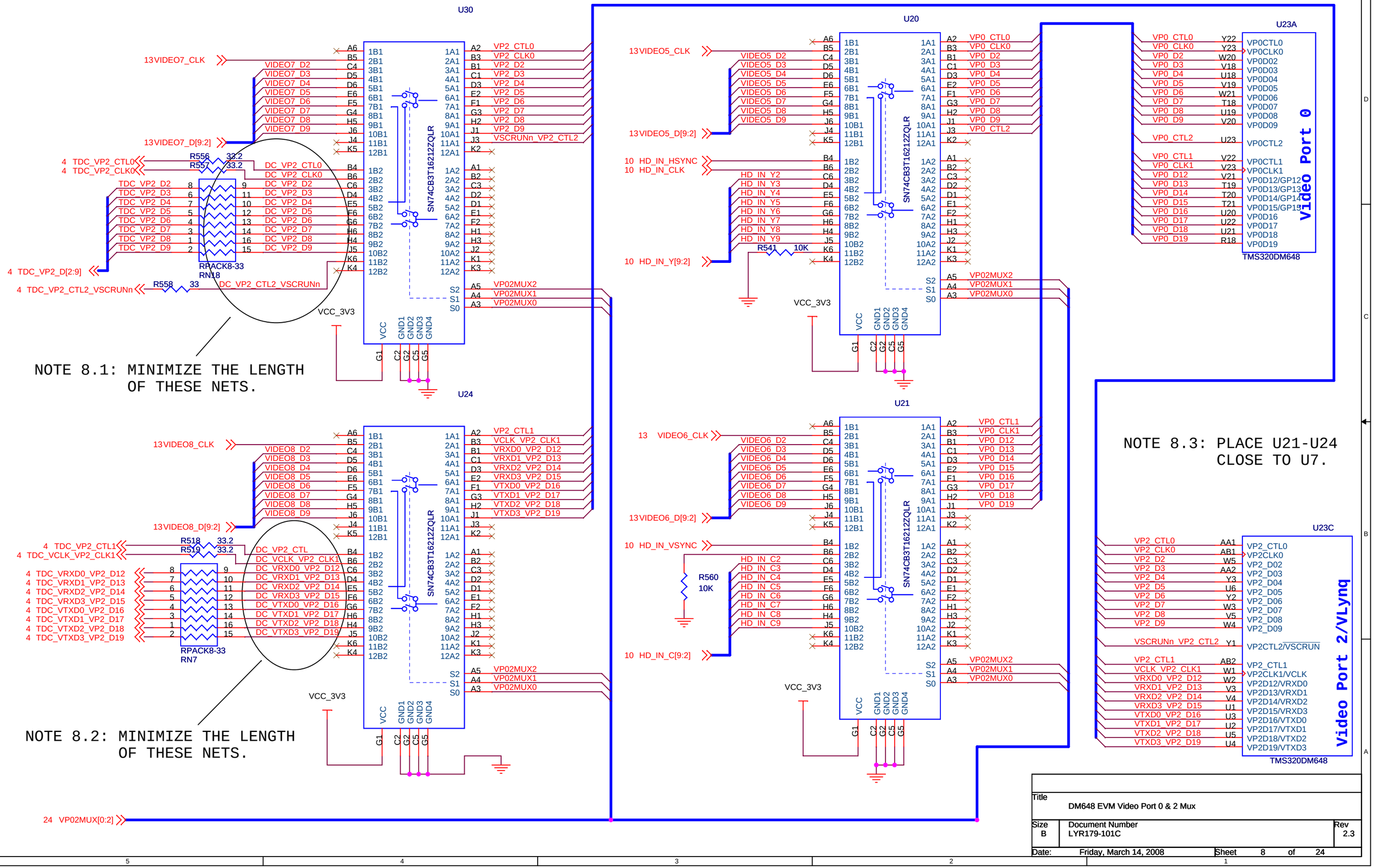

Title	DM648 EVM Video Port 0 & 2 Mux	
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NOTE 9.3: BYPASS CAPS ON THIS PAGE
(0.1uF) ASSOCIATED WITH U11.

NOTE 9.4: ISOLATE DIGITAL AND ANALOG GNDs AND CONNECT AT A SINGLE LOCATION IN THE GROUND PLANE.

Title	DM648 EVM SD Video In Channels 1 through 4		
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PLACE R341, R343 OVER THE SPLIT PLANE.

NOTE 10.3: MINIMIZE THE LENGTH OF THESE NETS.

NOTE 10.4: PLACE THESE COMPONENTS NEAR J10.

NOTE 10.1: BYPASS CAPS ON THIS PAGE (0.1uF) ASSOCIATED WITH U12.

NOTE 10.2: ISOLATE DIGITAL AND ANALOG GNDs AND CONNECT AT A SINGLE LOCATION IN THE GROUND PLANE.

Title	DM648 EVM - HD VIDEO IN
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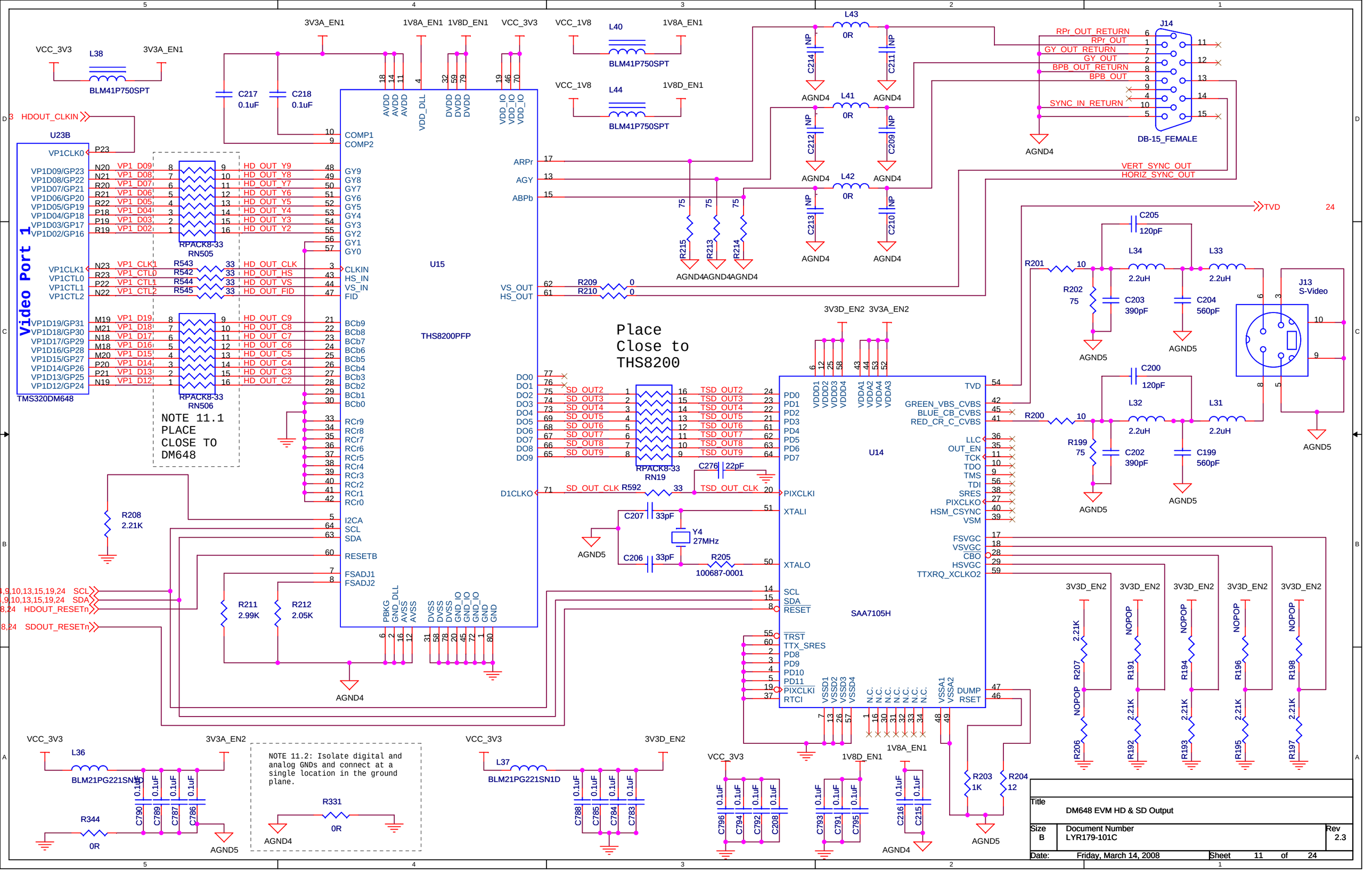
Video Port 1
U23B
TMS320DM648
VP1CLK0
VP1D09/GP23
VP1D08/GP22
VP1D07/GP21
VP1D06/GP20
VP1D05/GP19
VP1D04/GP18
VP1D03/GP17
VP1D02/GP16
VP1CLK1
VP1CTL0
VP1CTL1
VP1CTL2
VP1D19/GP31
VP1D18/GP30
VP1D17/GP29
VP1D16/GP28
VP1D15/GP27
VP1D14/GP26
VP1D13/GP25
VP1D12/GP24
HDOUT_CLKIN
RPACK8-33
RN505
RN506
NOTE 11.1
PLACE
CLOSE TO
DM648
U15
THS8200PFP
COMP1
COMP2
GY9
GY8
GY7
GY6
GY5
GY4
GY3
GY2
GY1
GY0
CLKIN
HS_IN
VS_IN
FID
BCb9
BCb8
BCb7
BCb6
BCb5
BCb4
BCb3
BCb2
BCb1
BCb0
RCr9
RCr8
RCr7
RCr6
RCr5
RCr4
RCr3
RCr2
RCr1
RCr0
I2CA
SCL
SDA
RESETB
FSADJ1
FSADJ2
R208
2.21K
R211
2.99K
R212
2.05K
C217
0.1uF
C218
0.1uF
L38
BLM41P750SPT
L40
L44
L43
L41
L42
0R
C214
C211
C212
C209
C213
C210
NP
AGND4
ARPr
AGY
ABPb
R215
R213
R214
75
VS_OUT
HS_OUT
R209
R210
J14
DB-15_FEMALE
RPr_OUT_RETURN
RPr_OUT
GY_OUT_RETURN
GY_OUT
BPB_OUT_RETURN
BPB_OUT
SYNC_IN_RETURN
VERT_SYNC_OUT
HORIZ_SYNC_OUT
TVD
J13
S-Video
C205
120pF
C203
390pF
C204
560pF
C200
C202
C199
L34
L33
L32
L31
2.2uH
R201
R202
R200
R199
AGND5
Place
Close to
THS8200
SD_OUT2
SD_OUT3
SD_OUT4
SD_OUT5
SD_OUT6
SD_OUT7
SD_OUT8
SD_OUT9
RPACK8-33
RN19
TSD_OUT2
TSD_OUT3
TSD_OUT4
TSD_OUT5
TSD_OUT6
TSD_OUT7
TSD_OUT8
TSD_OUT9
C276
22pF
SD_OUT_CLK
TSD_OUT_CLK
R592
33
D1CLKO
PIXCLKI
XTALI
XTALO
C207
33pF
C206
33pF
Y4
27MHz
R205
100687-0001
SAA7105H
SCL
SDA
RESET
TRST
TTX_SRES
PD8
PD9
PD10
PD11
PIXCLKI
RTCI
DUMP
RSET
R203
1K
R204
12
GREEN_VBS_CVBS
BLUE_CB_CVBS
RED_CR_C_CVBS
LLC
OUT_EN
TCK
TDO
TMS
TDI
SRES
PIXCLKO
HSM_CSYNC
VSM
FSVGC
VSVGC
CBO
HSVGC
TTXRQ_XCLKO2
R207
R191
R194
R196
R198
R206
R192
R193
R195
R197
NOPOP
2.21K
3V3D_EN2
3V3A_EN2
1V8A_EN1
1V8D_EN1
VCC_3V3
VCC_1V8
L36
L37
BLM21PG221SN1D
0.1uF
C790
C789
C787
C786
C788
C785
C784
C783
C796
C794
C792
C208
C793
C791
C795
C216
C215
R344
0R
R331
NOTE 11.2: Isolate digital and
analog GNDs and connect at a
single location in the ground
plane.
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DM648 EVM HD & SD Output
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B
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NOTE 12.1: Place Close To DM648

U52 U53 U49 U50 U51 — SN74CBT16214CDL

U23D — TMS320DM648

Video Port 3/EMIF

Video Port 4/EMIF

EMIF/Bootmode

RPACK8-33 RN14 RN502 RN15 RN503 RN16 RN17 RN504

Title	DM648 EVM VIDEO MUX 3 AND 4
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NOTE 13.3: BYPASS CAPS ON THIS PAGE
(0.1uF) ASSOCIATED WITH U10.

NOTE 13.1:
SILKSCREEN:
VIDEO IN5

VIDEO IN6

J4
Dual RCA Jack
R37 37.4
R34 37.4
R35 37.4
R36 37.4
C38 0.1uF
C33 0.1uF
AGND2

NOTE 13.2:
SILKSCREEN:
VIDEO IN7

VIDEO IN8

J3
Dual RCA Jack
R32 37.4
R30 37.4
R31 37.4
R33 37.4
C28 0.1uF
C23 0.1uF
AGND2

C37 0.1uF
C32 0.1uF
C27 0.1uF
C22 0.1uF
AGND2

C35 1uF
C36 1uF
C34 1uF
C30 1uF
C31 1uF
C29 1uF
C25 1uF
C26 1uF
C24 1uF
C41 1uF
C39 1uF
C40 1uF
AGND2

3V3D_DEC2
R42 2.21K
R41 2.21K

3V3D_DEC2
C42 C43 C44
0.1uF 0.1uF 0.1uF

1V8D_DEC2
C122 C121 C21 C45
0.1uF 0.1uF 0.1uF 0.1uF

1V8A_DEC2
C563 C564 C562 C561 C560 C559
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF
AGND2

3V3D_DEC2
R39 2.21K
R40 NOPOP

3 TVP5154_CLKIN2

NOTE 13.4: ISOLATE DIGITAL AND
ANALOG GNDs AND CONNECT
AT A SINGLE LOCATION IN
THE GROUND PLANE.
R336 0R
AGND2

U10
TVP5154PNP

1V8A_DEC2: 8 AVDD, 19 AVDD, 28 AVDD, 127 AVDD, 4 PLL_VDD, 13 PLL_VDD, 24 PLL_VDD, 33 PLL_VDD
1V8D_DEC2: 46 DVDD18, 65 DVDD18, 81 DVDD18, 98 DVDD18, 115 DVDD18
3V3D_DEC2: 114 IOVDD33, 97 IOVDD33, 80 IOVDD33, 64 IOVDD33, 45 IOVDD33

2 AIP1A
11 AIP2A
22 AIP3A
31 AIP4A
3 AIP1B
12 AIP2B
23 AIP3B
32 AIP4B
6 REFM1
7 REFP1
17 REFM2
18 REFP2
26 REFM3
27 REFP3
125 REFM4
126 REFP4
118 I2CA0
117 I2CA1
122 PDN
123 XOUT
124 XIN/OSC

9 AGND, 16 AGND, 20 AGND, 29 AGND, 35 AGND, 128 AGND, 1 AI1GND, 10 AI2GND, 21 AI3GND, 30 AI4GND, 5 PLL_GND, 14 PLL_GND, 25 PLL_GND, 34 PLL_GND
36 TMS, 47 DGND, 66 DGND, 82 DGND, 99 DGND, 116 DGND, 44 IOGND, 63 IOGND, 79 IOGND, 96 IOGND, 113 IOGND
AGND2

1V8A_DEC2
L14 BLM41P750SPT
3V3D_DEC2
VCC_3V3
L13 BLM41P750SPT
VCC_1V8
1V8A_DEC2
L15 BLM41P750SPT
VCC_1V8
1V8D_DEC2

CLK1 103
SCLK1 104
CH1_OUT0 112
CH1_OUT1 111
CH1_OUT2 110
CH1_OUT3 109
CH1_OUT4 108
CH1_OUT5 107
CH1_OUT6 106
CH1_OUT7 105
AVID1 101
FID1/GLCO1 94
IREQ1/GPCL1/VBLK1 102
HSYNC1 100
VSYNC1/PALI1 95

R43 33
VCH5_OUT0 1
VCH5_OUT1 2
VCH5_OUT2 3
VCH5_OUT3 4
VCH5_OUT4 5
VCH5_OUT5 6
VCH5_OUT6 7
VCH5_OUT7 8
16 VIDEO5_D2
15 VIDEO5_D3
14 VIDEO5_D4
13 VIDEO5_D5
12 VIDEO5_D6
11 VIDEO5_D7
10 VIDEO5_D8
9 VIDEO5_D9
RPACK8-33
RN3
VIDEO5_CLK 8
VIDEO5_D[9:2] 8

CLK2 84
SCLK2 85
CH2_OUT0 93
CH2_OUT1 92
CH2_OUT2 91
CH2_OUT3 90
CH2_OUT4 89
CH2_OUT5 88
CH2_OUT6 87
CH2_OUT7 86
AVID2 78
FID2/GLCO2 75
IREQ2/GPCL2/VBLK2 83
HSYNC2 77
VSYNC2/PALI2 76

R38 33
VCH6_OUT0 1
VCH6_OUT1 2
VCH6_OUT2 3
VCH6_OUT3 4
VCH6_OUT4 5
VCH6_OUT5 6
VCH6_OUT6 7
VCH6_OUT7 8
16 VIDEO6_D2
15 VIDEO6_D3
14 VIDEO6_D4
13 VIDEO6_D5
12 VIDEO6_D6
11 VIDEO6_D7
10 VIDEO6_D8
9 VIDEO6_D9
RPACK8-33
RN9
VIDEO6_CLK 8
VIDEO6_D[9:2] 8

CLK3 61
SCLK3 62
CH3_OUT0 74
CH3_OUT1 73
CH3_OUT2 72
CH3_OUT3 71
CH3_OUT4 70
CH3_OUT5 69
CH3_OUT6 68
CH3_OUT7 67
AVID3 59
FID3/GLCO3 56
IREQ3/GPCL3/VBLK3 60
HSYNC3 58
VSYNC3/PALI3 57

R29 33
VCH7_OUT0 1
VCH7_OUT1 2
VCH7_OUT2 3
VCH7_OUT3 4
VCH7_OUT4 5
VCH7_OUT5 6
VCH7_OUT6 7
VCH7_OUT7 8
16 VIDEO7_D2
15 VIDEO7_D3
14 VIDEO7_D4
13 VIDEO7_D5
12 VIDEO7_D6
11 VIDEO7_D7
10 VIDEO7_D8
9 VIDEO7_D9
RPACK8-33
RN8
VIDEO7_CLK 8
VIDEO7_D[9:2] 8

CLK4 42
SCLK4 43
CH4_OUT0 55
CH4_OUT1 54
CH4_OUT2 53
CH4_OUT3 52
CH4_OUT4 51
CH4_OUT5 50
CH4_OUT6 49
CH4_OUT7 48
AVID4 40
FID4/GLCO4 37
IREQ4/GPCL4/VBLK4 41
HSYNC4 39
VSYNC4/PALI4 38

R28 33
VCH8_OUT0 1
VCH8_OUT1 2
VCH8_OUT2 3
VCH8_OUT3 4
VCH8_OUT4 5
VCH8_OUT5 6
VCH8_OUT6 7
VCH8_OUT7 8
16 VIDEO8_D2
15 VIDEO8_D3
14 VIDEO8_D4
13 VIDEO8_D5
12 VIDEO8_D6
11 VIDEO8_D7
10 VIDEO8_D8
9 VIDEO8_D9
RPACK8-33
RN2
VIDEO8_CLK 8
VIDEO8_D[9:2] 8

SCA 119
SCL 120
RESETB 121
SDA 4,10,11,13,15,19,24
SCL 4,10,11,13,15,19,24
VIDEO1-4_RESETn 4,10,11,13,15,17,18,24

Title	DM648 EVM SD Video In Channels 5 through 8	
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NOTE 14.1: MINIMIZE THE LENGTH OF THESE NETS.

NOTE 14.2: PLACE R100 NEAR U23.

U23E

McASP

ACLKX AC7 0_CLKB_ACLKX
ACLKR AC6 0_CLKA_ACLKR
AFSR W6 0_FSA_AFSR
AFSX AA7 0_FSB_AFSX
AXR0 AB6 0_TR0_AXR0
AXR1 Y6 0_TR1_AXR1
AXR2 AA6 0_TX0_AXR2
AXR3 AB4 0_TX1_AXR3

AHCLKR AC4 1_CLKA_AHCLKR
AHCLKX AC3 1_CLKB_AHCLKX
AMUTEIN AB3 1_FSA_AMUTEIN
AMUTE U7 1_FSB_AMUTE
AXR4 Y5 1_TR0_AXR4
AXR5 V7 1_TR1_AXR5
AXR6 AA4 1_TX0_AXR6
AXR7 V6 1_TX1_AXR7

VCTL/AXR9 AA5
STCLK/AXR8 Y7

TMS320DM648

3 STCLK

R100 33

RPACK8-33 RN6

1 0_CLKB_ACLKX 16 T0_CLKB_ACLKX
2 0_CLKA_ACLKR 15 T0_CLKA_ACLKR
8 0_FSA_AFSR 9 T0_FSA_AFSR
3 0_FSB_AFSX 14 T0_FSB_AFSX
4 0_TR0_AXR0 13 T0_TR0_AXR0
6 0_TR1_AXR1 11 T0_TR1_AXR1
5 0_TX0_AXR2 12 T0_TX0_AXR2
7 0_TX1_AXR3 10 T0_TX1_AXR3

RPACK8-33 RN501

8 1_CLKA_AHCLKR 9 T1_CLKA_AHCLKR
7 1_CLKB_AHCLKX 10 T1_CLKB_AHCLKX
6 1_FSA_AMUTEIN 11 T1_FSA_AMUTEIN
5 1_FSB_AMUTE 12 T1_FSB_AMUTE
4 1_TR0_AXR4 13 T1_TR0_AXR4
3 1_TR1_AXR5 14 T1_TR1_AXR5
2 1_TX0_AXR6 15 T1_TX0_AXR6
1 1_TX1_AXR7 16 T1_TX1_AXR7

24 McASPMUX[0:2]

U8

SN74CB3T16212ZQLR

A2 1A1 1B1 A6
B3 2A1 2B1 B5
B1 3A1 3B1 C4
C1 4A1 4B1 D5
D3 5A1 5B1 D6
E2 6A1 6B1 E6
F1 7A1 7B1 F5
G3 8A1 8B1 G4
H2 9A1 9B1 H5
J1 10A1 10B1 J6
J3 11A1 11B1 J4
K2 12A1 12B1 K5

A1 1A2 1B2 B4
B2 2A2 2B2 B6
C3 3A2 3B2 C6
D2 4A2 4B2 D4
D1 5A2 5B2 E5
E1 6A2 6B2 F6
F2 7A2 7B2 G6
H1 8A2 8B2 H6
H3 9A2 9B2 H4
J2 10A2 10B2 J5
K1 11A2 11B2 K6
K3 12A2 12B2 K4

McASPMUX2 A5 S2
McASPMUX1 A4 S1
McASPMUX0 A3 S0

GND4 GND3 GND2 GND1 VCC
G5 C5 G2 C2 G1

VCC_3V3

ACLKX 15
ACLKR 15
AFSR 15
AFSX 15
AXR0 15
AXR1 15
AXR2 15
AXR3 15

0_CLKB 4
0_CLKA 4
0_FSA 4
0_FSB 4
0_TR0 4
0_TR1 4
0_TX0 4
0_TX1 4

U9

SN74CB3T16212ZQLR

A2 1A1 1B1 A6
B3 2A1 2B1 B5
B1 3A1 3B1 C4
C1 4A1 4B1 D5
D3 5A1 5B1 D6
E2 6A1 6B1 E6
F1 7A1 7B1 F5
G3 8A1 8B1 G4
H2 9A1 9B1 H5
J1 10A1 10B1 J6
J3 11A1 11B1 J4
K2 12A1 12B1 K5

A1 1A2 1B2 B4
B2 2A2 2B2 B6
C3 3A2 3B2 C6
D2 4A2 4B2 D4
D1 5A2 5B2 E5
E1 6A2 6B2 F6
F2 7A2 7B2 G6
H1 8A2 8B2 H6
H3 9A2 9B2 H4
J2 10A2 10B2 J5
K1 11A2 11B2 K6
K3 12A2 12B2 K4

McASPMUX2 A5 S2
McASPMUX1 A4 S1
McASPMUX0 A3 S0

GND4 GND3 GND2 GND1 VCC
G5 C5 G2 C2 G1

VCC_3V3

AHCLKX 15

AXR4 15
AXR5 15
AXR6 15
AXR7 15

1_CLKA 4
1_CLKB 4
1_FSA 4
1_FSB 4
1_TR0 4
1_TR1 4
1_TX0 4
1_TX1 4

VCTL 3

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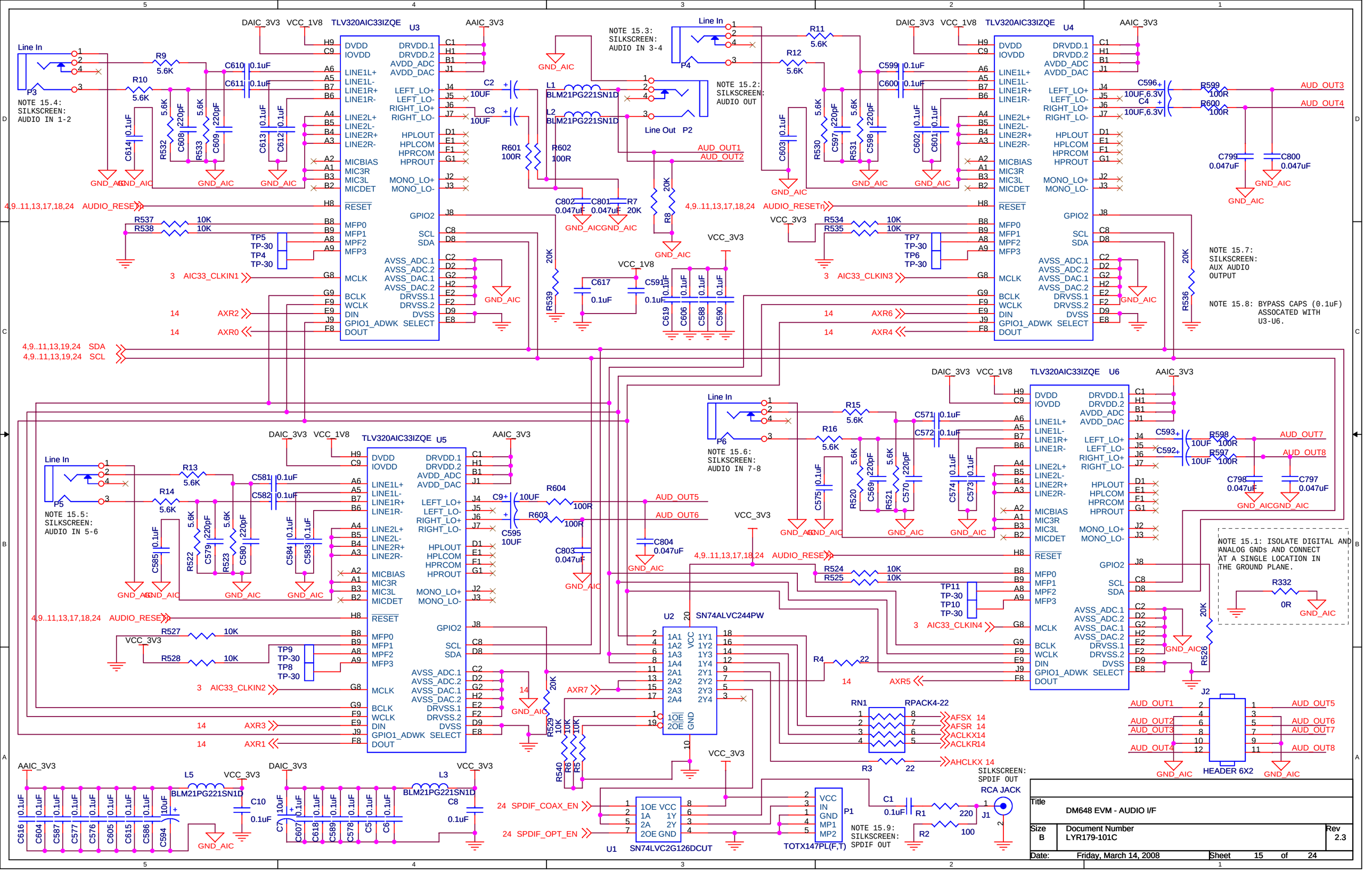
TLV320AIC33IZQE U3
TLV320AIC33IZQE U4
TLV320AIC33IZQE U5
TLV320AIC33IZQE U6
DAIC_3V3 VCC_1V8 AAIC_3V3
Line In
P3
P4
P5
P6
NOTE 15.4: SILKSCREEN: AUDIO IN 1-2
NOTE 15.3: SILKSCREEN: AUDIO IN 3-4
NOTE 15.2: SILKSCREEN: AUDIO OUT
NOTE 15.5: SILKSCREEN: AUDIO IN 5-6
NOTE 15.6: SILKSCREEN: AUDIO IN 7-8
Line Out P2
AUD_OUT1
AUD_OUT2
AUD_OUT3
AUD_OUT4
AUD_OUT5
AUD_OUT6
AUD_OUT7
AUD_OUT8
NOTE 15.7: SILKSCREEN: AUX AUDIO OUTPUT
NOTE 15.8: BYPASS CAPS (0.1uF) ASSOCATED WITH U3-U6.
NOTE 15.1: ISOLATE DIGITAL AND ANALOG GNDs AND CONNECT AT A SINGLE LOCATION IN THE GROUND PLANE.
AUDIO_RESETn
AIC33_CLKIN1
AIC33_CLKIN3
AIC33_CLKIN4
AIC33_CLKIN2
AXR0
AXR2
AXR4
AXR6
AXR1
AXR3
AXR5
AXR7
SDA
SCL
U2 SN74ALVC244PW
U1 SN74LVC2G126DCUT
RN1 RPACK4-22
AFSX 14
AFSR 14
ACLKX14
ACLKR14
AHCLKX 14
SILKSCREEN: SPDIF OUT
RCA JACK
TOTX147PL(F,T)
NOTE 15.9: SILKSCREEN: SPDIF OUT
SPDIF_COAX_EN
SPDIF_OPT_EN
HEADER 6X2
GND_AIC
VCC_3V3
VCC_1V8
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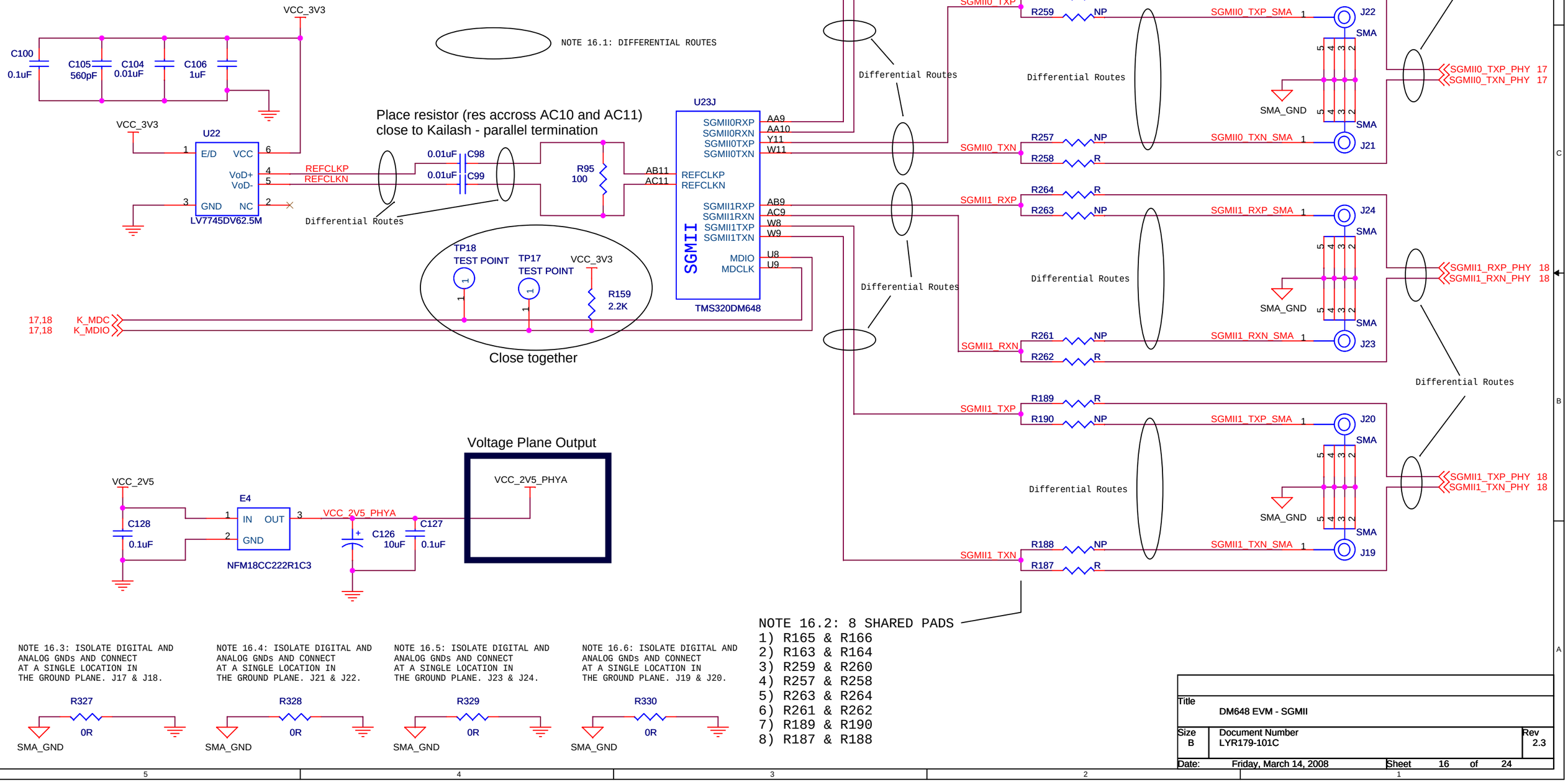
NOTE 16.1: DIFFERENTIAL ROUTES
Place resistor (res accross AC10 and AC11)
close to Kailash - parallel termination
Close together
Voltage Plane Output
Differential Routes
U23J
SGMII
TMS320DM648
U22
LV7745DV62.5M
E4
NFM18CC222R1C3
TP18
TEST POINT
TP17
TEST POINT
VCC_3V3
VCC_2V5
VCC_2V5_PHYA
SGMII0_RXP
SGMII0_RXN
SGMII0_TXP
SGMII0_TXN
SGMII1_RXP
SGMII1_RXN
SGMII1_TXP
SGMII1_TXN
SMA_GND
17,18 K_MDC
17,18 K_MDIO
NOTE 16.2: 8 SHARED PADS
1) R165 & R166
2) R163 & R164
3) R259 & R260
4) R257 & R258
5) R263 & R264
6) R261 & R262
7) R189 & R190
8) R187 & R188
NOTE 16.3: ISOLATE DIGITAL AND ANALOG GNDs AND CONNECT AT A SINGLE LOCATION IN THE GROUND PLANE. J17 & J18.
NOTE 16.4: ISOLATE DIGITAL AND ANALOG GNDs AND CONNECT AT A SINGLE LOCATION IN THE GROUND PLANE. J21 & J22.
NOTE 16.5: ISOLATE DIGITAL AND ANALOG GNDs AND CONNECT AT A SINGLE LOCATION IN THE GROUND PLANE. J23 & J24.
NOTE 16.6: ISOLATE DIGITAL AND ANALOG GNDs AND CONNECT AT A SINGLE LOCATION IN THE GROUND PLANE. J19 & J20.
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NOTE 17.3: PLACE RESISTORS ON TOP OF BOARD.

U55A

88E1111-2

NOTE 17.2: DIFFERENTIAL ROUTES4 PAIR

J7

JK0-0036

U54

OSC 25 MHz

U55C

88E1111-2

U55B

88E1111-2

Phy Address = 0000
Enable pause = 0
Auto-Neg, advertise all capabilities, prefer Master
Crossover enabled
125 Mhz clock enabled
SGMII (with clock + Auto-Neg to copper)
Disable auto selection of fiber/copper interface
Disable energy detect
MDC/MDIO selected instead of TWSI
INTn signal is active low
50 Ohm terminiation for fiber

Configuration Information
Phy Address = 0000
ENA_PAUSE = 0
ANEG[3:0] = 1110
ENA_XC = 1
DIS_125 = 0
HWCFG_MODE = 0000
DIS_FC = 1
DIS_SLEEP = 1
SEL_TWSI = 0
INT_POL = 1
75/50 Ohm = 0

NOTE 17.1: BYPASS CAPS (0.1uF) ON THIS PAGE ASSOCIATED WITH U55.

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NOTE 18.3: PLACE RESISTORS ON TOP OF BOARD.

U57A

VCC_2V5_PHYA
LED1_TX R173 0
R172 0
R171 0
LED1_RX R167 0
LED1_DUPLEX R501 NP
R170 0
LED1_LINK10 R169 0
LED1_RX R168 0

TP16 TEST POINT
TP15 TEST POINT

D8 CONFIG[0]
E9 CONFIG[1]
F8 CONFIG[2]
G7 CONFIG[3]
F9 CONFIG[4]
G9 CONFIG[5]
G8 CONFIG[6]

B5 CRS
E2 GTX_CLK
M6 HSDAC-
M5 HSDAC+
L1 INTn

C1 RX_CLK
B1 RX_DV
D2 RX_ER
B2 RXD0
D3 RXD1
C3 RXD2
B3 RXD3
C4 RXD4
A1 RXD5
A2 RXD6
C5 RXD7

E1 TX_EN
F2 TX_ER
F1 TXD0
G2 TXD1
G3 TXD2
H2 TXD3
H1 TXD4
H3 TXD5
J1 TXD6
J2 TXD7
K7 NC.1
G1 NC.2

VCC_3V3
R186 NO-POP
17 PHY_INTn
R185 10K

16 SGMII1_RXP_PHY
16 SGMII1_RXN_PHY
16 SGMII1_TXP_PHY
16 SGMII1_TXN_PHY
TP36 TEST POINT
TP35 TEST POINT

A7 S_OUT+
A8 S_OUT-
A3 S_IN+
A4 S_IN-
A5 S_CLK+
A6 S_CLK-

4,9..11,13,15,17,24 PHY_RESETn
R184 4.99K 1%
K3 RESETn
M2 RSET

88E1111-2

B6 COL
L4 COMA
M1 MDIO
L3 MDC
K2 125CLK
J9 XTAL2
H9 XTAL1
D1 TX_CLK
H8 SEL_FREQ

K_MDIO 16,17
K_MDC 16,17

MDI[0]+ N1 PHY1_MDI0p
MDI[0]- N2 PHY1_MDI0n
MDI[1]+ N3 PHY1_MDI1p
MDI[1]- N4 PHY1_MDI1n
MDI[2]+ N6 PHY1_MDI2p
MDI[2]- N7 PHY1_MDI2n
MDI[3]+ N8 PHY1_MDI3p
MDI[3]- N9 PHY1_MDI3n

PHY1_125CLK
TP20 TEST POINT

VCC_3V3
L22 BLM18AG102SN1
C79 0.1uF
U56
VDD OE/NC
GND OUT
OSC 25 MHz
VCC_3V3

LED_TX D9
LED_RX C9
LED_LINK1000 A9
LED_LINK100 B8
LED_LINK10 C8
LED_DUPLEX E8

LED1_TX TP31 TEST POINT
LED1_RX TP30 TEST POINT
LED1_LINK1000 TP32 TEST POINT
LED1_LINK100 TP33 TEST POINT
LED1_LINK10 TP34 TEST POINT
LED1_DUPLEX TP37 TEST POINT

U57C
TMS L8 TP505 TEST POINT
TCK L9 TP504 TEST POINT
TDO K8 TP503
TDI L7 TP502 TEST POINT
TRSTn M9 TP501 TEST POINT
88E1111-2

NOTE 18.2: DIFFERENTIAL ROUTES4 PAIR

SGMII_AVDD_PHY1
R183 49.9 1%
R182 49.9 1%
R181 49.9 1%
R180 49.9 1%
R179 49.9 1%
R178 49.9 1%
R177 49.9 1%
R176 49.9 1%
C83 0.01uF
C82 0.01uF
C81 0.01uF
C80 0.01uF
C504 0.1uF
C503 0.1uF
C501 0.1uF
C502 0.1uF
R174 360
R175 360

J8
T1+ CT1 T1-
T2+ CT2 T2-
T3+ CT3 T3-
T4+ CT4 T4-
LED1-A LED1-K
LED2-AK LED2-KA
75 75 75 75
JK0-0036
L501 BLM41P750SPT

VCC_2V5
C511 0.1uF
C512 0.1uF
C525 0.1uF
C526 0.1uF
C522 0.1uF
C518 0.1uF
C519 0.1uF
C530 0.1uF

VCC_2V5_PHYA
C510 0.1uF
C509 0.1uF
C513 0.1uF
C528 0.1uF
C515 0.1uF
C517 0.1uF

VCC_2V5_PHYA
VCC_DVDD_PHY
VCC_2V5
U57B
AVDD.1 AVDD.2 AVDD.3 AVDD.4 AVDD.5 AVDD.6
DVDD.1 DVDD.2 DVDD.3 DVDD.4 DVDD.5 DVDD.6 DVDD.7 DVDD.8
VDDO.1 VDDO.2 VDDO.3 VDDOH.1 VDDOH.2 VDDOH.3 VDDOX.1 VDDOX.2
VSSC VSS.1 VSS.2 VSS.3 VSS.4 VSS.5 VSS.6 VSS.7 VSS.8 VSS.9 VSS.10 VSS.11 VSS.12 VSS.13 VSS.14 VSS.15 VSS.16 VSS.17 VSS.18 VSS.19 VSS.20 VSS.21 VSS.22 VSS.23
88E1111-2

SGMII_AVDD_PHY1
L23 BLM21PG221SN1D
C84 0.1uF
C85 0.1uF
C86 0.1uF

VCC_DVDD_PHY
C529 0.1uF
C527 0.1uF
C524 0.1uF
C523 0.1uF
C516 0.1uF
C514 0.1uF
C521 0.1uF
C520 0.1uF

Phy Address = 0001
Enable pause = 0
Auto-Neg, advertise all capabilities, prefer Master
Crossover enabled
125 Mhz clock enabled
SGMII (with clock + Auto-Neg to copper)
Disable auto selection of fiber/copper interface
Disable energy detect
MDC/MDIO selected instead of TWSI
INTn signal is active low
50 Ohm terminiation for fiber

Configuration Information
Phy Address = 0001
ENA_PAUSE = 0
ANEG[3:0] = 1110
ENA_XC = 1
DIS_125 = 0
HWCFG_MODE = 0000
DIS_FC = 1
DIS_SLEEP = 1
SEL_TWSI = 0
INT_POL = 1
75/50 Ohm = 0

NOTE 18.1: BYPASS CAPS (0.1uF) ON THIS PAGE ASSOCIATED WITH U57.

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4,24 UART/SPIn

NOTE 19.1: PLACE THESE PARTS NEAR U23

U23G

SPICS1/UARTTX D23 — R91 22.1
SPIDI/UARTRTS G23 — R87 22.1
SPIDO/UARTCTS F21 — R90 22.1
SPICS2/UARTRX F23 — R88 22.1
SPICK F22 — R89 22.1
SDA0 C23
SCL0 D22

TMS320DM648

U41 MAX3223

C1+ 2 — C224 0.1uF — C1- 4
C2+ 5 — C225 0.1uF — C2- 6
T1IN 13
T2IN 12
R1OUT 15
R2OUT 10
FORCEOFF 20

VCC 19 — VCC_3V3
V+ 3 — C226 0.1uF
V- 7 — C227 0.1uF
GND 18
FORCEON 14 — C228 0.1uF
T1OUT 17
T2OUT 8
R1IN 16
R2IN 9
INVALID 11
EN 1

L7 1uH — C17 10pF GND_E_RS232 — C13 10pF GND_E_RS232
L8 1uH — C18 10pF GND_E_RS232 — C14 10pF GND_E_RS232
L6 1uH — C16 10pF GND_E_RS232 — C12 10pF GND_E_RS232
L9 1uH — C19 10pF GND_E_RS232 — C15 10pF GND_E_RS232

NOTE 19.2: SILKSCREEN UART

DB9-MALE P7
11 — GND_E_RS232
5 9 4 8 3 7 2 6 1
10 — GND_E_RS232

UART_CTS
UART_TX
UART_RTS
UART_RX

R334 0R
R335 0R
GND_E_RS232
GND_E_CAN

U42 SN74CB3T3306DCUR
1 1OE VCC 8
2 1A 1B 3
5 2A 2B 6
7 2OE GND 4
VCC_3V3

R230 2.21K

U43 SN74CB3T3306DCUR
1 1OE VCC 8
2 1A 1B 3
5 2A 2B 6
7 2OE GND 4
VCC_3V3

R236 2.21K
SPI_CS2n 4

R237 10K

R233 2.21K
R234 10K
R235 10K
C223 0.1uF

U40 SOCKETED_SPI_EEPROM
1 CS VCC 8
2 SO HOLD 7
3 WP SCK 6
4 GND SI 5

NOTE 19.3: PLACE U40, U41 U42, AND U43 NEAR SPI_D1, SPI_D0, SPI_CS2n, AND SPI_CLK CONNECTIONS TO J15

SPI_DI 4
SPI_DO 4
SPI_CLK 4
SDA 4,9..11,13,15,24
SCL 4,9..11,13,15,24

JP4 HEADER 2X2
1 2
3 4

I2C Disconnect

JP3 HEADER 5X2
USB_GPIO7 1 2 USB_GPIO6
USB_GPIO5 3 4 USB_GPIO4
USB_3V3_SOURCE 5 6 GND
USB_GPIO3 7 8 USB_GPIO2
USB_SCL 9 10 USB_SDA

USB Interface Adapter EVM
USB-GPIO/I2C Headers

JP2 HEADER 5X2
USB_GPIO7 1 2 USB_GPIO6
USB_GPIO5 3 4 USB_GPIO4
USB_3V3_SOURCE 5 6 GND
USB_GPIO3 7 8 USB_GPIO2
USB_SCL 9 10 USB_SDA

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POWER

IO POWER

DVDD33 (AC19, AC2, V2, N2, Y4, AC5, R7, N7, J7, Y8, T8, P8, M8, T12, AB16, G1, T14, U15, V16, AB7, P16, M16, U17, R17, N17, AC23, W23, T23, M23, L7, K8, AB12, H16, J17, G19, E20, E22, H22, L17, K16)

CORE POWER

CVDD (L13, K14, L15, J15, P10, M10, N11, P12, M12, N13, M14, P14, L9, J9, K10, L11, K12, J11, N15, R13, R8, N9, T16, R15, V8, R9, R11)

CVDD1 (H9, J13)

UNKNOWN

CVDDESS (R9, R11)

DDR2 POWER

DVDD18 (E5, B1, C3, F8, F14, H12, C10, G13, C13, G15, H14, B15, F16, B18, F18, C21, B23, G17, G9, H10, B5, G11)

RSV12 (E1)
RSV14 (E3)
RSV18 (F6)

VCCMON (L19)
VDD33MON (G21)
VDD18MON (B2)

TP39 TP-30
TP38 TP-30
TP40 TP-30

VCC_3V3

R96 240

RSV21 (Y12)
RSV22 (W12)

VCC_1V8

R94 240
R113 240

RSV19 (C2)
RSV20 (C1)

R559 240

OUTPUT IMPEDANCE

GROUND

VSS (A1, C4, A5, E6, E7, K7, L8, J8, G8, F15, V9, K9, L10, J10, G10, K11, H11, G12, J12, L12, D12, K13, H13, G14, J14, L14, A15, H15, K15, L16, J16, G16, E17, H17, K17, A18, G18, E19, D20, G22, E23, A23, D9, AB23, M22, T22, W22, AB19, M17, P17, T17, V17, N16, R16, U16, AC16, M15, P15, T15, N14, R14, U14, M13, P13, T13, N12, R12, Y10, AC12, M11, P11, T11, AA11, N10, R10, AC8, AC10, M9, P9, T9, Y9, N8, AA8, M7, P7, T7, W7, AB5, AA3, N1, V1, AC1, H7, H8, E2, E4)

RSV7
RSV8
RSV11
RSV13

SERDES

AVDDR (AB10)

AVDDT (U11)
AVDDT (AB8)
AVDDA (V11)
AVDDA (W10)

DVDDD (T10)
DVDDD (U10)

SGMII_VCC_1V2

AVDLL2 (B22)

AVDLL1 (B10)

PLLV1 (N3)
PLLV2 (G7)

RSV1 (L20)
RSV2 (L21)

U23K
TMS320DM648

VCC_CORE

VCC_3V3

VCC_1V8

SGMII_VCC_1V2

E1, E2, E3, E5, E6, E7, E8
OUT IN GND
NFM18CC222R1C3

C110 560pF, C107 0.1uF, C101 0.1uF
C112 560pF, C109 0.1uF, C103 0.1uF
C111 560pF, C108 0.1uF, C102 0.1uF
C165 560pF, C166 0.1uF, C167 0.1uF
C169 560pF, C170 0.1uF, C171 0.1uF
C173 560pF, C172 0.1uF, C174 0.1uF
C175 560pF, C176 0.1uF, C177 0.1uF

C640 C722 C646 C626 C163 C638 C682 C643 C687 C637 C627 C636 C683 C679 C630 C677 C629 C678 C725 C655 C680 C667 C727 (0.1uF / 560pF / 10uF)

C158 C644 C624 C113 C117 C641 C647 C115 C92 C94 C90 C160 C691 C697 C696 C694 C693 C692 C688 C689 C699 C621 C657 (0.1uF / 560pF / 10uF)

C95 C684 C685 C628 C631 C632 C164 C649 C721 C650 C686 C161 C690 C695 C623 C159 C648 C114 C645 C91 C668 C700 C681 (0.1uF / 560pF / 10uF)

C651 C652 C723 C653 C724 C654 C635 C633 C634 C670 C97 C96 C639 C720 C162 C669 C625 C642 C116 C93 C726 C620 C656 (0.1uF / 560pF / 10uF)

C704 C718 C708 C701 C710 C712 C713 C719 C716 C717 C706 C705 C698 C703 C709 C702 C707 C714 C715 C711 C730 C728 C729 (0.1uF / 560pF / 10uF)

C662 C663 C671 C672 C673 C674 C675 C676 C659 C658 C660 C661 C664 C665 C666 (0.1uF / 560pF / 10uF)

NOTE 20.1: BYPASS CAPS (0.1uF & 560pF) ASSOCIATED WITH U23.

NOTE 20.2: PLACE E1-E3, E5-E8 CLOSE TO U23.

NOTE 20.3: PLACE FILTER CAPS NEAR ASSOCIATED EMI FILTERS (E1-E3, E5-E8).

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SILKSCREEN:
5V IN

J26
3 CENTER
1 SHUNT
2 SLEEVE
2.5 MM JACK
RASM712

TP66
TP-30

D2
1SMC5.0AT3G

R313
220

DS8
LED_GRN

C262
47uF

L48
BLM41P750SPT
L50
BLM41P750SPT
L49
BLM41P750SPT

C261
0.1uF

C259
10uF LESR

C260
0.1uF

SOURCE
WHILE NOT
IN PCI SLOT
VCC_5V

U48
TPS73201DBVT
1 IN
3 EN
GND
2
OUT 5
FB 4

R245
52.3K

C229
0.01uF

C230
100uF

SOURCE
VCC_MSP430_3V3

C231
22uF

R244
30.1K

TP49
3.3V_ENABLE

TP48
TP108

TP50
3.3V

R279
340
C239
2200pF
R277
10k
R275
33

C241
0.01uF

24 3V3_ENABLE
R278
0

R276
1K

C242
33pF
C240
6800pF
R281
4.02k

TP65
GND

R280
2.21k
R282
4.02k
C243
0.1uF

VCC_5V

TPS40190DRC
U61
1 EN
2 FB
3 COMP
4 VDD
5 GND
PWPd
11
HDRV 10
SW 9
BOOT 8
LDRV 7
BP5 6

C245
0.1uF

R284
3.3

C244
4.7uF

D1
MBR0530

R283
10k

Q3
Si4888DY
8 7 6 5
D D D D
4 G
S S S
1 2 3

Q6
Si4888DY
8 7 6 5
D D D D
4 G
S S S
1 2 3

L46
4.7uH

R285
NOPOP

C246
NOPOP

VCC_5V

C248
22uF
C247
22uF
C249
22uF

C250
330uF

TP52
5V

TP51
GND

C266
22uF
C265
22uF
C263
22uF
C264
22uF
C267
1uF

TP58
3.3V

TP59
GND

SOURCE
VCC_3V3

NOTE 21.1: THESE ARE OUPUTS
TO VOLTAGE PLANES.

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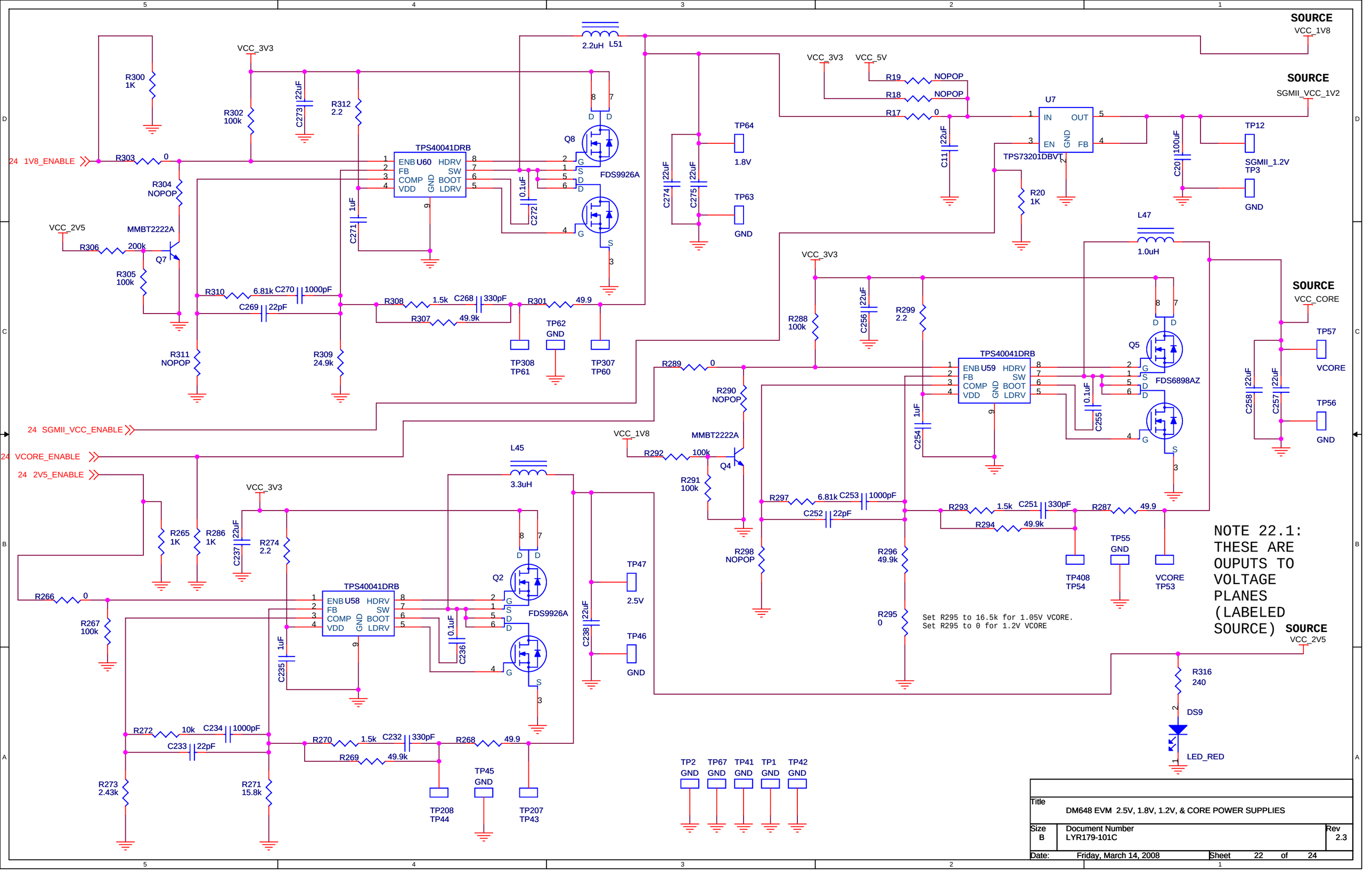

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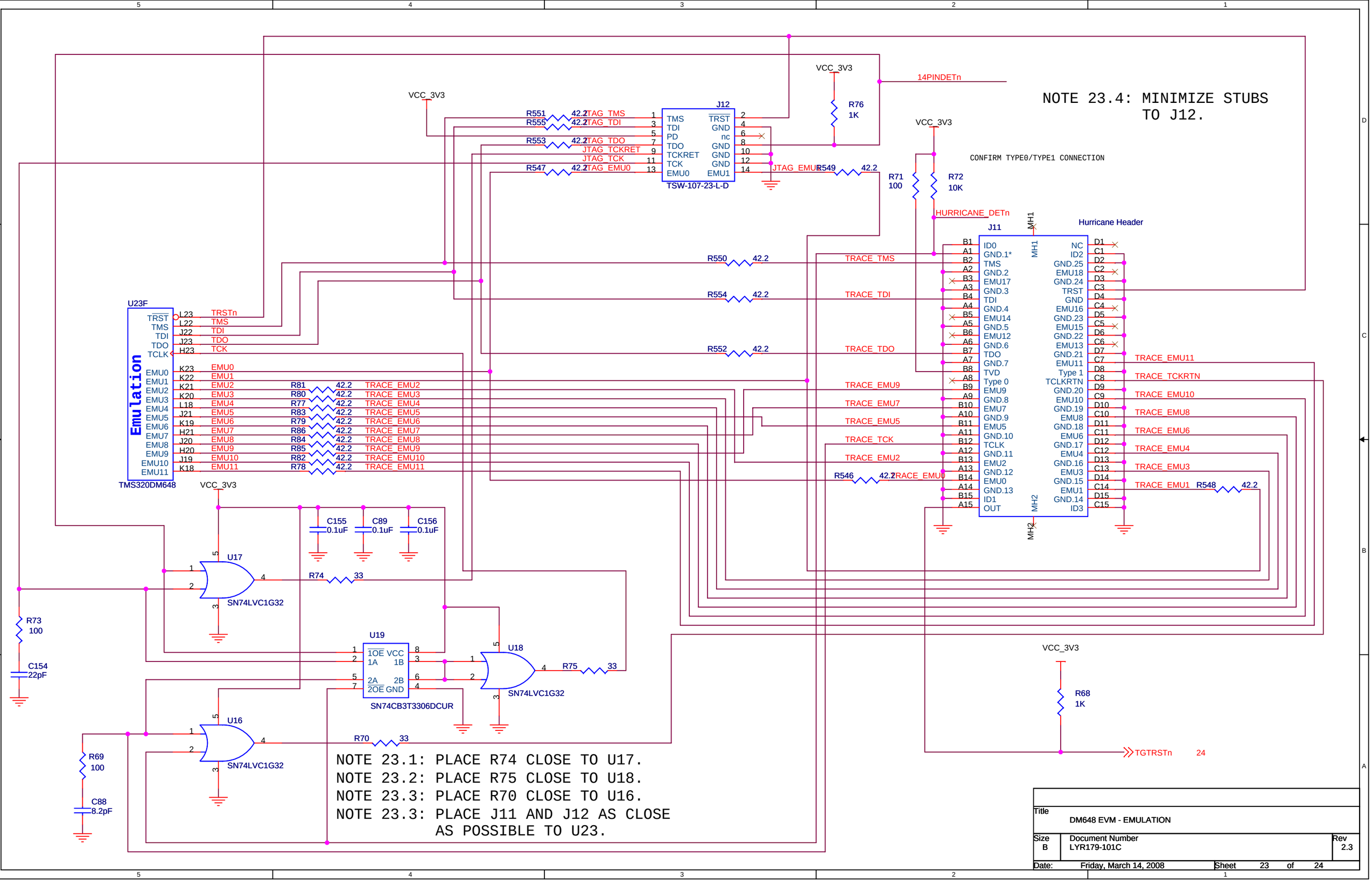
NOTE 23.4: MINIMIZE STUBS TO J12.
CONFIRM TYPE0/TYPE1 CONNECTION
J12
TSW-107-23-L-D
J11
Hurricane Header
MH1
MH2
U23F
Emulation
TMS320DM648
U17
U16
U18
U19
SN74LVC1G32
SN74CB3T3306DCUR
VCC_3V3
14PINDETn
HURRICANE_DETn
TGTRSTn
R76 1K
R71 100
R72 10K
R68 1K
R73 100
R74 33
R75 33
R70 33
R69 100
C154 22pF
C88 8.2pF
C155 0.1uF
C89 0.1uF
C156 0.1uF
R551 42.2 JTAG_TMS
R555 42.2 JTAG_TDI
R553 42.2 JTAG_TDO
JTAG_TCKRET
JTAG_TCK
R547 42.2 JTAG_EMU0
JTAG_EMU1 R549 42.2
R550 42.2 TRACE_TMS
R554 42.2 TRACE_TDI
R552 42.2 TRACE_TDO
TRACE_EMU9
TRACE_EMU7
TRACE_EMU5
TRACE_TCK
TRACE_EMU2
R546 42.2 TRACE_EMU0
TRACE_EMU11
TRACE_TCKRTN
TRACE_EMU10
TRACE_EMU8
TRACE_EMU6
TRACE_EMU4
TRACE_EMU3
TRACE_EMU1 R548 42.2
R81 R80 R77 R83 R79 R86 R84 R85 R82 R78 42.2 TRACE_EMU2 TRACE_EMU3 TRACE_EMU4 TRACE_EMU5 TRACE_EMU6 TRACE_EMU7 TRACE_EMU8 TRACE_EMU9 TRACE_EMU10 TRACE_EMU11
NOTE 23.1: PLACE R74 CLOSE TO U17.
NOTE 23.2: PLACE R75 CLOSE TO U18.
NOTE 23.3: PLACE R70 CLOSE TO U16.
NOTE 23.3: PLACE J11 AND J12 AS CLOSE AS POSSIBLE TO U23.
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USER CONTROLLED LEDS & SWITCHES

NOTE 24.1: PLACE THESE PARTS CLOSE TOGETHER

NOTE 24.2: SILKSCREEN: MSP430 GO by pin 1 RESET by pin 3

NOTE 24.3: SILKSCREEN: NTSC by pin 1 PAL by pin 3

NOTE 24.4: ISOLATE DIGITAL AND ANALOG GNDs AND CONNECT AT A SINGLE LOCATION IN THE GROUND PLANE.

SILKSCREEN: POWER

U63 PCA9535PW — RN24 RPACK8-33 — RN25 RPACK8-20K — DS11–DS17 LED_GRN — R318–R324 330

U44 MSP430F169IPM — L26 0R — C194 10u — C195 100n — C188 100n — C187 10u — Analog_GND

SW1 PUSHBUTTON SW — R115 33 — R116 10K — C193 1uF

J9 JTAG_MSP430 — Y3 32.768kHz — C191 18 pF — C192 18 pF — Y2 8MHz — C197 18 pF — C196 18 pF — C189 10u — C190 100n

JP1 3 PIN JUMPER — R45 1K — R44 1K — C123 0.1uF

R238 10K — R239 10K — BOOT_SW_INTn — USER_SW_INTn

R317 330 — DS10 LED_RED

R224 330 — R223 330 — DS2 LED_GRN — DS1 LED_RED

U46 PCA9535PW — U47 PCA9535PW

R240–R243 20K — SW4 DIP_SWITCH-4 — R247–R250 1.5K

R229 330 — DS7 LED_RED

R225–R228 330 — DS3–DS6 LED_GRN — LED_RED

JP5 3 PIN JUMPER — R252 1K — R251 1K

R133 10K — R134 NOPOP — R131 10K — R132 NOPOP — R129 10K — R130 NOPOP — R128 2.67K — R127 10K — R126 6.81K — R125 10K — R122 15K — R121 10K

R345 NOPOP — R333 1K — R349 NOPOP — R348 1K — R137 1K — R138 NOPOP — R139 470 — R140 470 — R338 0R — R120 NOPOP — R119 1K — R135 1K — R136 NOPOP

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