

# **TPS65910Ax User's Guide For AM335x Processors**

**Version C**

## **User's Guide**



Literature Number: SWCU093C  
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## ***TPS65910Ax User's Guide For AM335x Processors***

This user's guide can be used as a reference for connectivity between the TPS65910Ax power-management integrated circuit (PMIC) and the AM335x processor.

### **1 Introduction**

This user's guide can be used as a reference for connectivity between the TPS65910Ax PMIC and the AM335x processor. The TPS65910AA1 device is to support the AM335x processor with DDR2. TPS65910A3A1 and TPS65910A31A1 devices are to support the AM335x processor with DDR3. This user's guide does not provide details about the power resources or the functionality of the device. For such information, refer to the full specification document, *TPS65910 Data Manual*.

[Table 1](#) compares TPS65910Ax devices

**Table 1. TPS65910Ax comparison**

|                                     | <b>TPS65910A</b>                            | <b>TPS65910A3</b>                           | <b>TPS65910A31</b>                           |
|-------------------------------------|---------------------------------------------|---------------------------------------------|----------------------------------------------|
| <b>Memory</b>                       | DDR2<br>(VIO=1.8V)                          | DDR3<br>(VIO=1.5V)                          | DDR3<br>(VIO=1.5V)                           |
| <b>VRTC power mode in OFF state</b> | Low power mode<br>(VRTC_REG.VRTC_OFFMASK=0) | Low power mode<br>(VRTC_REG.VRTC_OFFMASK=0) | Full power mode<br>(VRTC_REG.VRTC_OFFMASK=1) |

### **2 Connection Diagram and TPS65910Ax EEPROM Definition**

[Figure 1](#) shows the connection diagram between the processor and the TPS65910A or TPS65910A3. [Figure 2](#) shows the connection diagram between the processor and TPS65910A31.

Notes for connection diagram:

- To support the processor power-up sequence, connect BOOT0 to ground and BOOT 1 to VRTC to select EEPROM boot mode.
- The TPS65910Ax digital control signal level is defined by the VDDIO connection.
- VAUX2 can support up to 300 mA for the specific case of a 3.3-V output level.
- The VDD1 and VDD2 connections shown in [Figure 1](#) and [Figure 2](#) is valid for processor version ZCZ (15 x 15). In ZCE (13 x 13), VDD\_MPU and VDD\_CORE are shorted internally. For ZCE, connect VDD1 to VDD\_MPU; VDD2 is free for system use.



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### Figure 2. AM335x Power Supply Connections with TPS65910A31

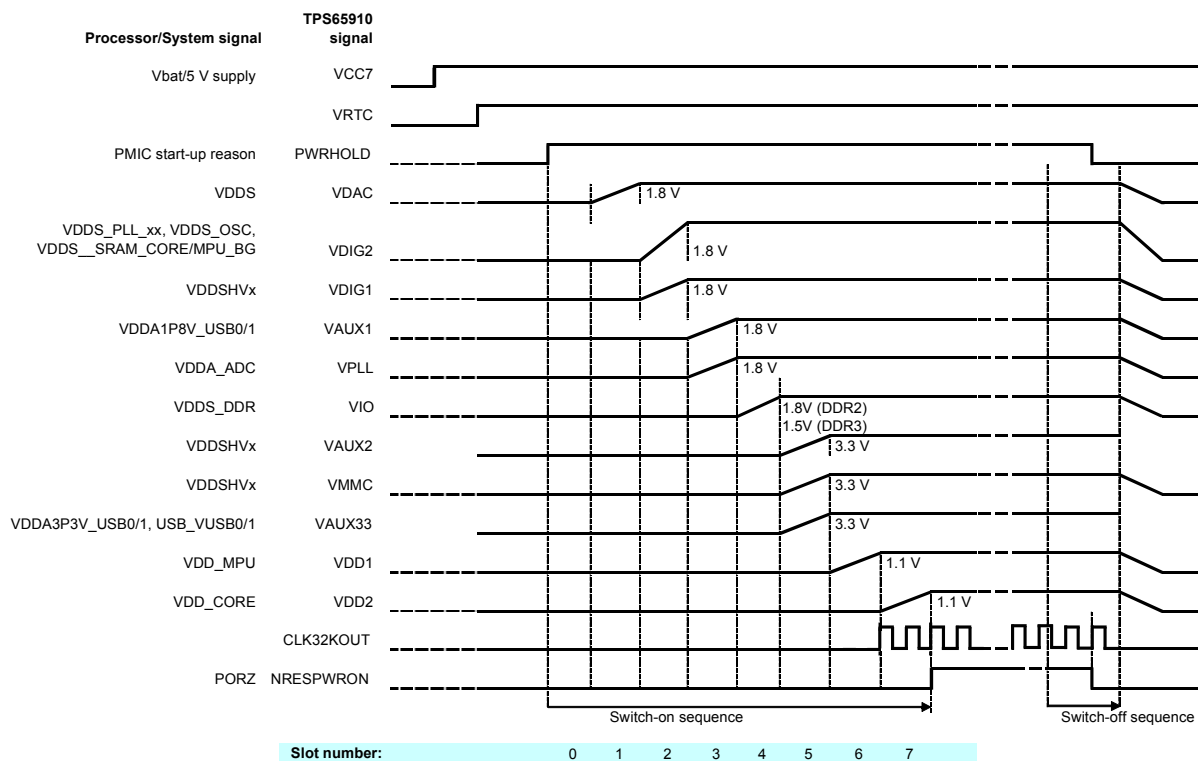
Table 2 lists the EEPROM definition of the TPS65910Ax and Figure 3 shows the corresponding power-up sequence.

**Table 2. EEPROM Configuration for TPS65910Ax**

| Register                     | Bit          | Description                                                                                                          | Option Selected                                                                            |
|------------------------------|--------------|----------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|
| VDD1_OP_REG                  | SEL          | VDD1 voltage level selection for boot                                                                                | 1.1                                                                                        |
| VDD1_REG                     | VGAIN_SEL    | VDD1 gain selection, x1 or x2                                                                                        | x1                                                                                         |
| EEPROM                       |              | VDD1 time slot selection                                                                                             | 6                                                                                          |
| DCDCCTRL_REG                 | VDD1_PSKIP   | VDD1 pulse skip mode enable                                                                                          | Skip enabled                                                                               |
| VDD2_OP_REG /<br>VDD2_SR_REG | SEL          | VDD2 voltage level selection for boot                                                                                | 1.1                                                                                        |
| VDD2_REG                     | VGAIN_SEL    | VDD2 gain selection, x1 or x3                                                                                        | x1                                                                                         |
| EEPROM                       |              | VDD2 time slot selection                                                                                             | 7                                                                                          |
| DCDCCTRL_REG                 | VDD2_PSKIP   | VDD2 pulse skip mode enable                                                                                          | Skip enabled                                                                               |
| VIO_REG                      | SEL          | VIO voltage selection                                                                                                | TPS65910AA1 1.8V (DDR2)<br>TPS65910A3A1 1.5V (DDR3)<br>TPS65910A31A1 1.5V (DDR3)           |
| EEPROM                       |              | VIO time slot selection                                                                                              | 4                                                                                          |
| DCDCCTRL_REG                 | VIO_PSKIP    | VIO pulse skip mode enable                                                                                           | Skip enabled                                                                               |
| EEPROM                       |              | VDD3 time slot                                                                                                       | OFF                                                                                        |
| VDIG1_REG                    | SEL          | LDO voltage selection                                                                                                | 1.8                                                                                        |
| EEPROM                       |              | LDO time slot                                                                                                        | 2                                                                                          |
| VDIG2_REG                    | SEL          | LDO voltage selection                                                                                                | 1.8                                                                                        |
| EEPROM                       |              | LDO time slot                                                                                                        | 2                                                                                          |
| VDAC_REG                     | SEL          | LDO voltage selection                                                                                                | 1.8                                                                                        |
| EEPROM                       |              | LDO time slot                                                                                                        | 1                                                                                          |
| VPLL_REG                     | SEL          | LDO voltage selection                                                                                                | 1.8                                                                                        |
| EEPROM                       |              | LDO time slot                                                                                                        | 3                                                                                          |
| VAUX1_REG                    | SEL          | LDO voltage selection                                                                                                | 1.8                                                                                        |
| EEPROM                       |              | LDO time slot                                                                                                        | 3                                                                                          |
| VMMC_REG                     | SEL          | LDO voltage selection                                                                                                | 3.3                                                                                        |
| EEPROM                       |              | LDO time slot                                                                                                        | 5                                                                                          |
| VAUX33_REG                   | SEL          | LDO voltage selection                                                                                                | 3.3                                                                                        |
| EEPROM                       |              | LDO time slot                                                                                                        | 5                                                                                          |
| VAUX2_REG                    | SEL          | LDO voltage selection                                                                                                | 3.3                                                                                        |
| EEPROM                       |              | LDO time slot                                                                                                        | 5                                                                                          |
| CLK32KOUT pin                |              | CLK32KOUT time slot                                                                                                  | 7                                                                                          |
| NRESPWRON pin                |              | NRESPWRON time slot                                                                                                  | 7 + 1                                                                                      |
| VRTC_REG                     | VRTC_OFFMASK | 0 = VRTC LDO will be in low-power mode during OFF state.<br>1 = VRC LDO will be in full-power mode during OFF state. | TPS65910AA1 Low-power mode<br>TPS65910A3A1 Low-power mode<br>TPS65910A31A1 High-power mode |
| DEVCTRL_REG                  | RTC_PWDN     | 0 = RTC in normal-power mode<br>1 = Clock gating of RTC register and logic, low-power mode                           | 1                                                                                          |
| DEVCTRL_REG                  | CK32K_CTRL   | 0 = Clock source is crystal/external clock.<br>1 = Clock source is internal RC oscillator.                           | RC                                                                                         |
| DEVCTRL2_REG                 | TSLOT_LENGTH | Boot sequence time slot duration:<br>0 = 0.5 ms<br>1 = 2 ms                                                          | 2 ms                                                                                       |

**Table 2. EEPROM Configuration for TPS65910Ax (continued)**

| Register     | Bit            | Description                                                                                                                                | Option Selected |
|--------------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------|-----------------|
| DEVCTRL2_REG | IT_POL         | 0 = INT1 signal will be active low.<br>1 = INT1 signal will be active high.                                                                | Active high     |
| INT_MSK_REG  | VMBHI_IT_MSK   | 0 = Device automatically switches on at NO SUPPLY-to-OFF or BACKUP-to-OFF transition.<br>1 = Start-up reason is required before switch-on. | 1               |
| VMBCH_REG    | VMBCH_SEL[1:0] | Select threshold for main battery comparator threshold VMBCH.                                                                              | 3 V             |


**Figure 3. Power-Up and Power-Down Timing Diagram**

### **3 First Initialization**

#### **3.1 I/O Polarity/Muxing Configuration**

Program DEVCTRL2\_REG.SLEEPSIG\_POL according to the GPIO level setting on the processor. This can be set to active low or active high for SLEEP transitions. Software configuration allows specific power resources to enter a low consumption state.

Set DEVCTRL\_REG.DEV\_SLP = 1 to allow SLEEP transitions when requested.

Update the GPIO0 configuration (GPIO0\_REG) based on your needs.

#### **3.2 Define Wake-Up/Interrupt Event (SLEEP or OFF)**

Select the appropriate bits in the INT\_MSK\_REG and INT\_MSK2\_REG registers to activate an interrupt to the processor on the INT1 line.

#### **3.3 Backup Battery Configuration**

If a backup battery is used, enable backup battery charging by setting the BBCH\_REG.BBCHEN bit to 1. The maximum charge voltage can be set based on the backup battery specifications by using the BBSEL bits.

#### **3.4 DCDC and Voltage Scaling Resource Configuration**

If the SmarReflex interface is not used for voltage scaling (power saving), these pins can be used to control the power resources.

Configure two operating voltages for DCDC1 and DCDC2

- VDDx\_OP\_REG.SEL= Roof voltage (ENx ball high)
- VDDx\_SR\_REG.SEL = Floor voltage (ENx ball low)

Assign control for DCDC1 to SCLSR\_EN1 and DCDC2 to SCLSR\_EN2:

- Set EN1\_SMPS\_ASS\_REG.VDD1\_EN1 = 1
- Set EN2\_SMPS\_ASS\_REG.VDD2\_EN1 = 2
- Set SLEEP\_KEEP\_RES\_ON\_REG.VDD1\_KEEPPON = 1 (allow low-power mode)
- Set SLEEP\_KEEP\_RES\_ON\_REG.VDD2\_KEEPPON = 1 (allow low-power mode)

#### **3.5 Sleep Platform Configuration**

Configure the state of the LDOs when the SLEEP signal is used (by default all resources go into SLEEP state; in SLEEP state the LDO voltage is maintained but transient and load capability are reduced).

Resources that must provide full load capability must be set in the SLEEP\_KEEP\_LDO\_ON\_REG register.

Resources that can be set off in SLEEP state to optimize power consumption must be set in the SLEEP\_SET\_LDO\_OFF\_REG register.

## 4 Event Management Through Interrupts

### 4.1 **INT\_STS\_REG.VMBHI\_IT**

The INT\_STS\_REG.VMBHI\_IT bit indicates that the supply (VBAT) is connected (leaving the BACKUP or NO SUPPLY state), the system must be initialized. (See [Section 3](#), *First Initialization*.)

### 4.2 **INT\_STS\_REG.PWRON\_IT**

INT\_STS\_REG.PWRON\_IT is triggered when the PWRON button is pressed. If device is in the OFF or SLEEP state, this acts as a wake-up event and resources are reinitialized.

### 4.3 **INT\_STS\_REG.PWRON\_LP\_IT**

INT\_STS\_REG.PWRON\_LP\_IT is the PWRON long-press interrupt. This interrupt is generated when the PWRON button is pressed for 6 seconds. The application processor can make a decision to acknowledge the interrupt. If this interrupt is not acknowledged in the next 2 seconds then the device interprets this as a power-down event.

### 4.4 **INT\_STS\_REG.HOTDIE\_IT**

INT\_STS\_REG.HOTDIE\_IT indicates that the temperature of die is reaching the maximum limit. Software must take action to decrease the power consumption before automatic shutdown.

### 4.5 **INT\_STS\_REG.VMBDCH\_IT**

INT\_STS\_REG.VMBDCH\_IT indicates that the input supply is low and the processor must prepare a shutdown to prevent losing data. This interrupt is linked to VBAT but does not apply to a system where the PMIC is connect to 5-V rails and not directly to VBAT.

### 4.6 **INT\_STS2\_REG.GPIO\_R/F\_IT**

INT\_STS2\_REG.GPIO\_R/F\_IT is the GPIO interrupt event and can be used to wake up the device from SLEEP state. This can be an interrupt coming from any peripheral device or alike. This wake-up event is not valid for transitions from the OFF state.

### 4.7 **INT\_STS\_REG.RTC\_ALARM\_IT**

INT\_STS\_REG.RTC\_ALARM\_IT is triggered when the RTC alarm set time is reached.

## 5 Revision History

[Table 3](#) lists the changes made since the previous version of this document.

**Table 3. Revision History**

| Section                                                             | Location                 | Additions/Modifications/Deletions                                                                    |
|---------------------------------------------------------------------|--------------------------|------------------------------------------------------------------------------------------------------|
| <a href="#">Connection Diagram and TPS65910Ax EEPROM Definition</a> | <a href="#">Figure 1</a> | Update <a href="#">Figure 1</a> : Replace Default OFF with DEFAULT ON in VD1G1, VD1G2, VAUX1, VAUX33 |
| <a href="#">Connection Diagram and TPS65910Ax EEPROM Definition</a> | <a href="#">Figure 2</a> | Update <a href="#">Figure 2</a> : Replace Default OFF with DEFAULT ON in VD1G1, VD1G2, VAUX1, VAUX33 |

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