



APPLICATION NOTES:

1. The schematic shown is based on the TPS40140EVM-003 featuring a 1.5V output at 32A
2. The FASTSSWAIT=1 reduces the internal wait time before soft-start to 4 switching cycles from a normal cycle count of 64 switching cycles. This is used to speed up the simulation. Using FASTSSWAIT=0 gives a internal wait time of 64 cycles.
3. The FASTPGVOLT=1 reduces the Power Good (PGOOD) enable Threshold of 1.4V to 0.8V to reduce the simulation time. So the user need not wait till the TRK pin reaches 1.4V. However the faults are still enabled only after TRK pin reaches 1.4V. Using FASTPGVOLT=0 gives a PGOOD enable threshold of 1.4V.
4. The Soft-Start capacitor has been reduced to 2nF. This is to reduce the simulation time. The actual EVM uses a SS capacitor of 22nF. The user is cautioned that using a smaller capacitor could impact the over-current behavior during startup. The faults are enabled only after TRK reaches 1.4V. However, using a smaller soft-start capacitor could mean that transients on the COMP pin would take time to settle and this could trigger an overcurrent condition when faults are enabled.
5. The DUMMY_TEMPIN input is used to simulate the thermal shutdown behavior of the IC. The actual part does not have a TEMPIN pin. The temperature input has been shown to rise to 90C in 10us. This is just a dummy input and does not reflect the actual temperature behavior of the part.
6. The output transistors and BOOT diodes in this test bench are different from that in the EVM. These parts have been used primarily based on their model availability and have not been justified based on component selection criterion.
7. The simulation time is around 56mins on a 3GHz machine.
8. The shutdown current, UVLO hysteresis(40mV), undervoltage delay, PGOOD delay, PGOOD trip hysteresis have not been modeled.
9. Typical values specified in the datasheet have been used to develop this model. Min and Max specifications in the datasheet have not been considered in this model.