TPS53640A 4-Phase, D-CAP+, Step-Down Controller with PMBus Interface for VR12 and VR12.5 Platforms

1 Features

- Intel® VR12.x Platform Serial VID (SVID) Compliant
- 4-Phase Operation
- Full VR12.5 Platform Server Feature Set Including Digital Current Monitor and VR_Fault
- Supports VR12.0 Platform Single Output
- 8-Bit DAC with 0.5-V to 2.5-V Output Range
- Dynamic Phase Shedding with Programmable Current Thresholds to Optimize the Efficiency at Light or Heavy Loads
- 8 Independent Levels of Overshoot Reduction (OSR) and Undershoot Reduction (USR)
- Driverless Configurations for Efficient High-Frequency Switching
- Supports TI NexFET™ MOSFET Power Stages
- Supports Both Zero Loadline and Accurate Loadline Applications
- Frequency Selection: 300-kHz to 1-MHz
- Patented AutoBalance Phase Balancing
- Per-Phase Current Limit
- PMBus™ System Interface for Telemetry of Voltage, Current, Power, Temperature, and Fault Conditions
- Programmable VID and Loadline Regulation via PMBus Interface
- Conversion Voltage Range: 4.5 V to 17 V
- Small 5 mm × 5 mm, 40-Pin QFN Package

2 Applications

- VR12.0 and VR12.5 Platform V_{CORE} and DDR Memory for Server Applications

3 Description

The TPS53640A device is a fully SVID-compliant,VR12.x platform step-down controller with PMBus interface. Advanced control features such as D-CAP+™ architecture, undershoot reduction (USR) and overshoot reduction (OSR) provide fast transient response, low output capacitance, and high efficiency. The TPS53640A device also provides novel phase interleaving strategy and dynamic phase shedding for efficiency improvement at differing loads. The TPS53640A device also supports single-phase operation in CCM or DCM for improving light-load efficiency. The full complement of VR12.5 platform I/O pins are integrated into the TPS53640A device including VR_RDY, ALERT, VR_HOT, and VR_FAULT.

Adjustable control of V_{CORE} slew rate and voltage positioning round out the VR12.5 platform features. In addition, the TPS53640A device supports the PMBus communication interface with systems for telemetry of voltage, current, power, temperature, and fault conditions. All parameters configured by pin settings can be also programmed via PMBus to minimize external component count.

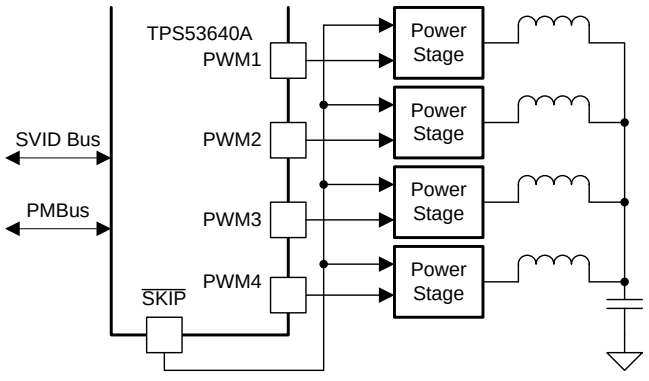
The TPS53640A device package is a space-saving, thermally-enhanced 40-pin QFN and is rated to operate from –10°C to 105°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS53640A	QFN (40)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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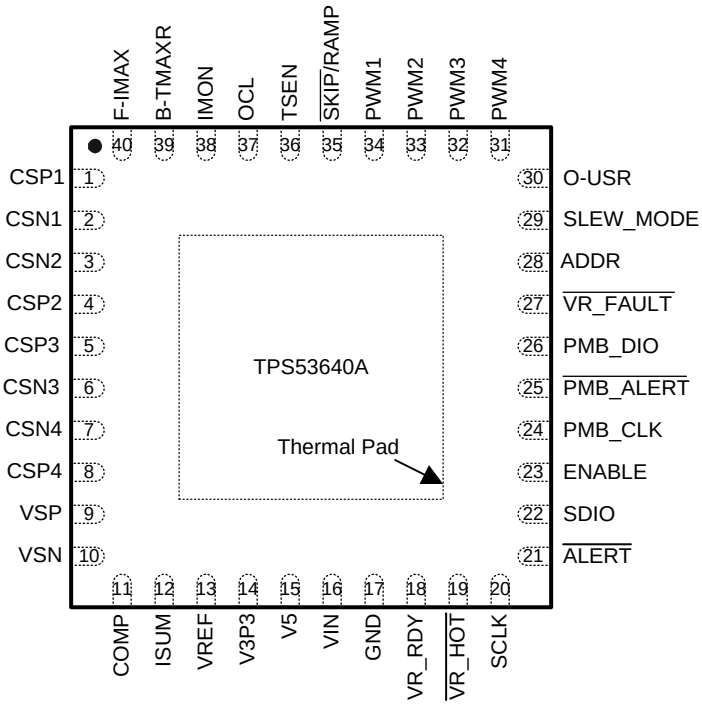
5 Pin Configuration and Functions

RSB (QFN) PACKAGE
40 PINS
(TOP VIEW)



NC = No internal connection

Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
ADDR	28	I	Voltage divider to VREF. A resistor connected between this pin and GND sets the lower three bits of the SVID address. The voltage level sets the highest bit of the SVID address and the 4-bit PMBus address. Both are latched at V3P3 power up.
$\overline{\text{ALERT}}$	21	O	SVID interrupt line. Open drain
B-TMAXR	39	I	Voltage divider to VREF. A resistor connected between this pin and GND sets the BOOT voltage (8 options). The voltage level sets the maximum temperature (T_{MAX}) for asserting $\overline{\text{VR\_HOT}}$ (8 options) and the lowest two bits of ramp compensation. Both are latched at V3P3 power up.
COMP	11	O	Output of the g_M error amplifier. Resistors and capacitors connected between this pin and the VREF pin set the compensation.
CSN1	2	I	Negative current sense inputs. Connect to the most negative node of current sense resistor or inductor DCR sense network.
CSN2	3		
CSN3	6		
CSN4	7		
CSP1	1	I	Positive current sense inputs. Connect to the most positive node of current sense resistor or inductor DCR sense network.
CSP2	4		
CSP3	5		
CSP4	8		
ENABLE	23	I	VR enable. 1-V I/O level; 100ns de-bounce. Regulator places PWM into tri-state mode when brought low.

(1) I = input, O = output, P = power, I/O = bi-directional, G = ground

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
F-IMAX	40	I	Voltage divider to VREF pin. A resistor connected between this pin and GND sets the operating frequency of the controller (8 options). The voltage level sets the maximum current (I_{MAX}) for IMON reporting. The I_{MAX} value is an 8-bit A/D where $V_{IMAX} = V_{VREF} \times I_{MAX} / 255$. Both are latched at V3P3 power up. Use resistors with a tolerance of 0.1% on this pin in order to get accurate I_{MAX} settings.
GND	17	G	Ground pin.
IMON	38	O	Analog current monitor output. Use resistors with a tolerance of 0.1% on this pin. $V_{IMON} = \frac{I_{OUT} \times R_{DCR} \times 40 \times R_{IMON}}{35\,k\Omega}$
ISUM	12	O	Use one NTC for thermal compensation of DCR current sensing for accurate load-line. $V_{ISUM} = \frac{I_{OUT} \times DCR \times 6 \times g_{M(isum)} \times R_{ISUM\_TC}}{n}$ (where n is the number of active phases)
OCL	37	I	A resistor (R_{OCL}) connected between this pin and the VREF pin sets the per-phase current limit threshold.
O-USR	30	I	Voltage divider to VREF. A resistor connected between this pin and GND selects 1 of 8 OSR thresholds. The voltage level sets 1 of 8 USR levels. Both are latched at V3P3 power up.
$\overline{\text{PMB\_ALERT}}$	25	O	I^2C PMBus interrupt line. Open drain.
PMB_CLK	24	I	I^2C PMBus clock. 3.3-V logic level. Open drain.
PMB_DIO	26	I/O	I^2C PMBus digital I/O line. 3.3-V logic level. Open drain.
PWM1	34	O	PWM signals for each phase
PWM2	33		
PWM3	32		
PWM4	31		
SCLK	20	I	SVID clock. 1-V logic level.
SDIO	22	I/O	SVID digital I/O line. 1-V logic level. Route between the SCLK pin and the $\overline{\text{ALERT}}$ pin to prevent cross-talk.
$\overline{\text{SKIP}}$-RAMP	35	O	This pin is active high during FCCM operation and active low during skip mode operation. A resistor connected between this pin and GND sets the highest bit of ramp compensations.
SLEW-MODE	29	I	Voltage divider to VREF. A resistor connected between this pin and GND sets 4 slew rates and the output voltage offset. Slow SLEWRATE = fast SLEWRATE/4. PMBus SLEWRATE = fast SLEWRATE. The voltage level sets 5-bit operation modes: B[4] for VR modes (1 for VR12.0; 0 for VR12.5). B[2] for enabling temperature compensations (1 for enable; 0 for disable). B[1] for enabling dynamic phase add/drop (1 for enable; 0 for disable). B[0] sets zero load-line (1 for zero load-line; 0 for non-zero load-line)
TSEN	36	I/O	Connect an NTC thermistor divider from the VREF pin to GND or to the TAO pin of TI power stages (ex: CSD95373A) to sense the highest temperature of the power stages and to sense the fault signal from the power stages.
V3P3	14	P	3.3-V power input. Used to power up all digital logic circuits. Bypass this pin to GND with a ceramic capacitor with a value greater than or equal to 1 µF. The slew rate of the 3.3-V supply must be higher than 1.5 V/ms.
V5	15	O	5-V, 10 mA, LDO reference voltage. Used to power up internal analog circuits. Bypass this pin to GND with a ceramic capacitor with a value greater than or equal to 1 µF. Do not use this pin to supply external components.
VIN	16	P	12-V voltage supply. Also used for input voltage sensing for on-time control and input undervoltage lockout.
VR_RDY	18	O	Power good open-drain output for the controller.
$\overline{\text{VR\_FAULT}}$	27	O	VR fault indicator (open-drain). The failures include overvoltage, over-temperature, and input overcurrent conditions. The fault signal should be used on the platform to remove the power source either by firing a shunting SCR to blow a fuse or by turning off the AC power supply. When the failure occurs, the $\overline{\text{VR\_FAULT}}$ pin is LOW, and causes the device to enter latch-off mode.
$\overline{\text{VR\_HOT}}$	19	O	VR12.5 thermal flag open drain output. Active low. Follow Intel *Platform Design Guide* for the pull-up resistor selection.
VREF	13	O	1.7-V, 500-µA, LDO reference voltage. Bypass this pin to GND with a ceramic capacitor with a value of 0.33 µF.
VSN	10	I	Negative input of the remote voltage sense.

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
VSP	9	I	Positive input of the remote voltage sense.
Thermal Pad		GND	Thermal pad. Connect to the ground plane with multiple vias.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Input Voltage	VIN	–0.3	19	V
	V3P3, ADDR, ENABLE, OCL, CSP1, CSP2, CSP3, CSP4, CSN1, CSN2, CSN3, CSN4, VSP,SCLK, SDIO, PMB_CLK, PMB_DIO, F-IMAX, B-TMAXR, SLEW-MODE, O-USR, IMON	–0.3	3.6	V
	TSEN, COMP	–0.3	6	
	GND, VSN	–0.3	0.3	
Output Voltage	VREF	–0.3	1.8	V
	V5	–0.3	6	
	VR_RDY, $\overline{\text{ALERT}}$, VR_$\overline{\text{HOT}}$, $\overline{\text{PMB\_ALERT}}$, $\overline{\text{VR\_FAULT}}$, ISUM	–0.3	3.6	
	PWM1, PWM2, PWM3, PWM4, $\overline{\text{SKIP}}$-RAMP	–0.3	3.6	
Operating Junction Temperature, T_J		–30	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal GND unless otherwise noted.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2.5	2.5	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1.5	1.5	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Input voltage	VIN	4.5	12	17	V
		V3P3	3.1	3.3	3.5	
		ADDR, B-TMAXR, OCL,F-IMAX, O-USR, IMON, SLEW-MODE	0.1		V_{VREF}	
		CSP1, CSP2, CSP3, CSP4, CSN1, CSN2, CSN3, CSN4, VSP, COMP	–0.1		2.5	
		ENABLE, PMB_CLK, PMB_DIO, SCLK, SDIO	–0.1		3.5	
		GND, VSN	–0.1		0.1	
V_O	Output voltage	VREF	–0.1		1.72	V
		V5	4.5		5.5	
		VR_RDY, $\overline{\text{ALERT}}$, $\overline{\text{VR\_HOT}}$, $\overline{\text{PMB\_ALERT}}$, $\overline{\text{VR\_FAULT}}$, ISUM, PWM1, PWM2, PWM3, PWM4, $\overline{\text{SKIP}}$-RAMP	–0.1		3.5	
T_A	Operating free air temperature		–10		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		QFN (40 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18	
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	7.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended free-air temperature range, V_{VIN} = 12 V; V_{V3P3} = 3.3 V; VSN = GND, V_{VSP} = V_{CORE} 4-phase operation (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY: CURRENTS, UVLO, AND POWER-ON RESET						
I_{VIN}	VIN supply current 4-phase active	$V_{VDAC} < V_{VSP} < V_{VDAC}$ + 100 mV, ENABLE = HI			5	mA
I_{V3P3}	V3P3 supply current	SVID bus idle, PMBus idle, ENABLE = HI			2.5	mA
$I_{V3P3SBY}$	V3P3 standby current	ENABLE = LO			2.5	mA
V_{3UVLOH}	V3P3 UVLO OK threshold	Ramp up	2.6	2.8	3	V
V_{3UVLOL}	V3P3 UVLO fault threshold	Ramp down	2.4	2.6	2.8	V
V_{V5}	V5 output	V_{VIN} = 12 V and 19 V, ENABLE = HI	4.8	5	5.2	V
REFERENCES: DAC AND VREF						
V_{VIDSTP}	VID step size	VR12.5: Change VID0 HI to LO to HI		10		mV
		VR12.0: Change VID0 HI to LO to HI		5		mV
V_{DAC0}	VDAC tolerance	VR12.0: 0.25 V ≤ V_{ID} ≤ 0.795V, I_{CORE} = 0 A	–8		8	mV
V_{DAC1}		VR12.0: 0.8 ≤ V_{ID} ≤ 0.995V, I_{CORE} = 0 A	–5		5	mV
V_{DAC2}		VR12.0: 1 V ≤ V_{ID} ≤ 1.52 V, I_{CORE} = 0 A	–0.5%		0.5%	
V_{DAC3}		VR12.5: 0.50 ≤ V_{ID} ≤ 0.99V, I_{CORE} = 0 A	–10		10	mV
V_{DAC4}		VR12.5: 1.00 V ≤ V_{ID} ≤ 1.49 V, I_{CORE} = 0 A	–8		8	mV
V_{DAC5}		VR12.5: 1.50 V ≤ V_{ID} ≤ 2.50 V, I_{CORE} = 0 A	–0.5%		0.5%	
V_{VREF}	VREF output	V_{VIN} = 4.5 V or , V_{VIN} = 12 V, or V_{VIN} = 19 V, I_{VREF}= 0 V	1.685	1.7	1.715	V
$V_{VREFSRC}$	VREF output source	0 A ≤ I_{VREF} = 500 µA	–4	-3		mV
$V_{VREFSNK}$	VREF output sink	–500 µA ≤ I_{VREF} = 0 A		3	4	mV
CURRENT SENSE: AMPLIFIER AND PHASE BALANCING						
I_{CS}	CS pin input bias current	CSPx	–50	0.2	50	nA
I_{BAL_TOL} (1)	Internal current share tolerance	V_{DAC} = 1.70 V	–3%		3%	
$V_{ISUMOFS}$	Internal ISUM amplifier offset	Output offset of I_{ISUM} amplifier by forcing CSPx = CSNx with R_{ISUM} = 4 kΩ	–4.2		4.2	mV
COMPENSATOR: VOLTAGE POSITIONING AND AMPLIFIER						
$g_{M(isum)}$	ISUM amplifier transconductance	V_{VSP} = 1.7 V	485	500	515	µS
$V_{CCLAMPN}$	COMP amplifier negative clamp voltage	(V_{VREF} – V_{COMP})		V_{RAMP} + 30		mV
$V_{CCLAMPP}$	COMP amplifier positive clamp voltage	4-phase operation, (V_{COMP} – V_{VREF})		2.25		V
$V_{COMPOFS}$	Closed-loop V_O offset	Closed-loop offset in 1-phase operation, V_{OUT} = 1.7 V, ZLL	–6		6	mV
VOLTAGE SENSE: VSP AND VSN						
I_{VSP}	VSP input bias current	Not in fault, disable or UVLO, V_{VSP} = V_{VDAC} = 2.3 V, V_{VSN} = 0 V			310	µA
I_{VSN}	VSN input bias current	Not in fault, disable or UVLO, V_{VSP} = V_{VDAC} = 2.3 V, V_{VSN} = 0 V			–18	µA

(1) Specified by design. Not production tested.

Electrical Characteristics (continued)

over recommended free-air temperature range, V_{VIN} = 12 V; V_{V3P3} = 3.3 V; VSN = GND, V_{VSP} = V_{CORE} 4-phase operation (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC (SCLK, SDIO, $\overline{\text{ALERT}}$, $\overline{\text{VR\_HOT}}$, VR_RDY AND ENABLE) INTERFACE PINS: I/O VOLTAGE AND CURRENT						
R_{RSVIDL}	Open drain pull-down resistance	SDIO, $\overline{\text{ALERT}}$, $\overline{\text{VR\_HOT}}$, pulldown resistance at 0.31 V	4	8	13	Ω
R_{RPGDL}	Open drain pull-down resistance	VR_RDY,RPD at 0.31 V		36	50	Ω
I_{VRTTLK}	Open drain leakage current	SDIO, $\overline{\text{ALERT}}$, $\overline{\text{VR\_HOT}}$,VR_RDY, Hi-Z leakage, apply 1.1 V in off state	–2	0.2	2	µA
V_{IL}	Low-level input voltage	SCLK, SDIO			0.45	V
V_{IH}	High-level input voltage		0.65			V
V_{hys}	Hysteresis		0.05			V
V_{ENL}	ENABLE logic low				0.3	V
V_{ENH}	ENABLE logic high		0.8			V
I_{ENH}	I/O 1.1-V leakage	Leakage current , V_{ENABLE} = 1.1 V			25	µA
OCL PIN: PER-PHASE OVER-CURRENT THRESHOLDS						
I_{OCL}	OCL source current	3 kΩ ≤ R_{OCL} ≤ 15 kΩ, MODE [2] = 1	9.5	10	10.5	µA
		3 kΩ ≤ R_{OCL} ≤ 30 kΩ, MODE [2] = 0	6.65	7	7.35	µA
T_{OCL} (2)	OCL source current temperature coefficient	3 kΩ ≤ R_{OCL} ≤ 15 kΩ,	3850	4000	4150	ppm/°C
SLEW-MODE PIN: SLEW RATES and MODE SELECTIONS						
SL_F	VSP Slew SetVID_Fast	SLEWRATE = 10 mV/µs	10			mV/µs
SL_S	VSP Slew SetVID_Slow	SLEWRATE = 10 mV/µs	2.5			mV/µs
SL_{SET}	Slew rate setting	$R_{SLEW-MODE}$ ≤ 20 kΩ or MFR_SPEC_13[1:0] = 00b	5			mV/µs
		$R_{SLEW-MODE}$ = 24 kΩ or MFR_SPEC_13[1:0] = 01b	10			mV/µs
		$R_{SLEW-MODE}$ = 30 kΩ or MFR_SPEC_13[1:0] = 10b	15			mV/µs
		$R_{SLEW-MODE}$ = 39 kΩ or MFR_SPEC_13[1:0] = 11b	20			mV/µs
		$R_{SLEW-MODE}$ = 56 kΩ or MFR_SPEC_13[1:0] = 00b	5			mV/µs
		$R_{SLEW-MODE}$ = 75 kΩ or MFR_SPEC_13[1:0] = 01b	10			mV/µs
		$R_{SLEW-MODE}$ = 100 kΩ or MFR_SPEC_13[1:0] = 10b	15			mV/µs
		$R_{SLEW-MODE}$ ≥ 150 kΩ or MFR_SPEC_13[1:0] = 11b	20			mV/µs
O-USR PIN: OVERSHOOT AND UNDERSHOOT REDUCTION THRESHOLD SETTING						
V_{OSR}	OSR voltage setting	R_{O-USR} ≤ 20 kΩ or MFR_SPEC_09[2:0] = 000b;	5	25	45	mV
		R_{O-USR} = 24 kΩ or MFR_SPEC_09[2:0] = 001b;	15	35	55	mV
		R_{O-USR} = 30 kΩ or MFR_SPEC_09[2:0] = 010b;	25	45	65	mV
		R_{O-USR} = 39 kΩ or MFR_SPEC_09[2:0] = 011b;	45	65	85	mV
		R_{O-USR} = 56 kΩ or MFR_SPEC_09[2:0] = 100b;	65	85	105	mV
		R_{O-USR} = 75 kΩ or MFR_SPEC_09[2:0] = 101b;	85	105	125	mV
		R_{O-USR} = 100 kΩ or MFR_SPEC_09[2:0] = 110b;	105	125	145	mV
		R_{O-USR} ≥ 150 kΩ (OSR OFF) or MFR_SPEC_09[2:0] = 111b;		OFF		mV
V_{USR}	USR voltage setting	V_{O-USR} = 0.2 V or MFR_SPEC_09[6:4] = 000b;	2	15	30	mV
		V_{O-USR} = 0.4 V or MFR_SPEC_09[6:4] = 001b;	10	25	40	mV
		V_{O-USR} = 0.6 V or MFR_SPEC_09[6:4] = 010b;	20	35	50	mV
		V_{O-USR} = 0.8 V or MFR_SPEC_09[6:4] = 011b;	40	55	70	mV
		V_{O-USR} = 1.0 V or MFR_SPEC_09[6:4] = 100b;	60	75	90	mV
		V_{O-USR} = 1.2 V or MFR_SPEC_09[6:4] = 101b;	80	95	110	mV
		V_{O-USR} = 1.4 V or MFR_SPEC_09[6:4] = 110b;	100	115	130	mV
		V_{O-USR} > 1.55 V (USR OFF) or MFR_SPEC_09[6:4] = 111b;		OFF		mV
V_{OSRHYS} (2)	OSR and USR voltage hysteresis	All settings	8.2	9.2	10	mV
F-IMAX PIN MAXIMUM CURRENT SETTINGS						
V_{IMAX} (2)	Maximum current values	$V_{F-IMAX(min)}$ = 133 mV or MFR_SPEC_10 = 20d		20		A
		$V_{F-IMAX(max)}$ = 1.7 V or MFR_SPEC_10 = 255d		255		

(2) Specified by design. Not production tested.

Electrical Characteristics (continued)

over recommended free-air temperature range, V_{VIN} = 12 V; V_{V3P3} = 3.3 V; VSN = GND, V_{VSP} = V_{CORE} 4-phase operation (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RAMP SETTINGS						
V_{RAMP}	Internal ramp voltage setting	MFR_SPEC_14[2:0] = 000b or R $\overline{SKIP}$-RAMP = 20 kΩ and $V_{B-TMAXR}$ ≤ 0.027 V or $V_{B-TMAXR}$ = 0.24 V or $V_{B-TMAXR}$ = 0.452 V or $V_{B-TMAXR}$ = 0.665 V or $V_{B-TMAXR}$ = 0.877 V or $V_{B-TMAXR}$ = 1.09 V or $V_{B-TMAXR}$ = 1.302 V or $V_{B-TMAXR}$ = 1.515 V with ±10 mV	16	20	24	mV_{PP}
		MFR_SPEC_14[2:0] = 000b or R $\overline{SKIP}$-RAMP = 20 kΩ and $V_{B-TMAXR}$ = 0.08 V or $V_{B-TMAXR}$ = 0.293 V or $V_{B-TMAXR}$ = 0.505 V or $V_{B-TMAXR}$ = 0.718 V or $V_{B-TMAXR}$ = 0.93 V or $V_{B-TMAXR}$ = 1.143 V or $V_{B-TMAXR}$ = 1.355 V or $V_{B-TMAXR}$ = 1.568 V with ±10 mV	36	40	44	
		MFR_SPEC_14[2:0] = 000b or R $\overline{SKIP}$-RAMP = 20 kΩ and $V_{B-TMAXR}$ = 0.133 V or $V_{B-TMAXR}$ = 0.346 V or $V_{B-TMAXR}$ = 0.558 V or $V_{B-TMAXR}$ = 0.771 V or $V_{B-TMAXR}$ = 0.983 V or $V_{B-TMAXR}$ = 1.196 V or $V_{B-TMAXR}$ = 1.408 V or $V_{B-TMAXR}$ = 1.621 V with ±10 mV	54	60	66	
		MFR_SPEC_14[2:0] = 000b or R $\overline{SKIP}$-RAMP = 20 kΩ and $V_{B-TMAXR}$ = 0.186 V or $V_{B-TMAXR}$ = 0.399 V or $V_{B-TMAXR}$ = 0.611 V or $V_{B-TMAXR}$ = 0.823 V or $V_{B-TMAXR}$ = 1.036 V or $V_{B-TMAXR}$ = 1.249 V or $V_{B-TMAXR}$ = 1.461 V with ±10 m V or $V_{B-TMAXR}$ ≥ 1.674 V	72	80	88	
		MFR_SPEC_14[2:0] = 000b or R $\overline{SKIP}$-RAMP ≥ 230 kΩ and VB-TMAXR ≤ 0.027 V or $V_{B-TMAXR}$ = 0.24 V or $V_{B-TMAXR}$ = 0.452 V or $V_{B-TMAXR}$ = 0.665 V or $V_{B-TMAXR}$ = 0.877 V or $V_{B-TMAXR}$ = 1.09 V or $V_{B-TMAXR}$ = 1.302 V or $V_{B-TMAXR}$ = 1.515 V with ±10 mV	90	100	110	
		MFR_SPEC_14[2:0] = 000b or R $\overline{SKIP}$-RAMP ≥ 230 kΩ and $V_{B-TMAXR}$ = 0.08 V or $V_{B-TMAXR}$ = 0.293 V or $V_{B-TMAXR}$ = 0.505 V or $V_{B-TMAXR}$ = 0.718 V or $V_{B-TMAXR}$ = 0.93 V or $V_{B-TMAXR}$ = 1.143 V or $V_{B-TMAXR}$ = 1.355 V or $V_{B-TMAXR}$ = 1.568 V with ±10 mV	108	120	132	
		MFR_SPEC_14[2:0] = 000b or R $\overline{SKIP}$-RAMP ≥ 230 kΩ and $V_{B-TMAXR}$ = 0.133 V or $V_{B-TMAXR}$ = 0.346 V or $V_{B-TMAXR}$ = 0.558 V or $V_{B-TMAXR}$ = 0.771 V or $V_{B-TMAXR}$ = 0.983 V or $V_{B-TMAXR}$ = 1.196 V or $V_{B-TMAXR}$ = 1.408 V or $V_{B-TMAXR}$ = 1.621 V with ±10 mV	135	150	165	
		MFR_SPEC_14[2:0] = 000b or R $\overline{SKIP}$-RAMP ≥ 230 kΩ and $V_{B-TMAXR}$ = 0.186 V or $V_{B-TMAXR}$ = 0.399 V or $V_{B-TMAXR}$ = 0.611 V or $V_{B-TMAXR}$ = 0.823 V or $V_{B-TMAXR}$ = 1.036 V or $V_{B-TMAXR}$ = 1.249 V or $V_{B-TMAXR}$ = 1.461 V with ±10 m V or $V_{B-TMAXR}$ ≥ 1.674 V	180	200	220	
B-TMAXR PIN: BOOT VOLTAGE AND MAXIMUM TEMPERATURE SETTINGS						
T_{MAX}	TMAX setting	$V_{B-TMAXR}$ ≤ 0.186 V or MFR_SPEC_12[2:0] = 000b;		90		°C
		0.24 V ≤ $V_{B-TMAXR}$ ≤ 0.399 V or MFR_SPEC_12[2:0] = 001b		95		
		0.452 V ≤ $V_{B-TMAXR}$ ≤ 0.611 V or MFR_SPEC_12[2:0] = 010b		100		
		0.665 V ≤ $V_{B-TMAXR}$ ≤ 0.823 V or MFR_SPEC_12[2:0] = 011b		105		
		0.877 V ≤ $V_{B-TMAXR}$ ≤ 1.036 V or MFR_SPEC_12[2:0] = 100b		110		
		1.09 V ≤ $V_{B-TMAXR}$ ≤ 1.249 V or MFR_SPEC_12[2:0] = 101b		115		
		1.302 V ≤ $V_{B-TMAXR}$ ≤ 1.461 V or MFR_SPEC_12[2:0] = 110b		120		
		1.515 V ≤ $V_{B-TMAXR}$ ≤ 1.674 V or MFR_SPEC_12[2:0] = 111b		125		
V_{BOOT5} (3)	BOOT voltage setting (VR12.5)	$R_{B-TMAXR}$ ≤ 20 kΩ		0		V
		R_v = 24 kΩ		1		
		$R_{B-TMAXR}$ = 30 kΩ		1.2		
		$R_{B-TMAXR}$ = 39 kΩ		1.35		
		$R_{B-TMAXR}$ = 56 kΩ		1.5		
		$R_{B-TMAXR}$ = 75 kΩ		1.65		
		$R_{B-TMAXR}$ = 100 kΩ		1.7		
		$R_{B-TMAXR}$ ≥ 150 kΩ		1.75		
V_{BOOT0} (3)	BOOT voltage setting (VR12.0)	$R_{B-TMAXR}$ ≤ 20 kΩ		0		V
		$R_{B-TMAXR}$ = 24 kΩ		0.9		
		$R_{B-TMAXR}$ = 30 kΩ		1		
		$R_{B-TMAXR}$ = 39 kΩ		1.05		
		$R_{B-TMAXR}$ = 56 kΩ		1.1		
		$R_{B-TMAXR}$ = 75 kΩ		1.2		
		$R_{B-TMAXR}$ = 100 kΩ		1.35		
		$R_{B-TMAXR}$ ≥ 150 kΩ		1.5		

(3) Specified by design. Not production tested.

Electrical Characteristics (continued)

over recommended free-air temperature range, V_{VIN} = 12 V; V_{V3P3} = 3.3 V; VSN = GND, V_{VSP} = V_{CORE} 4-phase operation (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION: OVP, UVP, VR_RDY, PHASE MISMATCH, AND VIN UVLO						
V_{OVPH5}	Fixed OVP voltage threshold	V_{CSN1} > V_{OVPH} for 1 µs, PWM → LO.	2.65	2.75	2.85	V
V_{RDYH5}	VR_RDY high threshold (VR12.5)	Measured at the VSP pin wrt / VID code. Device latches off.	350		400	mV
V_{RDYH0}	VR_RDY high threshold (VR12.0)	Measured at the VSP pin wrt / VID code. Device latches off.	170		200	mV
V_{RDYL5}	VR_RDY low threshold (VR12.5)	Measured at the VSP pin wrt. / VID code. Device latches off.	–325		–265	mV
V_{RDYL0}	VR_RDY low threshold (VR12.0)	Measured at the VSP pin wrt. / VID code. Device latches off.	–170		–130	mV
$t_{RDYDGLTO}$	VR_RDY deglitch time	Time from VSP out of overvoltage threshold VDAC boundary to VR_RDY low.			1	µs
$t_{RDYDGLTU}$	VR_RDY deglitch time	Time from VSP out of undervoltage threshold to VR_RDY low. (f_{SW}= 500 kHz)		32		µs
$V_{VINUVLO}$	VIN UVLO threshold	MFR_SPEC_16[1:0]=00	4.1	4.3	4.5	V
		MFR_SPEC_16[1:0]=01	5.8	6.0	6.3	V
		MFR_SPEC_16[1:0]=10	7.8	8.0	8.3	V
		MFR_SPEC_16[1:0]=11	9.6	9.9	10.2	V
V_{VINHYS}	VIN UVLO hysteresis voltage	Hysteresis voltage		0.275		V
TSEN PIN AND PROTECTIONS: THERMAL VOLTAGE LEVELS						
V_{TSEN}	Thermal voltage definition	T_J = 90°C	1104	1120	1136	mV
		T_J = 95°C	1144	1160	1176	mV
		T_J = 100°C	1184	1200	1216	mV
		T_J = 105°C	1224	1240	1256	mV
		T_J = 110°C	1264	1280	1296	mV
		T_J = 115°C	1304	1320	1336	mV
		T_J = 120°C	1344	1360	1376	mV
		T_J = 125°C	1384	1400	1416	mV
I_{TSENL}		Leakage current	–3		3	µA
I_{TSENL} (4)	TSEN low voltage detection	ENABLE turns from low to high			150	mV
I_{TSENH} (4)	TSEN high voltage detection	ENABLE turns from low to high	1.55			V
PWM and $\overline{SKIP}$/RAMP OUTPUT: I/O VOLTAGE AND CURRENT						
V_{PWML}	PWMx output low level	I_{LOAD} = –1 mA		0.15	0.3	V
V_{PWMH}	PWMx output high Level	I_{LOAD} = 1 mA	2.95			V
$V_{\overline{SKIPL}}$	$\overline{SKIP}$/RAMP output low Level	I_{LOAD} = –1 mA		0.15	0.3	V
$V_{\overline{SKIPH}}$	$\overline{SKIP}$/RAMP output high level	I_{LOAD} = 1 mA	2.95			V
$V_{PW-SKLK}$	PWMx tri-state	I_{LOAD} = ±100 µA	1.6	1.7	1.8	V
t_{P-S_H-L}	PWMx/$\overline{SKIP}$ H-L transition time	C_{LOAD} = 10 pF, I_{LOAD} = ± 100 µA, 10% to 90%, both edges			15	ns
t_{P-S_TRI}	PWMx tri-state transition	C_{LOAD} = 10 pF, I_{LOAD} = ± 100 µA, 10% or 90% to tri-state level, both edges			15	ns
R_{P-S_UV}	PWMx/$\overline{SKIP}$ resistance	ENABLE = LOW, or UVLO	10			MΩ
DYNAMIC PHASE SHEDDING: THRESHOLDS						
V_{DPSTHL} (5)	Dynamic phase add/drop low threshold voltage	MFR_SPEC_15[3] = 1b, 100% = 4 × V_{OCL}	4%	10%	14%	
V_{DPSTHH}	Dynamic phase add/drop high threshold voltage	MFR_SPEC_15[2:0] = 000b, 100% = 4 × V_{OCL}	8.5%	15%	19.5%	
		MFR_SPEC_15[2:0] = 001b, 100% = 4 × V_{OCL}	13.5%	20%	24.5%	
		MFR_SPEC_15[2:0] = 010b, 100% = 4 × V_{OCL}	18.5%	25%	29.5%	
		MFR_SPEC_15[2:0] = 011b, 100% = 4 × V_{OCL}	22.5%	30%	34.5%	
		MFR_SPEC_15[2:0] = 1xxb, 100% = 4 × V_{OCL}	27.5%	35%	39.5%	

(4) Specified by design. Not production tested.
(5) A dynamic phase add/drop low threshold voltage where MFR_SPEC_15[3] = 0b is not applicable.

Electrical Characteristics (continued)

over recommended free-air temperature range, V_{VIN} = 12 V; V_{V3P3} = 3.3 V; VSN = GND, V_{VSP} = V_{CORE} 4-phase operation (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL CURRENT MONITOR						
D_{IMON} (6)	SVID current monitor register (15h)	4-phase operation, I_{IMAX} = 188 A, $\sum i_L$ = 37.6 A	30h	33h	36h	Hex
		4-phase operation, I_{IMAX} = 188 A, $\sum i_L$ = 56.4 A	48h	4Ch	50h	
		4-phase operation, I_{IMAX} = 188 A, $\sum i_L$ = 188.0 A	F6h	FFh	FFh	
PROGRAMMABLE DROOP SETTINGS						
DROOP	Droop percentage settings	MFR_SPEC_08[7:0] = 00h		0%		
		MFR_SPEC_08[7:0] = 01h		25%		
		MFR_SPEC_08[7:0] = 02h		50%		
		MFR_SPEC_08[7:0] = 03h		75%		
		MFR_SPEC_08[7:0] = 04h and others		100%		
		MFR_SPEC_08[7:0] = 10h		80%		
		MFR_SPEC_08[7:0] = 20h		85%		
		MFR_SPEC_08[7:0] = 30h		90%		
		MFR_SPEC_08[7:0] = 40h		95%		
		MFR_SPEC_08[7:0] = 50h		105%		
		MFR_SPEC_08[7:0] = 60h		110%		
		MFR_SPEC_08[7:0] = 70h		115%		
		MFR_SPEC_08[7:0] = 80h		120%		
		MFR_SPEC_08[7:0] = 90h		125%		
		MFR_SPEC_08[7:0] = A0h		150%		
SVID/PMBUS ADDRESS SETTINGS (ADDR PIN)						
SADDRL	SVID address lower three bits set ($S_2S_1S_0$)	R_{ADDR} ≤ 20 kΩ		000		Bin
		R_{ADDR} = 24 kΩ		001		
		R_{ADDR} = 30 kΩ		010		
		R_{ADDR} = 39 kΩ		011		
		R_{ADDR} = 56 kΩ		100		
		R_{ADDR} = 75 kΩ		101		
		R_{ADDR} = 100 kΩ		110		
		R_{ADDR} ≥ 150 kΩ		111		
SADDRH	SVID address highest bit set (S_3)	V_{ADDR} ≤ 0.823 V		0		Bin
		V_{ADDR} ≥ 0.877 V		1		
PADDR	PMBus address bits set	V_{ADDR} ≤ 0.027 V or V_{ADDR} = 0.877 V with ±10 mV tolerance		1100000		Bin
		V_{ADDR} = 0.08 V or V_{ADDR} = 0.93 V with ±10 mV tolerance		1100001		
		V_{ADDR} = 0.133 V or V_{ADDR} = 0.983 V with ±10 mV tolerance		1100010		
		V_{ADDR} = 0.186 V or V_{ADDR} = 1.036 V with ±10 mV tolerance		1100011		
		V_{ADDR} = 0.24 V or V_{ADDR} = 1.09 V with ±10 mV tolerance		1100100		
		V_{ADDR} = 0.293 V or V_{ADDR} = 1.143 V with ±10 mV tolerance		1100101		
		V_{ADDR} = 0.346 V or V_{ADDR} = 1.196 V with ±10 mV tolerance		1100110		
		V_{ADDR} = 0.399 V or V_{ADDR} = 1.249 V with ±10 mV tolerance		1100111		
		V_{ADDR} = 0.452 V or V_{ADDR} = 1.302 V with ±10 mV tolerance		1110000		
		V_{ADDR} = 0.505 V or V_{ADDR} = 1.355 V with ±10 mV tolerance		1110001		
		V_{ADDR} = 0.558 V or V_{ADDR} = 1.408 V with ±10 mV tolerance		1110010		
		V_{ADDR} = 0.611 V or V_{ADDR} = 1.461 V with ±10 mV tolerance		1110011		
		V_{ADDR} = 0.665 V or V_{ADDR} = 1.515 V with ±10 mV tolerance		1110100		
		V_{ADDR} = 0.718 V or V_{ADDR} = 1.568 V with ±10 mV tolerance		1110101		
		V_{ADDR} = 0.771 V or V_{ADDR} = 1.621 V with ±10 mV tolerance		1110110		
		V_{ADDR} = 0.823 V or V_{ADDR} ≥ 1.674 V with ±10 mV tolerance		1110111		

(6) For applications using other configurations, please consult TI for design requirements.

Electrical Characteristics (continued)

over recommended free-air temperature range, V_{VIN} = 12 V; V_{V3P3} = 3.3 V; VSN = GND, V_{VSP} = V_{CORE} 4-phase operation (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SLEW RATES AND MODE SELECTIONS (SLEW-MODE PIN)						
VID_{OFS1}	VID Offset Bit [1]	$R_{SLEW-MODE}$ ≤ 39 kΩ or MFR_SPEC_05		00000		Bin
		$R_{SLEW-MODE}$ ≥ 56 kΩ or MFR_SPEC_05		00001		
MODE	MODE bits set ($M_4M_3M_2M_1M_0$)	$V_{SLEW-MODE}$ ≤ 0.027 V with ±10 mV		00000		Bin
		$V_{SLEW-MODE}$ = 0.08 V with ±10 mV		00001		
		$V_{SLEW-MODE}$ = 0.133 V with ±10 mV		00010		
		$V_{SLEW-MODE}$ = 0.186 V with ±10 mV		00011		
		$V_{SLEW-MODE}$ = 0.24 V with ±10 mV		00100		
		$V_{SLEW-MODE}$ = 0.293 V with ±10 mV		00101		
		$V_{SLEW-MODE}$ = 0.346 V with ±10 mV		00110		
		$V_{SLEW-MODE}$ = 0.399 V with ±10 mV		00111		
		$V_{SLEW-MODE}$ = 0.452 V with ±10 mV		01000		
		$V_{SLEW-MODE}$ = 0.505 V with ±10 mV		01001		
		$V_{SLEW-MODE}$ = 0.558 V with ±10 mV		01010		
		$V_{SLEW-MODE}$ = 0.611 V with ±10 mV		01011		
		$V_{SLEW-MODE}$ = 0.665 V with ±10 mV		01100		
		$V_{SLEW-MODE}$ = 0.718 V with ±10 mV		01101		
		$V_{SLEW-MODE}$ = 0.771 V with ±10 mV		01110		
		$V_{SLEW-MODE}$ = 0.823 V with ±10 mV		01111		
		$V_{SLEW-MODE}$ = 0.877 V with ±10 mV		10000		
		$V_{SLEW-MODE}$ = 0.93 V with ±10 mV		10001		
		$V_{SLEW-MODE}$ = 0.983 V with ±10 mV		10010		
		$V_{SLEW-MODE}$ = 1.036 V with ±10 mV		10011		
		$V_{SLEW-MODE}$ = 1.09 V with ±10 mV		10100		
		$V_{SLEW-MODE}$ = 1.143 V with ±10 mV		10101		
		$V_{SLEW-MODE}$ = 1.196 V with ±10 mV		10110		
		$V_{SLEW-MODE}$ = 1.249 V with ±10 mV		10111		
		$V_{SLEW-MODE}$ = 1.302 V with ±10 mV		11000		
		$V_{SLEW-MODE}$ = 1.355 V with ±10 mV		11001		
		$V_{SLEW-MODE}$ = 1.408 V with ±10 mV		11010		
		$V_{SLEW-MODE}$ = 1.461 V with ±10 mV		11011		
		$V_{SLEW-MODE}$ = 1.515 V with ±10 mV		11100		
		$V_{SLEW-MODE}$ = 1.568 V with ±10 mV		11101		
		$V_{SLEW-MODE}$ = 1.621 V with ±10 mV		11110		
		$V_{SLEW-MODE}$ ≥ 1.674 V		11111		

6.6 I/O Timing Requirements

PARAMETER			MIN	TYP	MAX	UNIT
$t_{STARTUP1}$	Startup time(1)	V_{BOOT} > 0 V, no faults, C_{REF} = 1 µF			1.2	ms
$t_{STARTUP2}$	Startup time(2)	V_{BOOT}> 0 V, no faults, C_{REF} = 1 µF			1.2	ms
$t_{\overline{SU\text{-}ALERT}}$	$\overline{ALERT}$ delay(3) (4)	Time from V_{DAC}= V_{BOOT} and VR_Settled = OK to $\overline{ALERT}$ going low			1	µs
$t_{RDY(pod)}$	VR_RDY Power on delay time(3)	$\overline{ALERT}$ going low to VR_RDY going high (non-zero V_{BOOT})			6	µs
$t_{OFF(min)}$	Controller minimum OFF time	Fixed value	20(3)	40		ns
$t_{VCC(vid)}$	VID Change to VSP change(3)	ACK of SetVID_x command to start of voltage ramp			1	µs
$t_{EN(rdy)}$	ENABLE low to VR_RDY low			20	100	ns
$t_{VRT(dgl)}$	$\overline{VR\_HOT}$ deglitch time		0.4		0.5	ms

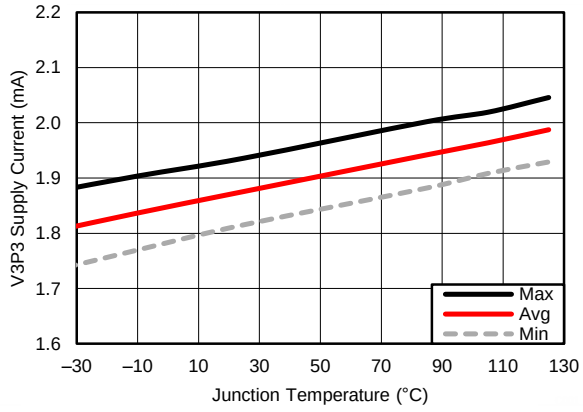
(1) Time from ENABLE to VOUT ramp.
(2) Time from ENABLE until the controller responds to SVID commands.
(3) Specified by design. Not production tested.
(4) Time from when V_{DAC}= V_{BOOT} and VR_Settled = OK to $\overline{ALERT}$ going low

6.7 Switching Characteristics

T_A = 25°C

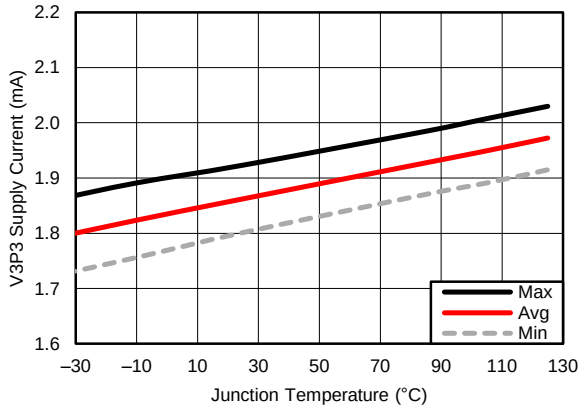
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F-IMAX PIN: FREQUENCY SETTINGS						
f_S	Switching frequency	V_{VIN} = 12 V, V_{VSP} = 1.7 V $R_{F\text{-}IMAX}$ = 20 kΩ or MFR_SPEC_12[6:4] = 000b	270	300	330	kHz
		V_{VIN} = 12 V, V_{VSP} = 1.7 V $R_{F\text{-}IMAX}$ = 24 kΩ or MFR_SPEC_12[6:4] = 001b	360	400	440	
		V_{VIN} = 12 V, V_{VSP} = 1.7 V $R_{F\text{-}IMAX}$ = 30 kΩ or MFR_SPEC_12[6:4] = 010b	450	500	550	
		V_{VIN} = 12 V, V_{VSP} = 1.7 V $R_{F\text{-}IMAX}$ = 39 kΩ or MFR_SPEC_12[6:4] = 011b	540	600	660	
		V_{VIN} = 12 V, V_{VSP} = 1.7 V $R_{F\text{-}IMAX}$ = 56 kΩ or MFR_SPEC_12[6:4] = 100b	630	700	770	
		V_{VIN} = 12 V, V_{VSP} = 1.7 V $R_{F\text{-}IMAX}$ = 75 kΩ or MFR_SPEC_12[6:4] = 101b	720	800	880	
		V_{VIN} = 12 V, V_{VSP} = 1.7 V $R_{F\text{-}IMAX}$ = 100 kΩ or MFR_SPEC_12[6:4] = 110b	810	900	990	
		V_{VIN} = 12 V, V_{VSP} = 1.7 V $R_{F\text{-}IMAX}$ = 150 kΩ or MFR_SPEC_12[6:4] = 111b	900	1000	1100	

6.8 Typical Characteristics



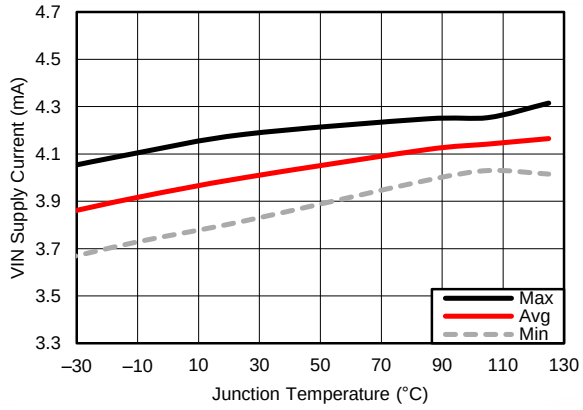
Power State 0

Figure 1. V3P3 Supply Current vs Junction Temperature



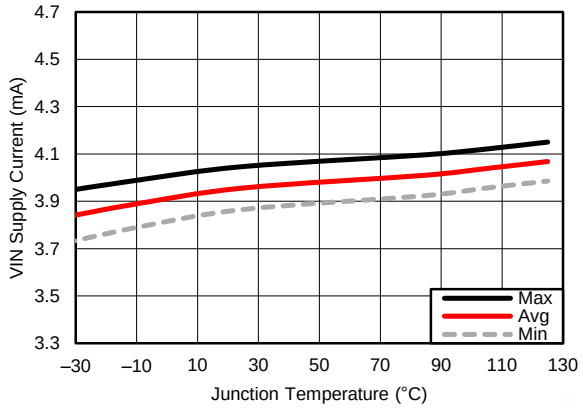
Power State 1

Figure 2. V3P3 Supply Current vs Junction Temperature



Power State 0

Figure 3. VIN Supply Current vs Junction Temperature



Power State 1

Figure 4. VIN Supply Current vs Junction Temperature

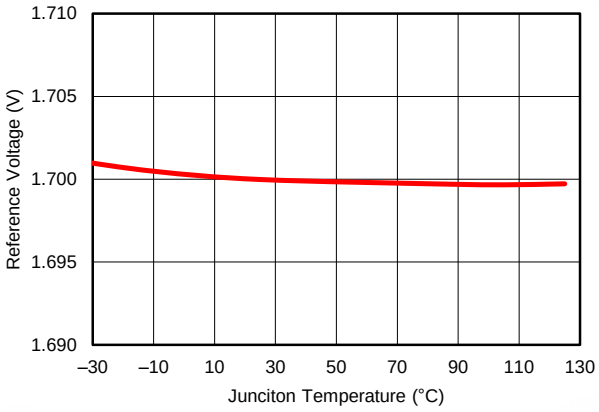


Figure 5. Reference Voltage vs Junction Temperature

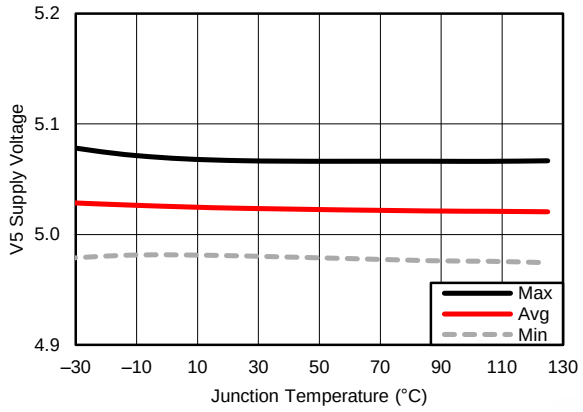


Figure 6. V5 Supply Current vs Junction Temperature

Typical Characteristics (continued)

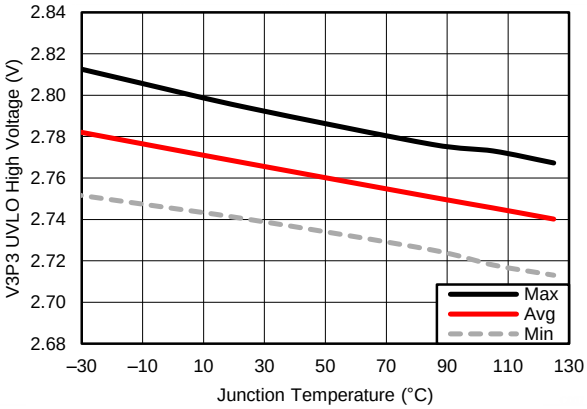


Figure 7. V3P3 UVLO High Voltage vs Junction Temperature

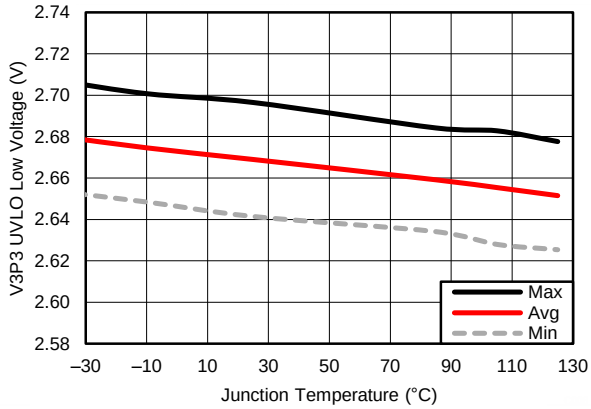


Figure 8. V3P3 UVLO Low Voltage vs Junction Temperature

7 Detailed Description

7.1 Overview

The TPS53640A device is a DCAP+™ mode adaptive on-time controller.

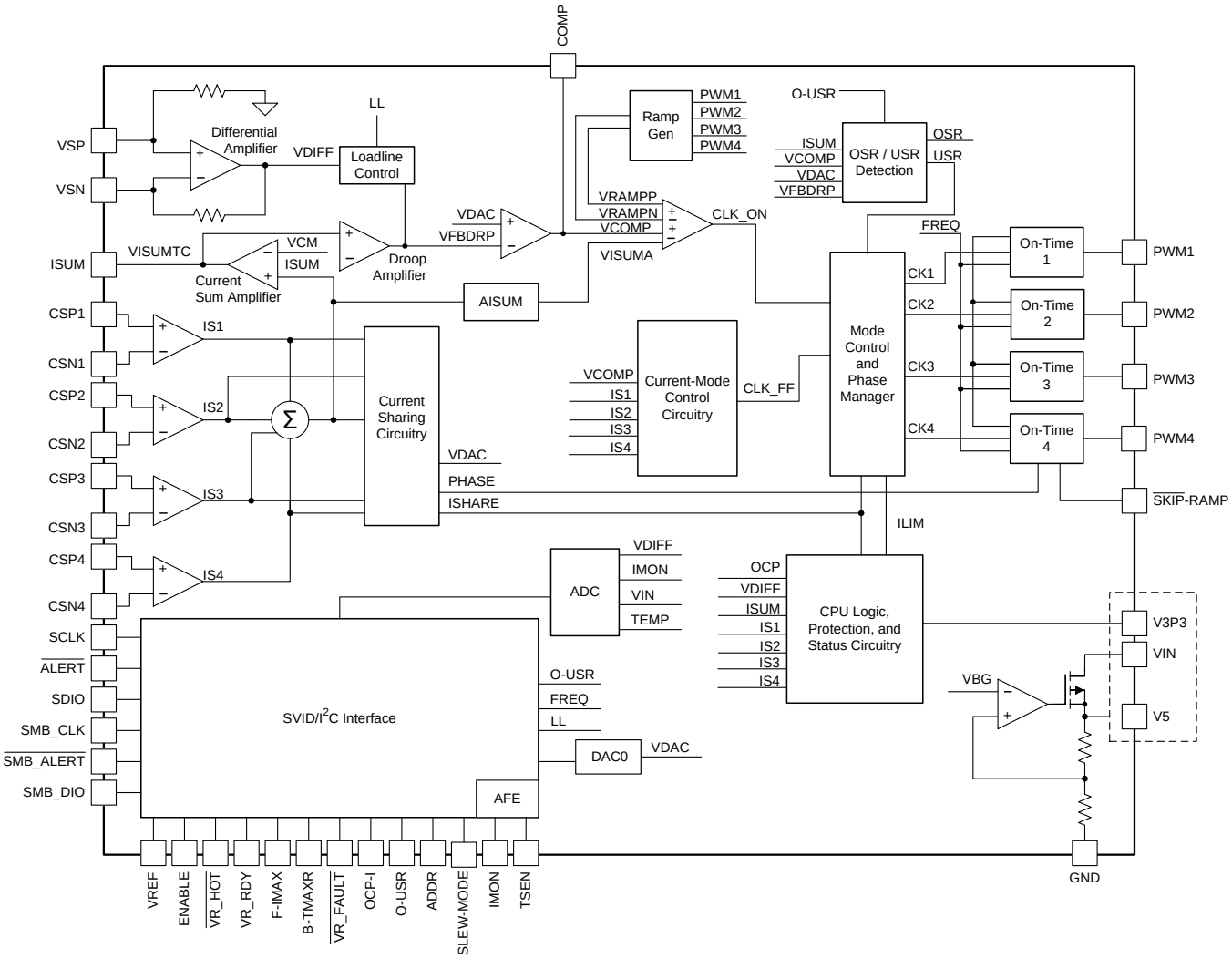
The output voltage is set using a DAC that outputs a reference in accordance with the 8-bit VID code defined in *Intel VR12.0/VR12.5 PWM Specification* document. In adaptive on-time converters, the controller varies the on-time as a function of input and output voltage to maintain a nearly constant frequency during steady-state conditions. In conventional voltage-mode constant on-time converters, each cycle begins when the output voltage crosses to a fixed reference level. However, in the TPS53640A device, the cycle begins when the current feedback reaches an error voltage level which corresponds to the amplified voltage difference between the DAC voltage and the feedback output voltage with droop. In the case of multi-phase operations, the current feedback from all the phases is summed, and is amplified using the ISUM pin to adjust the load-line.

This approach has three advantages:

- The load-line can be precisely adjusted and temperature-compensated by changing the resistor network on ISUM pin.
- The amplifier DC gain sets an accurate linear load-line. CPU core applications require this setting.
- The device filters the error voltage input to the PWM comparator. This filtering improves the noise performance.

The TPS53640A device uses a dynamic phase shedding concept to improve the efficiency without losing load transient performance. Both the architecture (which does not allow the high-side gate drive outputs of more than one phase to be ON in any condition except transients) and the current ripple (which forces the pulses to be spaced equally) maintains the phase displacement. The TPS53640A device includes a current balancing loop feature to adjust the ON-time of each phase without any user intervention, compensation, or extra components.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation

As shown in the Functional Block Diagram and , in 4-phase continuous conduction mode, the converter operates as shown in Figure 9.

Feature Description (continued)

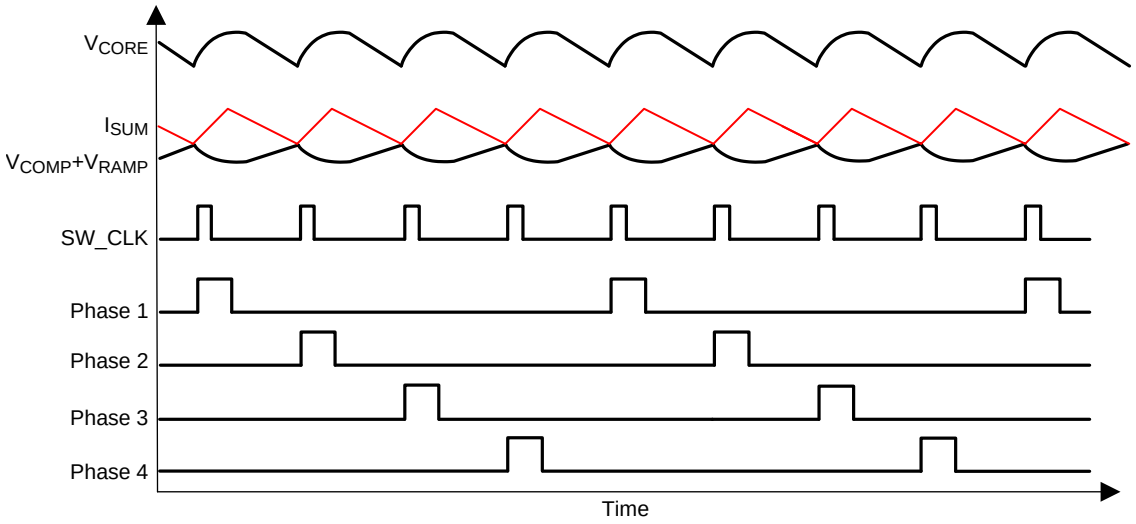


Figure 9. D-CAP+ Mode Basic Waveforms

Starting with the condition that the high-side MOSFETs are off and the low-side MOSFETs are on, the summed current feedback (I_{SUM}) is higher than the summed error amplifier output (V_{COMP}) and the internal ramp signal (V_{RAMP}). I_{SUM} falls until it hits $V_{COMP}+V_{RAMP,}$ which contains a component of the output ripple voltage. The PWM comparator senses where the two waveforms cross and triggers the on-time generator. This generates the internal SW_CLK. Each SW_CLK corresponds to one switching ON pulse for one phase.

In case of single-phase operation, every SW_CLK generates a switching pulse on the same phase. Also, V_{ISUM} corresponds to just a single-phase inductor current.

In case of multi-phase operation, the SW_CLK gets distributed to each of the phases in a cycle. This approach of using the summed inductor current and cyclically distributing the ON pulses to each phase automatically gives the required interleaving of 360 / *n*, where *n* is the number of phases.

7.3.2 Current Sensing

The TPS53640A device provides independent channels of current feedback for every phase to increase the system accuracy and reduce the dependence of circuit performance on layout compared to an externally summed architecture. The four differential pairs, CSP1 and CSN1, CSP2 and CSN2, CSP3 and CSN3, and CSP4 and CSN4 provide current sensing for the four individual phases. The current sensing signals from both the inductor DCR sensing networks and the DC load-line are temperature-compensated through an NTC network on the ISUM pin.

Feature Description (continued)

7.3.3 Setting the Load-Line (DROOP)

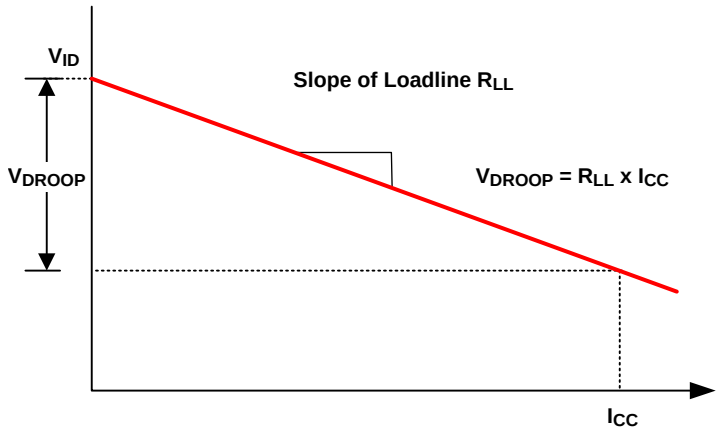


Figure 10. Load Line Slope

$$V_{DROOP} = R_{LL} \times I_{CC} = g_{M(isum)} \times R_{ISUM} \times R_{CS} \times \frac{6}{4} \times I_{CC}$$

where

- R_{LL} is the desired load line setting
- R_{CS} is the effective current sense resistance of the DCR of the inductor
- I_{CC} is the load current
- R_{ISUM} is the equivalent resistance from the ISUM pin to VREF pin to adjust the load line
- $g_{M(isum)}$ is the gain of the internal I_{SUM} amplifier, (0.5 mS typ) (1)

7.3.4 Load Transients

When there is a sudden load increase, the output voltage immediately drops. The device reacts to this drop in a rising voltage on the COMP pin. This rise forces the PWM pulses to become more frequent which causes the inductor current to rapidly increase. As the inductor current reaches the new load current, the device reaches a steady-state operating condition and the PWM switching resumes the steady-state frequency.

When there is a sudden load release, the output voltage rises suddenly. The device reacts to this sudden rise in a drop in voltage on the COMP pin. This drop forces a delay in the PWM pulses until the inductor current reaches the new load current. At that point, the switching resumes and steady-state switching continues.

NOTE: In Figure 11 and Figure 12, the voltage ripple on V_{CORE}, V_{RAMP}, and V_{COMP} are omitted for the sake of simplicity.

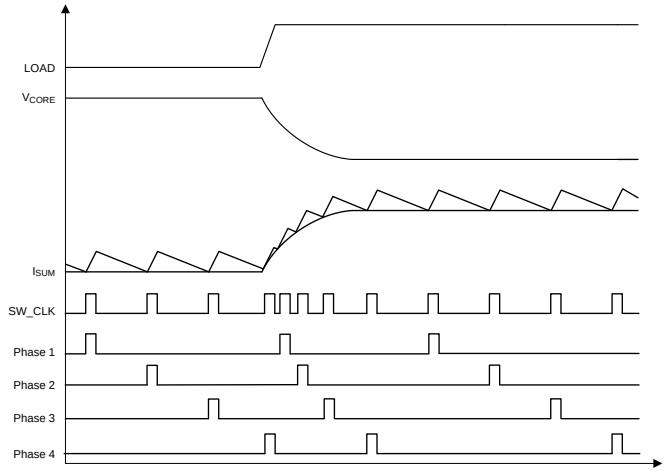


Figure 11. Load Insertion

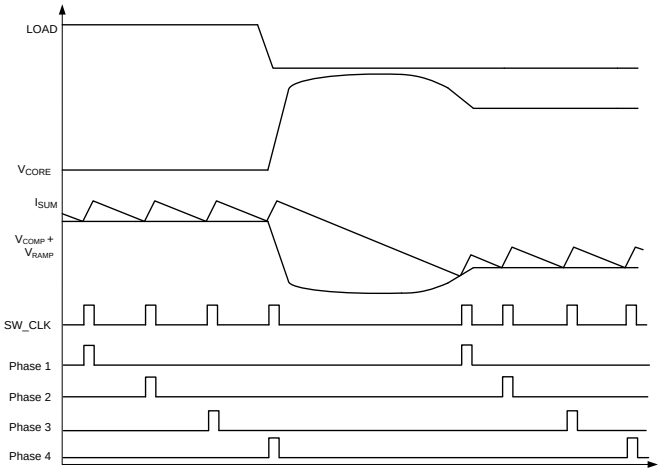


Figure 12. Load Release

Feature Description (continued)

7.3.5 Overshoot Reduction (OSR)

The problem of overshoot in low duty-cycle synchronous buck converters is well known, and results from the output inductor having a small voltage (V_{CORE}) with which to respond to a transient load release.

Figure 13 shows a simplified single phase converter. In an ideal converter, with typical input voltage of 12 V and a 1.8-Voutput, the inductor has 10.2 V (12 V – 1.8 V) to respond to a transient load increase, but only 1.8-V to respond as soon as the load releases.

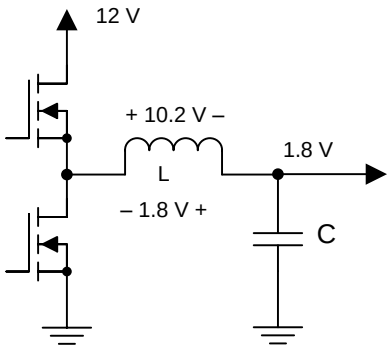


Figure 13. Synchronous Converter Circuit

With the overshoot reduction feature enabled, when the output voltage increases beyond the difference between the DAC voltage and the summed voltage of V_{CORE} and I_{SUM} which exceeds the OSR threshold, the PWM signal tri-states and turns off both the high-side and low-side MOSFETs. When the low-side MOSFET is turned off, the energy in the inductor is partially dissipated by the body diode. The ON pulse-width immediately truncates regardless of the load transient timing. This feature can further reduce the overshoot compared to the conventional constant on-time controllers. See Figure 14.

Feature Description (continued)

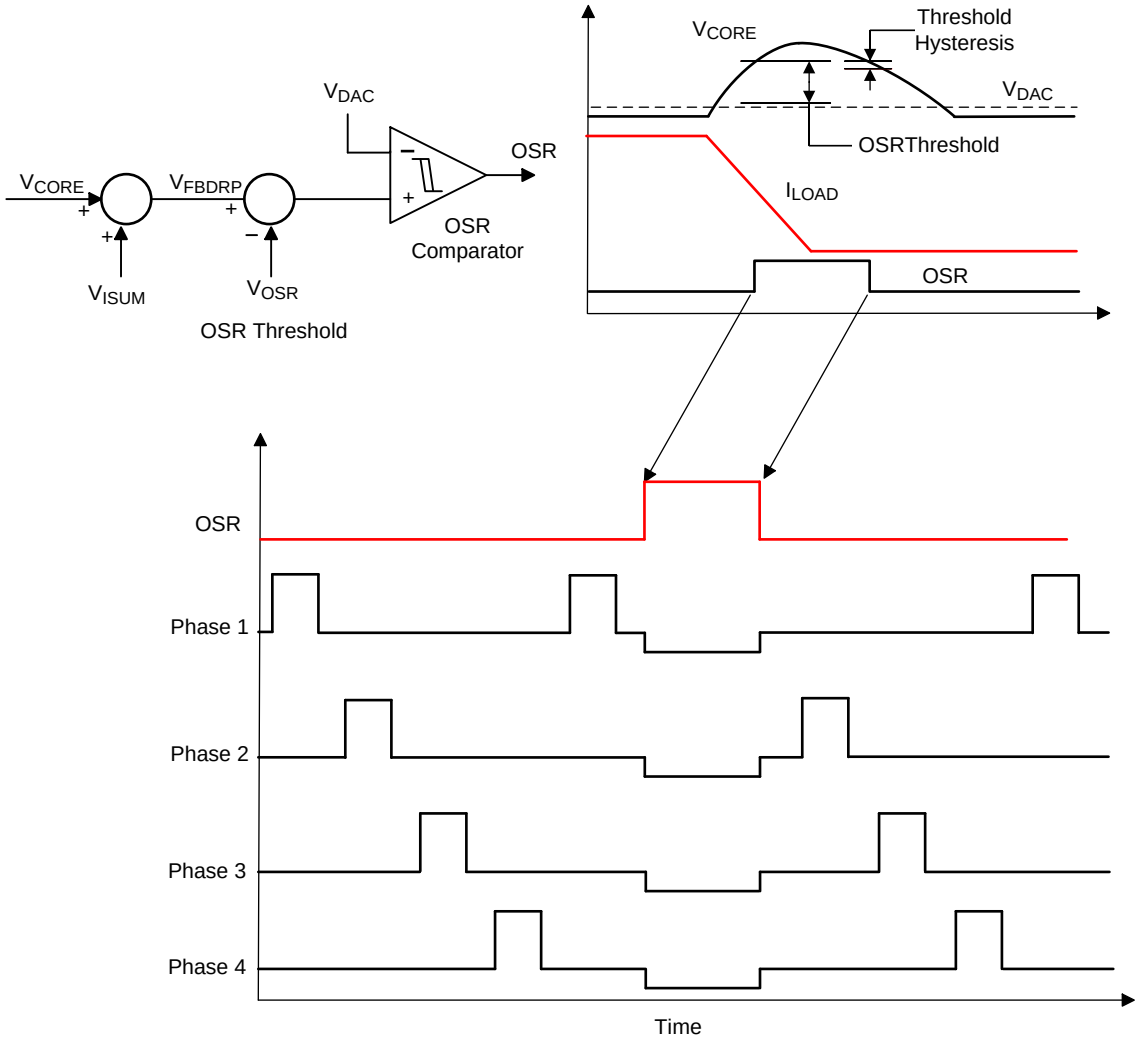


Figure 14. Performance for a Load Transient Release with OSR Enabled

7.3.6 Undershoot Reduction (USR)

When the transient load increase becomes quite large, it becomes difficult to meet the energy demanded by the load especially at lower input voltages. Then it is necessary to quickly increase the energy in the inductors during the transient load increase. The TPS53640A device achieves this required increase by enabling pulse overlapping. In order to maintain the interleaving of the multi-phase configuration and yet be able to have pulse-overlapping during load-insertion, the device enters undershoot reduction (USR) mode only when necessary and when the difference between DAC voltage and the summed voltage of V_{CORE} and V_{ISUM} exceeds the USR voltage level specified in the *Electrical Characteristics* table.

The waveforms in Figure 15 show the performance with undershoot reduction, which helps to reduce the amount of capacitance required to meet the specification.

When the transient condition ceases, the device resumes interleaving of the phases.

Feature Description (continued)

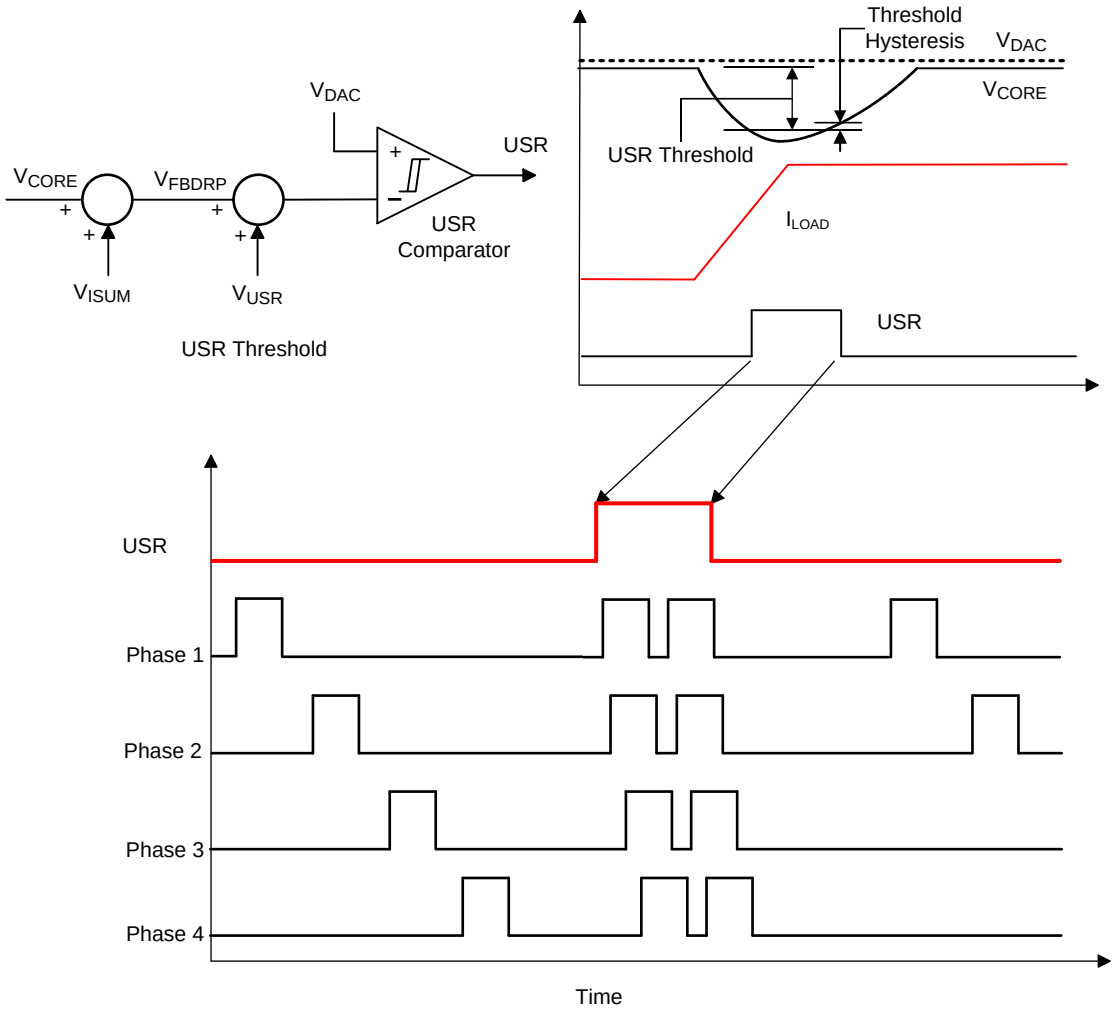


Figure 15. Performance for a Load Transient Step-up With USR Enabled

7.3.7 AutoBalance™ Current Sharing

The basic mechanism for current sharing is to sense the average phase current, then adjust the pulse width of each phase to equalize the current in each phase as shown in . The PWM comparator (not shown) starts a pulse when the feedback voltage meets the reference. The pulse terminates when the voltage at $C_{t(on)}$ matches the on-time reference, which normally equals the DAC voltage (V_{DAC}). The current source, proportional to the input voltage, charges the $C_{t(on)}$ capacitor.

In order to understand how this part of the circuit operates, first assume that the 5-µs averaged value from each phase current are equal. In this case, the PWM modulator terminates at V_{DAC}, and the normal pulse width is delivered to the system. If instead, I1 > I_{AVG}, then an offset is subtracted from V_{DAC}, and the pulse width for Phase 1 is shortened to reduce the phase current in Phase 1 for balancing. If I1 < I_{AVG}, then a longer pulse is generated to increase the phase current in Phase 1 to achieve current balancing.

Feature Description (continued)

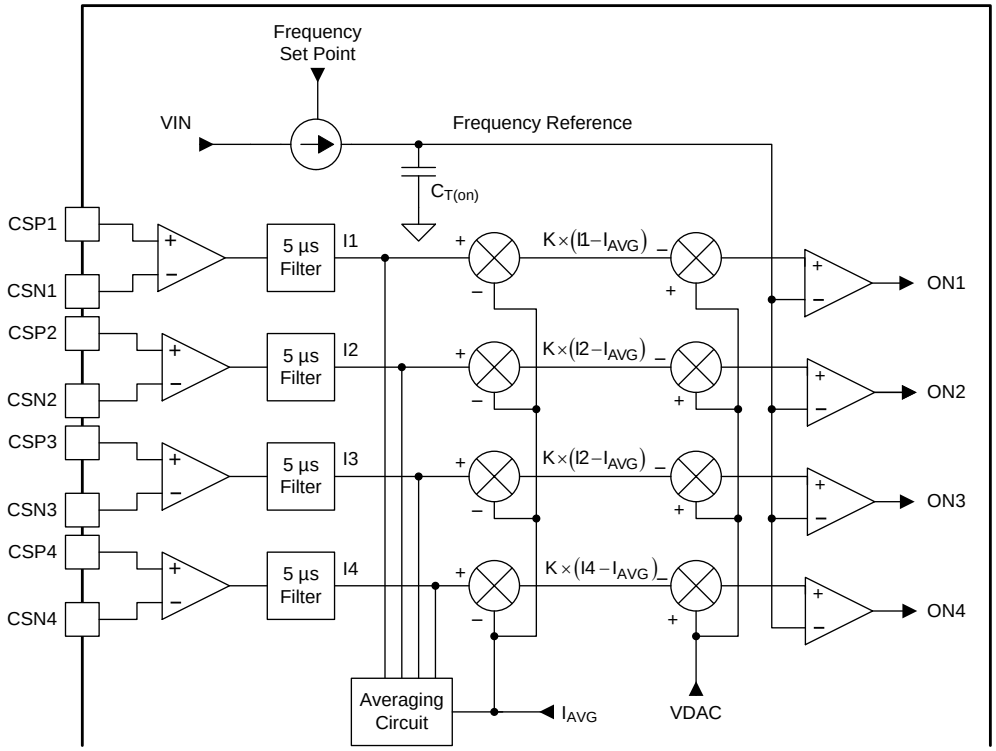


Figure 16. Block Diagram of AutoBalance Current Sharing

7.3.8 Dynamic VID

In the VR12.0/VR12.5 standard, there are three basic types of VID command settings.

- SetVID_Fast
- SetVID_Slow
- SetVID_Decay

The slew rate for SetVID_Fast command is the slew rate set by the resistor at SLEW-MODE pin as defined in the *Electrical Characteristics* table. The slew rate of SetVID_Slow command is ¼ of the SetVID_Fast command slew rate. During a SetVID_Decay change, the voltage decays by the rate of the load current. The DAC voltage is stepped down at the same rate as the load voltage decay. Additionally, during a SetVID_Fast or SetVID_Slow VID-up transition, the controller speeds up the response of the output voltage to meet the Intel timing requirement. It is possible to observe an overshoot at the output voltage on a VID-up transition. This overshoot is allowed by the Intel VR12.0 and 12.5 Specifications.

Table 1. VID Table

VID Hex VALUE	VR12.0 VOLTAGE (V)	VR12.5 VOLTAGE (V)
0	0	0.
1	0.25	0.50
2	0.255	0.51
3	0.26	0.52
4	0.265	0.53
5	0.27	0.54
6	0.275	0.55
7	0.28	0.56
8	0.285	0.57
9	0.29	0.58
0A	0.295	0.59
0B	0.3	0.60
0C	0.305	0.61
0D	0.31	0.62
0E	0.315	0.63
0F	0.32	0.64
10	0.325	0.65
11	0.33	0.66
12	0.335	0.67
13	0.34	0.68
14	0.345	0.69
15	0.35	0.70
16	0.355	0.71
17	0.36	0.72
18	0.365	0.73
19	0.37	0.74
1A	0.375	0.75
1B	0.38	0.76
1C	0.385	0.77
1D	0.39	0.78
1E	0.395	0.79
1F	0.4	0.80
20	0.405	0.81
21	0.41	0.82
22	0.415	0.83
23	0.42	0.84
24	0.425	0.85
25	0.43	0.86
26	0.435	0.87
27	0.44	0.88
28	0.445	0.89
29	0.45	0.90
2A	0.455	0.91
2B	0.46	0.92
2C	0.465	0.93
2D	0.47	0.94
2E	0.475	0.95

Table 1. VID Table (continued)

VID Hex VALUE	VR12.0 VOLTAGE (V)	VR12.5 VOLTAGE (V)
2F	0.48	0.96
30	0.485	0.97
31	0.49	0.98
32	0.495	0.99
33	0.50	1.00
34	0.505	1.01
35	0.51	1.02
36	0.515	1.03
37	0.52	1.04
38	0.525	1.05
39	0.53	1.06
3A	0.535	1.07
3B	0.54	1.08
3C	0.545	1.09
3D	0.55	1.10
3E	0.555	1.11
3F	0.56	1.12
40	0.565	1.13
41	0.57	1.14
42	0.575	1.15
43	0.58	1.16
44	0.585	1.17
45	0.59	1.18
46	0.595	1.19
47	0.6	1.20
48	0.605	1.21
49	0.61	1.22
4A	0.615	1.23
4B	0.62	1.24
4C	0.625	1.25
4D	0.63	1.26
4E	0.635	1.27
4F	0.64	1.28
50	0.645	1.29
51	0.65	1.30
52	0.655	1.31
53	0.66	1.32
54	0.665	1.33
55	0.67	1.34
56	0.675	1.35
57	0.68	1.36
58	0.685	1.37
59	0.69	1.38
5A	0.695	1.39
5B	0.7	1.40
5C	0.705	1.41
5D	0.71	1.42

Table 1. VID Table (continued)

VID Hex VALUE	VR12.0 VOLTAGE (V)	VR12.5 VOLTAGE (V)
5E	0.715	1.43
5F	0.72	1.44
60	0.725	1.45
61	0.73	1.46
62	0.735	1.47
63	0.74	1.48
64	0.745	1.49
65	0.75	1.50
66	0.755	1.51
67	0.76	1.52
68	0.765	1.53
69	0.77	1.54
6A	0.775	1.55
6B	0.78	1.56
6C	0.785	1.57
6D	0.79	1.58
6E	0.795	1.59
6F	0.8	1.60
70	0.805	1.61
71	0.81	1.62
72	0.815	1.63
73	0.82	1.64
74	0.825	1.65
75	0.83	1.66
76	0.835	1.67
77	0.84	1.68
78	0.845	1.69
79	0.85	1.70
7A	0.855	1.71
7B	0.86	1.72
7C	0.865	1.73
7D	0.87	1.74
7E	0.875	1.75
7F	0.88	1.76
80	0.885	1.77
81	0.89	1.78
82	0.895	1.79
83	0.9	1.80
84	0.905	1.81
85	0.91	1.82
86	0.915	1.83
87	0.92	1.84
88	0.925	1.85
89	0.93	1.86
8A	0.935	1.87
8B	0.94	1.88
8C	0.945	1.89

Table 1. VID Table (continued)

VID Hex VALUE	VR12.0 VOLTAGE (V)	VR12.5 VOLTAGE (V)
8D	0.95	1.90
8E	0.955	1.91
8F	0.96	1.92
90	0.965	1.93
91	0.97	1.94
92	0.975	1.95
93	0.98	1.96
94	0.985	1.97
95	0.99	1.98
96	0.995	1.99
97	1	2.
98	1.5	2.01
99	1.01	2.02
9A	1.015	2.03
9B	1.02	2.04
9C	1.025	2.05
9D	1.03	2.06
9E	1.035	2.07
9F	1.04	2.08
A0	1.045	2.09
A1	1.05	2.10
A2	1.055	2.11
A3	1.06	2.12
A4	1.065	2.13
A5	1.07	2.14
A6	1.075	2.15
A7	1.08	2.16
A8	1.085	2.17
A9	1.09	2.18
AA	1.095	2.19
AB	1.1	2.20
AC	1.105	2.21
AD	1.11	2.22
AE	1.115	2.23
AF	1.12	2.24
B0	1.125	2.25
B1	1.13	2.26
B2	1.135	2.27
B3	1.14	2.28
B4	1.145	2.29
B5	1.15	2.30
B6	1.155	2.31
B7	1.16	2.32
B8	1.165	2.33
B9	1.17	2.34
BA	1.175	2.35
BB	1.18	2.36

Table 1. VID Table (continued)

VID Hex VALUE	VR12.0 VOLTAGE (V)	VR12.5 VOLTAGE (V)
BC	1.185	2.37
BD	1.19	2.38
BE	1.195	2.39
BF	1.2	2.40
C0	1.205	2.41
C1	1.21	2.42
C2	1.215	2.43
C3	1.22	2.44
C4	1.225	2.45
C5	1.23	2.46
C6	1.235	2.47
C7	1.24	2.48
C8	1.245	2.49
C9	1.25	2.50
CA	1.255	n/a
CB	1.26	
CC	1.265	
CD	1.27	
CE	1.275	
CF	1.28	
D0	1.285	
D1	1.29	
D2	1.295	
D3	1.3	
D4	1.305	
D5	1.31	
D6	1.315	
D7	1.32	
D8	1.325	
D9	1.33	
DA	1.335	
DB	1.34	
DC	1.345	
DD	1.35	

Table 1. VID Table (continued)

VID Hex VALUE	VR12.0 VOLTAGE (V)	VR12.5 VOLTAGE (V)
DE	1.355	
DF	1.36	
E0	1.365	
E1	1.37	
E2	1.375	
E3	1.38	
E4	1.385	
E5	1.39	
E6	1.395	
E7	1.4	
E8	1.405	
E9	1.41	
EA	1.415	
EB	1.42	
EC	1.425	
ED	1.43	
EE	1.435	
EF	1.44	
F0	1.445	
F1	1.45	
F2	1.455	
F3	1.46	
F4	1.465	
F5	1.47	
F6	1.475	
F7	1.48	
F8	1.485	
F9	1.49	
FA	1.495	
FB	1.5	
FC	1.505	
FD	1.51	
FE	1.515	
FF	1.52	

7.3.9 Power-State Changes

A SetVID_Fast and a SetVID_Slow command automatically puts the device into power state PS0. A SetVID_Decay command automatically puts the device into power state in PS2. The controller operates in the maximum phase mode when it is in power state PS0, if the phase-shedding feature is not enabled. All phases are active in power state PS0. However, in power state PS1, PS2 the device operates in single phase. Additionally, the device can operate in forced continuous mode (FCCM) in power states PS0 and PS1. Alternatively, in power state PS2, the device operates in diode emulation mode (skip mode) for additional power savings and higher efficiency.

During a SetVID_Fast or SetVID_slow transition for a VID-up transition, an offset is added at the DAC to speed up the response of the output voltage to meet the Intel VR12 timing requirement. Therefore, it is possible to observe an overshoot at the output voltage during a VID-up transition period. This overshoot is allowed by the Intel VR12 Specification.

Table 2. Power-State Changes

POWER STATE	PHASES	OPERATING MODE
PS0	Maximum Configured	FCCM
PS1	1	
PS2	1	DCM

7.3.10 PWM and $\overline{\text{SKIP}}$ Signals

The PWM and $\overline{\text{SKIP}}$-RAMP signals are output of controller to drive the TI NexFET power stages. Both the signals are 3.3-V logic based. The PWM signal is logic high when the high-side MOSFET is turned ON. The PWM signal is logic low to turn on the low-side MOSFET. When both high-side and low-side MOSFETs are expected to be OFF, the PWM signal is driven to tri-state condition (1.7 V). The $\overline{\text{SKIP}}$-RAMP pin is asserted low during the soft-start period until the VR_RDY pin goes high and in operating in PS2 mode.

7.3.11 Undervoltage Lockout (UVLO)

The TPS53640A device continuously monitors the voltage on pins V3P3, VIN and V5 to ensure that the voltage is high enough to bias the device properly and to provide sufficient gate drive potential to maintain high efficiency.

The device starts operating when the V3P3 voltage is above the $V_{V3UVLOH}$ threshold and stops operating when the pin voltages fall below $V_{V3UVLOL}$ (in this case assuming that V_{VIN} is also above $V_{VINUVLO}$). The operation can also stop when the VIN voltage falls below the value of ($V_{VINUVLO}$ – V_{VINHYS}). The device generates the V5 voltage from the VIN supply using an LDO. Therefore, the V5 UVLO function is dependent on the VIN voltage.

7.3.12 Power Good (VR_RDY)

The VR_RDY pin is an active high, open drain ouput. It communicates the output voltage condition with respect to the provided V_{DAC} target. It follows the requirements of VR12.0 or VR12.5. The upper and lower voltage limits are listed in the *Electrical Characteristics* table for the VR_RDY to remain high.

7.3.13 Output Undervoltage Protection (UVP)

Output undervoltage protection works in conjunction with the current protection. If the output voltage drops below the VR_RDY low threshold, then the device drives the PWM into a tri-state condition so that both high-side and low-side MOSFETs are turned off. The controller remains in this state until V3P3 pin supply is re-cycled.

7.3.14 Overcurrent Limit (OCL)

The TPS53640A device includes a valley-current-based limit function by using a per-phase OCL comparator. A resistor connected between the OCL pin and the VREF pin generates the OCL comparison threshold. A constant, 10-µA current source flows through this 1-% tolerance resistor (R_{OCL}).

Using the valley current limit, select an OCL current level using Equation 2. To set the per-phase overcurrent limit threshold, subtract half of the ripple current from the maximum average current.

$$I_{OCL} = K \times \left(\frac{I_{MAX}}{n} \right) - \left(\frac{I_{RIPPLE}}{2} \right) \quad (2)$$

where

- K is the maximum operating margin percentage
- n is the number of active phases
- I_{RIPPLE} is the ripple current

This instantaneous load current, OCL-based voltage signal is compared to the OCL reference.

The OCL resistor value can be calculated as shown in Equation 3.

$$R_{OCL} = I_{OCL} \times R_{DCR} \times \frac{Gain}{10\,\mu A}$$

where

- R_{DCR} is the selected inductor DCR
- Gain is the current sensing amplifier gain (approximately 6) (3)

If the current sense voltage at OCL comparator goes above the OCL resistor reference threshold, the converter delays the next ON pulse until the difference drops below the OCL limit. In OCL mode, the output voltage continues to drop until the UVP threshold is reached. When the UVP threshold is reached, the output voltage regulation stops with PWM driven into tri-state logic operation.

7.3.15 Overcurrent Protection (OCP)

An overcurrent event is detected in the digital domain by comparing the digitized current monitor (I_{MON}) with the OC_FAULT_LIMIT value which is set to 1.25 × $I_{CC(Mmax)}$ by default.

7.3.16 Overvoltage Protection (OVP)

The OVP condition is detected when the output voltage V_{OUT} > VDAC + V_{VR_RDY}-high threshold. In this case the controller drives the VR_RDY pin to inactive (low state) and drives all PWM to logic low which turns on the low-side MOSFET to discharge the output. However the OVP threshold is blanked during a Dynanmic VID change. In order to continually protect the processor, there is second OVP level. The second OVP level is fixed at V_{OVPH5} (approximately 2.75 V) and is always active while V_{V3P3} is above the UVLO threshold. If the fixed OVP condition is detected, the device drives the VR_RDY pin to inactive (logic low) and drives the PWM to logic low in order to turn on the low-side MOSFET. The controller remains in this state until the V3P3 pin supply is re-cycled.

7.3.17 Thermal Alert and $\overline{\text{VR-HOT}}$ Signal

The $\overline{\text{VR-HOT}}$ signal is an active-low, open-drain signal output that is used to protect output power chain. To use $\overline{\text{VR-HOT}}$, place an NTC at hottest area of power chain or use the TAO signal from the powerstage device. Connect the temperature-based voltage signal to the TSEN pin. For NTC-based circuit usage, refer the Design Tool. In this NTC circuit, connect the NTC plus one parallel resistor between the VREF pin and the TSEN pin, and connect a resistor between the TSEN pin and GND. Use a small filter capacitor for noise decoupling. As the TSEN pin voltage rises above the $\overline{\text{VR-HOT}}$ alert threshold, the device issues an SVID alert. As the temperature continues to rise above the $\overline{\text{VR-HOT}}$ threshold, the $\overline{\text{VR-HOT}}$ pin activates.

Table 3. VR-HOT Alert

SVID ALERT ASSERTED B[6]	$\overline{\text{VR-HOT}}$ ASSERTED B[7]
T_{SEN} > ($\overline{\text{VR-HOT}}$ threshold –20 mV)	T_{SEN} > $\overline{\text{VR-HOT}}$ threshold

7.3.18 Analog Current Monitor Signal (IMON) and Digital SVID Current Output

The TPS53640A device provides a analog current monitor function. The current monitor signal on the IMON pin provides a signal proportional to the real load current measured using Inductor DCR sensing.

$$V_{IMON} = \frac{I_{OUT} \times R_{DCR} \times 40 \times R_{IMON}}{35\,k\Omega}$$

where

- I_{OUT} is the total output current
- $I_{CC(max)}$ is the maximum current set by SVID ICC_MAX register (21h)
- V_{IMON} is the analog current monitor pin (IMON)voltage
- R_{IMON} is the desired impedance on IMON pin and is calculated in Equation 5 (4)

$$R_{IMON} = \frac{0.85\,V}{I_{CC(max)} \times R_{DCR} \times 10 \times \frac{4}{35\,k\Omega}} \quad (5)$$

Connect a capacitor in parallel to the R_{IMON} resistor to set the averaging time for the current monitor. Equation 5 sets the maximum current $I_{CC(max)}$ value equivalent to 850 mV, which is reported FFh in SVID output current register 15h.

7.4 Device Functional Modes

7.4.1 Number of Active Phases

The TPS53640A device operates in 4-phase mode.

7.5 Programming

7.5.1 User Selections

The following user selections are latched when 3.3-V is applied to the V3P3 pin (with a slew rate > 1.5 V/ms). These values can be changed via the PMBus interface. The *Electrical Characteristics* table summarizes the values of the selections.

7.5.1.1 Switching Frequency

The resistor from F-IMAX pin to GND sets the switching frequency from 300 kHz to 1 MHz. See the *Electrical Characteristics* table for the resistor settings corresponding to each frequency selection. It is to be noted that the operating frequency is a quasi-fixed frequency in the sense that the ON time is fixed based on the input voltage (at the VIN pin) and output voltage (set by VID). The OFF time varies based on various factors such as load and power-stage components.

7.5.1.2 Maximum Current $I_{CC(max)}$ Information

The voltage on the F-IMAX pin sets the SVID $I_{CC(max)}$ register (15h). See the *Electrical Characteristics* table for the details.

7.5.1.3 Boot Voltage

The resistor from B-TMAXR pin to GND sets the boot voltage. See *Electrical Characteristics* table for the resistor settings corresponding to boot voltage selections.

7.5.1.4 TMAX Information

The voltage on the B-TMAXR pin can set the TMAX information of the CPU. See the *Electrical Characteristics* table for the details.

7.5.1.5 Overcurrent Limit (OCL) Level

The resistor from OCL to VREF sets the per-phase OCL level of the VR controller. See the *Electrical Characteristics* table for the details.

7.5.1.6 Overshoot Reduction (OSR) and Undershoot Reduction (USR) Level

The resistor to GND and the voltage on O-USR pin set the OSR and USR levels for CPU channel. See the *Electrical Characteristics* table for details.

7.5.1.7 Slew Rate Selection

The SetVID Fast slew rate is set by the resistor on the SLEW-MODE pin to GND. The SetVID Slow is 1/4 of the SetVID Fast rate.

Programming (continued)

7.5.1.8 Mode Selections

The TPS53640A device supports different operating modes, including VR12.0/VR12.5, phase interleaving mode, dynamic phase shedding, and zero load line. The voltage on SLEW-MODE pin sets the desired operating modes. See the *Electrical Characteristics* table for details.

Table 4. MFR_SPEC_13 Mode Settings

MODE BIT	COMMAND BIT		
M_4	MFR_SPEC_13[7]	$VR12_{MODE}$	0: VR12.5. 1: VR12.0.
M_3	MFR_SPEC_13[6]	—	—
M_2	MFR_SPEC_13[5]	$TEMPCOMP_{EN}$	0: Disable temperature compensation for IMON and OCL 1: Enable temperature compensation for IMON and OCL
M_1	MFR_SPEC_13[4]	DPS_{EN}	0: Disable dynamic phase shedding. 1: Enable dynamic phase shedding.
M_0	MFR_SPEC_13[3]	ZLL_{SET}	0: Non-zero load-line 1: Zero load-line

7.5.1.9 SVID and PMBus Addresses

The resistor to GND and the voltage on ADDR pin set the device address for SVID and PMBus interfaces. See *Electrical Characteristics* table for details.

7.5.1.10 Ramp Selection

The internal ramp can be selected by the resistor from SKIP#-RAMP pin to GND. See *Electrical Characteristics* table for details.

7.5.2 Supported Protections and Fault Reports

The TPS53640A device supports different types of fault protections, and the warning or fault reports can be found in the corresponding PMBus or SVID registers. The TPS53640A also supports $\overline{VR\_FAULT}$ to indicate catastrophic faults to the system. If the fault causes the controller to latch-off, then the device requires V3P3 pin re-cycling to clear the latched faults.

Table 5. Supported Protections and Fault Reports

CATEGORY	FAULT NAME	DESCRIPTIONS	LATCH-OFF	ALERT	REPORT
VOLTAGE	OVF_F	V_O > 2.75 V	Y	$\overline{VR\_FAULT}$ $\overline{PMB\_ALERT}$	PMBus
	OVF_T	$V_O > VID + V_{RDYH5/0}$	Y	$\overline{PMB\_ALERT}$	PMBus
	UVF	$V_O < VID - V_{RDYL}$	Y	$\overline{PMB\_ALERT}$	PMBus
	VIN_OVF	V_{VIN} > VIN_OV_FAULT_LIMIT when the switcher is enabled	N	$\overline{PMB\_ALERT}$	PMBus
	VIN_UVF	$V_{VIN} < V_{12UVLO}$ when the switcher is enabled	N	$\overline{PMB\_ALERT}$	PMBus
CURRENT	OCF	$I_O \geq$ IOUT_OC_FAULT_LIMIT	Y	$\overline{PMB\_ALERT}$	PMBus
	ICCMAX_F	$I_{IMON} \geq I_{CC(max)}$	N	$\overline{SVID\_ALERT}$	SVID
	OCW	$I_O \geq$ IOUT_OC_WARN_LIMIT	N	$\overline{PMB\_ALERT}$	PMBus
	IOCF	$I_{IN} \geq$ IIN_OC_FAULT_LIMIT	Y	$\overline{VR\_FAULT}$ $\overline{PMB\_ALERT}$	PMBus
	IOCW	$I_{IN} \geq$ IIN_OC_WARN_LIMIT	N	$\overline{PMB\_ALERT}$	PMBus

Table 5. Supported Protections and Fault Reports (continued)

CATEGORY	FAULT NAME	DESCRIPTIONS	LATCH-OFF	ALERT	REPORT
TEMPERATURE	OTF	$T_J \geq$ OT_FAULT_LIMIT	Y	$\overline{\text{VR\_FAULT}}$ $\overline{\text{PMB\_ALERT}}$	PMBus
	OTW	$T_J \geq$ OT_WARNING_LIMIT	N	$\overline{\text{PMB\_ALERT}}$	PMBus
	TMAX_F	$T_J \geq T_{MAX}$ (TEMP_ZONE[7]=1)	N	$\overline{\text{VR\_HOT}}$	SVID
	TZONE_F	T_J_ZONE[6]=1	N	$\overline{\text{SVID\_ALERT}}$	SVID
	TS_VREF	TSEN pin short to VREF	Y	$\overline{\text{PMB\_ALERT}}$	PMBus
	TS_GND	TSEN pin short to GND	Y	$\overline{\text{PMB\_ALERT}}$	PMBus
	TS_PS	$V_{TSEN} > 2.5$ V	Y	$\overline{\text{VR\_FAULT}}$ $\overline{\text{PMB\_ALERT}}$	PMBus

7.5.3 SVID/PMBus Controlled Output Voltage

TPS53640A device supports both SVID and PMBus interfaces, but the SVID_PMBUS_SEL (MFR_SPECIFIC_02 command of PMBus command set) determines the output voltage control. The arbitration based on these bits is described as follows.

SVID_PMBUS_SEL	EFFECT
10b	V_{OUT} programming available only via SVID
01b	V_{OUT} programming available only via the PMBus interface

The MFR_SPECFIC_02 command selects SVID or PMBus to control the output voltage. During power-on-reset (POR), the SVID_PMBUS_SEL defaults to 10b. The SVID bus has control of the output voltage. Writing 01b to these bits enables PMBus control of the output voltage. With PMBus control, absolute VID is controlled by writing a VID word to VOUT_COMMAND (0x21).

7.5.3.1 SVID Bus Behavior During PMBus Control

The SVID bus must continue to respond to SVID transactions from the CPU normally excepting that no SetVID command changes the output voltage. Instead, the controller must assert SVID $\overline{\text{ALERT}}$ immediately after receiving the SetVID command and set the VR_settled bit in Status1 (0x10). Thus the VR controller does not cause the CPU to hang while waiting for SVID $\overline{\text{ALERT}}$ assertion due to a SetVID command.

7.5.3.2 PMBus Controlled Output Voltage Changes

Changes in output voltage that are initiated by PMBus control should use fast slew rate in a way similar to SetVID Fast.

7.6 Register Maps

7.6.1 PMBus Description

7.6.1.1 PMBus General

Timing and electrical characteristics of the PMBus can be found in the *PMB Power Management Protocol Specification, Part 1, revision 1.1* available at http://PMBus.org. The TPS53640A device supports both the 100-kHz and 400-kHz bus timing requirements. The TPS53640A device does not stretch pulses on the PMBus when communicating with the master device.

Communication over the TPS53640A device PMBus interface can support the packet error checking (PEC) scheme if desired. If the master supplies CLK pulses for the PEC byte, PEC is used. If the CLK pulses are not present before a STOP, the PEC is not used.

The TPS53640A device supports a subset of the commands in the PMBus 1.1 specification. Most of the controller parameters can be programmed using the PMBus and stored as defaults for later use. All commands that require data input or output use the literal format. The exponent of the data words is fixed at a reasonable value for the command and altering the exponent is not supported. Direct format data input or output is not supported by the TPS53640A device. See the *Supported PMBus Commands* section for specific details.

Register Maps (continued)

The TPS53640A device also supports the SMBALERT response protocol. The SMBALERT response protocol is a mechanism by which a slave (the TPS53640A device) can alert the bus master that it wants to talk. The master processes this event and simultaneously accesses all slaves on the bus (that support the protocol) through the alert response address. Only the slave that caused the alert acknowledges this request. The host performs a modified receive byte operation to get the slave's address. At this point, the master can use the PMBus status commands to query the slave that caused the alert. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) specification.

Table 6. VID Code Offset

VID_{OFS1}	OFFSET ON VID CODE
0	No offsets
1	10 mV for VR12.0 20 mV for VR12.5

Table 7. SVID Default Register Settings

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
$VMAX_0$	Maximum output voltage (VR12.0)	Register 30h		FFh		Hex
$VMAX_5$	Maximum output voltage (VR12.5)	Register 30h		FFh		
PID	Protocol ID	Register 05h, VR12.0 Mode		01h		
		Register 05h, VR12.5 Mode		02h		

Table 8. IMON Pin: Current Monitor

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
VAL_{ADC}	SVID IMON ADC Output	4-phase, I_{MAX} = 188 A , $\sum i_L$ = 37.6 A	30h	33h	36h	Hex
		4-phase, I_{MAX} = 188 A , $\sum i_L$ = 56.4 A	48h	4Ch	50h	
		4-phase, I_{MAX} = 188 A , $\sum i_L$ = 188.0 A	F6h	FFh	FFh	

7.6.1.2 PMBus Settings

7.6.1.3 PMBus Connections

The TPS53640A device can operate in either standard mode (100 k bits per second) or fast mode (400 k bits per second). Connection for the PMBus interface should follow the high-power DC specifications given in *Section 3.1.3 of the System Management Bus (SMBus) Specification V2.0* for the 400-kHz bus speed or the Low Power DC specifications in *Section 3.1.2*. The complete SMBus specification is available from the SMBus website, smbus.org.

7.6.1.4 Supported Data Formats

The TPS53640A device supports both linear and VID data formats. The linear data format is used for all telemetry reporting data, and VID formatting for certain other commands. (see Supported PMBus Commands for more details on which command supports which data type). Examples of commands that support VID formatting include VOUT_MODE (Read-only Byte) and VOUT_COMMAND (Read/Write Word). An example of each can be seen below in Figure 17 and Figure 18.

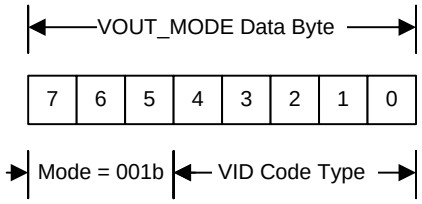


Figure 17. VOUT_MODE Data Byte for VID Mode

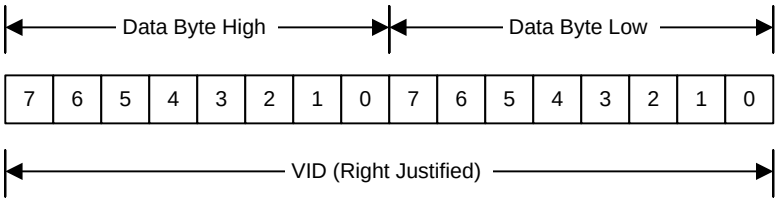


Figure 18. VOUT_COMMAND Data Bytes for VID Mode

The Linear Data Format is a two byte value with:

- An 11-bit, two's complement mantissa, and
- A 5-bit, two's complement exponent (scaling factor).

The format of the two bytes is shown in Figure 19.

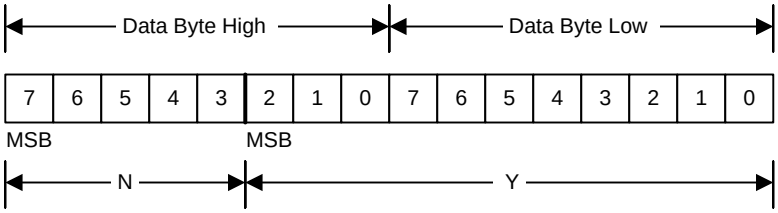


Figure 19. Linear Data Format Data Bytes

The relation between Y, N, and the *real world* value is as shown in Equation 6.

$$X = Y \times 2^{N} \quad (6)$$

where

- X is the *real world* value
- Y is an 11-bit, two's complement integer
- N is a 5-bit, two's complement integer

Note that devices that use the Linear format must accept and be able to process any value of N.

7.6.1.5 PMBus Command Format

The TPS53640A device is a PMBus-compliant device. Figure 20 through Figure 31 show the major communication protocols used. For full details on the PMBus communication protocols, please visit http://pmbus.org.

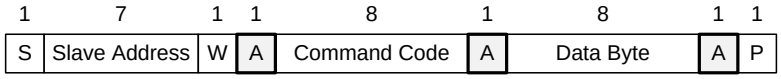


Figure 20. Write Byte Protocol

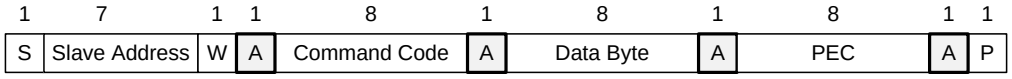


Figure 21. Write Byte Protocol with PEC

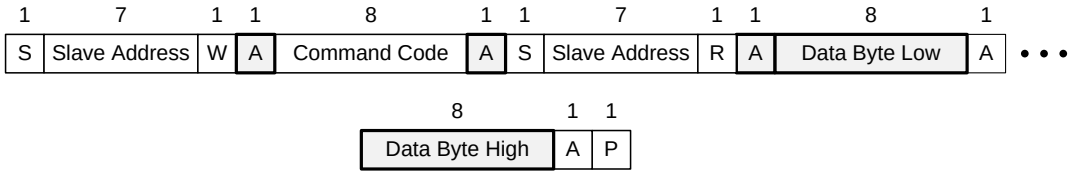


Figure 22. Write Word Protocol

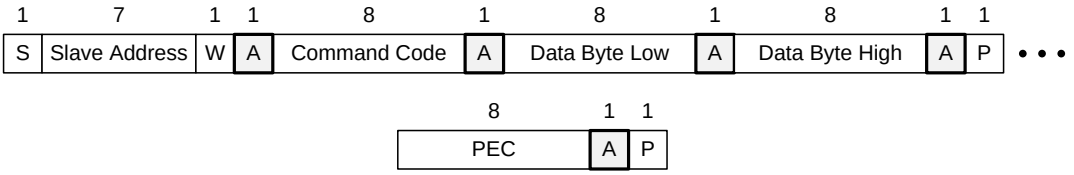


Figure 23. Write Word Protocol with PEC

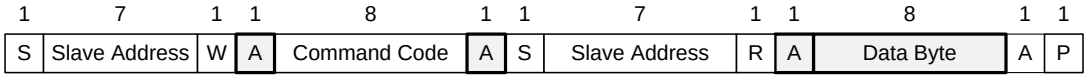


Figure 24. Read Byte Protocol

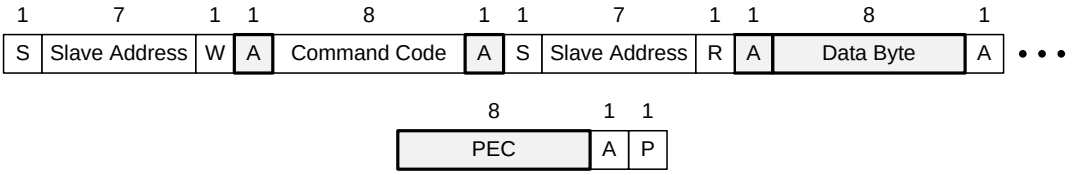


Figure 25. Read Byte Protocol with PEC

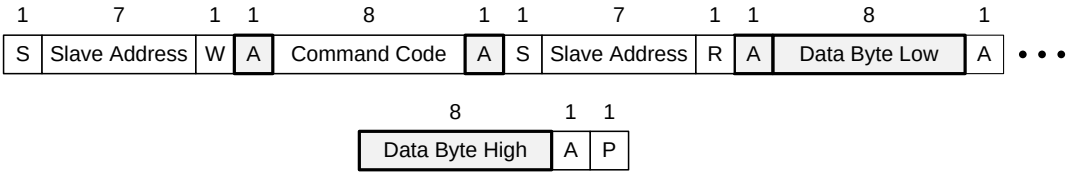


Figure 26. Read Word Protocol

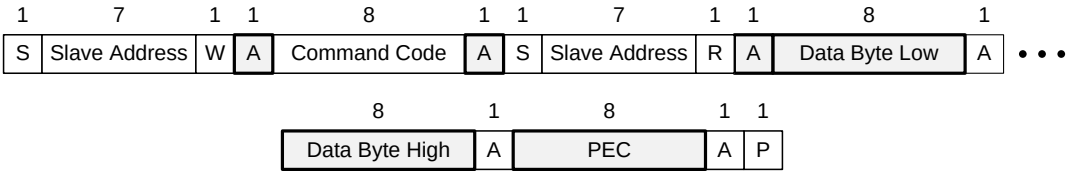


Figure 27. Read Word Protocol with PEC

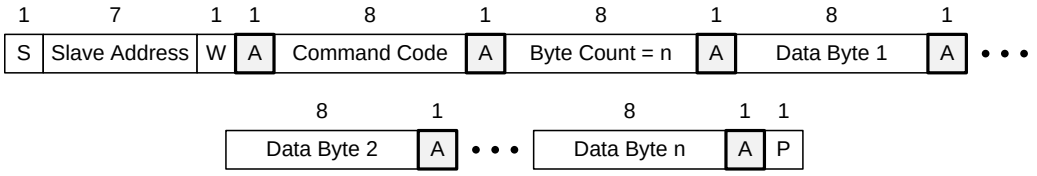


Figure 28. Block Write Protocol

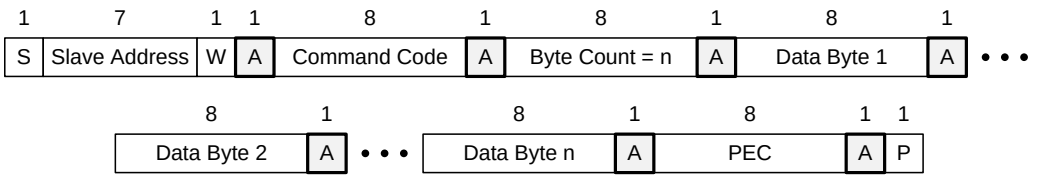


Figure 29. Block Write Protocol with PEC

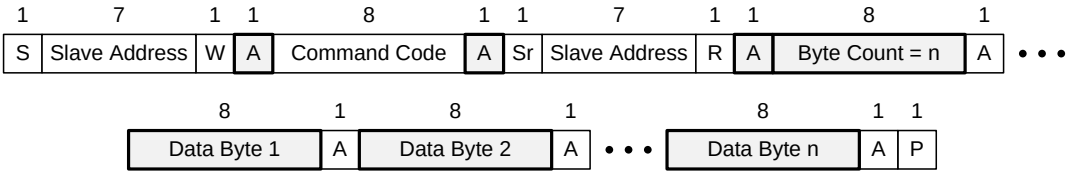


Figure 30. Block Read Protocol

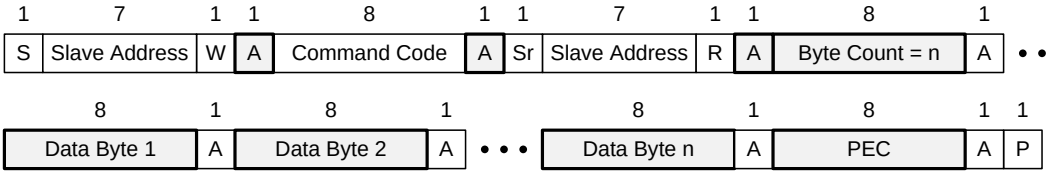


Figure 31. Block Read Protocol with PEC

7.6.2 PMBus Functionality

7.6.2.1 PMBus Address

System Level Clarifications

The *default state* of all configuration registers should be detected from pin settings, but users can overwrite the settings via PMBus after power up.

The TPS53640A device has a dedicated pin (ADDR) for determining the address for the PMBus communication. The first seven bits of the address byte for the slave address are $11P_40P_2P_1P_0$, where $P_4P_2P_1P_0$ is set by the ADDR pin. The device supports a total of 16 possible addresses as shown in Table 9.

Table 9. Address Selection Summary

PARAMETER		CONDITIONS	ADDRESS
PADDR	PMBus Address Bits Set ($11P_40P_2\ P_1P_0$)	V_{ADDR} ≤ 0.027 V or V_{ADDR} = 0.877 V with ±10 mV tolerance	1100000
		V_{ADDR} = 0.08 V or V_{ADDR} = 0.93 V with ±10 mV tolerance	1100001
		V_{ADDR} = 0.133 V or V_{ADDR} = 0.983 V with ±10 mV tolerance	1100010
		V_{ADDR} = 0.186 V or V_{ADDR} = 1.036 V with ±10 mV tolerance	1100011
		V_{ADDR} = 0.24 V or V_{ADDR} = 1.09 V with ±10 mV tolerance	1100100
		V_{ADDR} = 0.293 V or V_{ADDR} = 1.143 V with ±10 mV tolerance	1100101
		V_{ADDR} = 0.346 V or V_{ADDR} = 1.196 V with ±10 mV tolerance	1100110
		V_{ADDR} = 0.399 V or V_{ADDR} = 1.249 V with ±10 mV tolerance	1100111
		V_{ADDR} = 0.452 V or V_{ADDR} = 1.302 V with ±10 mV tolerance	1110000
		V_{ADDR} = 0.505 V or V_{ADDR} = 1.355 V with ±10 mV tolerance	1110001
		V_{ADDR} = 0.558 V or V_{ADDR} = 1.408 V with ±10 mV tolerance	1110010
		V_{ADDR} = 0.611 V or V_{ADDR} = 1.461 V with ±10 mV tolerance	1110011
		V_{ADDR} = 0.665 V or V_{ADDR} = 1.515 V with ±10 mV tolerance	1110100
		V_{ADDR} = 0.718 V or V_{ADDR} = 1.568 V with ±10 mV tolerance	1110101
		V_{ADDR} = 0.771 V or V_{ADDR} = 1.621 V with ±10 mV tolerance	1110110
		V_{ADDR} = 0.823 V or V_{ADDR} ≥ 1.674 V with ±10 mV tolerance	1110111

7.6.2.2 Pin Strap Settings

The TPS53640A device supports only PMBus command sets listed in Table 10. The default state of all the configuration registers should be detected from pin strap settings, but users can overwrite the settings via PMBus after the power-up sequence is complete. The pin strap settings can be found in the Electrical Characteristics table.

7.6.2.3 Supported PMBus Commands

The TPS53640A device supports the following commands from the PMBus 1.1 specification.

Table 10. PMBus Factory Default Setting

CODE	COMMAND NAME	TYPE	DESCRIPTION: PMBus Command	FACTORY DEFAULT VALUE
01h	OPERATION	R/W Byte	Turn the unit on and off in conjunction with the input from the ENABLE pin. Set the output voltage to the upper or lower MARGIN voltages.	00h
02h	ON_OFF_CONFIG	R/W Byte	Configures the combination of ENABLE pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.	17h
03h	CLEAR_FAULTS	Send Byte	Clears any faults bits that have been set if the fault is no longer present. At the same time, simultaneously clears all bits in all status registers and negates the PMB_ALERT signal output if it is asserted.	NONE
10h	WRITE_PROTECT	R/W Byte	Used to control writing to the PMBus device. Can be used to prevent unwanted writes to the device.	00h
19h	CAPABILITY	Read Byte	Provides a way for the host to determine the capabilities of the PMBus device.	B0h
20h	VOUT_MODE	Read Byte	Read-Only VOUT Mode Indicator.	3Eh
21h	VOUT_COMMAND	R/W Word	Causes the device to set its output voltage to the commanded value.	VBOOT
24h	VOUT_MAX	R/W Word	Sets the upper limit on the output voltage the unit can command regardless of any other commands or combinations. Provides a safeguard against a user accidentally setting the output voltage to a possibly destructive level.	00C9h
25h	VOUT_MARGIN_HIGH	R/W Word	Loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin High."	0000h
26h	VOUT_MARGIN_LOW	R/W Word	Loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin Low."	0000h
41h	VOUT_OV_FAULT_RESPONSE	Read Byte	Instructs the device on what action to take in response to an output overvoltage fault.	80h
45h	VOUT_UV_FAULT_RESPONSE	Read Byte	Instructs the device on what action to take in response to an output undervoltage fault.	00h
46h	IOUT_OC_FAULT_LIMIT	R/W Word	Sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent fault condition.	125% IMAX
47h	IOUT_OC_FAULT_RESPONSE	Read Byte	Instructs the device on what action to take in response to an output overcurrent fault.	C0h
4Ah	IOUT_OC_WARN_LIMIT	R/W Word	Sets the value of the output current that causes an output overcurrent warning condition.	IMAX
4Fh	OT_FAULT_LIMIT	R/W Word	Sets the temperature, in degree Celsius, that causes an over-temperature fault condition.	0073h
50h	OT_FAULT_RESPONSE	Read Byte	Instructs the device on what action to take in response to an output over-temperature fault.	80h
51h	OT_WARN_LIMIT	R/W Word	Sets the temperature, in degrees Celsius, that causes an over-temperature warning condition.	005Fh

Table 10. PMBus Factory Default Setting (continued)

CODE	COMMAND NAME	TYPE	DESCRIPTION: PMBus Command	FACTORY DEFAULT VALUE
55h	VIN_OV_FAULT_LIMIT	R/W Word	Sets the input voltage, in volts, that causes an overvoltage fault condition.	000Eh
5Bh	IIN_OC_FAULT_LIMIT	R/W Word	Sets the input current, in amperes, that causes an overcurrent fault condition.	00FFh
5Ch	IIN_OC_FAULT_RESPONSE	Read Byte	Instructs the device on what action to take in response to an input overcurrent fault.	C0h
5Dh	IIN_OC_WARN_LIMIT	R/W Word	Sets the input current, in amperes, that causes an overcurrent warning condition.	00FFh
78h	STATUS_BYTE	Read Byte	Single byte status indicator	Dependent on the Startup Condition
79h	STATUS_WORD	Read Word	Full 2-byte status indicator	Dependent on the Startup Condition
7Ah	STATUS_VOUT	Read Byte	Output voltage fault status detail	Dependent on the Startup Condition
7Bh	STATUS_IOUT	Read Byte	Output current fault status detail	Dependent on the Startup Condition
7Ch	STATUS_INPUT	Read Byte	Input voltage and current fault status detail	Dependent on the Startup Condition
7Dh	STATUS_TEMPERATURE	Read Byte	Temperature fault status detail	Dependent on the Startup Condition
7Eh	STATUS_CML	Read Byte	Communication, memory, and logic fault status detail	Dependent on the Startup Condition
80h	STATUS_MFR_SPECIFIC	Read Byte	Manufacturer specific fault status detail	Dependent on the Startup Condition
88h	READ_VIN	Read Word	Read input voltage, in volts	
89h	READ_IIN	Read Word	Read input current, in amperes	
8Bh	READ_VOUT	Read Word	Read output voltage, in volts	
8Ch	READ_IOUT	Read Word	Read output current, in amperes	
8Dh	READ_TEMPERATURE_1	Read Word	Read temperature, in degrees Celsius	
96h	READ_POUT	Read Word	Read output power, in watts	
97h	READ_PIN	Read Word	Read input power, in watts	
98h	PMBUS_REVISION	Read Byte	PMBus Revision Information	11h
99h	MFR_ID	Read Block	Loads the unit with the text character that contains the manufacturer's ID. One byte.	54h
9Ah	MFR_MODEL	Read Block	Loads the unit with the text character that contains the model number of the manufacturer. One byte.	34h
9Bh	MFR_REVISION	Read Block	Loads the unit with the text character that contains the revision number of the manufacturer.	

Table 10. PMBus Factory Default Setting (continued)

CODE	COMMAND NAME	TYPE	DESCRIPTION: PMBus Command	FACTORY DEFAULT VALUE
D2h	MFR_SPECIFIC_02	R/W Byte	Selects SVID or PMBus to control the output voltage	02h
D4h	MFR_SPECIFIC_04	Read Word	Returns the actual, measured output voltage in volts.	
D5h	MFR_SPECIFIC_05	R/W Byte	Used to trim the output voltage.	00h
D8h	MFR_SPECIFIC_08	R/W Byte	Sets the droop as a percentage of the loadline.	04h
D9h	MFR_SPECIFIC_09	R/W Byte	Sets the threshold for OSR and USR control.	O-USR pin
DAh	MFR_SPECIFIC_10	R/W Byte	Sets the maximum operating current, IMAX.	F-IMAX pin
DBh	MFR_SPECIFIC_11	R/W Byte	Sets the boot voltage, VBOOT.	B-TMAXR pin
DCh	MFR_SPECIFIC_12	R/W Byte	Sets the switching frequency and the maximum operating temperature TMAX.	F-IMAX and B-TMAXR pins
DDh	MFR_SPECIFIC_13	R/W Byte	Sets the slew rate and other operation modes.	SLEW-MODE pin
DEh	MFR_SPECIFIC_14	R/W Byte	Sets the ramp amplitude in mV.	B-TMAXR and $\overline{\text{SKIP}}$-RAMP pins
DFh	MFR_SPECIFIC_15	R/W Byte	Sets the threshold for dynamic phase shedding as a percentage of the OCL.	00h
E0h	MFR_SPECIFIC_16	R/W Byte	Sets the threshold for the input voltage UVLO.	00h
E2h	MFR_SPECIFIC_18	R/W Byte	Sets the averaging time for telemetry reporting.	50h
E4h	MFR_SPECIFIC_20	R/W Byte	Sets the maximum number of operational phase numbers on the fly.	Hardware Specific
FCh	MFR_SPECIFIC_44	Read Word	Returns DEVICE_CODE information	00D3h

7.6.2.3.1 OPERATION (01h)

Format N/A

Description The OPERATION command is used to turn the device output on or off in conjunction with the input from the ENABLE pin. It is also used to set the output voltage to the upper or lower MARGIN levels.

Default 00h

Figure 32. OPERATION Register

7	6	5	4	3	2	1	0
ON_OFF	SOFT_OFF	OPMARGIN				Reserved	
R/W	R-0	R/W				R-00	

Table 11. OPERATION Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ON_OFF	R/W	0	The On/Off bit is used to enable the IC via PMBus. The necessary condition for this bit to be effective is that the CMD bit in the ON_OFF CONFIG register is set high. However, the CMD bit being high is not a sufficient condition to enable the IC via the On bit, as specified below: 0: (Default) The device output is not enabled via PMBus. 1: The device output is enabled if: a. The supply voltage VIN is greater than the VIN_UVLO threshold, the cmd bit is high, and b. The bit CP in the ON_OFF CONFIG register is low, or c. The bit CP is high and the ENABLE pin is asserted.
6	SOFT_OFF	R	0	This bit is not supported and always set to 0 on this device. 0: No Soft off
5-2	OPMARGIN	R/W	0	If Margin Low is enabled, load the value from the VOUT_MARGIN_HIGH register. If Margin High is enabled, load the value from the VOUT_MARGIN_HIGH register. 00xx: Turn off VOUT margin function 0101: Turn on VOUT margin low and ignore fault 0110: Turn on VOUT margin low and act on fault 1001: Turn on VOUT margin high and ignore fault 1010: Turn on VOUT margin high and act on fault
1-0	Reserved	R	00	Always set to 0.

7.6.2.3.2 ON_OFF_CONFIG (02h)

Format N/A

Description The ON_OFF_CONFIG command configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.

Default 17h

Figure 33. ON_OFF_CONFIG Register

7	6	5	4	3	2	1	0
Reserved			PU	CMD	CP	PL	SP
R-000			R-1	R/W	R/W	R-1	R-1

Table 12. ON_OFF_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R	000	Always set to 0.
4	PU	R	1	This bit is not supported and always set to 1 on this device. 1: Device will act on ENABLE pin assertion and/or ON_OFF bit (OPERATION[7]).
3	CMD	R/W	0	The CMD bit controls how the device responds to the OPERATION[7] bit. 0: (Default) Device ignores the ON_OFF OPERATION[7] bit. 1: Device responds to the ON_OFF OPERATION[7] bit.
2	CP	R/W	1	The CP bit controls how the device responds to the ENABLE pin 0: Device ignores the ENABLE pin, and ON/OFF is controlled only by the OPERATION command 1: Device responds to the ENABLE pin.
1	PL	R	1	This bit is not supported and always set to 1 on this device. 1: ENABLE pin has active high polarity.
0	SP	R	1	This bit is not supported and always set to 1 on this device. 1: Turn off output as fast as possible.

7.6.2.3.3 CLEAR_FAULTS (03h)

Format N/A

Description Clears any faults bits that have been set. At the same time, simultaneously clears all bits in all status registers and negates the PMB_ALERT signal output if it is asserted.
The CLEAR_FAULTS command does not cause a unit that has latched off for a condition to restart. If the fault is still present when the bit is cleared, the fault bit shall immediately be set again and the host notified by the usual means.

Default NONE

Figure 34. CLEAR_FAULTS Register

7	6	5	4	3	2	1	0
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
—	—	—	—	—	—	—	—

Table 13. CLEAR_FAULTS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	N/A	—	—	No data bytes are sent, only the command code is sent.

7.6.2.3.4 WRITE_PROTECT (10h)

Format N/A

Description The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command has one data byte as described below.
NOTE: Invalid data written to WRITE_PROTECT[7:5] causes the 'CML' bit in the STATUS_BYTE and the 'US_DATA' bit in the STATUS_CML registers to be set. INVALID DATA ALSO RESULTS IN NO WRITE PROTECTION (WRITE_PROTECT = 00h).

Default 00h

Figure 35. WRITE_PROTECT Register

7	6	5	4	3	2	1	0
bit7	bit6	bit5	Not Used				
R/W	R/W	R/W	R-0 0000				

Table 14. WRITE_PROTECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	bit7	R/W	0	0: (Default) See Table 15. 1: Disable all writes except for the WRITE_PROTECT command (bit5 and bit6 must be 0 to be valid).
6	bit6	R/W	0	0: (Default) See Table 15. 1: Disable all writes except for the WRITE_PROTECT and OPERATION commands (bit5 and bit7 must be 0 to be valid).
5	bit5	R/W	0	0: (Default) See Table 15. 1: Disable all writes except for the WRITE_PROTECT, OPERATION, and ON_OFF_CONFIG commands (bit6 and bit7 must be 0 to be valid).
4-0	Not Used	R	0 0000	Reads are always set to 0.

Table 15. WRITE_PROTECT Data Byte Values

Data Byte Value	Action
1000 0000	Disables all writes except to the WRITE_PROTECT command.
0100 0000	Disables all writes except to the WRITE_PROTECT and OPERATION commands.
0010 0000	Disables all writes to the WRITE_PROTECT, OPERATION, and ON_OFF_CONFIG commands.
Others	Fault data.

7.6.2.3.5 CAPABILITY (19h)

Format N/A

Description This command provides a way for a host system to determine some key capabilities of this PMBus device.

Default B0h

Figure 36. CAPABILITY Register

7	6	5	4	3	2	1	0
PEC	SPD		$\overline{\text{PMBALERT}}$	Reserved			
R-1	R-01		R-1	R-0000			

Table 16. CAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PEC	R	1	Packet Error Checking is supported. 1: Default
6-5	SPD	R	01	Maximum supported bus speed is 400 kHz. 01: Default
4	$\overline{\text{PMBALERT}}$	R	1	This device does have a $\overline{\text{PMBALERT}}$ pin and does support the SMBus Alert Response Protocol. 1: Default
3-0	Reserved	R	0000	Always set to 0.

7.6.2.3.6 VOUT_MODE (20h)

Format	VID
Description	The PMBus specification dictates that the data word for the VOUT_MODE command is one byte that consists of a 3-bit Mode and 5-bit parameter, as shown below. This command is read-only. If the host sends a VOUT_MODE command for writing, the device will reject the command and declare a communication fault for invalid data and respond as described in *PMBus specification II* section 10.2.2.
Default	3Eh

Figure 37. VOUT_MODE Register

7	6	5	4	3	2	1	0
DATA_MODE			DATA_PARAMETER				
R-001			R-1 1110				

Table 17. VOUT_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	DATA_MODE	R	001	VID mode.
4-0	DATA_PARAMETER	R	1 1110	PMBus Device Manufacturer Specific (Intel VR12.x VID).

7.6.2.3.7 VOUT_COMMAND (21h)

Format	VID
Description	VOUT_COMMAND causes the device to set its output voltage to the commanded value with two data bytes. These data bytes consist of a right-justified VID code with VID0 in bit 0 of the lower data byte, VID1 in bit 1 of the lower byte and so forth. The VID table mapping is determined by the selected SVID protocols from SLEW_MODE pin or MFR_SPECIFIC_13.
Default	VBOOT

Figure 38. VOUT_COMMAND Register

15	14	13	12	11	10	9	8
Reserved							
R-0000 0000							
7	6	5	4	3	2	1	0
VOUT							
R/W							

Table 18. VOUT_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0000 0000	Always set to 0.
7-0	VOUT	R/W		Used to set the commanded VOUT. Cannot be set to a level above the value set by VOUT_MAX.

7.6.2.3.8 VOUT_MAX (24h)

Format VID

Description The VOUT_MAX command sets an upper limit on the output voltage that the unit can command regardless of an other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level.
The device detects that an attempt has been made to program the output to a voltage greater than the value set by the VOUT_MAX command. This will then be treated as a warning condition and not a fault condition. If an attempt is make to program the output voltage higher than the limit set by this command, the device shall respond as follows:

- The commanded output voltage shall be set to VOUT_MAX,
- The OTHER bit shall be set in the STATUS_BYTE,
- The VOUT bit shall be set in the STATUS_WORD,
- The VOUT_MAX warning bit shall be set in the STATUS_VOUT register, and
- The device notifies the host (asserts PMBUS_ALERT).

The data bytes are two bytes, which are in right-justified VID format. The VID table mapping is determined by the selected SVID protocols from the SLEW_MODE pin or MFR_SPECIFIC_13.

Default 00C9h .

Figure 39. VOUT_MAX Register

15	14	13	12	11	10	9	8
Reserved							
R-0000 0000							
7	6	5	4	3	2	1	0
VOUT_MAX							
R/W							

Table 19. VOUT_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0000 0000	Always set to 0.
7-0	VOUT_MAX	R/W	1100 1001	Used to set the maximum VOUT of the device.

7.6.2.3.9 VOUT_MARGIN_HIGH (25h)

Format VID

Description The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to *Margin High*. The data bytes are two bytes, which are in right-justified VID format. The VID table mapping determined by the selected SVID protocols from the SLEW_MODE pin or MFR_SPECIFIC_13.

Default 0000h

Figure 40. VOUT_MARGIN_HIGH Register

15	14	13	12	11	10	9	8
Reserved							
R-0000 0000							
7	6	5	4	3	2	1	0
VOUT_MARGIN_HIGH							

R/W

Table 20. VOUT_MARGIN_HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0000 0000	Always set to 0.
7-0	VOUT_MARGIN_HIGH	R/W	0000 0000	Used to set the value for the VOUT Margin High.

7.6.2.3.10 VOUT_MARGIN_LOW (26h)

Format VID

Description The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to *Margin Low*. The data bytes are two bytes, which are in right-justified VID format. The VID table mapping determined by the selected SVID protocols from the SLEW_MODE pin or MFR_SPECIFIC_13.

Default 0000h

Figure 41. VOUT_MARGIN_LOW Register

15	14	13	12	11	10	9	8
Reserved							
R-0000 0000							
7	6	5	4	3	2	1	0
VOUT_MARGIN_LOW							
R/W							

Table 21. VOUT_MARGIN_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0000 0000	Always set to 0.
7-0	VOUT_MARGIN_LOW	R/W	0000 0000	Used to set the value for the VOUT Margin Low.

7.6.2.3.11 VOUT_OV_FAULT_RESPONSE (41h)

Format N/A

Description The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output overvoltage fault. Upon triggering the overvoltage fault, the controller is latched off, and the following actions are taken:

- Set the VOUT_OV_FAULT bit in the STATUS_BYTE,
- Set the VOUT bit in the STATUS_WORD,
- Set the VOUT_OV_FAULT bit in the STATUS_VOUT register, and
- The device notifies the host (asserts PMB_ALERT).

Default 80h

Figure 42. VOUT_OV_FAULT_RESPONSE Register

7	6	5	4	3	2	1	0
VOUT_OV_FAULT_RESPONSE							
R-1000 0000							

Table 22. VOUT_OV_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VOUT_OV_FAULT_RESPONSE	R	1000 0000	Upon triggering the overvoltage fault, the controller will shut the device down immediately and will not attempt to restart. The output remains disabled until the fault is cleared.

7.6.2.3.12 VOUT_UV_FAULT_RESPONSE (45h)

Format N/A

Description The VOUT_UV_FAULT_RESPONSE instructs the device on what action to take in response to an output undervoltage fault. Upon triggering the undervotlage fault, the following actions are taken:

- Set the OTHER bit in the STATUS_BYTE,
- Set the VOUT bit in the STATUS_WORD,
- Set the VOUT_UV_FAULT bit in the STATUS_VOUT register, and
- The device notifies the host (asserts PMB_ALERT).

Default 00h

Figure 43. VOUT_UV_FAULT_RESPONSE Register

7	6	5	4	3	2	1	0
VOUT_UV_FAULT_RESPONSE							
R-0000 0000							

Table 23. VOUT_UV_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VOUT_UV_FAULT_RESPONSE	R	0000 0000	Upon triggering the undervoltage fault, the controller will continue operation without interruption.

7.6.2.3.13 IOUT_OC_FAULT_LIMIT (46h)

Format Linear

Description The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in amperes, that causes an overcurrent fault condition. Upon triggering the overcurrent fault, the following actions are taken:

- Set the IOUT_OC_FAULT bit in the STATUS_BYTE,
- Set the IOUT bit in the STATUS_WORD,
- Set the IOUT_OC_FAULT bit in the STATUS_IOUT register, and
- The device notifies the host (asserts PMB_ALERT).

Default 125% IMAX

Figure 44. IOUT_OC_FAULT_LIMIT Register

15	14	13	12	11	10	9	8
OCF_LIMIT_EXPONENT					OCF_LIMIT_MANTISSA		
R/W					R/W		
7	6	5	4	3	2	1	0
OCF_LIMIT_MANTISSA							
R/W							

Table 24. IOUT_OC_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	OCF_LIMIT_EXPONENT	R/W		5-bit, two's complement exponent (scaling factor).
10-0	OCF_LIMIT_MANTISSA	R/W		11-bit, two's complement mantissa.

7.6.2.3.14 IOUT_OC_FAULT_RESPONSE (47h)

Format	N/A
Description	The IOUT_OC_FAULT_RESPONSE instructs the device on what action to take in response to an output overcurrent fault. Upon triggering the overcurrent fault, the controller is latched off, and the following actions are taken: • Set the IOUT_OC_FAULT bit in the STATUS_BYTE, • Set the IOUT bit in the STATUS_WORD, • Set the IOUT_OC_FAULT bit in the STATUS_IOUT register, and • The device notifies the host (asserts PMB_ALERT).
Default	C0h

Figure 45. IOUT_OC_FAULT_RESPONSE Register

7	6	5	4	3	2	1	0
IOUT_OC_FAULT_RESPONSE							
R-1100 0000							

Table 25. IOUT_OC_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IOUT_OC_FAULT_RESPONSE	R	1100 0000	Upon triggering the output overcurrent fault, the device will shut down immediately (disables the output), and will not attempt to restart. The output then remains disabled until the fault is cleared.

7.6.2.3.15 IOUT_OC_WARN_LIMIT (4Ah)

Format	Linear
Description	The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes an output overcurrent warning condition. Upon triggering the overcurrent warning, the following actions are taken: • Set the OTHER bit in the STATUS_BYTE, • Set the IOUT bit in the STATUS_WORD, • Set the IOUT OC Warning bit in the STATUS_IOUT register, and • The device notifies the host (asserts PMB_ALERT).
Default	IMAX

Figure 46. IOUT_OC_WARN_LIMIT Register

15	14	13	12	11	10	9	8
OCW_LIMIT_EXPONENT					OCW_LIMIT_MANTISSA		
R/W					R/W		
7	6	5	4	3	2	1	0
OCW_LIMIT_MANTISSA							
R/W							

Table 26. IOUT_OC_WARN_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	OCW_LIMIT_EXPONENT	R/W		5-bit, two's complement exponent (scaling factor).
10-0	OCW_LIMIT_MANTISSA	R/W		11-bit, two's complement mantissa.

7.6.2.3.16 OT_FAULT_LIMIT (4Fh)

Format	Linear
Description	The OT_FAULT_LIMIT command sets the value of the temperature limit, in degrees Celsius, that causes an over-temperature fault condition. The default value is 115C. Upon triggering the over-temperature fault, the following actions are taken: • Set the TEMPERATURE bit in the STATUS_BYTE, • Set the OT_FAULT bit in the STATUS_TEMPERATURE register, and • The device notifies the host (asserts PMB_ALERT and VR_FAULT).
Default	0073h

Figure 47. OT_FAULT_LIMIT Register

15	14	13	12	11	10	9	8
OT_LIMIT_EXPONENT					OT_LIMIT_MANTISSA		
R/W					R/W		
7	6	5	4	3	2	1	0
OT_LIMIT_MANTISSA							
R/W							

Table 27. OT_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	OT_LIMIT_EXPONENT	R/W	0000 0	5-bit, two's complement exponent (scaling factor).
10-0	OT_LIMIT_MANTISSA	R/W	000 0111 0011	11-bit, two's complement mantissa.

7.6.2.3.17 OT_FAULT_RESPONSE (50h)

Format N/A

Description The OT_FAULT_RESPONSE instructs the device on what action to take in response to an over-temperature fault. Upon triggering the over-temperature fault, the controller is latched off, and the following actions are taken:

- Set the TEMPERATURE bit in the STATUS_BYTE,
- Set the OT_FAULT bit in the STATUS_TEMPERATURE register, and
- The device notifies the host (asserts PMB_ALERT and VR_FAULT).

Default 80h

Figure 48. OT_FAULT_RESPONSE Register

7	6	5	4	3	2	1	0
OT_FAULT_RESPONSE							
R-1100 0000							

Table 28. OT_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OT_FAULT_RESPONSE	R	1100 0000	Upon triggering the over-temperature fault, the device will shut down immediately (disables the output), and will not attempt to restart. The output then remains disabled until the fault is cleared.

7.6.2.3.18 OT_WARN_LIMIT (51h)

Format Linear

Description The OT_WARN_LIMIT command sets the temperature, in degrees Celsius, at which it should indicate an over-temperature warning condition. The default value is 95C. Upon triggering the over-temperature warning, the following actions are taken:

- Sets the TEMPERATURE bit in the STATUS_BYTE,
- Sets the OT Warning bit in the STATUS_TEMPERATURE register, and
- The device notifies the host (asserts PMB_ALERT).

Default 005Fh

Figure 49. OT_WARN_LIMIT Register

15	14	13	12	11	10	9	8
OTW_WARN_EXPONENT					OTW_WARN_MANTISSA		
R/W					R/W		
7	6	5	4	3	2	1	0
OTW_WARN_MANTISSA							
R/W							

Table 29. OT_WARN_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	OTW_WARN_EXPONENT	R/W	0000 0	5-bit, two's complement exponent (scaling factor).
10-0	OTW_WARN_MANTISSA	R/W	000 0101 1111	11-bit, two's complement mantissa.

7.6.2.3.19 VIN_OV_FAULT_LIMIT (55h)

Format	Linear
Description	The VIN_OV_FAULT_LIMIT command sets the value of the input voltage that causes an input overvoltage fault condition. The default value is 14V. Upon triggering an input voltage fault, the following actions are taken: • Sets the OTHER bit in the STATUS_BYTE, • Sets the INPUT bit in the upper byte of the STATUS_WORD, • Sets the VIN_OV_FAULT bit in the STATUS_INPUT register, and • The device notifies the host (asserts PMB_ALERT).
Default	000Eh

Figure 50. VIN_OV_FAULT_LIMIT Register

15	14	13	12	11	10	9	8
VIN_OVF_EXPONENT					VIN_OVF_MANTISSA		
R/W					R/W		
7	6	5	4	3	2	1	0
VIN_OVF_MANTISSA							
R/W							

Table 30. VIN_OV_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	VIN_OVF_EXPONENT	R/W	0000 0	5-bit, two's complement exponent (scaling factor).
10-0	VIN_OVF_MANTISSA	R/W	000 0000 1110	11-bit, two's complement mantissa.

7.6.2.3.20 IIN_OC_FAULT_LIMIT (5Bh)

Format	Linear
Description	The IIN_OC_FAULT_LIMIT command sets the value of the input current, in amperes, that the causes an input overcurrent fault condition. Upon triggering the overcurrent fault, the following actions are taken: • Sets the OTHER bit in the STATUS_BYTE, • Sets the INPUT bit in the STATUS_WORD, • Sets the IIN_OC_FAULT bit in the STATUS_INPUT register, and • The device notifies the host (asserts PMB_ALERT).
Default	00FFh

Figure 51. IIN_OC_FAULT_LIMIT Register

15	14	13	12	11	10	9	8
INOCF_LIMIT_EXPONENT					INOCF_LIMIT_MANTISSA		
R/W					R/W		
7	6	5	4	3	2	1	0
INOCF_LIMIT_MANTISSA							
R/W							

Table 31. IIN_OC_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	INOCF_LIMIT_EXPONENT	R/W	0000 0	5-bit, two's complement exponent (scaling factor).
10-0	INOCF_LIMIT_MANTISSA	R/W	000 1111 1111	11-bit, two's complement mantissa.

7.6.2.3.21 IIN_OC_FAULT_RESPONSE (5Ch)

Format N/A

Description The IIN_OC_FAULT_RESPONSE instructs the device on what action to take in response to an input overcurrent fault. Upon triggering the input overcurrent fault, the controller is latched off, and the following actions are taken:

- Sets the OTHER bit in the STATUS_BYTE,
- Sets the INPUT bit in the STATUS_WORD,
- Sets the IIN_OC_FAULT bit in the STATUS_INPUT register, and
- The device notifies the host (asserts PMB_ALERT).

Default C0h

Figure 52. IIN_OC_FAULT_RESPONSE Register

7	6	5	4	3	2	1	0
IIN_OC_FAULT_RESPONSE							
R-1100 0000							

Table 32. IIN_OC_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IIN_OC_FAULT_RESPONSE	R	1100 0000	Upon triggering the input overcurrent fault, the device will shut down immediately (disables the output), and will not attempt to restart. The output then remains disabled until the fault is cleared.

7.6.2.3.22 IIN_OC_WARN_LIMIT (5Dh)

Format	Linear
Description	The IIN_OC_WARN_LIMIT command sets the value of the input current, in amperes, that causes the input overcurrent warning condition. The default setting is 255A. Upon triggering the overcurrent warning, the following actions are taken: • Sets the OTHER bit in the STATUS_BYTE, • Sets the INPUT bit in the STATUS_WORD, • Sets the IIN OC Warning bit in the STATUS_INPUT register, and • The device notifies the host (asserts PMB_ALERT).
Default	00FFh

Figure 53. IIN_OC_WARN_LIMIT Register

15	14	13	12	11	10	9	8
INOCW_LIMIT_EXPONENT					INOCW_LIMIT_MANTISSA		
R/W					R/W		
7	6	5	4	3	2	1	0
INOCW_LIMIT_MANTISSA							
R/W							

Table 33. IIN_OC_WARN_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	INOCW_LIMIT_EXPONENT	R/W	0000 0	5-bit, two's complement exponent (scaling factor).
10-0	INOCW_LIMIT_MANTISSA	R/W	000 1111 1111	11-bit, two's complement mantissa.

7.6.2.3.23 STATUS_BYTE (78h)

Format	N/A
Description	The STATUS_BYTE command returns a single byte of information with the a summary of critical faults. The STATUS_BYTE command is the same register as the low byte of the STATUS_WORD command. It should be noted that all faults and warnings except VIN_UV trigger the assertion of PMB_ALERT.
Default	Dependent on the Startup Condition

Figure 54. STATUS_BYTE Register

7	6	5	4	3	2	1	0
BUSY	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMP	CML	OTHER
R-0	R	R	R	R	R	R	R

Table 34. STATUS_BYTE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUSY	R	0	Not supported and always set to 0
6	OFF	R		This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. 0: Raw status indicating the IC is providing power to VOUT. 1: Raw status indicating the IC is not providing power to VOUT.
5	VOUT_OV	R		Output Over-Voltage Fault Condition 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault occurred
4	IOUT_OC	R		Output Over-Current Fault Condition 0: Latched flag indicating no IOUT OC fault has occurred. 1: Latched flag indicating an IOUT OC fault has occurred.
3	VIN_UV	R		Input Under-Voltage Fault Condition 0: Latched flag indicating VIN is above the UVLO threshold. 1: Latched flag indicating VIN is below the UVLO threshold.
2	TEMP	R		Over-Temperature Fault/Warning 0: Latched flag indicating no OT fault or warning has occurred. 1: Latched flag indicating an OT fault or warning has occurred.
1	CML	R		Communications, Memory or Logic Fault 0: Latched flag indicating no communication, memory, or logic fault has occurred. 1: Latched flag indicating a communication, memory, or logic fault has occurred.
0	OTHER	R		Other Fault This bit is used to flag faults not covered with the other bit faults. In this case, UVF or OCW faults are examples of other faults not covered by the bits [7:1] in this register. 0: No fault has occurred 1: A fault or warning not listed in bits [7:1] has occurred.

7.6.2.3.24 STATUS_WORD (78h)

Format	N/A
Description	The STATUS_WORD command returns two bytes of information with a summary of critical faults, such as over-voltage, overcurrent, over-temperature, etc. It should be noted that all faults and warnings except VIN_UV trigger the assertion of PMB_ALERT. **NOTE**: The STATUS_WORD low byte is the STATUS_BYTE.
Default	Dependent on the Startup Condition

Figure 55. STATUS_WORD Register

15	14	13	12	11	10	9	8
VOUT	IOUT	INPUT	MFR	PGOOD	FANS	OTHER	UNKNOWN
R	R	R	R	R	R-0	R-0	R-0
7	6	5	4	3	2	1	0
BUSY	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMP	CML	OTHER
R-0	R	R	R	R	R	R	R

Table 35. STATUS_WORD Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VOUT	R		Output Voltage Fault/Warning 0: Latched flag indicating no VOUT fault or warning has occurred. 1: Latched flag indicating a VOUT fault or warning has occurred.
14	IOUT	R		Output Current Fault/Warning 0: Latched flag indicating no IOUT fault or warning has occurred. 1: Latched flag indicating an IOUT fault or warning has occurred.
13	INPUT	R		Input Voltage/Current Fault/Warning 0: Latched flag indicating no VIN or IIN fault or warning has occurred. 1: Latched flag indicating a VIN or IIN fault or warning has occurred.
12	MFR	R		MFR_SPECIFIC Fault 0: Latched flag indicating no MFR_SPECIFIC fault has occurred. 1: Latched flag indicating a MFR_SPECIFIC fault has occurred.
11	PGOOD	R		Power Good Status 0: Raw status indicating VRRDY pin is at logic high. 1: Raw status indicating VRRDY pin is at logic low.
10	FANS	R	0	Not supported and always set to 0.
9	OTHER	R	0	Not supported and always set to 0.
8	UNKNOWN	R	0	Not supported and always set to 0.
7	BUSY	R	0	See information in Table 34
6	OFF	R		
5	VOUT_OV	R		
4	IOUT_OC	R		
3	VIN_UV	R		
2	TEMP	R		
1	CML	R		
0	OTHER	R		

7.6.2.3.25 STATUS_VOUT (7Ah)

Format	N/A
Description	The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults.
Default	Dependent on the Startup Condition

Figure 56. STATUS_VOUT Register

7	6	5	4	3	2	1	0
VOUT_OVF	VOUT_OVW	VOUT_UVW	VOUT_UVF	VOUT_MAXW	TON_MAX	TOFF_MAX	VOUT_TRACK
R	R-0	R-0	R	R	R-0	R-0	R-0

Table 36. STATUS_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VOUT_OVF	R		Output Over-Voltage Fault 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault has occurred.
6	VOUT_OVW	R	0	Not supported and always set to 0.
5	VOUT_UVW	R	0	Not supported and always set to 0.
4	VOUT_UVF	R		Output Under-Voltage Fault 0: Latched flag indicating no VOUT UV fault has occurred. 1: Latched flag indicating a VOUT UV fault has occurred.
3	VOUT_MAXW	R		Output Voltage Max Exceeded Warning 0: Latched flag indicating no VOUT_MAX warning has occurred. 1: Latched flag indicating that an attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX command.
2	TON_MAX	R	0	Not supported and always set to 0.
1	TOFF_MAX	R	0	Not supported and always set to 0.
0	VOUT_TRACK	R	0	Not supported and always set to 0.

7.6.2.3.26 STATUS_IOUT (7Bh)

Format	N/A
Description	The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults.
Default	Dependent on the Startup Condition

Figure 57. STATUS_IOUT Register

7	6	5	4	3	2	1	0
IOUT_OCF	IOUT_OCUVF	IOUT_OCW	IOUT_UCF	CUR_SHAREF	POW_LIMIT	POUT_OPF	POUT_OPW
R	R-0	R	R-0	R-0	R-0	R-0	R-0

Table 37. STATUS_IOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IOUT_OCF	R		Output Over-Current Fault 0: Latched flag indicating no IOUT OC fault has occurred. 1: Latched flag indicating a IOUT OC fault has occurred .
6	IOUT_OCUVF	R	0	Not supported and always set to 0.
5	IOUT_OCW	R		0: Latched flag indicating no IOUT OC warning has occurred 1: Latched flag indicating a IOUT OC warning has occurred
4	IOUT_UCF	R	0	Not supported and always set to 0.
3	CUR_SHAREF	R	0	Not supported and always set to 0.

Table 37. STATUS_IOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	POW_LIMIT	R	0	Not supported and always set to 0.
1	POUT_OPF	R	0	Not supported and always set to 0.
0	POUT_OPW	R	0	Not supported and always set to 0.

7.6.2.3.27 STATUS_INPUT (7Ch)

Format N/A

Description The STATUS_INPUT command returns one byte of information relating to the status of the converter's input voltage and current related faults.

Default Dependent on the Startup Condition

Figure 58. STATUS_INPUT Register

7	6	5	4	3	2	1	0
VIN_OVF	VIN_OVW	VIN_UVW	VIN_UVF	VIN_OFF	IIN_OCF	IIN_OCW	PIN_OPW
R	R-0	R-0	R	R-0	R	R	R-0

Table 38. STATUS_INPUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VIN_OVF	R		Input Over-Voltage Fault 0: Latched flag indicating no VIN OV fault has occurred. 1: Latched flag indicating a VIN OV fault has occurred.
6	VIN_OVW	R	0	Not supported and always set to 0.
5	VIN_UVW	R	0	Not supported and always set to 0.
4	VIN_UVF	R		Input Under-Voltage Fault 0: Latched flag indicating no VIN UV fault has occurred. 1: Latched flag indicating a VIN UV fault has occurred.
3	VIN_OFF	R	0	Not supported and always set to 0.
2	IIN_OCF	R		Input Over-Current Fault 0: Latched flag indicating no IIN OC fault has occurred. 1: Latched flag indicating a IIN OC fault has occurred.
1	IIN_OCW	R		Input Over-Current Warning 0: Latched flag indicating no IIN OC warning has occurred. 1: Latched flag indicating a IIN OC warning has occurred.
0	PIN_OPW	R	0	Not supported and always set to 0.

7.6.2.3.28 STATUS_TEMPERATURE (7Dh)

Format N/A

Description The STATUS_ TEMPERATURE command returns one byte of information relating to the status of the converter's temperature related faults.

Default Dependent on the Startup Condition

Figure 59. STATUS_TEMPERATURE Register

7	6	5	4	3	2	1	0
OTF	OTW	UTW	UTF	Reserved			
R	R	R-0	R-0	R-0000			

Table 39. STATUS_TEMPERATURE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OTF	R		Over-Temperature Fault 0: (Default) A temperature fault has not occurred. 1: A temperature fault has occurred.
6	OTW	R		Over-Temperature Warning 0: (Default) A temperature warning has not occurred. 1: A temperature warning has occurred.
5	UTW	R	0	Not supported and always set to 0.
4	UTF	R	0	Not supported and always set to 0.
3-0	Reserved	R	0000	Always set to 0.

7.6.2.3.29 STATUS_CML (7Eh)

Format	N/A
Description	The STATUS_ CML command returns one byte with contents regarding communication, logic, or memory conditions.
Default	Dependent on the Startup Condition

Figure 60. STATUS_CML Register

7	6	5	4	3	2	1	0
US_CMD	US_DATA	PEC_FAIL	Reserved	PRO_FAULT	Reserved	COM_FAIL	CML_OTHER
R	R	R	R-0	R-0	R-0	R	R-0

Table 40. STATUS_CML Register Field Descriptions

Bit	Field	Type	Reset	Description
7	US_CMD	R		Invalid or Unsupported Command Received 0: Latched flag indicating no invalid or unsupported command has received. 1: Latched flag indicating an invalid or unsupported command has received.
6	US_DATA	R		Invalid or Unsupported Data Received 0: Latched flag indicating no invalid or unsupported data has received. 1: Latched flag indicating an invalid or unsupported data has received.
5	PEC_FAIL	R		Packet Error Check Failed 0: Latched flag indicating no packet error check has failed 1: Latched flag indicating a packet error check has failed
4	Reserved	R	0	Always set to 0.
3	PRO_FAULT	R	0	Not supported and always set to 0.
2	Reserved	R	0	Always set to 0.
1	COM_FAIL	R		Other Communication Faults 0: Latched flag indicating no communication fault other than the ones listed in this table has occurred. 1: Latched flag indicating a communication fault other than the ones listed in this table has occurred.
0	CML_OTHER	R	0	Not supported and always set to 0.

7.6.2.3.30 STATUS_MFR_SPECIFIC (80h)

Format	N/A
Description	The STATUS_ MFR_SPECIFIC command returns one byte containing manufacturer-specific faults or warnings.
Default	Dependent on the Startup Condition

Figure 61. STATUS_MFR_SPECIFIC Register

7	6	5	4	3	2	1	0
MFR_FAULT_PS	MFR_PBF	TSEN_VREF	TSEN_GND	MFR_MAXPHW	Reserved		
R	R	R	R	R	R-000		

Table 41. STATUS_MFR_SPECIFIC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MFR_FAULT_PS	R		Power Stage Fault 0: Latched flag indicating no fault from TI power stage has occurred. 1: Latched flag indicating a fault from TI power stage has occurred.
6	MFR_PBF	R		Pre-OVP Fault 0: Latched flag indicating no pre-bias fault (Vout] 2.75V at startup) has occurred. 1: Latched flag indicating a pre-bias fault (Vout] 2.75V at startup) has occurred.
5	TSEN_VREF	R		0: Latched flag indicating that TSEN [1.55V before soft-start. 1: Latched flag indicating that TSEN]= 1.55V before soft-start.
4	TSEN_GND	R		0: Latched flag indicating that TSEN] 150mV before soft-start. 1: Latched flag indicating that TSEN [= 150mV before soft-start.
3	MFR_MAXPHW	R		Maximum Phase Warning If the selected operational phase number set in MFR_SPECIFIC_20[2:0] is larger than the maximum available phase number specified by the hardware, then MFR_MAXPHW is set, and the operational phase number is changed to the maximum available phase number. 0: Latched flag indicating no maximum phase warning has occurred. 1: Latched flag indicating a maximum phase warning has occurred.
2-0	Reserved	R	000	Always set to 0.

7.6.2.3.31 READ_VIN (88h)

Format	Linear
Description	The READ_VIN command returns the input voltage in volts.
Default	

Figure 62. READ_VIN Register

15	14	13	12	11	10	9	8
READ_VIN_EXPONENT					READ_VIN_MANTISSA		
R					R		
7	6	5	4	3	2	1	0
READ_VIN_MANTISSA							
R							

Table 42. READ_VIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	READ_VIN_EXPONENT	R		5-bit, two's complement exponent (scaling factor).
10-0	READ_VIN_MANTISSA	R		11-bit, two's complement mantissa.

7.6.2.3.32 READ_IIN (89h)

Format	Linear
Description	The READ_IIN command returns the input current in amperes.
Default	

Figure 63. READ_IIN Register

15	14	13	12	11	10	9	8
READ_IIN_EXPONENT					READ_IIN_MANTISSA		
R					R		
7	6	5	4	3	2	1	0
READ_IIN_MANTISSA							
R							

Table 43. READ_IIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	READ_IIN_EXPONENT	R		5-bit, two's complement exponent (scaling factor).
10-0	READ_IIN_MANTISSA	R		11-bit, two's complement mantissa.

7.6.2.3.33 READ_VOUT (8Bh)

Format VID

Description The READ_VOUT command returns the actual, measured output voltage.

Default

Figure 64. READ_VOUT Register

15	14	13	12	11	10	9	8
READ_VOUT_VID							
R							
7	6	5	4	3	2	1	0
READ_VOUT_VID							
R							

Table 44. READ_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	READ_VOUT_VID	R		16-bit, VID format

7.6.2.3.34 READ_IOUT (8Ch)

Format Linear

Description The READ_IOUT command returns the output current in amperes.

Default

Figure 65. READ_IOUT Register

15	14	13	12	11	10	9	8
READ_IOUT_EXPONENT					READ_IOUT_MANTISSA		
R					R		
7	6	5	4	3	2	1	0
READ_IOUT_MANTISSA							
R							

Table 45. READ_IOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	READ_IOUT_EXPONENT	R		5-bit, two's complement exponent (scaling factor).
10-0	READ_IOUT_MANTISSA	R		11-bit, two's complement mantissa.

7.6.2.3.35 READ_TEMPERATURE_1 (8Dh)

Format	Linear
Description	The READ_TEMPERATURE_1 command returns the temperature in degrees Celsius (°C).
Default	

Figure 66. READ_TEMPERATURE_1 Register

15	14	13	12	11	10	9	8
READ_TEMP_1_EXPONENT					READ_TEMP_1_MANTISSA		
R					R		
7	6	5	4	3	2	1	0
READ_TEMP_1_MANTISSA							
R							

Table 46. READ_TEMPERATURE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	READ_TEMP_1_EXPONENT	R		5-bit, two's complement exponent (scaling factor).
10-0	READ_TEMP_1_MANTISSA	R		11-bit, two's complement mantissa.

7.6.2.3.36 READ_POUT (96h)

Format	Linear
Description	The READ_POUT command returns the output power in watts.
Default	

Figure 67. READ_POUT Register

15	14	13	12	11	10	9	8
READ_POUT_EXPONENT					READ_POUT_MANTISSA		
R					R		
7	6	5	4	3	2	1	0
READ_POUT_MANTISSA							
R							

Table 47. READ_POUT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	READ_POUT_EXPONENT	R		5-bit, two's complement exponent (scaling factor).
10-0	READ_POUT_MANTISSA	R		11-bit, two's complement mantissa.

7.6.2.3.37 READ_PIN (97h)

Format Linear

Description The READ_PIN command returns the output power in watts.

Default

Figure 68. READ_PIN Register

15	14	13	12	11	10	9	8
READ_PIN_EXPONENT					READ_PIN_MANTISSA		
R					R		
7	6	5	4	3	2	1	0
READ_PIN_MANTISSA							
R							

Table 48. READ_PIN Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	READ_PIN_EXPONENT	R		5-bit, two's complement exponent (scaling factor).
10-0	READ_PIN_MANTISSA	R		11-bit, two's complement mantissa.

7.6.2.3.38 PMBus_REVISION (98h)

Format N/A

Description The PMBus_REVISION command returns the revision of the PMBus to which the device is compliant.

Default 11h

Figure 69. PMBus_REVISION Register

7	6	5	4	3	2	1	0
PMBUS_REV							
R-0001 0001							

Table 49. PMBus_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PMBUS_REV	R	0001 0001	Compliant to revision 1.1 of the PMBus specification.

7.6.2.3.39 MFR_ID (99h)

Format N/A

Description The MFR_ID command loads the unit with the text character that contains the manufacturer's ID. This is typically done once at the time of manufacture.

Default 54h

Figure 70. MFR_ID Register

7	6	5	4	3	2	1	0
MFR_ID							
R-0101 0100							

Table 50. MFR_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MFR_ID	R	0101 0100	Loads the unit with the text character that contains the manufacturer's ID.

7.6.2.3.40 MFR_MODEL (9Ah)

Format N/A

Description The MFR_MODEL command loads the unit with the text character that contains the model number of the manufacturer. This is typically done once at the time of manufacture.

Default 35h

Figure 71. MFR_MODEL Register

7	6	5	4	3	2	1	0
MFR_MODEL							
R-011 0101							

Table 51. MFR_MODEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MFR_MODEL	R	0011 0101	Loads the unit with the text character that contains the model number of the manufacturer.

7.6.2.3.41 MFR_REVISION (9Bh)

Format N/A

Description The MFR_REVISION ocmmand loads the unit with the text character that contains the revision number of the manufacturer. This is typically done once at the time of manufacture.

Default

Figure 72. MFR_REVISION Register

7	6	5	4	3	2	1	0
MFR_REVISION							
R							

Table 52. MFR_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MFR_REVISION	R		Loads the unit with the text character that contains the revision number of the manufacturer.

7.6.2.3.42 MFR_SPECIFIC_02 (SVID/PMBus Control) (D2h)

Format N/A

Description The MFR_SPECIFIC_02 command selects SVID or PMBus to control the output voltage. This register defaults to 0x02 – SVID bus has control of Vout. Writing 0x01 to this register enables PMBus control of Vout. With PMBus control, absolute VID is controlled by writing a VID word to VOUT_COMMAND (0x21).

SVID Bus behavior during PMBus control:

- No SetVID command is expected from SVID when PMBus is enabled to control VOUT.

PMBus controlled VOUT changes:

- Changes in VOUT initiated by PMBus control should use fast slew rate - similar to SetVID fast.

Default 02h

Figure 73. MFR_SPECIFIC_02 (SVID/PMBus Control) Register

7	6	5	4	3	2	1	0
Reserved						SVID_PMBUS_SEL	
R-00 0000						R/W	

Table 53. MFR_SPECIFIC_02 (SVID/PMBus Control) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R	00 0000	Always set to 0.
1-0	SVID_PMBUS_SEL	R/W	10	SVID or PMBus VOUT Control 00: Reserved. 01: PMBUS controls VOUT, and SVID cannot change VOUT. 10: PMBus cannot change VOUT, and SVID controls VOUT. 11: Reserved.

7.6.2.3.43 MFR_SPECIFIC_04 (Read VOUT) (D4h)

Format Linear

Description The MFR_SPECIFIC_04 command returns the actual, measured output voltage in volts.

Default

Figure 74. MFR_SPECIFIC_04 (Read VOUT) Register

15	14	13	12	11	10	9	8
MFR_SPEC_04_MANTISSA							
R							
7	6	5	4	3	2	1	0
MFR_SPEC_04_MANTISSA							
R							

Table 54. MFR_SPECIFIC_04 (Read VOUT) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MFR_SPEC_04_MANTISSA	R		Unsigned 16-bit mantissa with an exponent value of n=-9.

7.6.2.3.44 MFR_SPECIFIC_05 (VOUT Trim) (D5h)

Format	Signed Two's Complement
Description	The MFR_SPECIFIC_05 command is used to trim the VR output voltage in volts. LSB resolution is 5mV/10mV based on the selected VR12.0/VR12.5.
Default	00h

Figure 75. MFR_SPECIFIC_05 (VOUT Trim) Register

7	6	5	4	3	2	1	0
VOUT_TRIM							
R/W							

Table 55. MFR_SPECIFIC_05 (VOUT Trim) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VOUT_TRIM	R/W	0000 0000	Sets the VR output trim voltage. 0111 1111: 0.635 V in VR12.0 and 1.27V in VR12.5 0111 1110: 0.630 V in VR12.0 and 1.26 V in VR12.5 ..... 0000 0001: 0.005 V in VR12.0 and 0.01 V in VR12.5 0000 0000: 0 V 1111 1111: –0.005 V in VR12.0 and –0.01 V in VR12.5 ..... 1000 0001: –0.635 V in VR12.0 and –1.27 V in VR12.5 1000 0000: –0.640 V in VR12.0 and –1.28 V in VR12.5

7.6.2.3.45 MFR_SPECIFIC_08 (Droop) (D8h)

Format	N/A
Description	The MFR_SPECIFIC_08 command sets the load line as percentage of the default one. For example, if slope is set as 1mohm = 100%, then 0.5mohm = 50%
Default	04h

Figure 76. MFR_SPECIFIC_08 (Droop) Register

7	6	5	4	3	2	1	0
DROOP							
R/W							

Table 56. MFR_SPECIFIC_08 (Droop) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DROOP	R/W	0000 0100	0000 0000: 0% 0000 0001: 25% 0000 0010: 50% 0000 0011: 75% 0000 0100: 100% 0001 0000: 80% 0010 0000: 85% 0011 0000: 90% 0100 0000: 95% 0101 0000: 105% 0110 0000: 110% 0111 0000: 115% 1000 0000: 120% 1001 0000: 125% 1010 0000: 150% Others: 100%

7.6.2.3.46 MFR_SPECIFIC_09 (OSR/USR) (D9h)

Format	N/A
Description	The MFR_SPECIFIC_09 command sets the threshold for OSR and USR control. The setting can override the default setting from the O-USR pin.
Default	O-USR pin

Figure 77. MFR_SPECIFIC_09 (OSR/USR) Register

7	6	5	4	3	2	1	0
Reserved	USR			Reserved	OSR		
R-0	R/W			R-0	R/W		

Table 57. MFR_SPECIFIC_09 (OSR/USR) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0	Always set to 0.
6-4	USR	R/W		Undershoot Reduction 000: 15 mV 001: 25 mV 010: 35 mV 011: 55 mV 100: 75 mV 101: 95 mV 110: 115 mV 111: USR off
3	Reserved	R	0	Always set to 0.
2-0	OSR	R/W		Overshoot Reduction 000: 25 mV 001: 35 mV 010: 45 mV 011: 65 mV 100: 85 mV 101: 105 mV 110: 125 mV 111: OSR off

7.6.2.3.47 MFR_SPECIFIC_10 (Maximum Operating Current) (DAh)

Format	N/A
Description	The MFR_SPECIFIC_10 command sets the maximum operating current (IMAX, unit: A) of the converter. The setting can override the default setting from the F-IMAX pin
Default	F-IMAX pin

Figure 78. MFR_SPECIFIC_10 (Maximum Operating Current) Register

7	6	5	4	3	2	1	0
IMAX							
R/W							

Table 58. MFR_SPECIFIC_10 (Maximum Operating Current) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IMAX	R/W		Set maximum operating current. The value in hexadecimal is directly converted to the decimal IMAX equivalent.

7.6.2.3.48 MFR_SPECIFIC_11 (VBOOT) (DBh)

Format	VID
Description	The MFR_SPECIFIC_11 command sets the boot voltage in 8-bit VID format. The data byte contains of a right-justified VID code with VID0 in bit 0 of the lower data byte, VID1 in bit 1 of the lower byte and so forth. The VID table mapping is determined by the selected SVID protocols from SLEW_MODE or MFR_SPECIFIC_13. The setting can override the default setting from the B-TMAXR pin.
Default	B-TMAXR pin

Figure 79. MFR_SPECIFIC_11 (VBOOT) Register

7	6	5	4	3	2	1	0
VBOOT							
R/W							

Table 59. MFR_SPECIFIC_11 (VBOOT) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VBOOT	R/W		Set the boot voltage according to the selected VID table.

7.6.2.3.49 MFR_SPECIFIC_12 (Switching Frequency and Maximum Operating Temperature) (DCh)

Format N/A

Description The MFR_SPECIFIC_12 command sets the switching frequency and the maximum operating temperature (TMAX). The settings can override the default setting from the F-IMAX, and B-TMAXR pins.

Default F-IMAX and B-TMAXR pins

Figure 80. MFR_SPECIFIC_12 (Switching Frequency and Maximum Operating Temperature) Register

7	6	5	4	3	2	1	0
Reserved	FSW			Reserved	TMAX		
R-0	R/W			R-0	R/W		

Table 60. MFR_SPECIFIC_12 (Switching Frequency and Maximum Operating Temperature) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0	Always set to 0.
6-4	FSW	R/W		Switching Frequency 000: 300 kHz 001: 400 kHz 010: 500 kHz 011: 600 kHz 100: 700 kHz 101: 800 kHz 110: 900 kHz 111: 1 MHz
3	Reserved	R	0	Always set to 0.
2-0	TMAX	R/W		Maximum Temperature 000: 90°C 001: 95°C 010: 100°C 011: 105°C 100: 110C 101: 115°C 110: 120°C 111: 125°C

7.6.2.3.50 MFR_SPECIFIC_13 (Slew Rate and Other Operation Modes) (DDh)

Format N/A

Description The MFR_SPECIFIC_13 command sets the slew rates and the operation modes. The settings can override the default setting from the SLEW-MODE pin.

Default SLEW-MODE pin

Figure 81. MFR_SPECIFIC_13 (Slew Rate and Other Operation Modes) Register

7	6	5	4	3	2	1	0
VR12_MODE	PI_SET	TEMPCOMP_EN	DPS_EN	ZLL_SET	Reserved	SLEW	
R/W	R-0	R/W	R/W	R/W	R-0	R/W	

Table 61. MFR_SPECIFIC_13 (Slew Rate and Other Operation Modes) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VR12_MODE	R/W		VR12 Mode 0: VR12.5. 1: VR12.0.
6	PI_SET	R/W	0	0: 4-phase individual interleaving 1: 1/3 and 2/4-phase interleaving
5	TEMPCOMP_EN	R/W		Temperature Compensation Enable 0: Disable temperature compensation for IMON and OCL. 1: Enable temperature compensation for IMON and OCL.
4	DPS_EN	R/W		Dynamic Phase Shedding Enable 0: Disable dynamic phase shedding. 1: Enable dynamic phase shedding.
3	ZLL_SET	R/W		Load Line 0: Non-zero load line 1: Zero load line
2	Reserved	R	0	Always set to 0.
1-0	SLEW	R/W		Slew Rate for SetVID Fast 00: 5 mV/us 01:10 mV/us 10: 15 mV/us 11: 20 mV/us

7.6.2.3.51 MFR_SPECIFIC_14 (Ramp Height) (DEh)

Format N/A

Description The MFR_SPECIFIC_14 command sets the ramp amplitude for compensation. The settings can override the default setting from the B-TMAXR and $\overline{\text{SKIP}}$-RAMP pins.

Default B-TMAXR and $\overline{\text{SKIP}}$-RAMP pins

Figure 82. MFR_SPECIFIC_14 Register

7	6	5	4	3	2	1	0
RAMP							
R/W							

Table 62. MFR_SPECIFIC_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RAMP	R/W		Ramp Amplitude 000: 20 mV_{PP} 001: 40 mV_{PP} 010: 60 mV_{PP} 011: 80 mV_{PP} 100: 100 mV_{PP} 101: 120 mV_{PP} 110: 150 mV_{PP} 111: 200 mV_{PP}

7.6.2.3.52 MFR_SPECIFIC_15 (Dynamic Phase Shedding Thresholds) (DFh)

Format N/A

Description The MFR_SPECIFIC_15 command sets the threshold of the dynamic phase shedding as a percentage. 100% is defined as 4 times of the selected overcurrent limit (OCL) level, which is set by OCL pin.

Default 00h

Figure 83. MFR_SPECIFIC_15 (Dynamic Phase Shedding Thresholds) Register

7	6	5	4	3	2	1	0
Reserved				DPS_TH_LOW	DPS_TH_HIGH		
R-0000				R/W	R/W		

Table 63. MFR_SPECIFIC_15 (Dynamic Phase Shedding Thresholds) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R	0000	Always set to 0.
3	DPS_TH_LOW	R/W	0	Switch from 2 Phase to 1 Phase Operation 0: Disable decreasing to 1 phase operation. 1: 10% load.
2-0	DPS_TH_HIGH	R/W	000	Switch from Maximum Phase to 2 Phase Operation 000: 15% load. 001: 20% load. 010: 25% load. 011: 30% load. Others: 35% load.

7.6.2.3.53 MFR_SPECIFIC_16 (VIN UVLO) (E0h)

Format N/A

Description The MFR_SPECIFIC_16 command sets the threshold for the Vin Undervoltage Lockout (UVLO).

Default 00h

Figure 84. MFR_SPECIFIC_16 (VIN UVLO) Register

7	6	5	4	3	2	1	0
Reserved						VIN_UVLO	
R-00 0000						R/W	

Table 64. MFR_SPECIFIC_16 (VIN UVLO) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R	00 0000	Always set to 0.
1-0	VIN_UVLO	R/W	00	Input Voltage UVLO 00: 4.3 V 01: 6.0 V 10: 8.0 V 11: 9.9 V

7.6.2.3.54 MFR_SPECIFIC_18 (Telemetry Averaging Time) (E2h)

Format

Description The MFR_SPECIFIC_18 command sets the averaging time for telemetry reporting.

Default 50h

Figure 85. MFR_SPECIFIC_18 (Telemetry Averaging Time) Register

7	6	5	4	3	2	1	0
Reserved	FILTER_PIN			Reserved		FILTER_IV	
R-0	R/W			R-00		R/W	

Table 65. MFR_SPECIFIC_18 (Telemetry Averaging Time) Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0	Always set to 0.
6-4	FILTER_PIN	R/W	101	Averaging Time for Input Power Reporting 000: Bypass. 001: 4 ms 010: 11 m 011: 23 m 100: 38 ms 101: 100 ms 110: 200 ms 111: 450 ms
3-2	Reserved	R	00	Always set to 0.
1-0	FILTER_IV	R/W	00	Averaging Time for Current and Voltage Reporting 00: Bypass. 01: 2 ms 10: 4 ms 11: 10 ms

7.6.2.3.55 MFR_SPECIFIC_20 (Maximum Operational Phase Number) (E4h)

Format N/A

Description The MFR_SPECIFIC_20 command sets the maximum operational phase numbers on-the-fly. If the maximum operational phase number is set higher than the available phase numbers specified by hardware, then the operational phase number remains unchanged, and the STAUTS_MFR_SPECIFIC[3] is set while asserting PMB_ALERT.

Default Hardware Specific

Figure 86. MFR_SPECIFIC_20 (Maximum Operational Phase Number) Register

7	6	5	4	3	2	1	0
Reserved						PHASE_NUM	
R-0 0000						R/W	

Table 66. MFR_SPECIFIC_20 (Maximum Operational Phase Number) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R	0 0000	Always set to 0.
2-0	PHASE_NUM	R/W		Phase Number 000: 1-phase operation. 001: 2-phase operation. 010: 3-phase operation. 011: 4-phase operation. Others: 4-phase operation, but will assert STATUS_MFR_SPECIFIC[3] and PMB_ALERT.

7.6.2.3.56 MFR_SPECIFIC_44 (DEVICE_CODE) (FCh)

Format

Description The MFR_SPECIFIC_44 command reads back the DEVICE_CODE information.

Default 00D3h

Figure 87. MFR_SPECIFIC_44 (DEVICE_CODE) Register

15	14	13	12	11	10	9	8
DEVICE_CODE							
R							
7	6	5	4	3	2	1	0
DEVICE_CODE							
R							

Table 67. MFR_SPECIFIC_44 (DEVICE_CODE) Register Field Descriptions

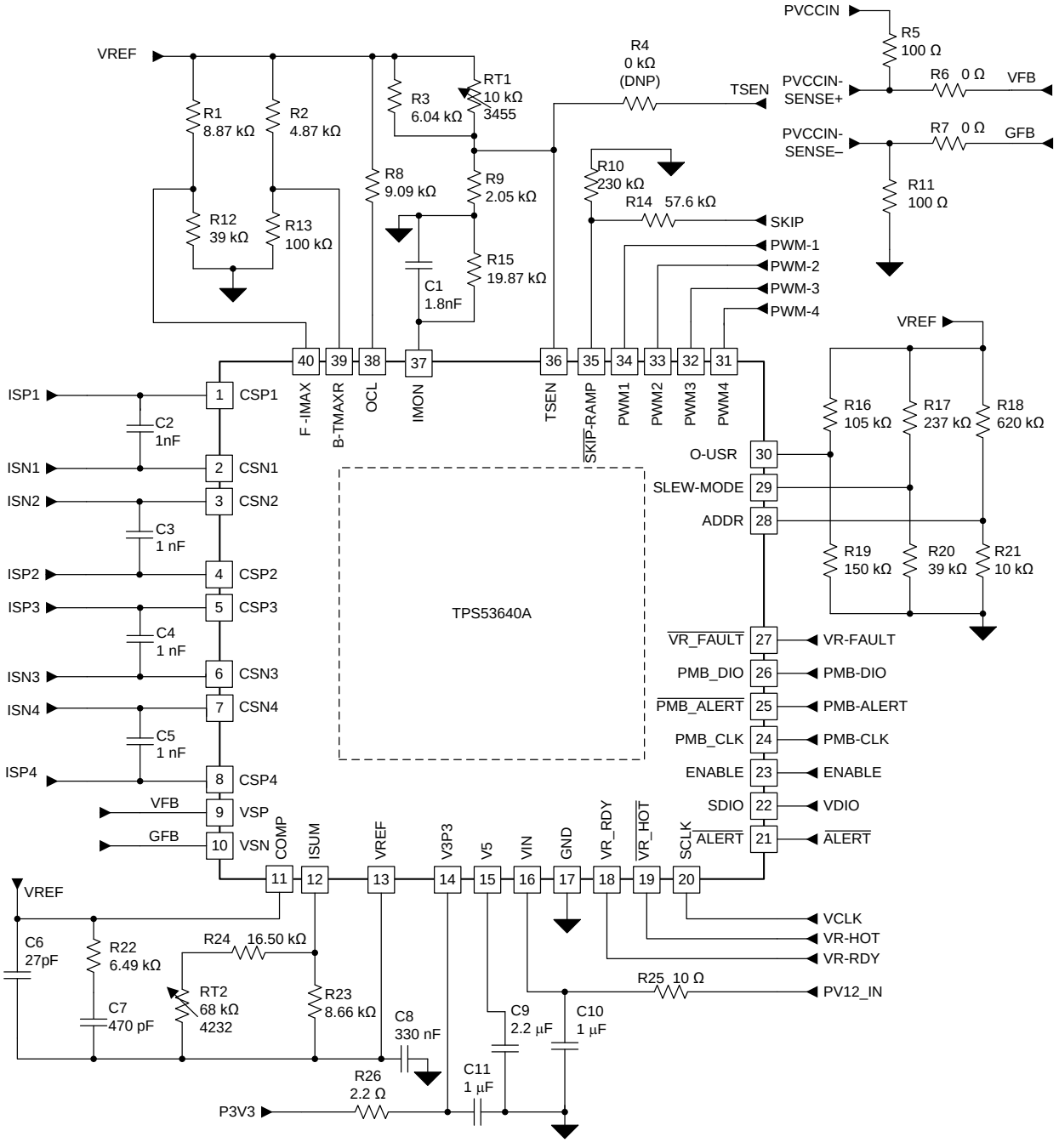
Bit	Field	Type	Reset	Description
15-0	DEVICE_CODE	R	0000 0000 1101 0011	Device Code

8 Application and Implementation

8.1 Application Information

The TPS53640A device has a very simple design procedure. Please contact your local TI representative to get a copy of the TI design tool spreadsheet. This design uses the Intel Grantley Platform 160-W CPU VR.

8.2 Typical Application



Place resistors RT1 and RT2 near the 1-phase inductor, L1.

Figure 88. 4-Phase, VR12.5 Grantley Platform 160-W CPU

Typical Application (continued)

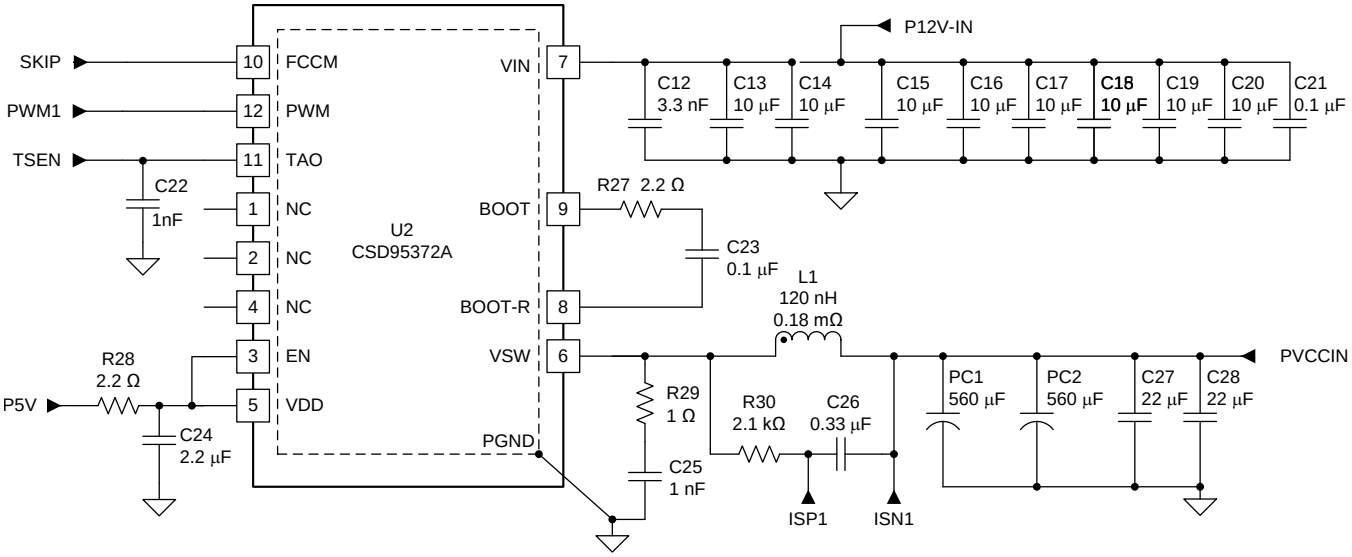


Figure 89. Power Stage U2

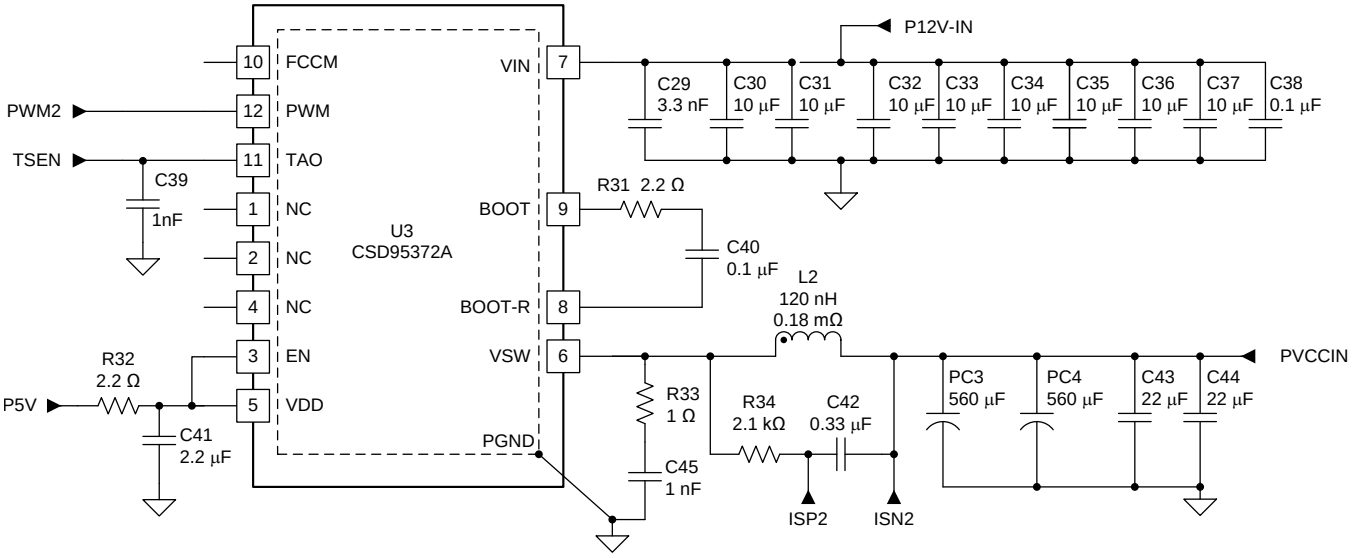


Figure 90. Power Stage U3

Typical Application (continued)

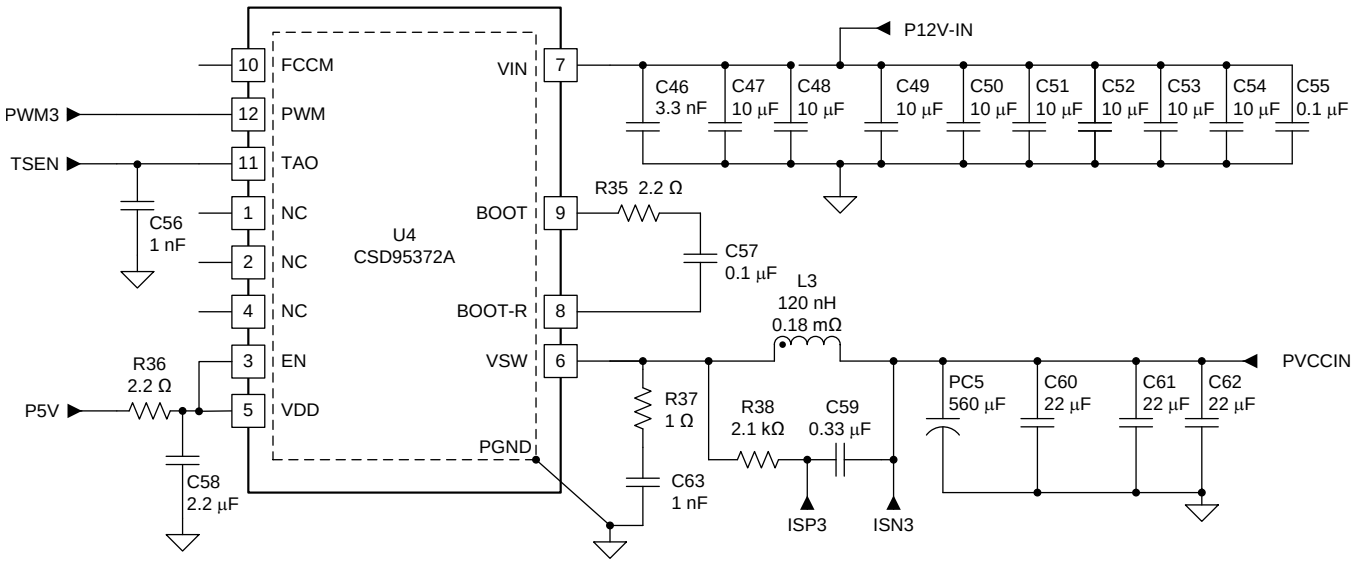


Figure 91. Power Stage U4

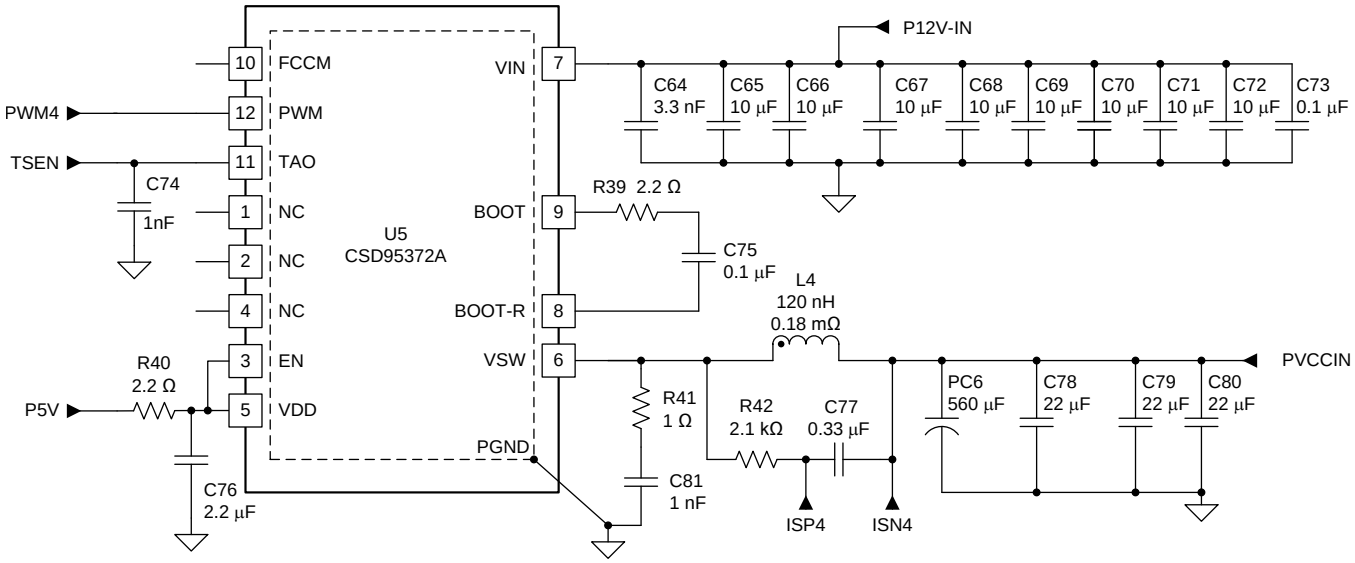


Figure 92. Power Stage U5

Typical Application (continued)

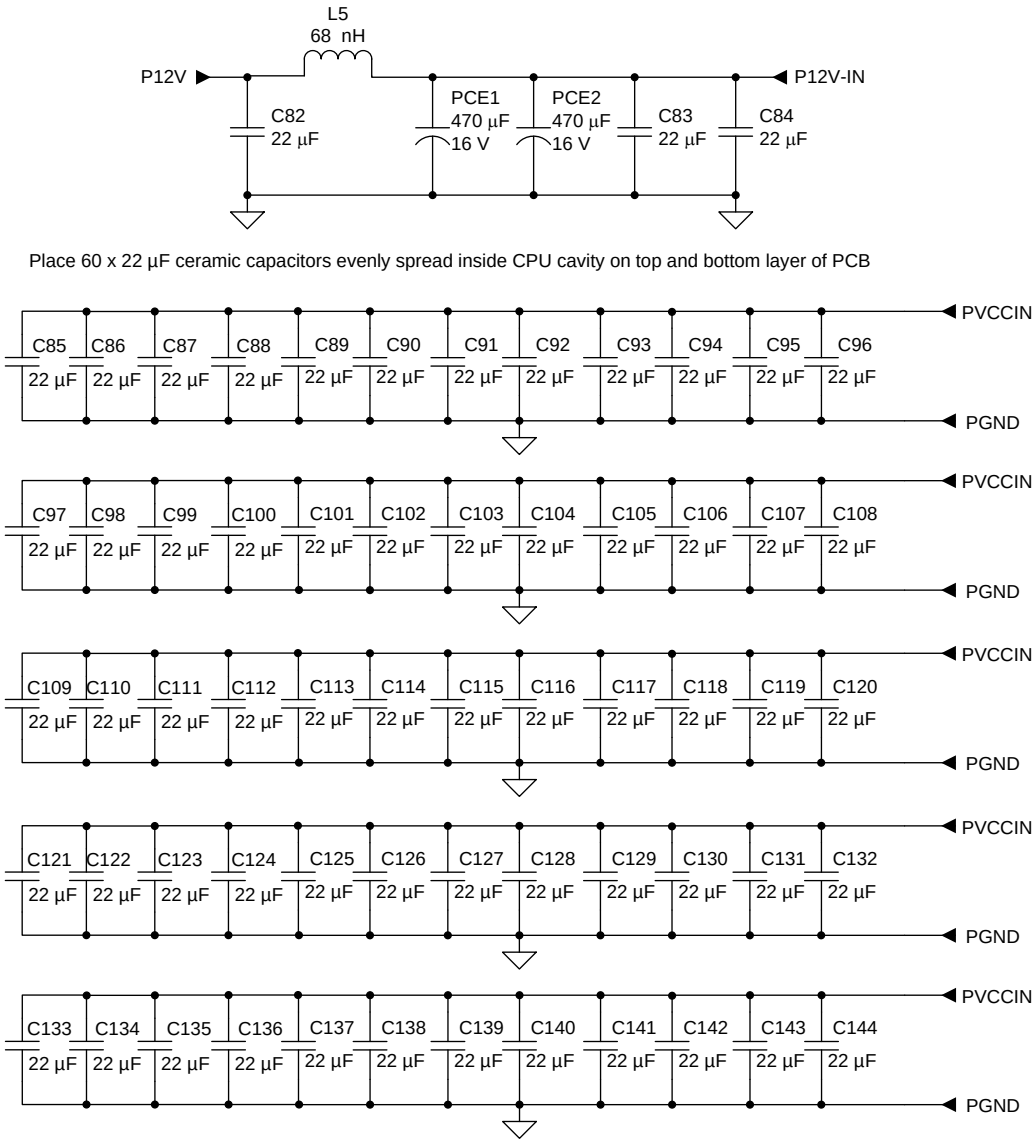


Figure 93. Power Stage Filter

8.2.1 Design Requirements

- VR12.5, Grantley Platform, 160-W CPU
- Number of phases 4
- Input Voltage 10.8 V to 13.2 V
- VID_PS0 (0A): 1.8 V
- $I_{CC(tdc)}$: 97 A
- $I_{CC(max)}$: 208 A
- $I_{DYN(max)}$: 158 A
- Load-line: 1.05 mΩ
- Fast Slew Rate (min.): 20 mV/µs
- Boot Voltage, V_{BOOT}: 1.7 V
- Maximum temperature, T_{MAX}: 120°C
- SVID Address: 00h

Typical Application (continued)

- PMBus Address: 60h

8.2.2 Detailed Design Procedure

8.2.2.1 Step One: Select Switching Frequency

The value of a resistor (R_F) between the F-IMAX pin and GND selects the switching frequency. The frequency is an approximate frequency and is expected to vary based on load and input voltage.

Table 68. Frequency Selection Table

SELECTION RESISTOR (R_F) VALUE (kΩ)	OPERATING FREQUENCY (f_{SW}) (kHz)
20	300
24	400
30	500
39	**600**
56	700
75	800
100	900
150	1000

For this design, choose 600 kHz for the switching frequency. So, R_F = 39 kΩ.

8.2.2.2 Step Two: Set the Maximum Processor Current ($I_{CC(max)}$)

The voltage on the F-IMAX pin sets the maximum processor current from the value of the resistors connected from the VREF pin to the F-IMAX pin (R_{IMAX}). Equation 7 shows the maximum processor current calculation.

$$R_{IMAX} = \frac{R_F \times \left(255 - I_{CC(max)}\right)}{I_{CC(max)}} \quad (7)$$

From Table 68, R_F = 39 kΩ. Therefore R_{MAX} = 8.813 kΩ. The closest standard resistance value is 8.06 kΩ.

8.2.2.3 Step Three: Select the VID Offset and Fast Slew Rate

The VID offset is 0 mV for this design. The resistor (R_{SLEW}) (connected between the SLEW-MODE pin and GND) sets the slew rate. Table 69 show a summary of these settings. For a minimum 20-mV/µs slew rate, the resistor R_{SLEW} = 39 kΩ.

Table 69. Slew Rate Selection

SELECTION RESISTOR R_{SLEW} (kΩ)	MINIMUM SLEW RATE (mV/µs)	OFFSET (VID STEP) (mV)
20	5	0
24	10	
30	15	
39	20	
56	5	+20
75	10	
100	15	
150	20	

8.2.2.4 Step Four: Select the Operation Mode

The resistor (R_{MODE}) is connected between the VREF pin and the SLEW-MODE pin. After selecting the value of R_{SLEW}, set the operation mode by choosing the voltage on the SLEW-MODE pin as summarized in Table 70 and the *Electrical Characteristics* table. In this design, VR 12.5 mode is selected with disabling dynamic phase shedding, and non-zero load line. From the *Step Three: Select the VID Offset and Fast Slew Rate* section, use the values R_{SLEW} = 39 kΩ, so R_{MODE} = 237 kΩ to select the desired operating modes.

Table 70. Operation Mode v.s Resistor Selection

OPERATION MODES			BIT DESCRIPTION
Mode bit M4	MFR_SPEC_13[7]	$VR12_{MODE}$	**0: VR12.5**
			1: VR12.0
Mode bit M2	MFR_SPEC_13[5]	$TEMPCOMP_{EN}$	0: Disable temperature compensation for IMON and OCL
			1: Enable temperature compensation for IMON and OCL
Mode bit M1	MFR_SPEC_13[4]	DPS_{EN}	**0: Disable dynamic phase shedding**
			1: Enable dynamic phase shedding
Mode bit M0	MFR_SPEC_13[3]	ZLL_{SET}	**0: Non-zero load line**
			1: Zero load line

8.2.2.5 Step Five: Select the Inductor

Smaller values of inductor have better transient performance but higher ripple and lower efficiency. Higher values have the opposite characteristics. It is common practice to limit the ripple current to 20% to 40% of the maximum per-phase current. In this design example, 30% of the maximum per-phase current is used.

$$I_{P-P} = \left(\frac{I_{CC(max)}}{n}\right) \times \%ripple = \left(\frac{208\,A}{4}\right) \times 0.30 = 15.6\,A \tag{8}$$

$$L = \frac{V \times dT}{I_{P-P}} = \frac{\left[V_{IN(max)} - V_{CORE}\right] \times \frac{V_{CORE}}{\left[f_{SW} \times V_{IN(max)}\right]}}{I_{P-P}} = \frac{11.4\,V \times 227\,ns}{15.6\,A} = 165\,nH \tag{9}$$

Considering the transient performance requirement, this example uses an inductor with a specification of 120 nH and 0.180 mΩ.

8.2.2.6 Step Six: Select the Per-Phase Valley Current Limit

As described generally in the *Overcurrent Limit (OCL)* section, the resistor (R_{OCL}) from the OCL pin to the VREF pin selects the per-phase valley current limit. The required protection current level with reference to inductor saturation limit can be transformed to OCL pin resistor as shown in Equation 10.

$$I_{OCL} = K \times \left(\frac{I_{CC(max)}}{n}\right) - \left(\frac{I_{RIPPLE}}{2}\right) = 150\% \times \left(\frac{208}{4}\right) - \left(\frac{15.6}{2}\right) = 70.2\,A \tag{10}$$

where

- K is the maximum operating margin
- $I_{CC(max)}$ is the maximum processor current
- I_{RIPPLE} is the ripple current
- n is the number of phases

The selected inductor with a value of 120 nH and saturation current of I_{SAT} = 70.2 + 15.6 = 85.8 A. This saturation current level can be used to raise the OCL level so that during transient and dynamic VID operations, no OCL event impacts converter operation. So the I_{OCL} is selected to be 70.2 A to use in the OCL resistor calculation in Equation 11.

$$R_{OCL} = I_{OCL} \times R_{DCR} \times \frac{Gain}{10\,\mu A} = 70.2 \times 0.18\,m\Omega \times \frac{6}{10\,\mu A} = 7.5\,k\Omega$$

where

- R_{DCR} is the inductor DCR resistance
- Gain is the current sensing gain
- 10 µA is the OCL sourcing current when enabling temperature compensation (11)

So the inductor used in application should have a saturation current level of I_{SAT} > 85 A.

8.2.2.7 Step Seven: Select R_{ADDR} for Corresponding SVID and PMBus Address

Calculate the value of the resistor to be placed between the ADDR pin and GND.

Table 71. ADDR Pin Resistor Guide for Standard SVID and PMBUS Addresses

VR NAME	SVID	PMBus ADDRESS	RESISTOR TO	
			GND (R_{SVID}) (kΩ)	VREF (R_{PMBUS}) (kΩ)
VCCIN-CPU0	00h	60h	10	118
VCCIN-CPU1	00h	60h	10	118

The slave address of the TPS53640A device must be set in order to communicate with CPUs or other system controllers via SVID or PMBus interfaces. The TPS53640A device supports both SVID and PMBus interfaces, and the slave addresses for both interfaces can be set separately. The resistor R_{SVID}, connected between the ADDR pin and GND sets the lower three bits of the SVID address based on the EC Table. After R_{SVID} is selected, set the the highest one bit of the SVID address and four-bits of the PMBus address. THese address can be set by the voltage on ADDR pin with the resistor, $R_{S\text{-}PMBus}$, based on the values shown in the *Electrical Characteristics* table.

The values for this design example are

- R_{SVID} = 10 kΩ
- R_{PMBus} = 620 kΩ

These values correspond to 000 as the SVID address and 1100000 as the PMBus address.

8.2.2.7.1 SVID Use Instructions

The SVID bus pins (SCLK, SDIO, and $\overline{\text{ALERT}}$) are all open drain and require appropriate pull-up resistence from the VCCIO voltage rail. Consult the complete SVID bus schematic and layout guide that are available in the Intel PDG document. The $\overline{\text{VR-HOT}}$ is a signal common to the Intel processor and therefore the same PDG instruction should be followed.

8.2.2.7.2 PMBus Use Instructions

The PMBus pins (PMB_CLK, PMB_DIO, and PMB_ALERT) are all open-drain and require a 10-kΩ pull-up resistor on the P3V3 rail to function as a connector suitable for PMBus hardware HPA172 (USB-to-Serial) converter.

8.2.2.7.3 Programming the Device via PMBus

Because all of the settings can be configured externally using resistors, programming the device using the PMBus interface is optional. However, the system controller can override the configurations or can program the device to change the operation modes via the PMBus interface. Refer to Supported PMBus Commands which summarizes the supported PMBus commands to assist in firmware development.

8.2.2.8 Step Eight: Calculate the Required Load-Line Resistance

The load line is set by the resistor, R_{ISUM}, that is placed between the ISUM pin and the VREF pin.

$$R_{ISUM} = R_{LL} \times \frac{1}{g_{M(isum)} \times R_{DCR} \times A_{CS}} = 1.05\,m\Omega \times \frac{1}{0.5\,mS \times 0.18\,m\Omega \times 1.5} = 7.87\,k\Omega$$

where

- R_{LL} is the desired load line
- $g_{M(isum)}$ is the ISUM amplifier transconductance

- R_{DCR} is the inductor DCR resistance
- A_{CS} is the current sensing gain from inductor DCR sense voltage signal (12)

Because the sensed current from inductor DCR is not temperature-compensated, this design requires an NTC network in order to complete a simple application circuit. Using the TI Design Tool, first select the NTC resistor and then calculate the series and parallel compensation resistor for the NTC which actually divides the calculated R_{ISUM} value. In this example a NTC of 68 kΩ-4232 is used and the series and parallel resistors are 16.5 kΩ and 8.66 kΩ, respectively.

8.2.2.9 Step Nine: Set the BOOT Voltage

A resistor (R_{BOOT}) connected between the B-TMAXR pin and GND, sets the BOOT voltage as shown inTable 72. BOOT voltage selection also depends on the operation mode selected as described in the *Step Four: Select the Operation Mode* section. For this design example, select 1.7 V as the BOOT voltage for VR12.5 mode operation, therefore R_{BOOT} = 100 kΩ.

Table 72. Boot Voltage Resistor Selection

RESISTOR VALUE ($R_{B-TMAXR}$) (kΩ)	BOOT VOLTAGE (V)	
	VR12.0	VR12.5
20	0.00	0.00
24	0.90	1.00
30	1.00	1.20
39	1.05	1.35
56	1.10	1.50
75	1.20	1.65
100	1.35	1.70
150	1.50	1.75

8.2.2.10 Step Ten: Set the Maximum Temperature Level

After selecting the R_{BOOT} value, select the maximum temperature (T_{MAX}) level for the temperature zone and compensation ramp level. The voltage on B-TMAXR pin sets the T_{MAX} level. A resistor (R_{TMAX}) between the VREF pin and the B-TMAXR pin sets thevoltage on B-TMAXR according to the associations shown in Table 73 . In this design example, T_{MAX} is selected as 120°C, and R_{BOOT} is selected as 100 kΩ, so R_{TMAX} = 24 kΩ.

Table 73. Maximum Temperature Level Selection

$V_{B-TMAXR}$	OR	MFR_SPEC_12[2:0]	T_{MAX} (°C)
$V_{B-TMAXR}$ ≤ 0.186 V	or	000b	90
0.24 V ≤ $V_{B-TMAXR}$ ≤ 0.399 V		001b	95
0.452V ≤ $V_{B-TMAXR}$ ≤ 0.611 V		010b	100
0.665 V ≤ $V_{B-TMAXR}$ ≤ 0.823 V		011b	105
0.877 V ≤ $V_{B-TMAXR}$ ≤ 1.036 V		100b	110
1.09 V ≤ $V_{B-TMAXR}$ ≤ 1.249 V		101b	115
1.302 V ≤ $V_{B-TMAXR}$ ≤ 1.461 V		110b	**120**
1.515 V ≤ $V_{B-TMAXR}$ ≤ 1.674 V		111b	125

The TSEN pin offers temperature sensing by two methods.

- Connecting the TAO pins of the CSD95373A component of all phases. The CSD95372A devices report their hottest temperature to the controller.
- Use an NTC circuit with parallel compensation resistor connected between the VREF and TSEN pins and a resistor provide the TSEN pin voltage by a divider. Calculate this combination using the TI Design Tool. Enter the expected NTC resistor value and the corresponding B25-100 range value. Then enter the TSEN-GND pin resistor value and optimize the error by referring to the graph as low as ±1%. Use these final adjusted values.

8.2.2.11 Step Eleven: Determine the Compensation Ramp

Selecting the PWM comparator compensation ramp value is a two-step process.

1. Select the proper range of ramp values, low range (20 mV, 40 mV, 60 mV, 80 mV) or high range (100 mV, 120 mV, 150 mV, 200 mV). Using Table 74 to select the proper value, connect a resistor between the $\overline{SKIP}$-RAMP pin and GND. Use a resistor with a value ≤ 20 kΩ for the lower range or ≥ 230 kΩ for the higher range.
2. Select one of the four ramp values within the selected range. To do this, calculate the value of the resistor between the B-TMAXR pin and the VREF pin required to achieve the proper voltage on B-TMAXR. The TI-provided design tool can be used to select the proper values. It is suggested to use a 57.6-kΩ resistor between the $\overline{SKIP}$-RAMP pin and the FCCM pin of the TI NextFET powerstage to meet the low-level input voltage level.

Table 74. $\overline{SKIP}$-Ramp Pin to GND Resistor and Voltage on B-TMAXR Pin

$\overline{SKIP}$-RAMP PIN TO GND RESISTOR AND VOLTAGE ON B-TMAXR PIN	mV_{P-P}
MFR_SPEC_14[2:0] = 000b or R $\overline{SKIP}$-RAMP ≤ 20 kΩ and $V_{B-TMAXR}$ ≤ 0.027 V or $V_{B-TMAXR}$ = 0.24 V or $V_{B-TMAXR}$ = 0.452 V or $V_{B-TMAXR}$ = 0.665 V or $V_{B-TMAXR}$ = 0.877 V or $V_{B-TMAXR}$ = 1.09 V or $V_{B-TMAXR}$ = 1.302 V or $V_{B-TMAXR}$ = 1.515 V with ±10 mV	20
MFR_SPEC_14[2:0] = 000b or R $\overline{SKIP}$-RAMP ≤ 20 kΩ and $V_{B-TMAXR}$ = 0.08 V or $V_{B-TMAXR}$ = 0.293V or $V_{B-TMAXR}$ = 0.505 V or $V_{B-TMAXR}$ = 0.718 V or $V_{B-TMAXR}$ = 0.93V or $V_{B-TMAXR}$ = 1.143 V or $V_{B-TMAXR}$ = 1.355 V or $V_{B-TMAXR}$ = 1.568 V with ±10 mV	40
MFR_SPEC_14[2:0] = 000b or R $\overline{SKIP}$-RAMP ≤ 20 kΩ and $V_{B-TMAXR}$ = 0.133 V or $V_{B-TMAXR}$ = 0.346 V or $V_{B-TMAXR}$ = 0.558 V or $V_{B-TMAXR}$ = 0.771 V or $V_{B-TMAXR}$ = 0.983 V or $V_{B-TMAXR}$ = 1.196 V or $V_{B-TMAXR}$ = 1.408 V or $V_{B-TMAXR}$ = 1.621 V with ±10 mV	60
MFR_SPEC_14[2:0] = 000b or R $\overline{SKIP}$-RAMP ≤ 20 kΩ and $V_{B-TMAXR}$ = 0.186V or $V_{B-TMAXR}$ = 0.399 V or $V_{B-TMAXR}$ = 0.611 V or $V_{B-TMAXR}$ = 0.823V or $V_{B-TMAXR}$ = 1.036 V or $V_{B-TMAXR}$ = 1.249 V or $V_{B-TMAXR}$ = 1.461V with ±10mV or VB-TMAXR ≥ 1.674 V	80
MFR_SPEC_14[2:0] = 000b or R $\overline{SKIP}$-RAMP ≥ 230 kΩ and VB-TMAXR ≤ 0.027 V or $V_{B-TMAXR}$ = 0.24 V or $V_{B-TMAXR}$ = 0.452 V or $V_{B-TMAXR}$ = 0.665 V or $V_{B-TMAXR}$ = 0.877 V or $V_{B-TMAXR}$ = 1.09 V or $V_{B-TMAXR}$ = 1.302 V or $V_{B-TMAXR}$ = 1.515 V with ±10 mV	100
MFR_SPEC_14[2:0] = 000b or R $\overline{SKIP}$-RAMP ≥ 230 kΩ and $V_{B-TMAXR}$ = 0.08 V or $V_{B-TMAXR}$ = 0.293 V or $V_{B-TMAXR}$ = 0.505 V or $V_{B-TMAXR}$ = 0.718 V or $V_{B-TMAXR}$ = 0.93 V or $V_{B-TMAXR}$ = 1.143 V or $V_{B-TMAXR}$ = 1.355 V or $V_{B-TMAXR}$ = 1.568 V with ±10 mV	120
MFR_SPEC_14[2:0] = 000b or R $\overline{SKIP}$-RAMP ≥ 230 kΩ and $V_{B-TMAXR}$ = 0.133 V or $V_{B-TMAXR}$ = 0.346 V or $V_{B-TMAXR}$ = 0.558 V or $V_{B-TMAXR}$ = 0.771 V or $V_{B-TMAXR}$ = 0.983 V or $V_{B-TMAXR}$ = 1.196 V or $V_{B-TMAXR}$ = 1.408 V or $V_{B-TMAXR}$ = 1.621 V with ±10 mV	150
MFR_SPEC_14[2:0] = 000b or R $\overline{SKIP}$-RAMP ≥ 230 kΩ and $V_{B-TMAXR}$ = 0.186 V or $V_{B-TMAXR}$ = 0.399 V or $V_{B-TMAXR}$ = 0.611 V or $V_{B-TMAXR}$ = 0.823 V or $V_{B-TMAXR}$ = 1.036 V or $V_{B-TMAXR}$ = 1.249 V or $V_{B-TMAXR}$ = 1.461 V with ±10 mV or $V_{B-TMAXR}$ ≥ 1.674 V	200

8.2.2.12 Step Twelve: Set OSR and USR Thresholds

Setting the OSR and USR thresholds can help improve load transient performance in some types of applications.

A resistor, R_{OSR}, connected between the O-USR pin and GND sets the overshoot reduction (OSR) threshold. The corresponsing resistor settings are shown in Table 75.

Table 75. OSR Threshold and Resistor Selection

RESISTOR VALUES R_{OSR} (kΩ)	OSR VOLTAGE THRESHOLD (mV)
20	25
24	35
30	45
39	65
56	85
75	105
100	125
150	OFF

The required OSR setting is based on the load-transient performance and amount of the actual output capacitance. The suggested method is to begin with OSR OFF and perform the load transient per Intel guidelines. If the overshoot can meet the specification with the chosen output capacitance, then maintain OSR as OFF. So the resistor R_{OSR} can be selected as 150 kΩ. Otherwise the OSR threshold can be lowered by choosing a lower setting from Table 75 to reduce the overshoot and meet the specifications.

After selecting the R_{OSR} value, set the undershoot reduction (USR) threshold. The voltage on O-USR pin sets the undershoot reduction (USR) threshold using the resistor, R_{USR}, which is connected between the O-USR pin and the VREF pin set. The corresponsing resistor settings are shown in Table 76.

Table 76. USR Threshold and Resistor Selection

VOLTAGE V_{O-USR} (V)	USR VOLTAGE THRESHOLD (mV)
$V_{O-USR} \le 0.3$	15
$0.35 \le V_{O-USR} \le 0.45$	24
$0.55 \le V_{O-USR} \le 0.65$	35
$0.75 \le V_{O-USR} \le 0.85$	55
$0.95 \le V_{O-USR} \le 1.05$	75
$1.15 \le V_{O-USR} \le 1.25$	95
$1.35 \le V_{O-USR} \le 1.45$	115
$V_{O-USR} \ge 1.55$	OFF

The design procedure for the USR threshold is similar to the OSR setting. The initial setting of USR threshold is to start with USR OFF, and lower the threshold to enable pulse-overlap during the load transients to meet the load insertion transient requirement, so for this example use a 75-mV USR threshold. So in this application the value of the R_{OSR} resistor is 150 kΩ and the value of the R_{O-USR} resistor is 105 kΩ.

8.2.2.13 Step Thirteen: Digital Current Monitor (IMON) Gain and Filter Setting

In order to have correct digital current monitoring values, determine the gain of the analog current monitor by setting IMON voltage to 0.85 V for maximum output current $I_{CC(max)}$. In this case, the digital value reported to CPU via SVID interface at register 15h is “FF” based on Intel specifications. Calculate the value of R_{IMON} using Equation 13.

$$R_{IMON} = \frac{V_{IMON}}{I_{CC(max)} \times R_{DCR} \times Gain \times SF} = \frac{0.85\,V}{208\,A \times 0.18\,m\Omega \times 10 \times \frac{4}{35\,k\Omega}} = 19.87\,k\Omega \quad (13)$$

where

- $I_{CC(max)}$ is the total maximum output current
- V_{IMON} is the voltage on the IMON pin
- R_{DCR} is inductor DCR
- Gain is the IMON output pin amplifier gain
- SF is is the internal current gain scaling factor

In this design example, $I_{CC(max)}$ = 208 A, so the resistance, R_{IMON}, is calculated as 19.87 kΩ. In order to meet the averaging interval specification defined by the CPU vendor, a capacitor, C_{IMON}, occurs in parallel with R_{IMON}, and is calculated to meet the filtering requirement. Therefore, the suggested C_{IMON} value is 1.8 nF in this design example.

8.2.2.14 Step Fourteen: Compensation Design

Figure 94 shows a Type-II compensator accounting for the DCAP+ architecture of the TPS53640A device as shown in Figure 94. The value of $g_{M(COMP)}$, the COMP amplifier transconductance, is typically 0.5 mS. The value of resistor R_{COMP} determines the gain and the compensation pole and zero locations. The value of capacitor C_{COMPS} determines the compensation zero level to increase the phase margin, and the value of capacitor C_{COMPP} determines the compensation pole to filter out the high-frequency noise. The actual compensator design must be optimized based on the experimental test results and bode plot measurements.

In this example the values of this compensation network that establish the compensation zero at approximately 70 kHz and the compensator pole at approximately 1 MHz are:

- R_{COMP} = 6.65 kΩ
- C_{COMPS} = 470 pF
- C_{COMPP} = 27 pF

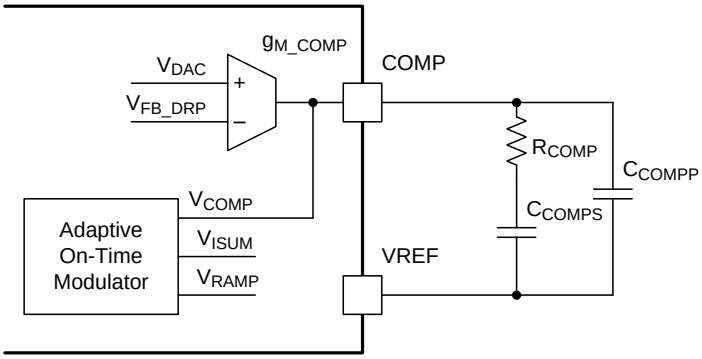
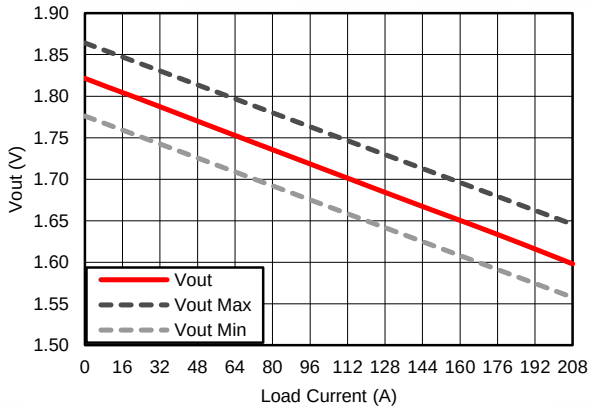


Figure 94. Type-II Compensator Circuit

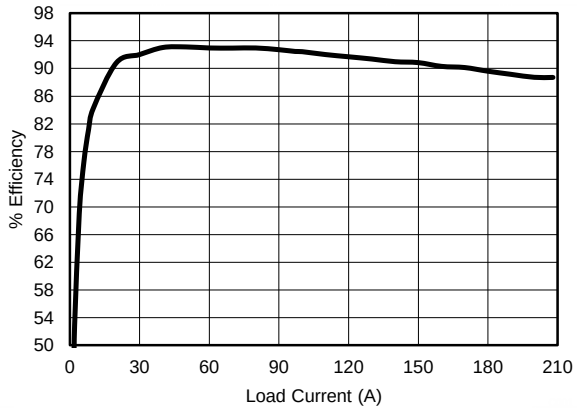
8.2.3 Application Curves



Power Stage 0

V_O = 1.82 V Non-Zero Load-Line (NZLL)

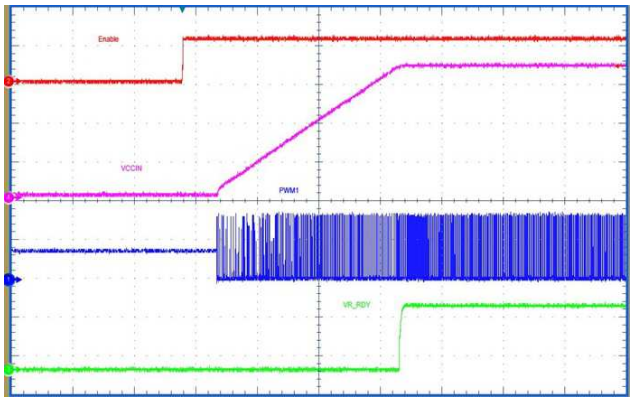
Figure 95. Output Voltage vs. Load Current



Power Stage 0 V_I = 12 V

f_{SW} = 600 kHz DPS Disabled

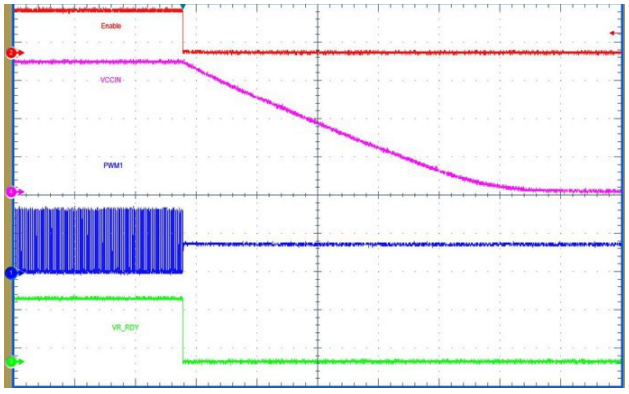
Figure 96. Efficiency vs. Load Current



V_I = 12 V V_O = 1.7 V

I_{LOAD} = 0 A

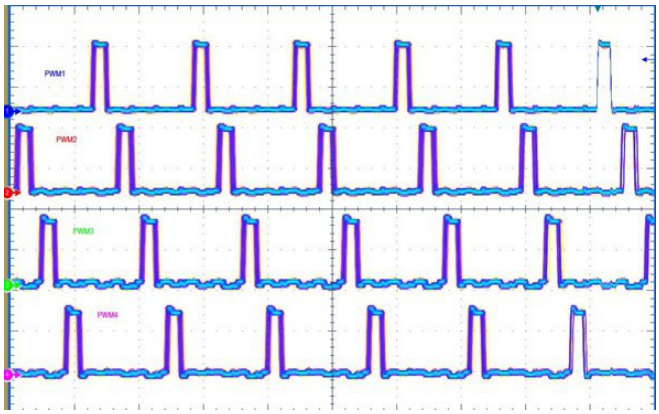
Figure 97. Enable Start-Up



V_I = 12 V V_O = 1.7 V

I_{LOAD} = 10 A

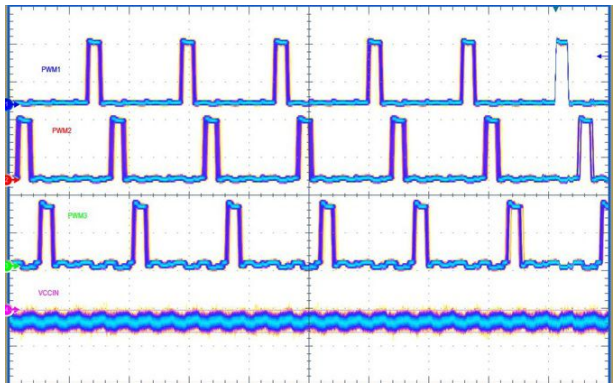
Figure 98. Enable Shutdown



V_I = 12 V V_O = 1.8 V

I_{LOAD} = 0 A

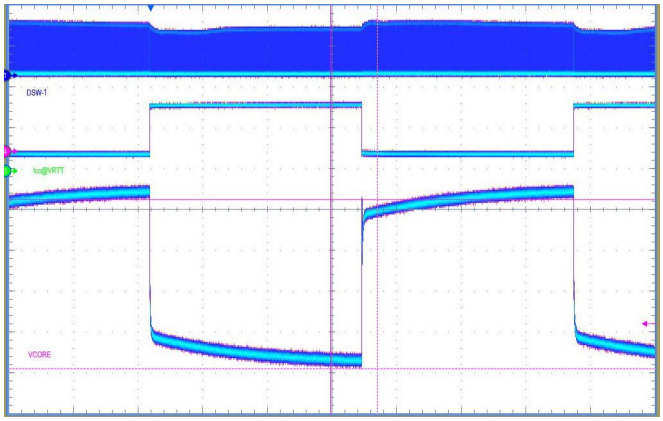
Figure 99. PWM Jitter



V_I = 12 V V_O = 1.8 V

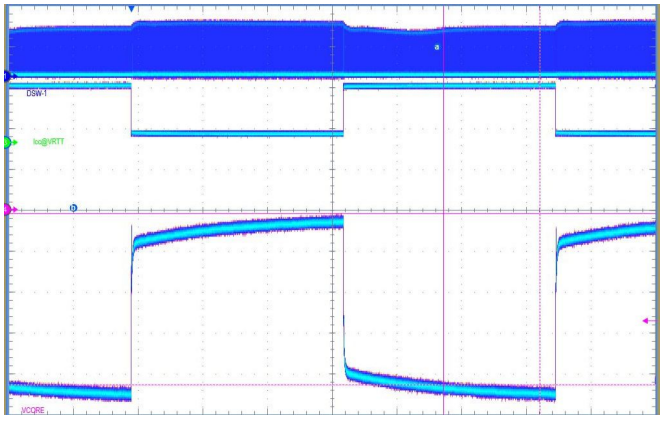
I_{LOAD} = 10 A

Figure 100. Output Ripple



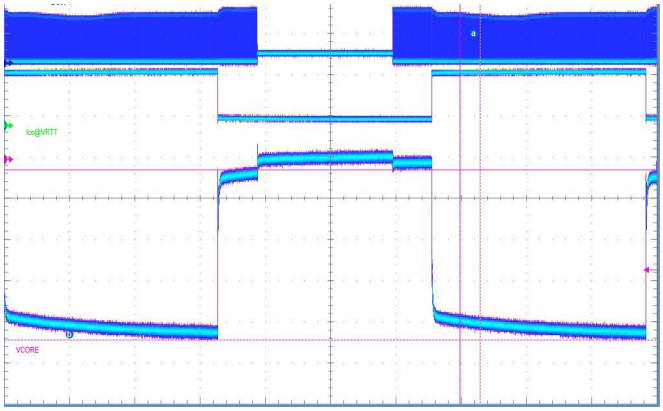
V_I = 12 V
I_{LOAD} = 50 A to 208 A
V_O = 1.82 V
di/dt = 600A/µs

Figure 101. Transient Undershoot



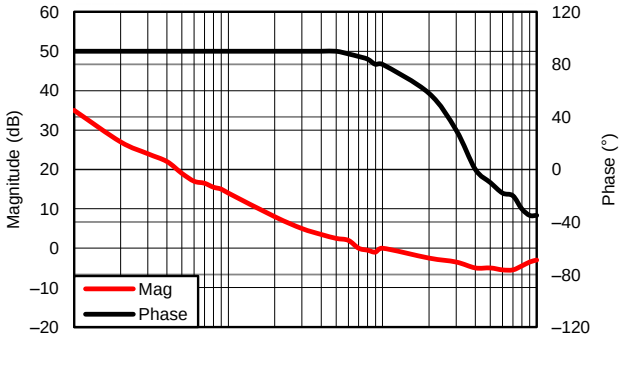
V_I = 12 V
I_{LOAD} = 22 A to 180 A
V_O = 1.82 V
di/dt = 600A/µs

Figure 102. Transient Overshoot



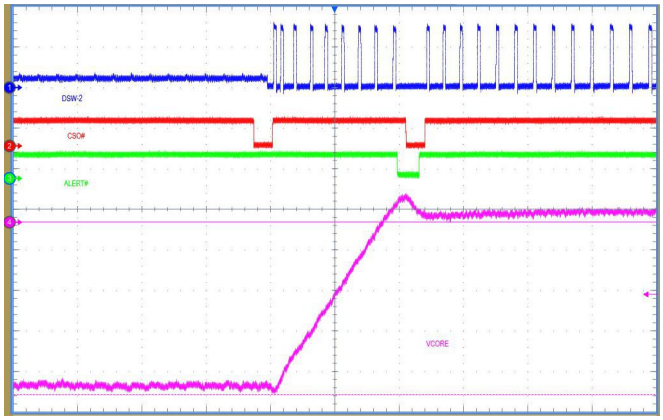
V_I = 12 V
I_{LOAD} 3 A to 161 A
V_O = 1.82 V
PS2 to PS0
di/dt = 600A/µs

Figure 103. Transient PS2 to PS0



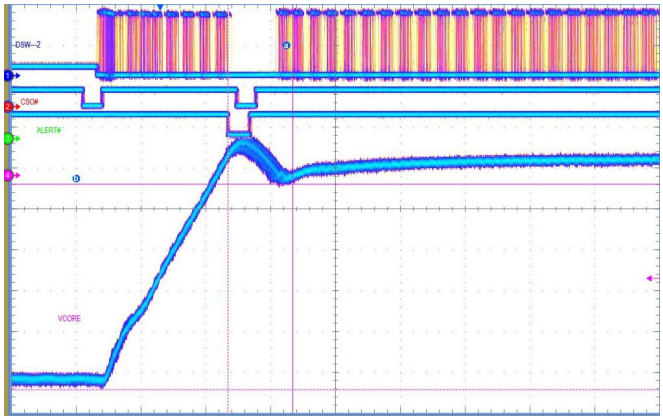
Power State 0
I_O = 120 A
V_O = 1.82 V
V_I = 12 V
f_{SW} = 600 kHz

Figure 104. Bode Plot



Power State 0
I_O = 20 A
Slew Rate = 20 mV/µs
V_O = 1.6 V to 1.82 V

Figure 105. DVID Operation



Power State 2
I_O = 5 A
Slew Rate = 20 mV/µs
V_O = 1.6 V to 1.82 V

Figure 106. DVID Operation

9 Power Supply Recommendations

The TPS53640A device operates from a 3.3-V supply at the V3P3 pin and a 12-V supply on the VIN pin. The 12-V supply internally generates the 5-V supply from an LDO. For best results, consider the UVLO range for VIN, V3P3 and V5 pin voltages, use well regulated supplies and use the recommended filter network. Ensure that the rising slew rate on the V3P3 pin is higher than 1.5 V/ms.

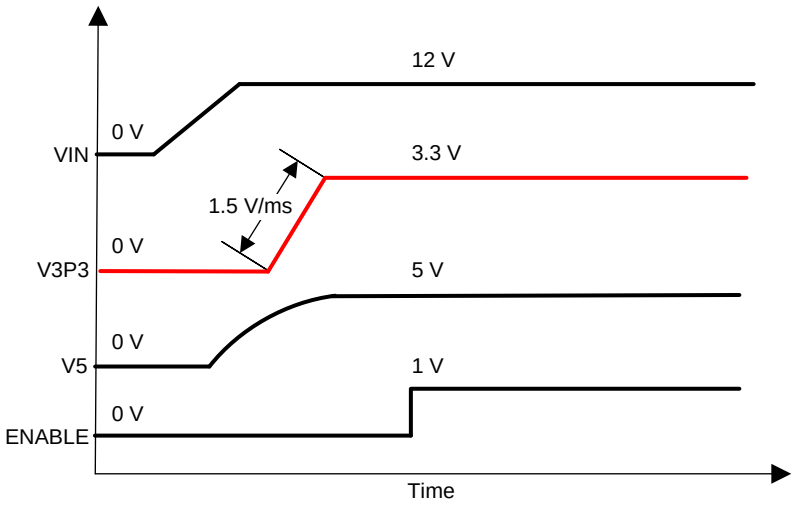


Figure 107. Power Supply Waveforms

10 Layout

10.1 Layout Guidelines

Use the following guidelines for proper layout.

10.1.1 Schematic Design Guideline

10.1.1.1 Schematic Review Checklist

- Ensure that the pin-out of the controller shown on the schematic matches the pin-out of datasheet.
- Refer to an applicable TI reference design to check for connection and component values.
- Use a design tool to confirm calculated component values.
- Carefully confirm choice of inductor and DCR.
- Carefully confirm choice of output capacitors.
- V3P3 (pin14) must be connected to a 3.3-V supply which its startup slew rate is higher than 1.5V/ms.
- Decouple V3P3 and VIN to GND with a ceramic capacitor with a value of at least 1 µF.
- Decouple V5 to GND with at least a ceramic capacitor with a value of at least 4.7 µF.
- Decouple VCCIO to GND (SVID pull-up) with a capacitance of at least 0.1 µF to GND and close to controller
- Confirm the current sensing feedback and reference voltage to CSD95372A.
- Add a 1-nF capacitor and a resistor placeholder between the TSEN pin and GND and close to the TSEN pin (pin 36) of the TPS53640A device.
- To achieve better output current reading accuracy, choose a resistor for R_{IMON} that specifies a tolerance of 0.1%.
- It is recommended to add a PMBus connector to enable system debugging.
- Strongly recommend that the device GND be separate from the system and Power GND.
- Output capacitors for CPU: Follow the Intel Platform Design Guide (PDG).
- Output capacitor for DDR4: Follow 8 pcs x 47 µF (0805) ceramic per DIMM.

10.1.2 PCB Design Guideline

The TPS53640A device is driven by the inductor-DCR current sensing method. The DCR sensed current signal is very noise sensitive, so place the power stage CSD95372A outside of the device. All gate-drive and switch-node traces must be local to the inductor and MOSFETs.

MOST CRITICAL LAYOUT REQUIREMENT
Separate noisy driver interface lines from sensitive analog and SVID interface lines.

10.1.2.1 PCB Layer Stack-up Recommendation

The following lists the recommended PCB layout stack-up:

- Top layer: Power 1.5 oz.
- Layer 2: Power and GND 1 oz.
- Layer 3: Signal 1 oz.
- Layer 4: Power and GND 2 oz.
- Layer 5: Power and GND 2 oz.
- Layer 6: Signal 1 oz.
- Layer 7: Power and GND 1 oz.
- Bottom layer: Power 1.5 oz.

10.1.2.2 Power Chain Symmetry

Because independent isolated current feedback is based on inductor DCR sensing, the TPS53640A device requires special care in the layout of the power-chain components. If it is possible, ensure that the phases are laid out in a symmetrical manner.

Layout Guidelines (continued)

Power Chain Symmetry Rule

The current feedback from each phase must be clean of noise and have the same effective current sense resistance.

10.1.2.3 Analog Component Placement

Place analog components as close to the TPS53640A device as possible. Place the components in the following order:

1. COMP pin and ISUM pin compensation components
2. Decoupling capacitors for VREF, V3P3, V5, VIN
3. Decoupling capacitor for the VCCIO rail which is a pull-up voltage for the SVID lines. This decoupling capacitor should be placed near the TPS53640A device to ensured SVID signal integrity.
4. Resistors for these pins:
   - OCL
   - F-IMAX
   - SLEW-MODE
   - B-TMAXR
   - IMON
   - O-USR

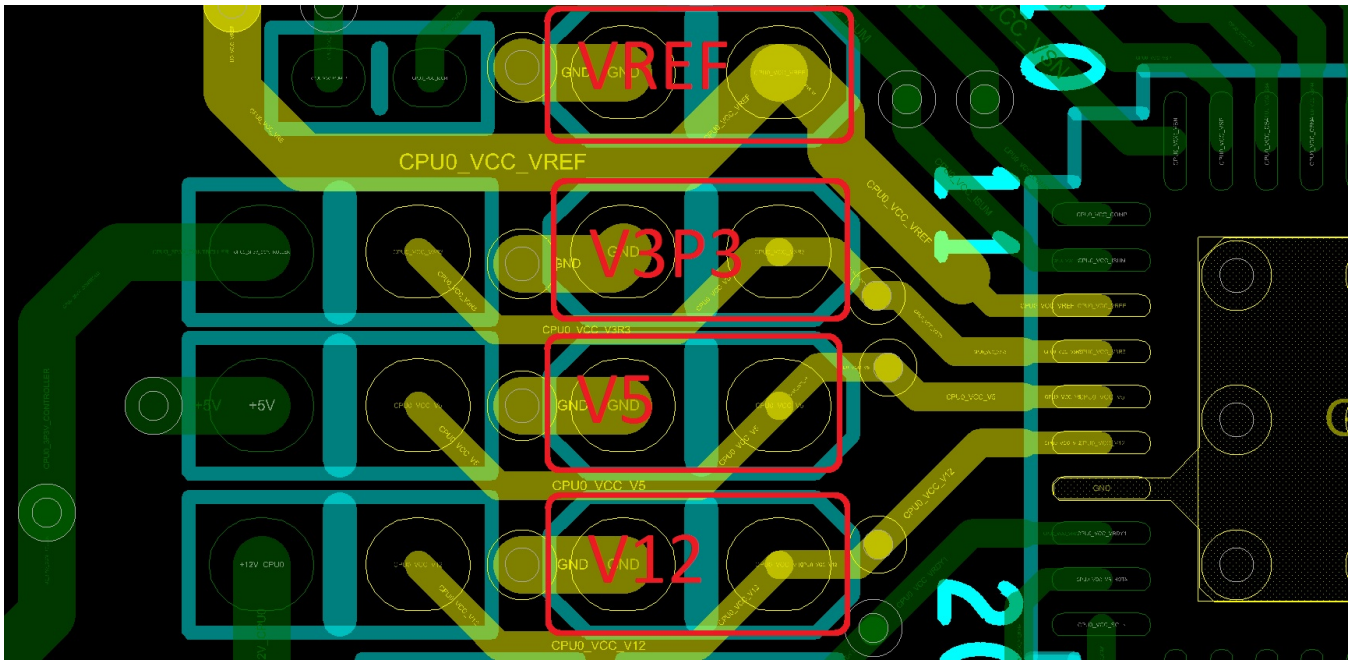


Figure 108. VREF, V3P3, V5 Decoupling Capacitors Placement

10.1.2.4 Grounding Recommendations

The TPS53640A device has an analog ground and a thermal pad. The following lists the standard procedure for connecting the analog ground and thermal pad:

- The thermal pad does not have an electrical connection to the IC, however, it must be connected to the ground of the device to give good ground shielding. Do not connect the pad to the power GND.
- Connect the thermal pad (analog ground pin) to a ground island with at least 9 standard vias (drill size 12 mil and pad diameter 26 mil). All analog components can connect to this analog ground island.
- The analog ground can be connected to any *quiet spot* on the system ground. A quiet spot is defined as a

Layout Guidelines (continued)

spot where no power supply switching currents are likely to flow. This applies to both the V_{DDQ} regulator and other regulators. Use a single-point connection from the analog ground to the power ground.

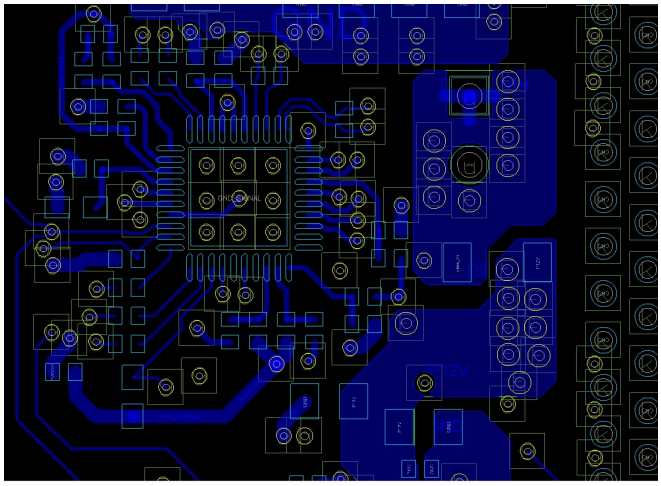


Figure 109. Typical Top Layer Placement

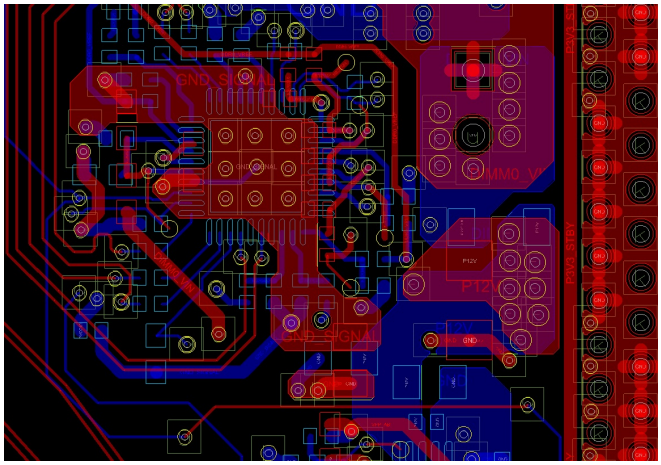


Figure 110. Typical GND Plane Placement

10.1.2.5 Current Sensing Lines

Given the physical layout of most systems, the current feedback (CSPx, CSNx) may have to pass near the power chain. Clean current feedback is required for a good load-line slope, current sharing, and current limiting performance of the TPS53640A device, so take the following precautions.

- Run the current feedback signals as a differential pair (10 mil) to the device. The CSPx-CSNx differential pair separation width can be between 5 mil. and 10 mil.
- Run the current feedback trace and the PWMx traces on different sides of the power stage.
- Ensure all vias in the CSPx and CSNx traces are isolated from all other signals.
- Dotted signal traces are recommended to be run in internal planes.
- If possible, change the name of the CSNx trace if possible to prevent automatic ties to the V_{CORE} plane.
- Put R_{SEQU} at the boundary between noisy and quiet areas.
- Make a Kelvin connection to the pads of the resistor or inductor used for current sensing.
- Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane.
- Place the compensation capacitor for DCR sensing (C_{SENSE}) as close to the CSx pins as possible.
- Place any noise filtering capacitors directly underneath these devices and connect to the CSx pins with the shortest trace length possible.

Layout Guidelines (continued)

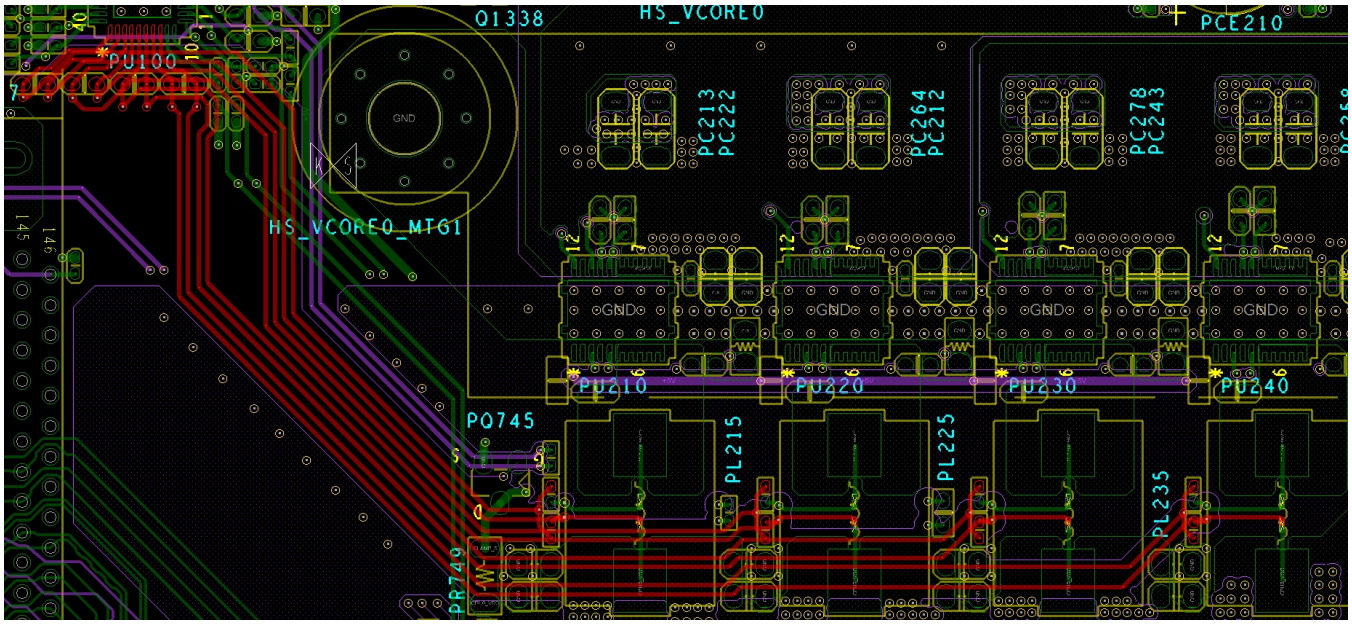


Figure 111. Current Sense Line Pairs

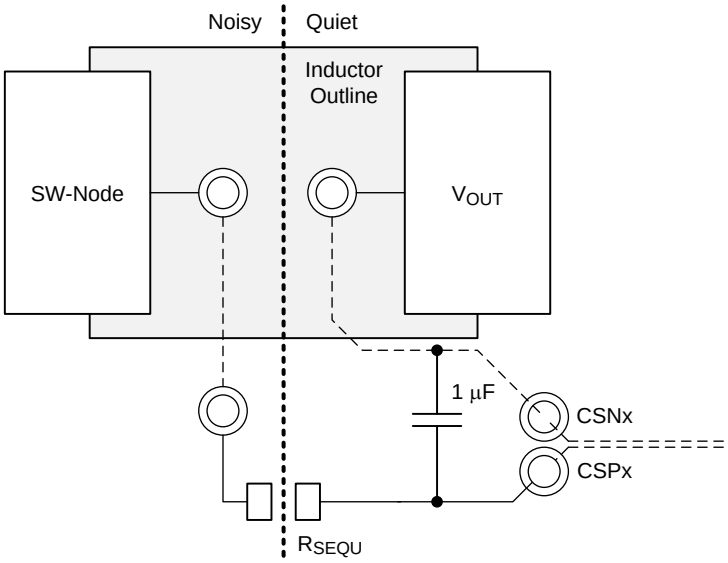


Figure 112. Kelvin Connections to the Inductor for DCR Sensing

Layout Guidelines (continued)

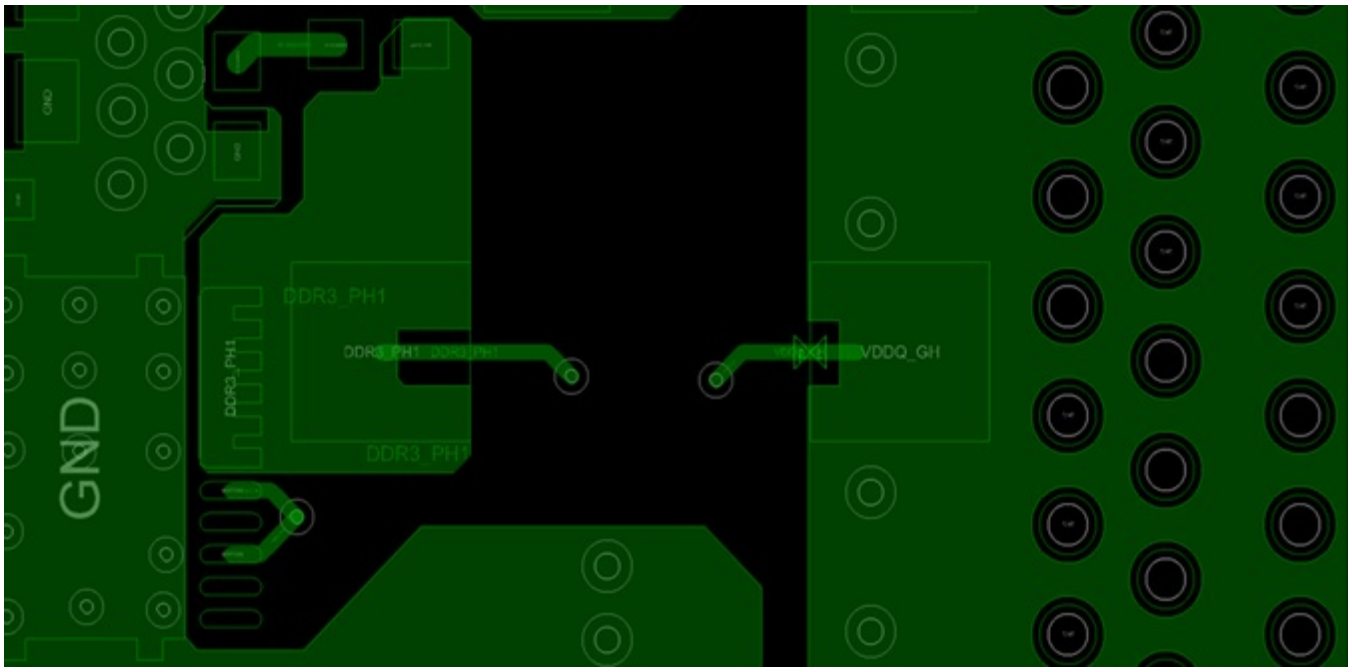


Figure 113. Kelvin Connections on PCB

Layout Guidelines (continued)

10.1.2.6 Feedback Voltage Sensing Lines

The voltage feedback coming from the CPU or DDR4 memory socket must be routed as differential pair to the VSP and VSN pins of the TPS53640A device. Avoid routing over switch-node and gate-drive traces.

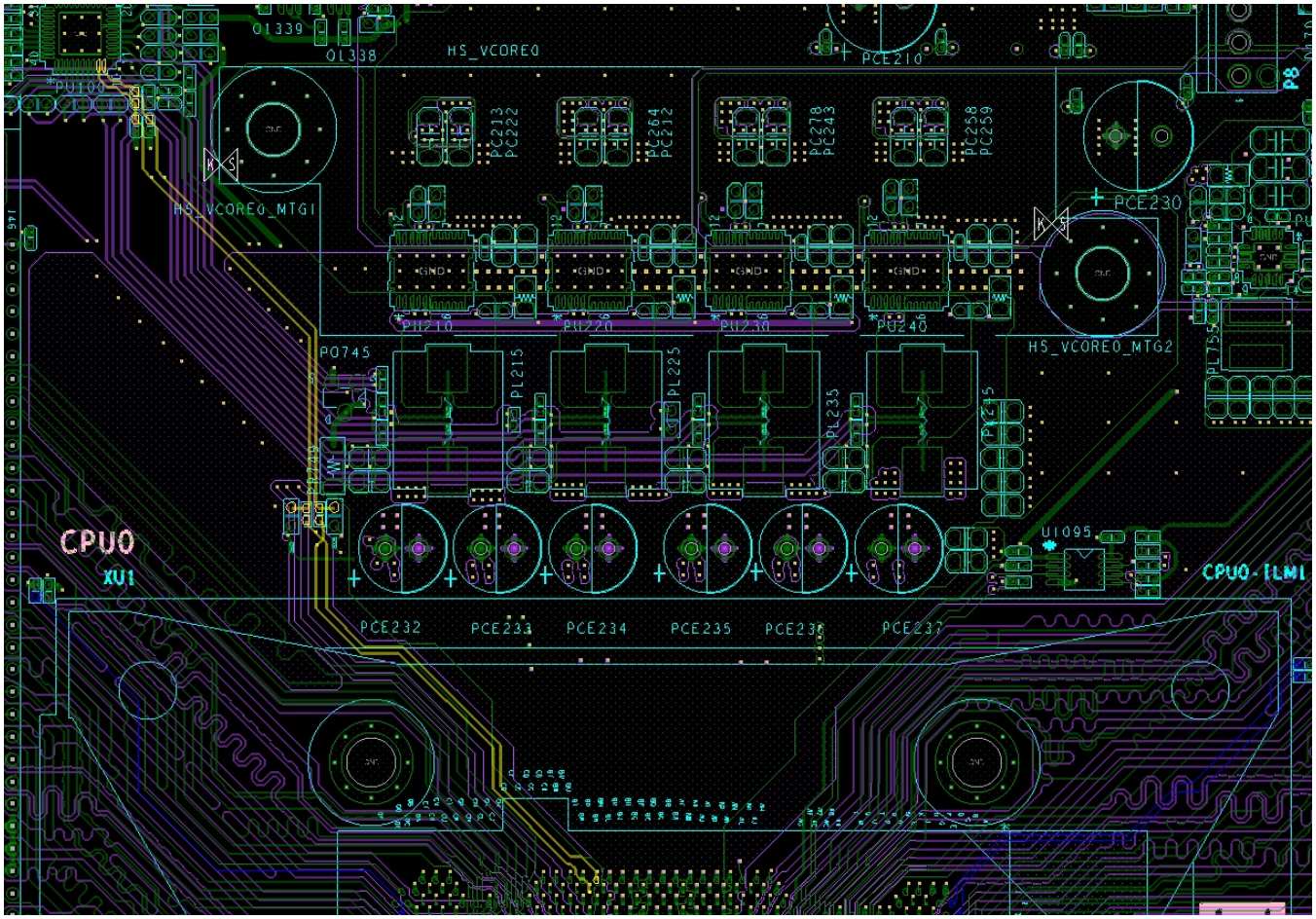


Figure 114. Voltage Sensing Lines on PCB

Layout Guidelines (continued)

10.1.2.7 SVID Lines

The routing of the SVID lines should follow the recommendation provided by Intel. These traces should follow the impedance matching as specified by Intel. Care should be taken to route the SDIO line between the SCLK and ALERT lines. Place a 0.1-µF bypass capacitor from the VCCIO pin (which is the pull-up rail for SVID termination resistors) to GND near the TPS53640A device.

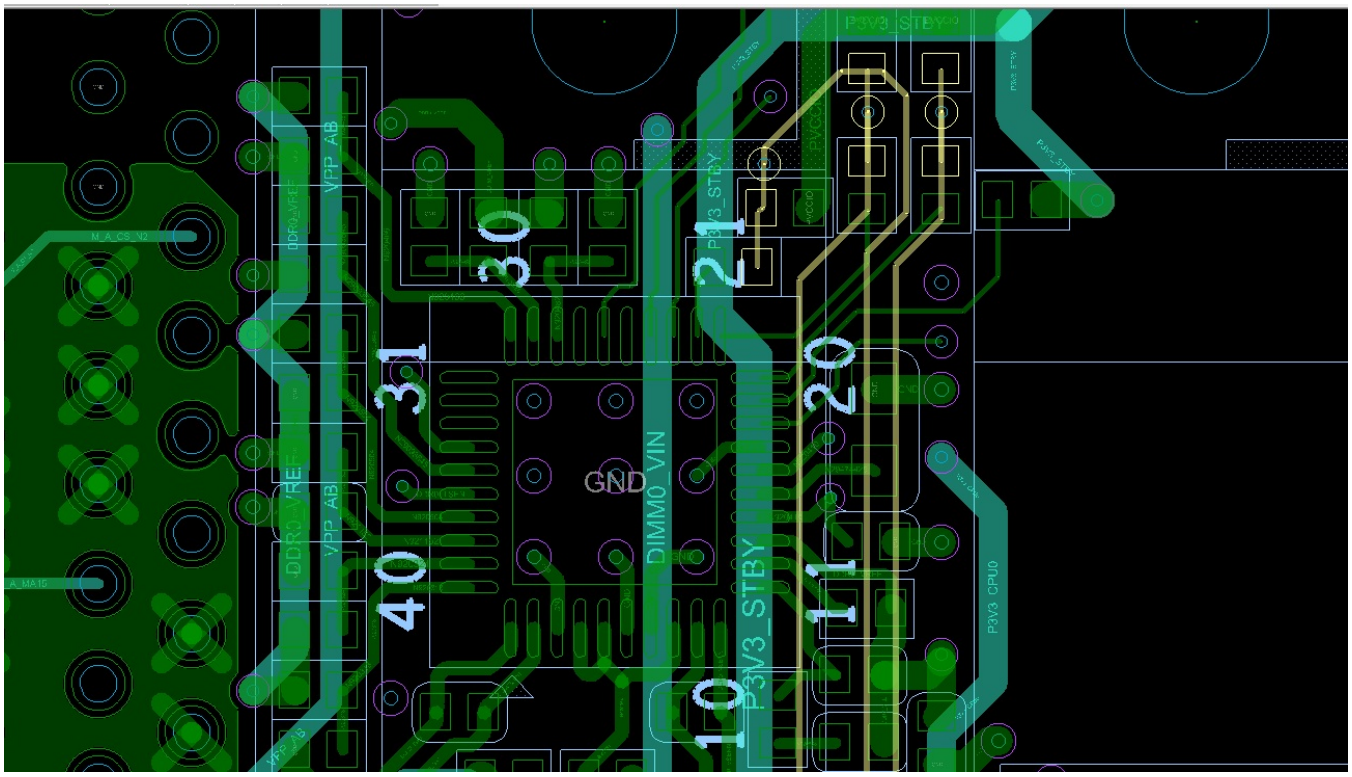


Figure 115. SVID Lines on PCB

Layout Guidelines (continued)

10.1.2.8 PWM and $\overline{\text{SKIP}}$ Lines

The PWM and $\overline{\text{SKIP}}$ lines should be routed from TPS53640A device to the driver without crossing any switch-node or the gate-drive signals.

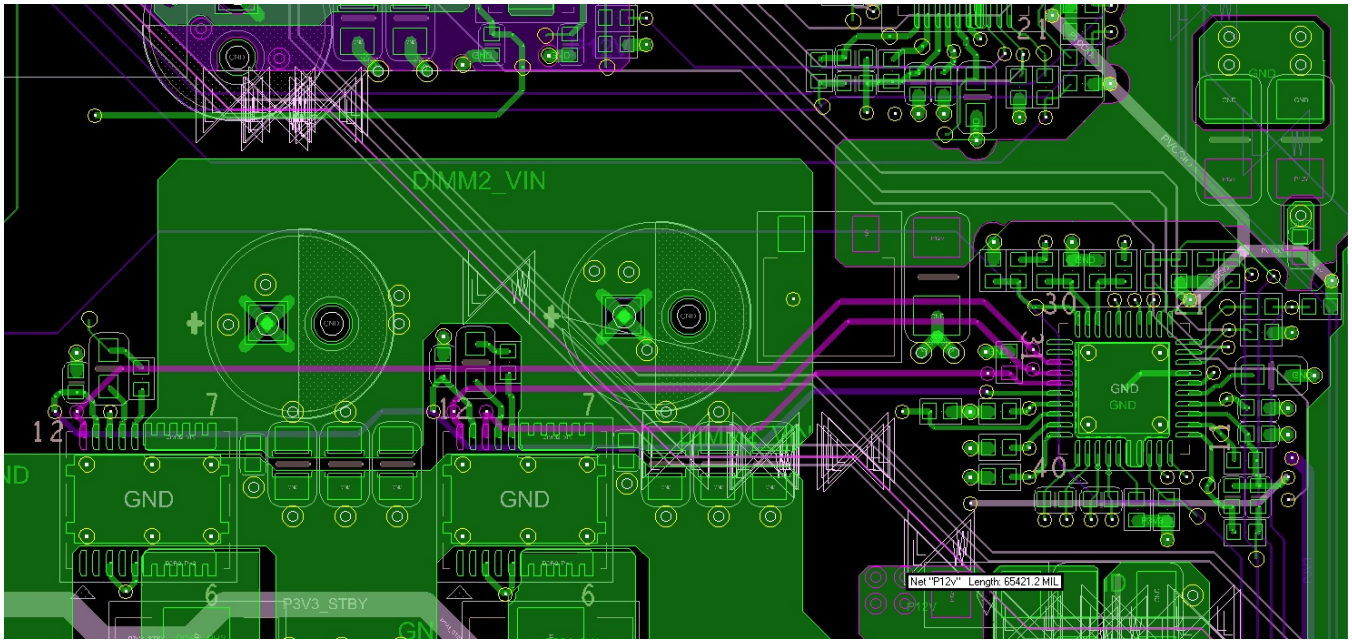


Figure 116. PWM and $\overline{\text{SKIP}}$ Lines on PCB

10.1.2.9 Conductor Widths

- Follow Intel guidelines with respect to the voltage feedback and logic interface connection requirements.
- Maximize the widths of power, ground, and drive signal connections.
- For conductors in the power path, ensure that the trace width is adequate for the amount of current flowing through the traces.
- Ensure that the number of vias is sufficient for connections between layers. In general, use at least one via per ampere of current.

Layout Guidelines (continued)

10.1.2.10 Power Stage Layout Guideline

- VIN capacitors should have the highest priority. Place the 0805 capacitor on the top-side of the PCB to the right of the power stage bridging the VIN pin and power ground. Place the larger capacitors on the top of the PCB next to the 0805 capacitor or place the larger capacitors on the bottom of the board directly underneath the VIN pin and the 0805 capacitor.
- Place the recommended bootstrap resistor and capacitor near pin 8 and pin 9 of TI NextFET powerstage. The preferred placement is on the top layer of the PCB. Also refer the layout shown in Figure 119.
- Place the bootstrap capacitor and bootstrap resistor as close as possible to the PU3 pin (pin 8) and the BOOT pin (pin 9). The preferred placement is on the top of the board.
- Place the snubber to the right of the switching node. If the snubber cannot be place on the top of the board, place the snubber on the bottom of the board.
- Place the VDD pin decoupling capacitor on the either top or the bottom of the board underneath and near the VDD pin (pin5).
- Place the TAO capacitor just to the left of the COMP pin (pin 11) on the top or on the bottom of the board in the same general area.
- If possible, use at least 12 power-ground vias underneath each power stage.
- Place multiple vias near the VIN copper pour in order to share the current with the inner layers.
- To avoid capacitive coupling issues, provide the TAO capacitors and traces with a large clearance from the VIN copper pour area.

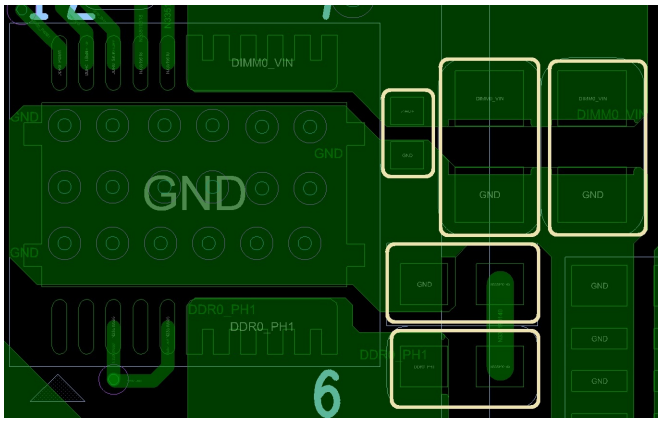


Figure 117. VIN Capacitor and Snubber Placement

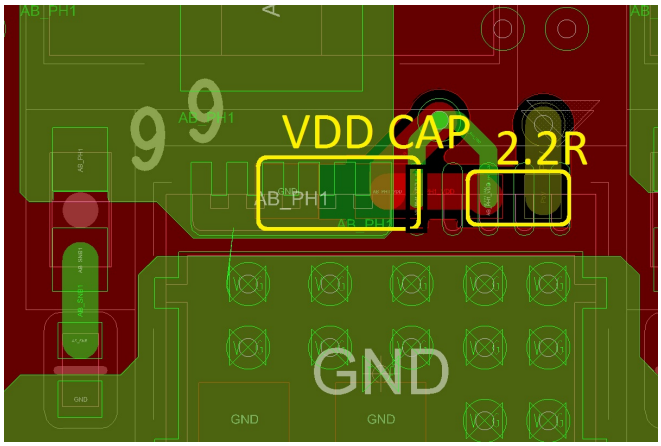


Figure 118. Power Stage VDD Capacitor Placement

Layout Guidelines (continued)

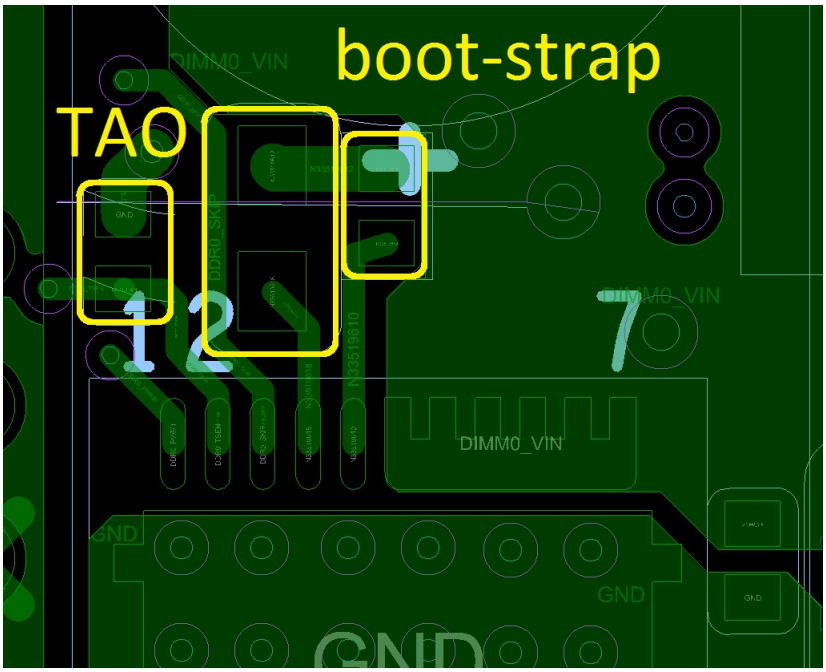


Figure 119. TAO Capacitor and Bootstrap Resistor-Capacitor Placement

10.2 Layout Example

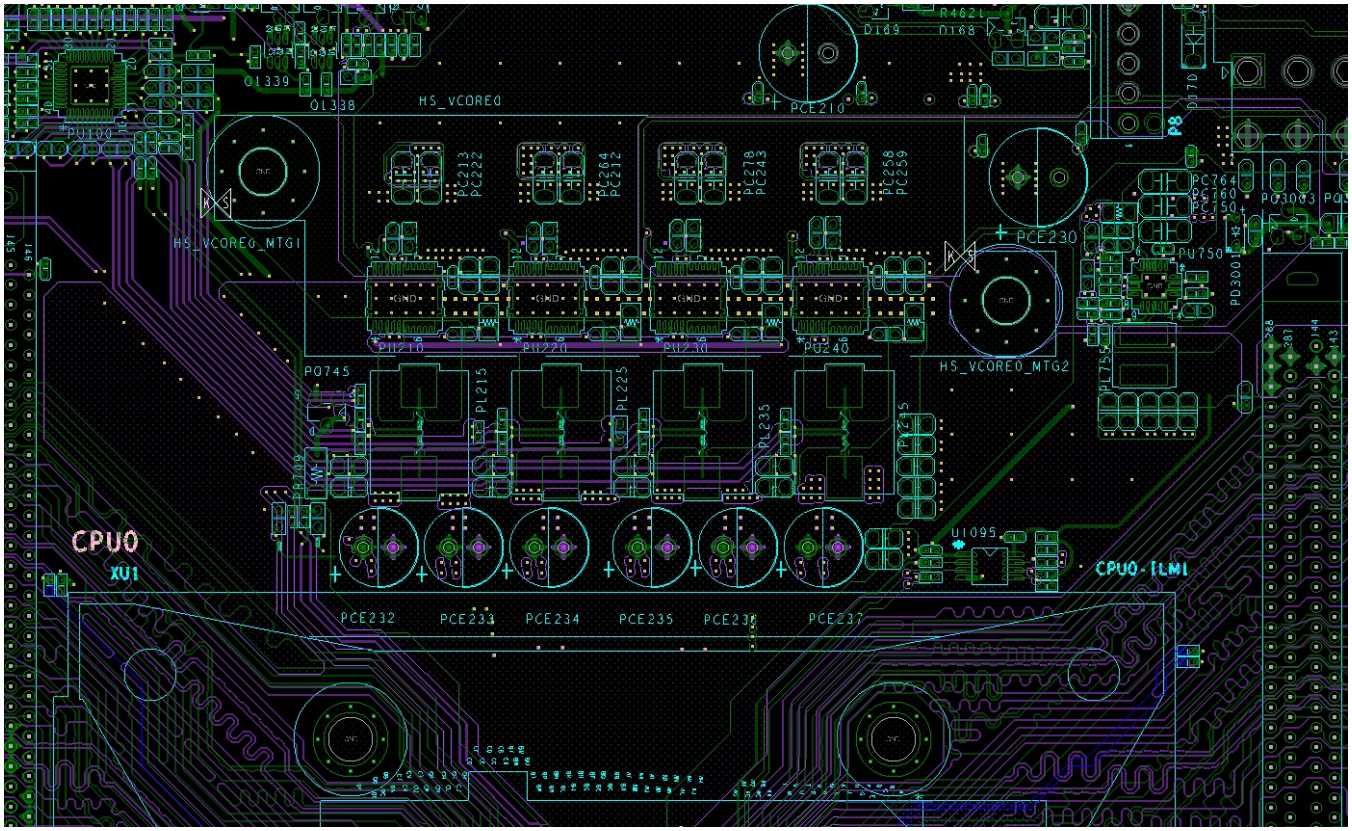


Figure 120. TPS53640A Layout Example

11 Device and Documentation Support

11.1 Trademarks

NexFET, D-CAP+ are trademarks of Texas Instruments.
Intel is a registered trademark of Intel Corporation.
PMBus is a trademark of SMIF, Inc.
All other trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4) (5)
TPS53640ARSBR	PREVIEW	QFN	RSB	40	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–10 to 105	TPS53640A
TPS53640A RSBT	PREVIEW	QFN	RSB	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–10 to 105	TPS53640A

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

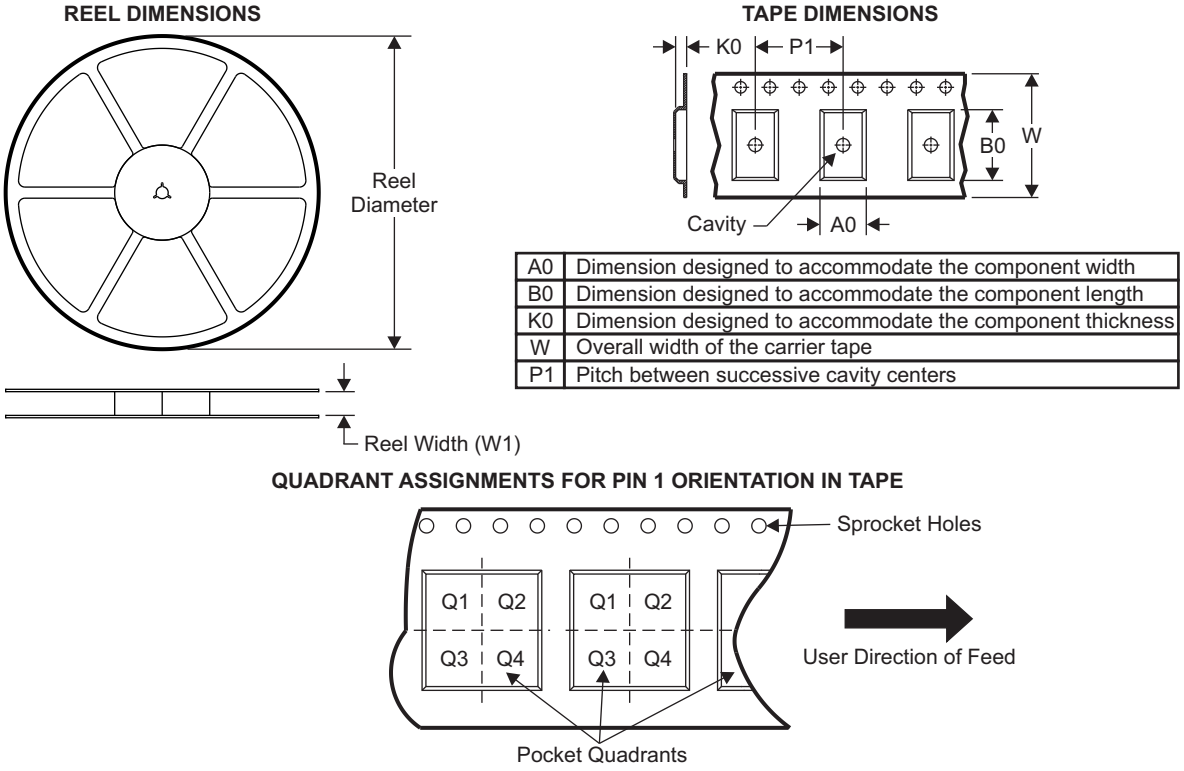
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

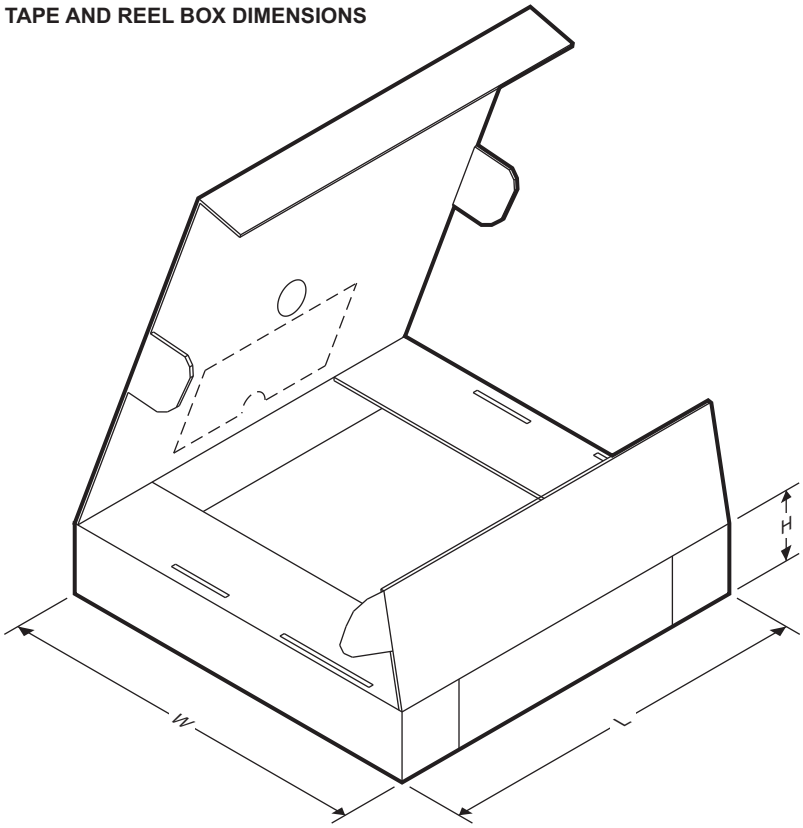
12.1.2 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53640ARSBR	QFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS53640ARSBT	QFN	RSB	40	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53640ARSBR	QFN	RSB	40	3000	367.0	367.0	35.0
TPS53640ARSBT	QFN	RSB	40	250	210.0	185.0	35.0

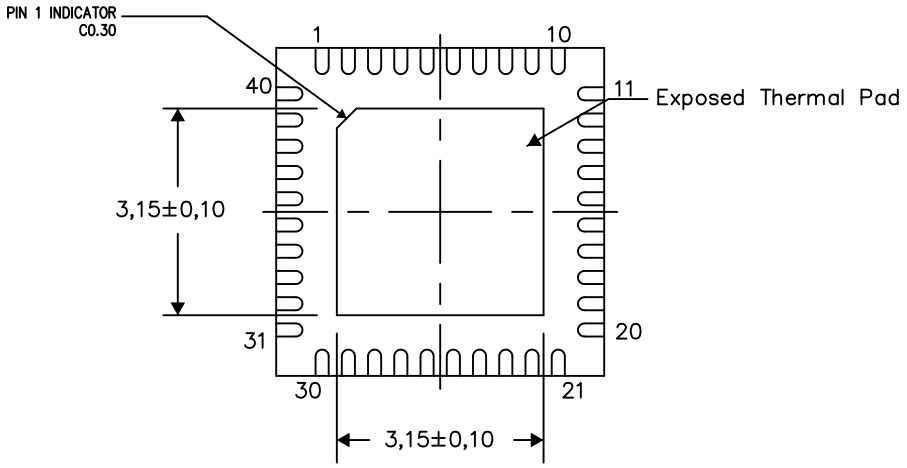
RSB (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



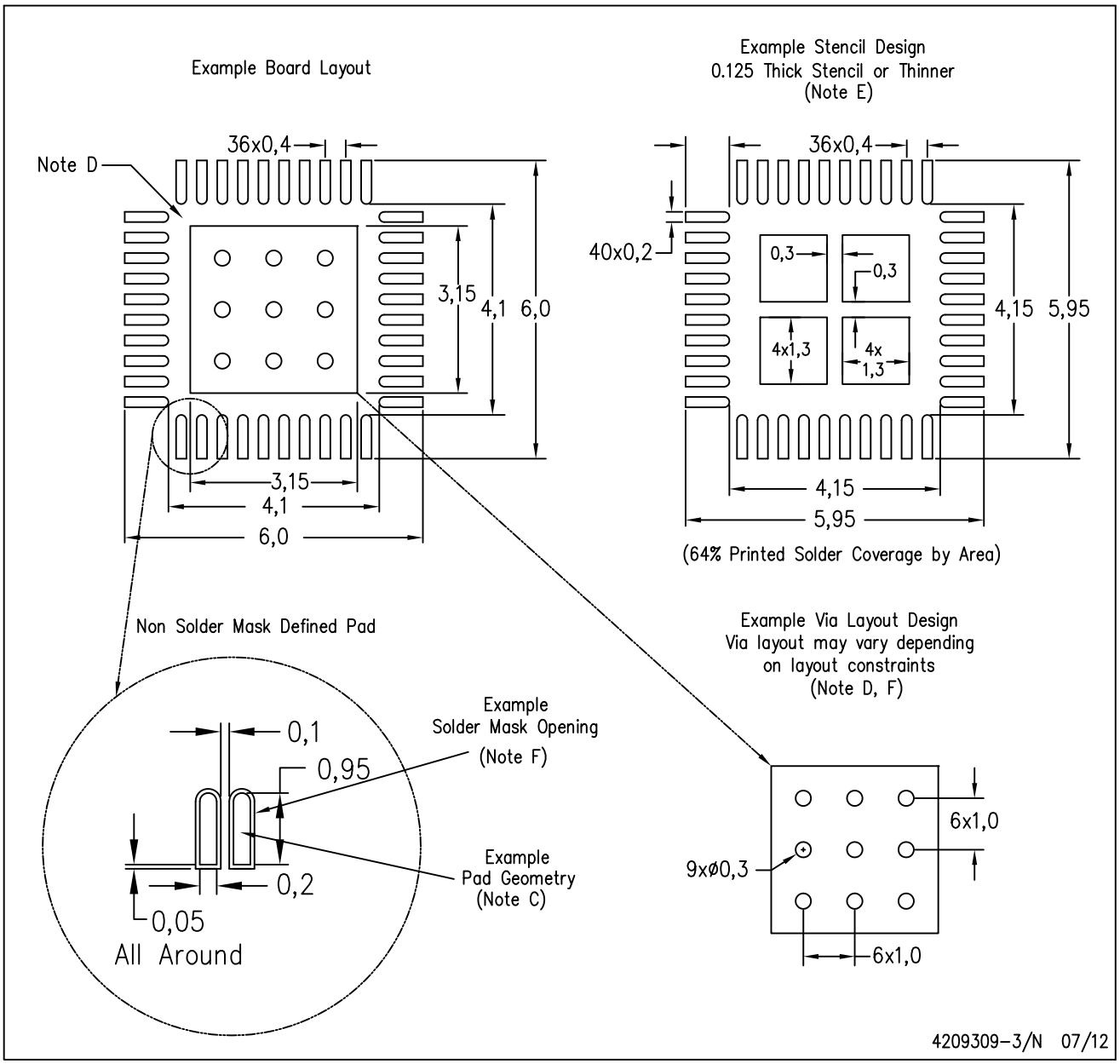
Bottom View

Exposed Thermal Pad Dimensions

4207183–3/P 06/12

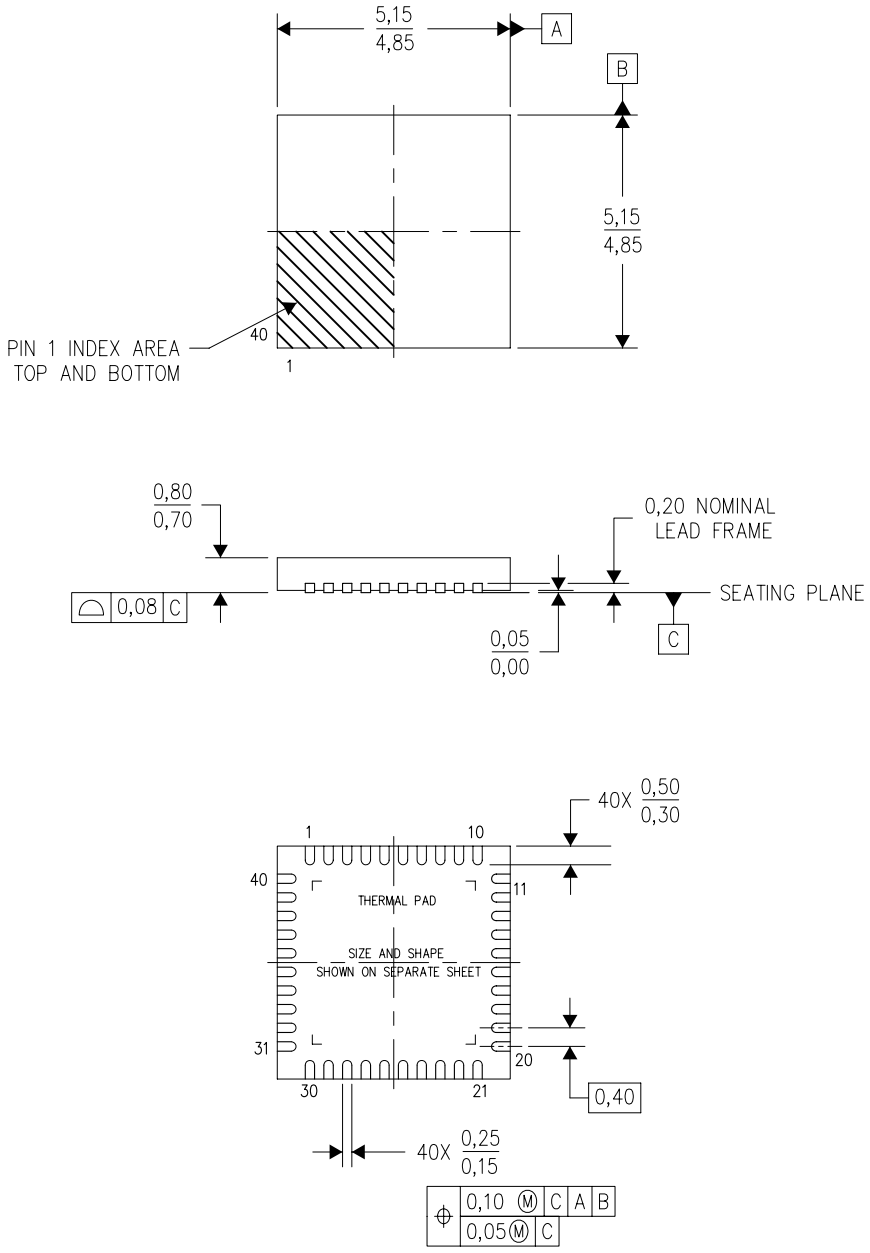
NOTE: All linear dimensions are in millimeters

RSB (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RSB (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



4207182/C 05/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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