LV14340 SIMPLE SWITCHER® 40 V 3.5 A, 2 MHz Step-Down Converter

1 Features

- 4 V to 40 V Input Range
- 3.5 A Continuous Output Current
- 100 mΩ High-Side MOSFET
- Minimum On Time: 100 ns
- Current Mode Control
- Adjustable Switching Frequency from 200 kHz to 2 MHz
- Frequency Synchronization to External Clock
- Internal Compensation for Ease of Use
- High Duty Cycle Operation Supported
- Precision Enable Input
- 1 µA Shutdown Current
- External Soft-start
- Thermal, Overvoltage and Short Protection
- 8-Pin SOIC with PowerPAD™ Package

2 Applications

- Automotive Battery Regulation
- Industrial Power Supplies
- Telecom and Datacom Systems
- Battery Powered Systems

3 Description

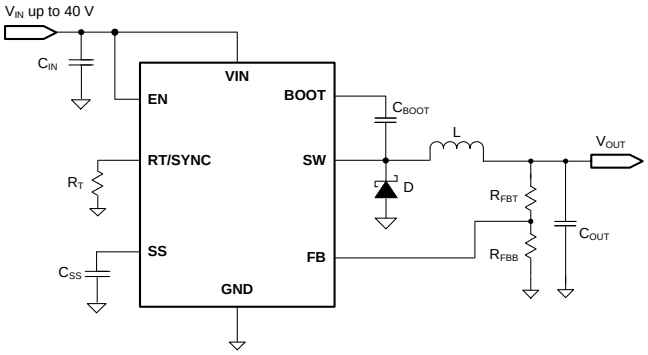
The LV14340 is a 40 V, 3.5 A step-down regulator with an integrated high-side MOSFET. With a wide input range from 4 V to 40 V, it's suitable for various applications from industrial to automotive for power conditioning from unregulated sources. A wide adjustable switching frequency range allows either efficiency or external component size to be optimized. Internal loop compensation means that the user is free from the tedious task of loop compensation design. This also minimizes the external components of the device. A precision enable input allows simplification of regulator control and system power sequencing. The device also has built-in protection features such as cycle-by-cycle current limit, thermal sensing, and shutdown due to excessive power dissipation, and output overvoltage protection.

Device Information(1)

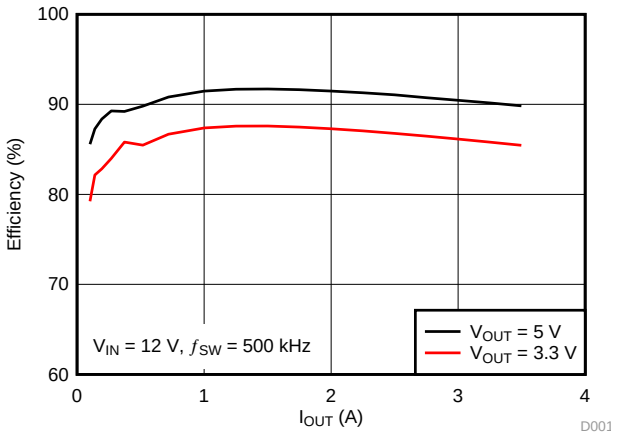
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LV14340	SOIC (8)	4.89 mm x 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



Efficiency vs Output Current



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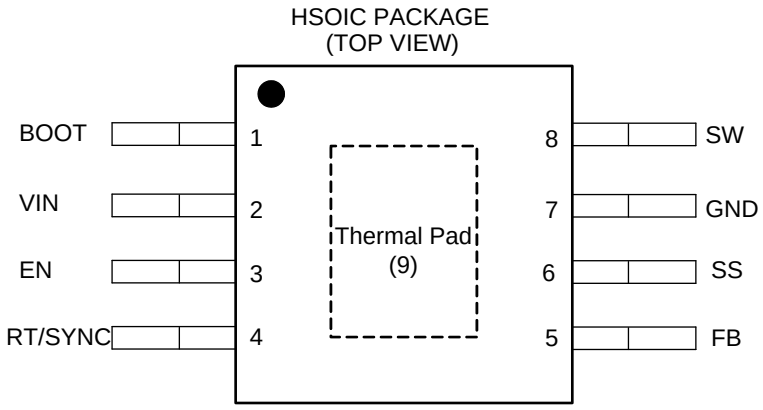
5 Revision History

Changes from Revision splat (June 2015) to Revision A **Page**

- Deleted S from part number ... 1

6 Pin Configuration and Functions

HSOIC
8-Pin
Top View



Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
BOOT	1	O	Bootstrap capacitor connection for high-side MOSFET driver. Connect a high quality 0.1 µF capacitor from BOOT to SW.
VIN	2	I	Connect to power supply and bypass capacitors C_{IN}. Path from VIN pin to high frequency bypass C_{IN} and GND must be as short as possible.
EN	3	I	Enable pin, with internal pull-up current source. Pull below 1.2 V to disable. Float or connect to VIN to enable. Adjust the input under voltage lockout with two resistors. See Enable and Adjustable Undervoltage Lockout.
RT/SYNC	4	I	Resistor Timing or External Clock input. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the operating mode returns to frequency programming by resistor.
FB	5	I	Feedback input pin, connect to the feedback divider to set V_{OUT}. Do not short this pin to ground during operation.
SS	6	O	Soft-start control pin. Connect to a capacitor to set soft-start time.
GND	7	G	System ground pin.
SW	8	O	Switching output of the regulator. Internally connected to high-side power MOSFET. Connect to power inductor.
Thermal Pad	9	G	Major heat dissipation path of the die. Must be connected to ground plane on PCB.

(1) I = Input, O = Output, G = Ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input Voltages	VIN, EN to GND	-0.3	44	V
	BOOT to GND	-0.3	49	
	SS to GND	-0.3	5	
	FB to GND	-0.3	7	
	RT/SYNC to GND	-0.3	3.6	
Output Voltages	BOOT to SW		6.5	V
	SW to GND	-3	44	
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM)(1)	±2000	V
		Charged device model (CDM)(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Buck Regulator	VIN	4	40	V
	VOUT	0.8	32	
	BOOT		45	
	SW	-1	40	
	FB	0	5	
Control	EN	0	40	V
	RT/SYNC	0	3.3	
	SS	0	3	
Frequency	Switching frequency range at RT mode	200	2000	kHz
	Switching frequency range at SYNC mode	250	2000	
Temperature	Operating junction temperature, T_J	-40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		DDA	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.9	
ψ_{JB}	Junction-to-board characterization parameter	25.4	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	25.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, the following conditions apply: V_{IN} = 4.0 V to 40 V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
POWER SUPPLY (VIN PIN)						
V_{IN}	Operation input voltage		4		40	V
UVLO	Undervoltage lockout thresholds	Rising threshold	3.5	3.7	3.9	V
		Hysteresis		285		mV
I_{SHDN}	Shutdown supply current	V_{EN} = 0 V, T_A = 25°C, 4.0 V ≤ V_{IN} ≤ 40 V		1	3	µA
I_Q	Operating quiescent current (non- switching)	V_{FB} = 1.0 V, T_A = 25°C		300		µA
ENABLE (EN PIN)						
V_{EN_TH}	EN Threshold Voltage		1.05	1.20	1.38	V
I_{EN_PIN}	EN PIN current	Enable threshold +50 mV		-4.6		µA
		Enable threshold -50 mV		-1		
I_{EN_HYS}	EN hysteresis current			-3.6		µA
EXTERNAL SOFT-START						
I_{SS}	SS pin current	T_A = 25°C		3		µA
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback voltage	T_J = 25°C	0.744	0.750	0.756	V
		T_J = -40°C to 125°C	0.735	0.750	0.765	V
HIGH-SIDE MOSFET						
R_{DS_ON}	On-resistance	V_{IN} = 12 V, BOOT to SW = 5.8 V		100	180	mΩ
High-side MOSFET CURRENT LIMIT						
I_{LIMT}	Current limit	V_{IN} = 12 V, T_A = 25°C, Open Loop	4.4	5.5	6.6	A
THERMAL PERFORMANCE						
T_{SHDN}	Thermal shutdown threshold			170		°C
T_{HYS}	Hysteresis			12		

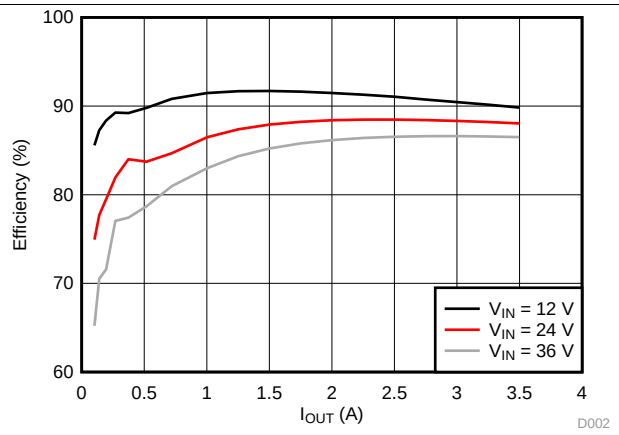
7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
f_{SW}	Switching frequency	R_T = 49.9 kΩ, 1% accuracy	400	500	600	kHz
V_{SYNC_HI}	SYNC clock high level threshold		1.7			V
V_{SYNC_LO}	SYNC clock low level threshold				0.5	
T_{SYNC_MIN}	Minimum SYNC input pulse width	Measured at 500 kHz, V_{SYNC_HI} > 3 V, V_{SYNC_LO} < 0.3 V		30		ns
T_{LOCK_IN}	PLL lock in time	Measured at 500 kHz		100		µs
T_{ON_MIN}	Minimum controllable on time	V_{IN} = 12 V, BOOT to SW = 5.8 V, I_{Load} = 1 A		100		ns
D_{MAX}	Maximum duty cycle	f_{SW} = 200 kHz		97%		

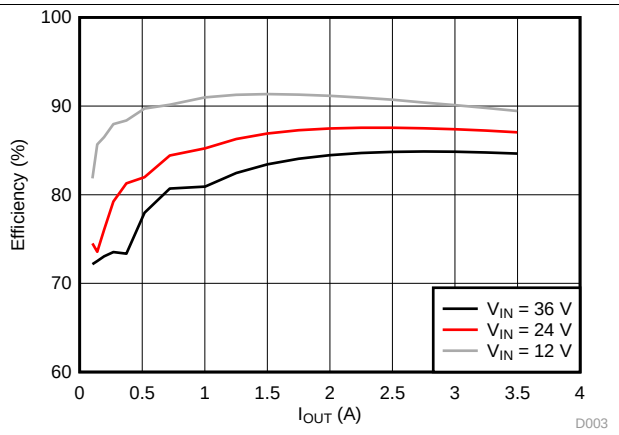
7.7 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 500 kHz, L = 5.6 µH, C_{OUT} = 47 µF x 2, T_A = 25°C.



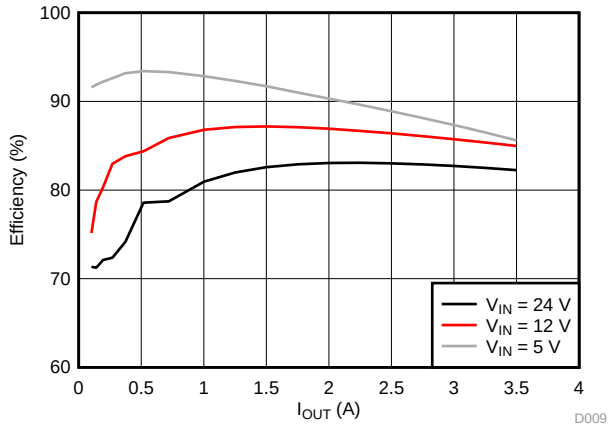
V_{OUT} = 5 V f_{SW} = 500 kHz

Figure 1. Efficiency vs. Load Current



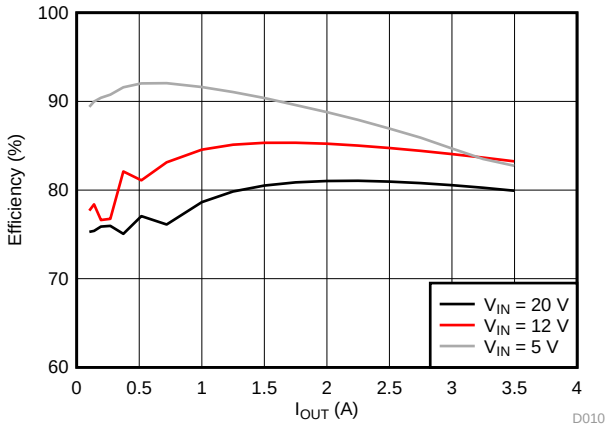
V_{OUT} = 5 V f_{SW} = 1 MHz

Figure 2. Efficiency vs. Load Current



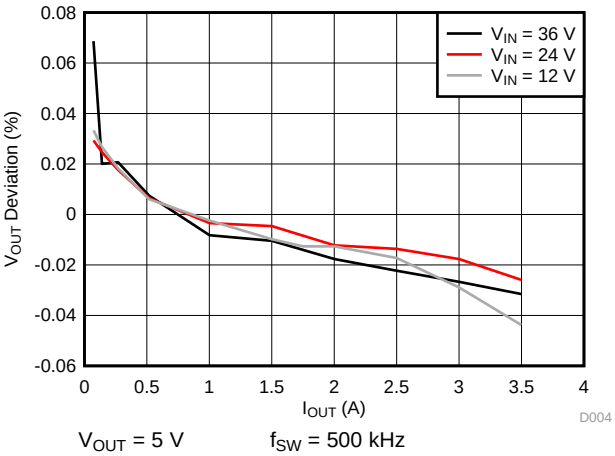
V_{OUT} = 3.3 V f_{SW} = 1 MHz

Figure 3. Efficiency vs. Load Current



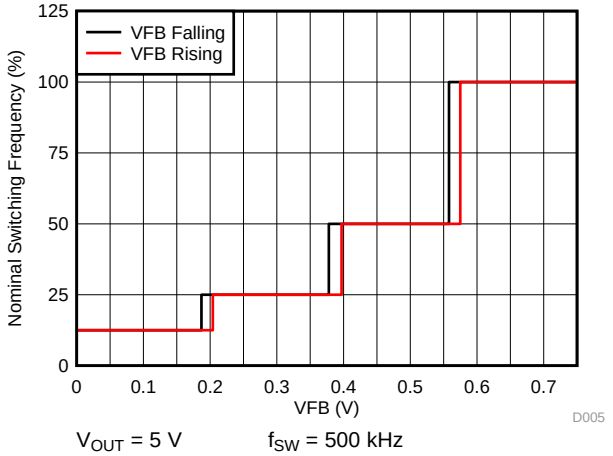
V_{OUT} = 3.3 V f_{SW} = 2 MHz

Figure 4. Efficiency vs. Load Current



V_{OUT} = 5 V f_{SW} = 500 kHz

Figure 5. Load Regulation

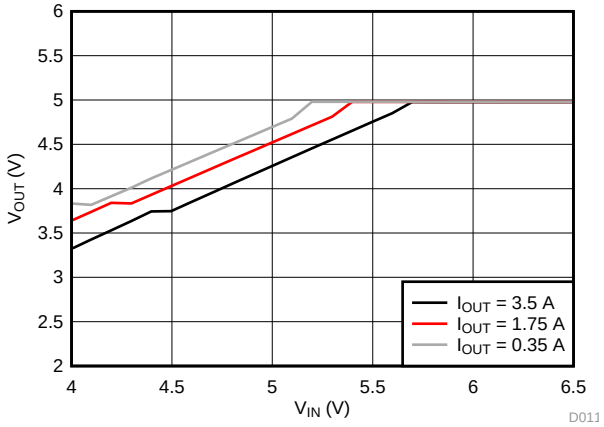


V_{OUT} = 5 V f_{SW} = 500 kHz

Figure 6. Frequency vs V_{FB}

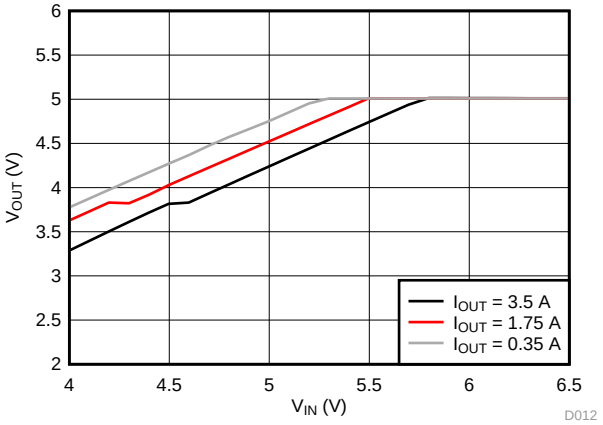
Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 500 kHz, L = 5.6 µH, C_{OUT} = 47 µF x 2, T_A = 25°C.



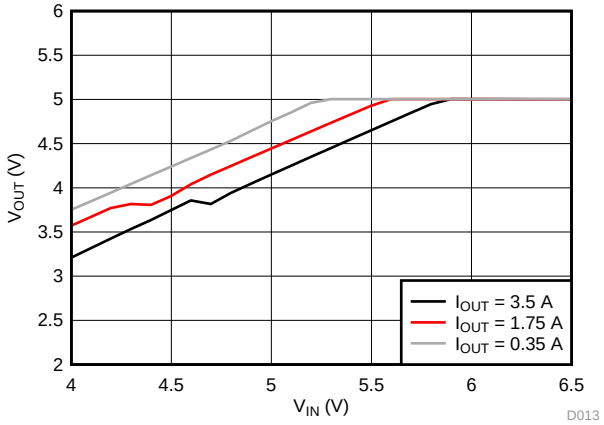
V_{OUT} = 5 V f_{SW} = 500 kHz

Figure 7. Dropout Curve



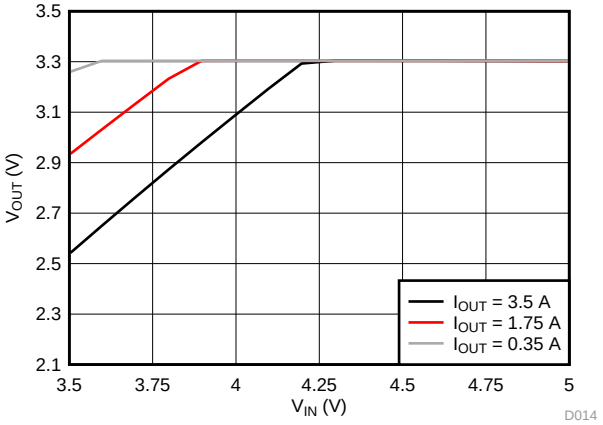
V_{OUT} = 5V f_{SW} = 1 MHz

Figure 8. Dropout Curve



V_{OUT} = 5 V f_{SW} = 2 MHz

Figure 9. Dropout Curve



V_{OUT} = 3.3 V f_{SW} = 2 MHz

Figure 10. Dropout Curve

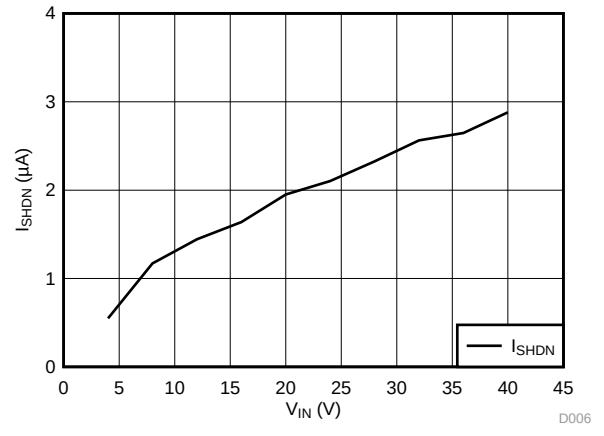
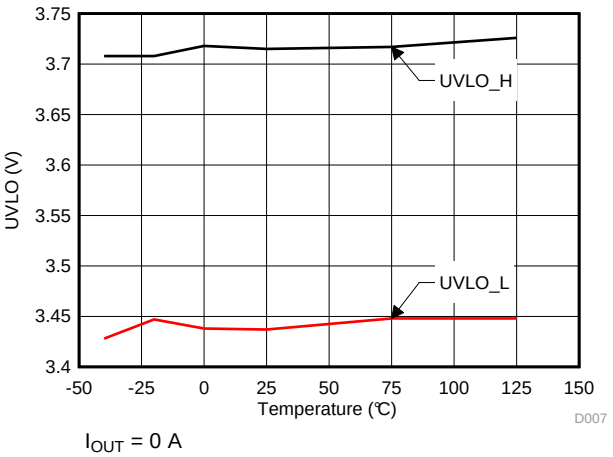


Figure 11. Shut-down Current



I_{OUT} = 0 A

Figure 12. UVLO Threshold

8 Detailed Description

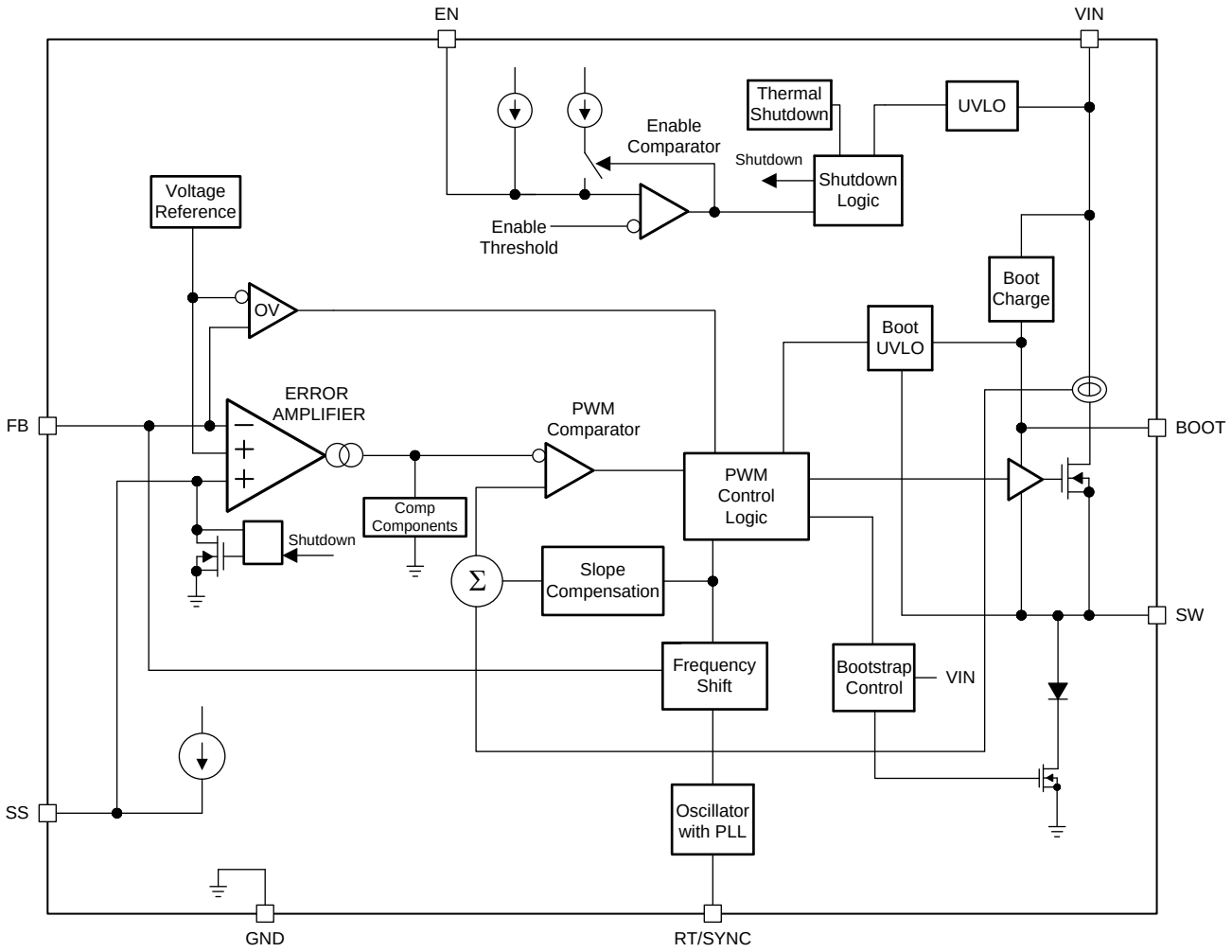
8.1 Overview

The LV14340 SIMPLE SWITCHER® regulator is an easy to use step-down DC-DC converter that operates from 4.0 V to 40 V supply voltage. It integrates a 100 mΩ (typical) high-side MOSFET, and is capable of delivering up to 3.5 A DC load current with exceptional efficiency and thermal performance in a very small solution size. The operating current is typically 300 µA under no load condition (not switching). When the device is disabled, the supply current is typically 1 µA. An extended family is available in 2 A and 5 A load options in pin to pin compatible packages.

The LV14340 implements constant frequency peak current mode control with pulse skipping mode at light load to achieve high efficiency. The device is internally compensated, which reduces design time, and requires fewer external components. The switching frequency is programmable from 200 kHz to 2 MHz by an external resistor R_T. The LV14340 is also capable of synchronization to an external clock within the 250 kHz to 2 MHz frequency range, which allows the device to be optimized to fit small board space at higher frequency, or high efficient power conversion at lower frequency.

Other optional features are included for more comprehensive system requirements, including precision enable, adjustable soft-start time, and approximate 97% duty cycle by BOOT capacitor recharge circuit. These features provide a flexible and easy to use platform for a wide range of applications. Protection features include over temperature shutdown, V_{OUT} overvoltage protection (OVP), V_{IN} under-voltage lockout (UVLO), cycle-by-cycle current limit, and short-circuit protection with frequency fold-back.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed Frequency Peak Current Mode Control

The following operation description of the LV14340 will refer to the Function Block Diagram and to the waveforms in Figure 13. LV14340 output voltage is regulated by turning on the high-side N-MOSFET with controlled ON time. During high-side switch ON time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current i_L increase with linear slope ($V_{IN} – V_{OUT}$) / L. When high-side switch is off, inductor current discharges through freewheel diode with a slope of $–V_{OUT}$ / L. The control parameter of Buck converter is defined as Duty Cycle D = t_{ON} /T_{SW}, where t_{ON} is the high-side switch ON time and T_{SW} is the switching period. The regulator control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal Buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = V_{OUT} / V_{IN}.

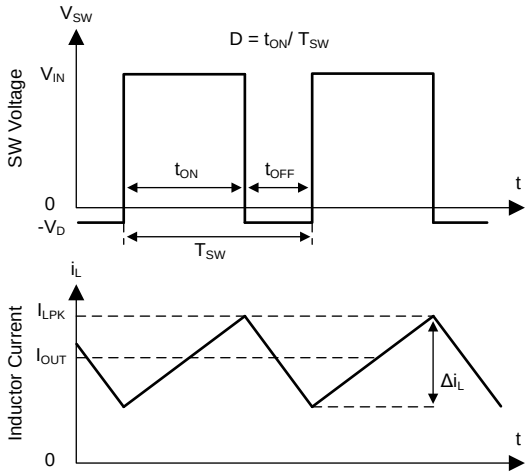


Figure 13. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The LV14340 employs fixed frequency peak current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current to control the ON time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, makes it easy to design, and provides stable operation with almost any combination of output capacitors. The regulator operates with fixed switching frequency at normal load condition. At very light load, the LV14340 will operate in pulse skipping mode to maintain high efficiency and the switching frequency will decrease with reduced load current.

8.3.2 Slope Compensation

The LV14340 adds a compensating ramp to the MOSFET switch current sense signal. This slope compensation prevents sub-harmonic oscillations at duty cycle greater than 50%. The peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

8.3.3 Pulse Skipping Mode

The LV14340 operates in pulse skipping mode (PSM) at light load current to improve efficiency by reducing switching and gate drive losses. If the output voltage is within regulation and the peak switching current at the end of any switching cycle is below the current threshold of 300 mA, the device enters PSM. The PSM current threshold is the peak switch current level corresponding to a nominal internal COMP voltage of 400 mV.

When in PSM, the internal COMP voltage is clamped at 400 mV and the high-side MOSFET is inhibited, and the device draws about 300 µA input quiescent current. Since the device is not switching, the output voltage begins to decay. The voltage control loop responds to the falling output voltage by increasing the internal COMP voltage. The high-side MOSFET is enabled and switching resumes when the error amplifier lifts internal COMP voltage above 400 mV. The output voltage recovers to the regulated value, and internal COMP voltage eventually falls below the PSM threshold at which time the device again enters PSM.

Feature Description (continued)

8.3.4 Low Dropout Operation and Bootstrap Voltage (BOOT)

The LV14340 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and the external low side diode conducts. The recommended value of the BOOT capacitor is 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 16 V or higher is recommended for stable performance over temperature and voltage.

When operating with a low voltage difference from input to output, the high-side MOSFET of the LV14340 will operate at approximate 97% duty cycle. When the high-side MOSFET is continuously on for 5 or 6 switching cycles (5 or 6 switching cycles for frequency lower than 1 MHz, and 10 or 11 switching cycles for frequency higher than 1 MHz) and the voltage from BOOT to SW drops below 3.2 V, the high-side MOSFET is turned off and an integrated low side MOSFET pulls SW low to recharge the BOOT capacitor.

Since the gate drive current sourced from the BOOT capacitor is small, the high-side MOSFET can remain on for many switching cycles before the MOSFET is turned off to refresh the capacitor. Thus the effective duty cycle of the switching regulator can be high, approaching 97%. The effective duty cycle of the converter during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low side diode voltage and the printed circuit board resistance.

8.3.5 Adjustable Output Voltage

The internal voltage reference produces a precise 0.75 V (typical) voltage reference over the operating temperature. The output voltage is set by a resistor divider from output voltage to the FB pin. It is recommended to use 1% tolerance or better and temperature coefficient of 100 ppm or lower divider resistors. Select the low side resistor R_{FBB} for the desired divider current and use Equation 1 to calculate high-side R_{FBT}. Larger value divider resistors are good for efficiency at light load. However, if the values are too high, the regulator will be more susceptible to noise and voltage errors from the FB input current may become noticeable. R_{FBB} in the range from 10 kΩ to 100 kΩ is recommended for most applications.

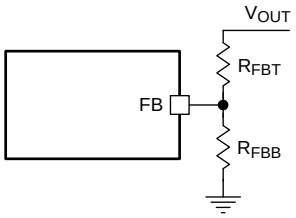


Figure 14. Output Voltage Setting

$$R_{FBT} = \frac{V_{OUT} - 0.75}{0.75} R_{FBB} \quad (1)$$

8.3.6 Enable and Adjustable Undervoltage Lockout

The LV14340 is enabled when the VIN pin voltage rises above 3.7 V (typical) and the EN pin voltage exceeds the enable threshold of 1.2 V (typical). The LV14340 is disabled when the VIN pin voltage falls below 3.52 V (typical) or when the EN pin voltage is below 1.2 V. The EN pin has an internal pull-up current source (typically I_{EN} = 1 µA) that enables operation of the LV14340 when the EN pin is floating.

Many applications will benefit from the employment of an enable divider R_{ENT} and R_{ENB} in Figure 15 to establish a precision system UVLO level for the stage. System UVLO can be used for supplies operating from utility power as well as battery power. It can be used for sequencing, ensuring reliable operation, or supply protection, such as a battery. An external logic signal can also be used to drive EN input for system sequencing and protection.

When EN terminal voltage exceeds 1.2 V, an additional hysteresis current (typically I_{HYS} = 3.6 µA) is sourced out of EN terminal. When the EN terminal is pulled below 1.2 V, I_{HYS} current is removed. This additional current facilitates adjustable input voltage UVLO hysteresis. Use Equation 2 and Equation 3 to calculate R_{ENT} and R_{ENB} for desired UVLO hysteresis voltage.

Feature Description (continued)

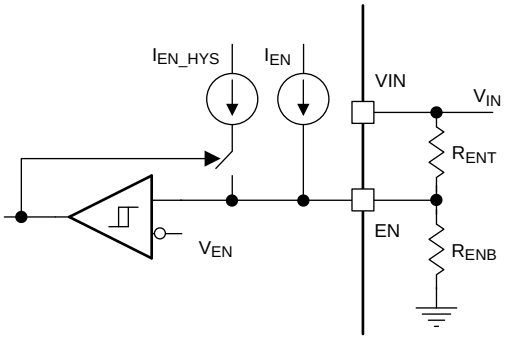


Figure 15. System UVLO By Enable Dividers

$$R_{ENT} = \frac{V_{START} - V_{STOP}}{I_{HYS}} \quad (2)$$

$$R_{ENB} = \frac{V_{EN}}{\frac{V_{START} - V_{EN}}{R_{ENT}} + I_{EN}} \quad (3)$$

where V_{START} is the desired voltage threshold to enable LV14340, V_{STOP} is the desired voltage threshold to disable device.

8.3.7 External Soft-Start

The LV14340 has soft-start pin for programmable output ramp up time. The soft-start feature is used to prevent inrush current impacting the LV14340 and its load when power is first applied. The soft-start time can be programed by connecting an external capacitor C_{SS} from SS pin to GND. An internal current source (typically I_{SS} = 3 µA) charges C_{SS} and generates a ramp from 0 V to V_{REF}. The soft-start time can be calculated by Equation 4:

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (4)$$

The internal soft-start resets while device is disabled or in thermal shutdown.

8.3.8 Switching Frequency and Synchronization (RT/SYNC)

The switching frequency of the LV14340 can be programmed by the resistor R_T from the RT/SYNC pin and GND pin. The RT/SYNC pin can't be left floating or shorted to ground. To determine the timing resistance for a given switching frequency, use Equation 5 or the curve in Figure 16. Table 1 gives typical R_T values for a given f_{SW}.

$$R_T(k\Omega) = 32537 \times f_{SW}(kHz)^{-1.045} \quad (5)$$

Feature Description (continued)

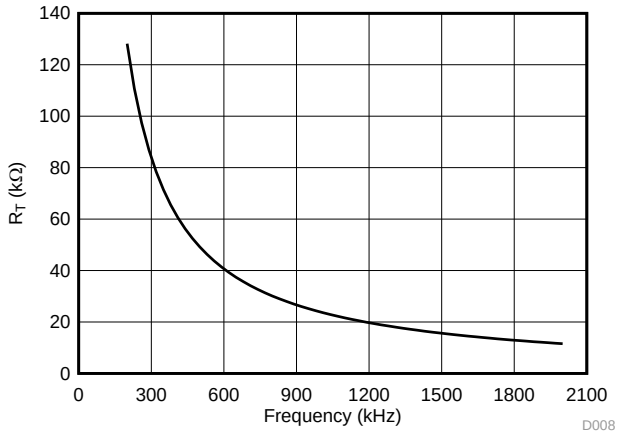


Figure 16. R_T vs Frequency Curve

Table 1. Typical Frequency Setting R_T Resistance

f_{SW} (kHz)	R_T (kΩ)
200	127
350	71.5
500	49.9
750	32.4
1000	23.7
1500	15.8
2000	11.5

The LV14340 switching action can also be synchronized to an external clock from 250 kHz to 2 MHz. Connect a square wave to the RT/SYNC pin through either circuit network shown in Figure 17. Internal oscillator is synchronized by the falling edge of external clock. The recommendations for the external clock include: high level no lower than 1.7 V, low level no higher than 0.5 V and have a pulse width greater than 30 ns. When using a low impedance signal source, the frequency setting resistor R_T is connected in parallel with an AC coupling capacitor C_{COUP} to a termination resistor R_{TERM} (e.g., 50 Ω). The two resistors in series provide the default frequency setting resistance when the signal source is turned off. A 10 pF ceramic capacitor can be used for C_{COUP}. Figure 18, Figure 19 and Figure 20 show the device synchronized to an external system clock.

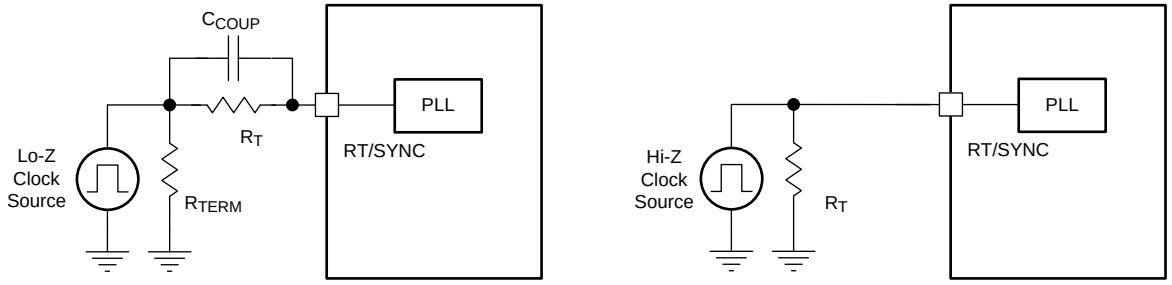


Figure 17. Synchronizing to an External Clock

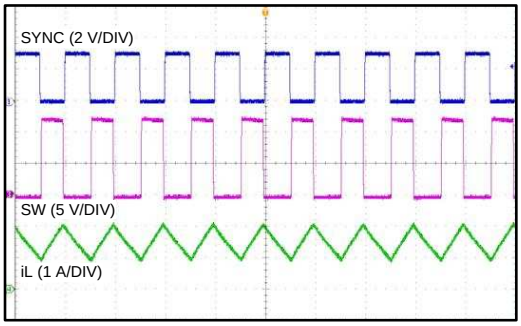


Figure 18. Synchronizing in CCM

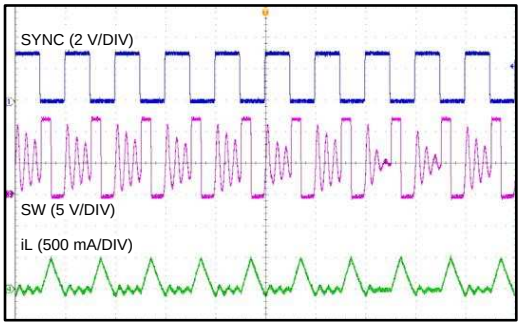


Figure 19. Synchronizing in DCM

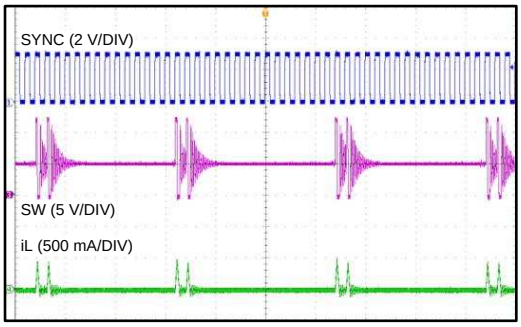


Figure 20. Synchronizing in PSM

Equation 6 calculates the maximum switching frequency limitation set by the minimum controllable on time and the input to output step down ratio. Setting the switching frequency above this value will cause the regulator to skip switching pulses to achieve the low duty cycle required at maximum input voltage.

$$f_{SW(max)} = \frac{1}{t_{ON}} \times \left(\frac{I_{OUT} \times R_{IND} + V_{OUT} + V_D}{V_{IN\_MAX} - I_{OUT} \times R_{DS\_ON} + V_D} \right) \quad (6)$$

where

- I_{OUT} = Output current
- R_{IND} = Inductor series resistance
- V_{IN_MAX} = Maximum input voltage
- V_{OUT} = Output voltage
- V_D = Diode voltage drop
- R_{DS_ON} = High-side MOSFET switch on resistance
- t_{ON} = Minimum on time

8.3.9 Overcurrent and Short Circuit Protection

The LV14340 is protected from overcurrent condition by cycle-by-cycle current limiting on the peak current of the high-side MOSFET. High-side MOSFET overcurrent protection is implemented by the nature of the Peak Current Mode control. The high-side switch current is compared to the output of the Error Amplifier (EA) minus slope compensation every switching cycle. Please refer to Functional Block Diagram for more details. The peak current of high-side switch is limited by a clamped maximum peak current threshold which is constant. So the peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

The LV14340 also implements a frequency fold-back to protect the converter in severe over-current or short conditions. The oscillator frequency is divided by 2, 4, and 8 as the FB pin voltage decrease to 75%, 50%, 25% of V_{REF}. The frequency fold-back increases the off time by increasing the period of the switching cycle, so that it provides more time for the inductor current to ramp down and leads to a lower average inductor current. Lower frequency also means lower switching loss. Frequency fold-back reduces power dissipation and prevents overheating and potential damage to the device.

8.3.10 Overvoltage Protection

The LV14340 employs an output overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low output capacitance. The OVP feature minimizes output overshoot by turning off high-side switch immediately when FB voltage reaches to the rising OVP threshold which is nominally 109% of the internal voltage reference V_{REF}. When the FB voltage drops below the falling OVP threshold which is nominally 107% of V_{REF}, the high-side MOSFET resumes normal operation.

8.3.11 Thermal Shutdown

The LV14340 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 170°C (typical). The high-side MOSFET stops switching when thermal shundown activates. Once the die temperature falls below 158°C (typical), the device reinitiates the power up sequence controlled by the internal soft-start circuitry.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LV14340 is a step down DC-to-DC regulator. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 3.5 A. The following design procedure can be used to select components for the LV14340. This section presents a simplified discussion of the design process.

9.2 Typical Application

The LV14340 only requires a few external components to convert from wide voltage range supply to a fixed output voltage. A schematic of 5 V/3.5 A application circuit is shown in Figure 21. The external components have to fulfill the needs of the application, but also the stability criteria of the device's control loop.

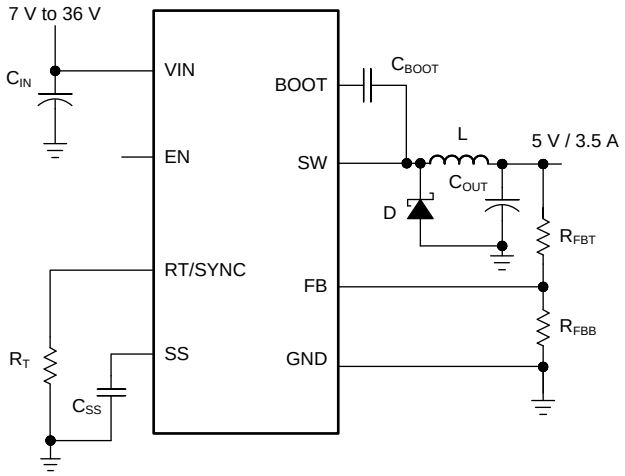


Figure 21. Application Circuit, 5-V Output

9.2.1 Design Requirements

This example details the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level:

Input Voltage, V_{IN}	7 V to 36 V, Typical 12 V
Output Voltage, V_{OUT}	5.0 V
Maximum Output Current I_{O_MAX}	3.5 A
瞬态响应 Transient Response 0.35 A to 3.5 A	5%
Output Voltage Ripple	50 mV
Input Voltage Ripple	400 mV
Switching Frequency f_{SW}	500 kHz
Soft-start time	5 ms

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Set-Point

The output voltage of LV14340 is externally adjustable using a resistor divider network. The divider network is comprised of top feedback resistor R_{FBT} and bottom feedback resistor R_{FBB}. Equation 7 is used to determine the output voltage:

$$R_{FBT} = \frac{V_{OUT} - 0.75}{0.75} R_{FBB} \tag{7}$$

Choose the value of R_{FBT} to be 100 kΩ. With the desired output voltage set to 5 V and the V_{FB} = 0.75 V, the R_{FBB} value can then be calculated using Equation 7. The formula yields to a value 17.65 kΩ. Choose the closest available value of 17.8 kΩ for R_{FBB}.

9.2.2.2 Switching Frequency

For desired frequency, use Equation 8 to calculate the required value for R_T.

$$R_T(k\Omega) = 32537 \times f_{SW}(kHz)^{-1.045} \tag{8}$$

For 500 kHz, the calculated R_T is 49.2 kΩ and standard value 49.9 kΩ can be used to set the switching frequency at 500 kHz.

9.2.2.3 Output Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current and the RMS current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Since the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use Equation 10 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. A reasonable value of K_{IND} should be 20%-40%. During an instantaneous short or over current operation event, the RMS and peak inductor current can be high. The inductor current rating should be higher than current limit.

$$\Delta i_L = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times L \times f_{SW}} \tag{9}$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \tag{10}$$

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. But too low of an inductance can generate too large of an inductor current ripple such that over current protection at the full load could be falsely trigged. It also generates more conduction loss since the RMS current is slightly higher. Larger inductor current ripple also implies larger output voltage ripple with same output capacitors. With peak current mode control, it is not recommended to have too small of an inductor current ripple. A larger peak current ripple improves the comparator signal to noise ratio.

For this design example, choose K_{IND} = 0.4, the minimum inductor value is calculated to be 6.12 µH, and a nearest standard value is chosen: 6.5 µH. A standard 6.5 µH ferrite inductor with a capability of 5 A RMS current and 7A saturation current can be used.

9.2.2.4 Output Capacitor Selection

The output capacitor(s), C_{OUT}, should be chosen with care since it directly affects the steady state output voltage ripple, loop stability and the voltage over/undershoot during load current transients.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta i_L \times ESR = K_{IND} \times I_{OUT} \times ESR \tag{11}$$

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\_C} = \frac{\Delta i_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K_{IND} \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \tag{12}$$

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with presence of large current steps and fast slew rate. When a fast large load increase happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The regulator's control loop usually needs three or more clock cycles to respond to the output voltage droop. The output capacitance must be large enough to supply the current difference for three clock cycles to maintain the output voltage within the specified range. Equation 13 shows the minimum output capacitance needed for specified output undershoot. When a sudden large load decrease happens, the output capacitors absorb energy stored in the inductor. The catch diode can't sink current so the energy stored in the inductor results in an output voltage overshoot. Equation 14 calculates the minimum capacitance required to keep the voltage overshoot within a specified range.

$$C_{OUT} > \frac{3 \times (I_{OH} - I_{OL})}{f_{SW} \times V_{US}} \tag{13}$$

$$C_{OUT} > \frac{I_{OH}^2 - I_{OL}^2}{(V_{OUT} + V_{OS})^2 - V_{OUT}^2} \times L$$

where

- K_{IND} = Ripple ratio of the inductor ripple current (Δi_L / I_{OUT})
- I_{OL} = Low level output current during load transient
- I_{OH} = High level output current during load transient
- V_{US} = Target output voltage undershoot
- V_{OS} = Target output voltage overshoot (14)

For this design example, the target output ripple is 50 mV. Presuppose ΔV_{OUT_ESR} = ΔV_{OUT_C} = 50 mV, and chose K_{IND} = 0.4. Equation 11 yields ESR no larger than 35.7 mΩ and Equation 12 yields C_{OUT} no smaller than 7 µF. For the target over/undershoot range of this design, V_{US} = V_{OS} = 5% × V_{OUT} = 250 mV. The C_{OUT} can be calculated to be no smaller than 75.6 µF and 30.8 µF by Equation 13 and Equation 14 respectively. In summary, the most stringent criteria for the output capacitor is 75.6 µF. Two 47 µF, 16 V, X7R ceramic capacitors with 5 mΩ ESR are used in parallel.

9.2.2.5 Schottky Diode Selection

The breakdown voltage rating of the diode is preferred to be 25% higher than the maximum input voltage. The current rating for the diode should be equal to the maximum output current for best reliability in most applications. In cases where the input voltage is much greater than the output voltage the average diode current is lower. In this case it is possible to use a diode with a lower average current rating, approximately (1-D) × I_{OUT} however the peak current rating should be higher than the maximum load current. A 4 A to 5 A rated diode is a good starting point.

9.2.2.6 Input Capacitor Selection

The LV14340 device requires high frequency input decoupling capacitor(s) and a bulk input capacitor, depending on the application. The typical recommended value for the high frequency decoupling capacitor is 4.7 µF to 10 µF. A high-quality ceramic capacitor type X5R or X7R with sufficiency voltage rating is recommended. To compensate the derating of ceramic capacitors, a voltage rating of twice the maximum input voltage is recommended. Additionally, some bulk capacitance can be required, especially if the LV14340 circuit is not located within approximately 5 cm from the input voltage source. This capacitor is used to provide damping to the voltage spike due to the lead inductance of the cable or the trace. For this design, two 2.2 µF, X7R ceramic capacitors rated for 100 V are used. A 0.1 µF for high-frequency filtering and place it as close as possible to the device pins.

9.2.2.7 Bootstrap Capacitor Selection

Every LV14340 design requires a bootstrap capacitor (C_{BOOT}). The recommended capacitor is 0.1 µF and rated 16 V or higher. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor must be a high-quality ceramic type with an X7R or X5R grade dielectric for temperature stability.

9.2.2.8 Soft-start Capacitor Selection

Use Equation 15 in order to calculate the soft-start capacitor value:

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)}$$

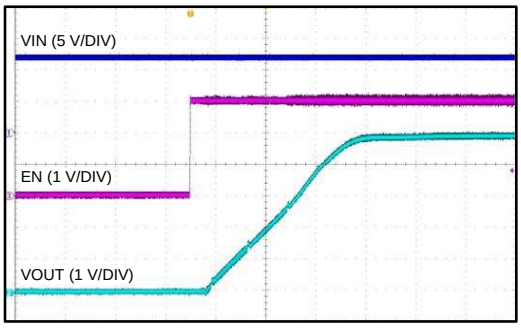
where

- C_{SS} = Soft-start capacitor value
- I_{SS} = Soft-start charging current (3 µA)
- t_{SS} = Desired soft-start time (15)

For the desired soft-start time of 5 ms and soft-start charging current of 3.0 µA, Equation 15 yields a soft-start capacitor value of 20 nF, a standard 22 nF ceramic capacitor is used.

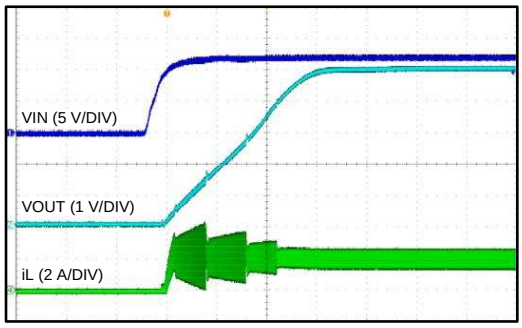
9.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 500 kHz, L = 5.6 µH, C_{OUT} = 47 µF x 2, T_A = 25°C.



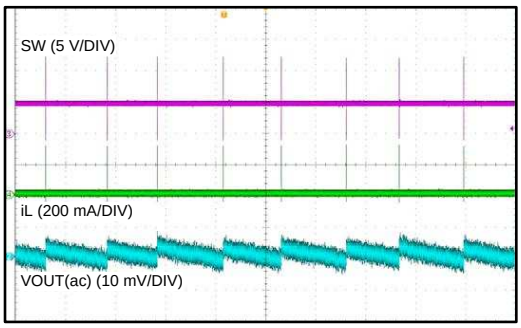
V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 2 A

Figure 22. Start-up By EN



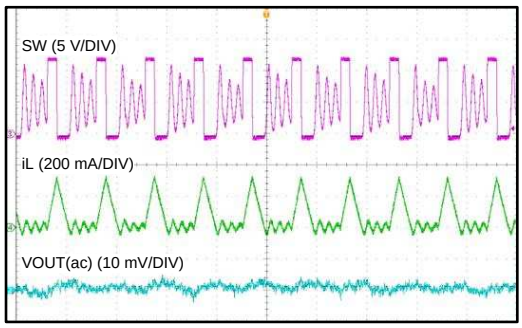
V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 2 A

Figure 23. Start-up By V_{IN}



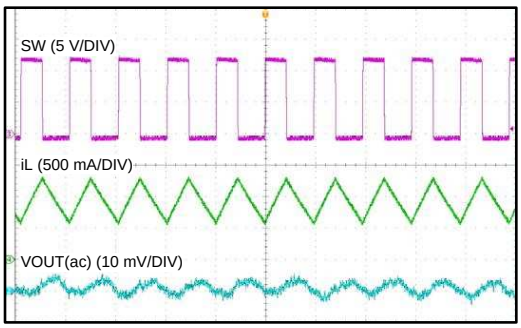
V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 0 A

Figure 24. Pulse Skipping Mode



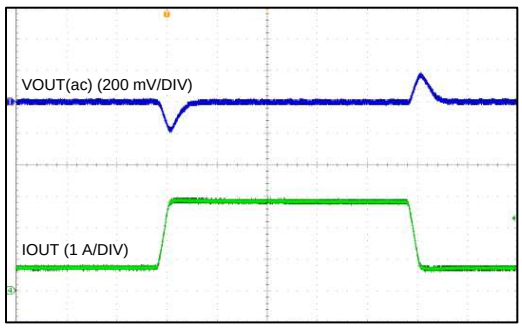
V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 100 mA

Figure 25. DCM Mode



V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 1.5 A

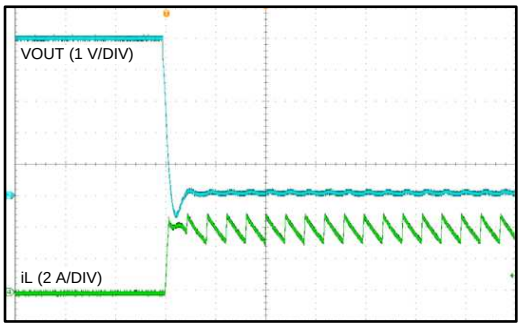
Figure 26. CCM Mode



I_{OUT}: 20% → 80% of 3.5 A Slew rate = 100 mA/µs

Figure 27. Load Transient

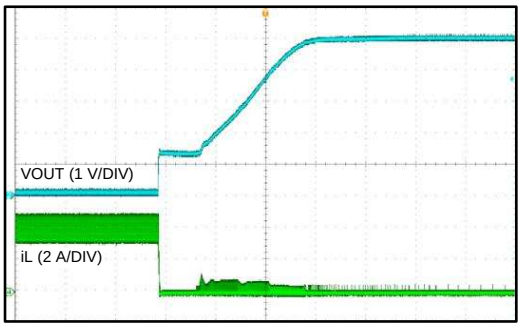
Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 500 kHz, L = 5.6 µH, C_{OUT} = 47 µF x 2, T_A = 25°C.



Time (40 µs/DIV)

V_{IN} = 12 V V_{OUT} = 5 V

Figure 28. Output Short



Time (2 ms/DIV)

V_{IN} = 12 V V_{OUT} = 5 V

Figure 29. Output Short Recovery

10 Power Supply Recommendations

The LV14340 is designed to operate from an input voltage supply range between 4 V and 40 V. This input supply should be able to withstand the maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LV14340 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LV14340, additional bulk capacitance may be required in addition to the ceramic input capacitors. The amount of bulk capacitance is not critical, but a 47 µF or 100 µF electrolytic capacitor is a typical choice.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The feedback network, resistor R_{FBT} and R_{FBB}, should be kept close to the FB pin. V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielding layer.
2. The input bypass capacitor C_{IN} must be placed as close as possible to the VIN pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD.
3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.
4. The output capacitor, C_{OUT} should be placed close to the junction of L and the diode D. The L, D, and C_{OUT} trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.
5. The ground connection for the diode, C_{IN}, and C_{OUT} should be as small as possible and tied to the system ground plane in only one spot (preferably at the C_{OUT} ground point) to minimize conducted noise in the system ground plane
6. For more detail on switching power supply layout considerations see Application Note AN-1149.

11.2 Layout Example

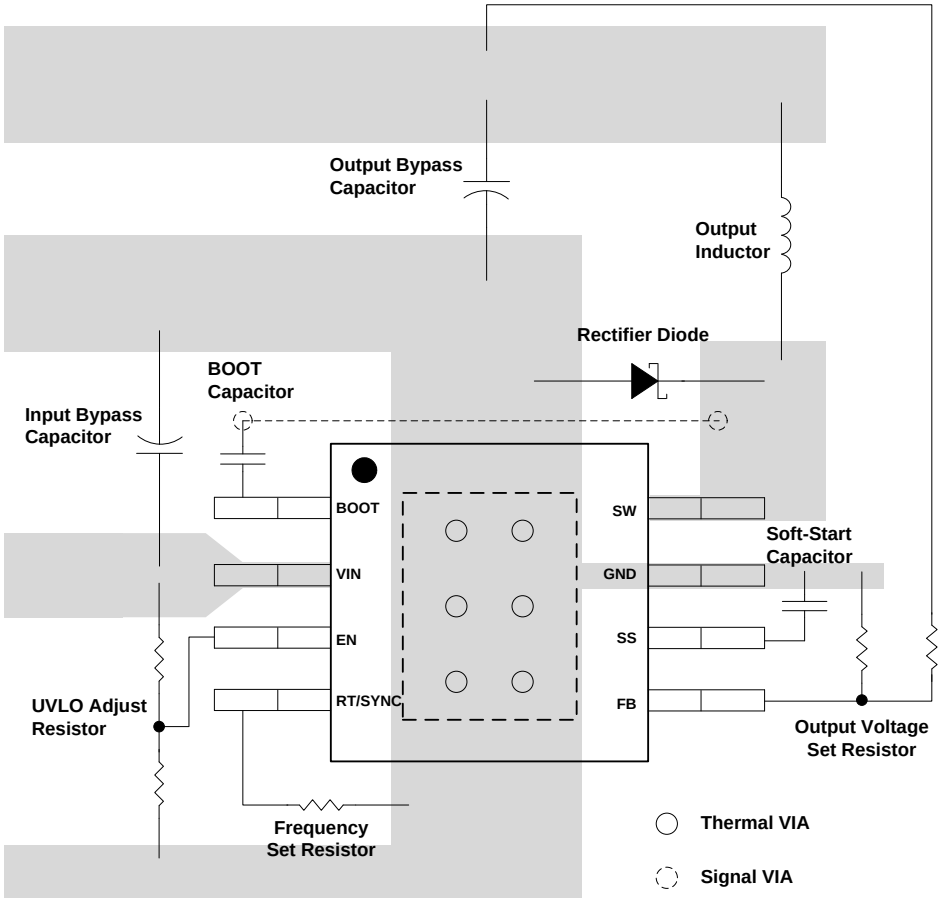


Figure 30. Layout

12 Device and Documentation Support

12.1 Trademarks

PowerPAD is a trademark of Texas Instruments.
SIMPLE SWITCHER is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4) (5)
LV14340DDA	ACTIVE	SO8 PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NiPdAu	Level-2-260C-1 YEAR	-40 to 125	DB3SV
LV14340DDAR	ACTIVE	SO8 PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NiPdAu	Level-2-260C-1 YEAR	-40 to 125	DB3SV

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

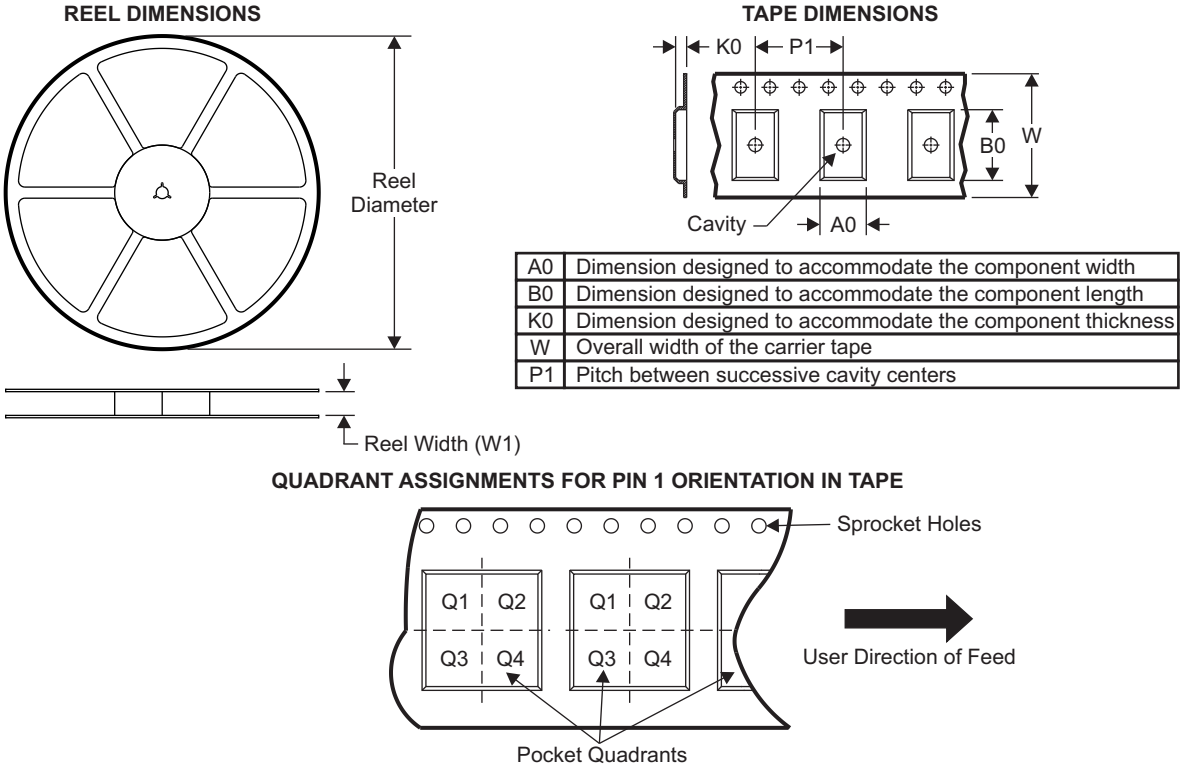
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

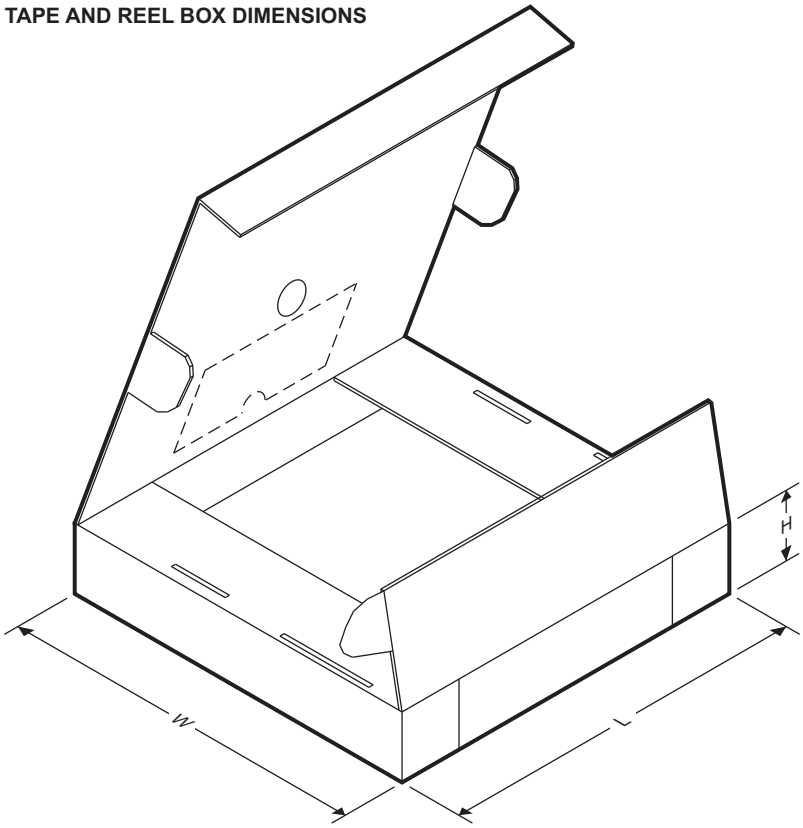
13.1.2 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

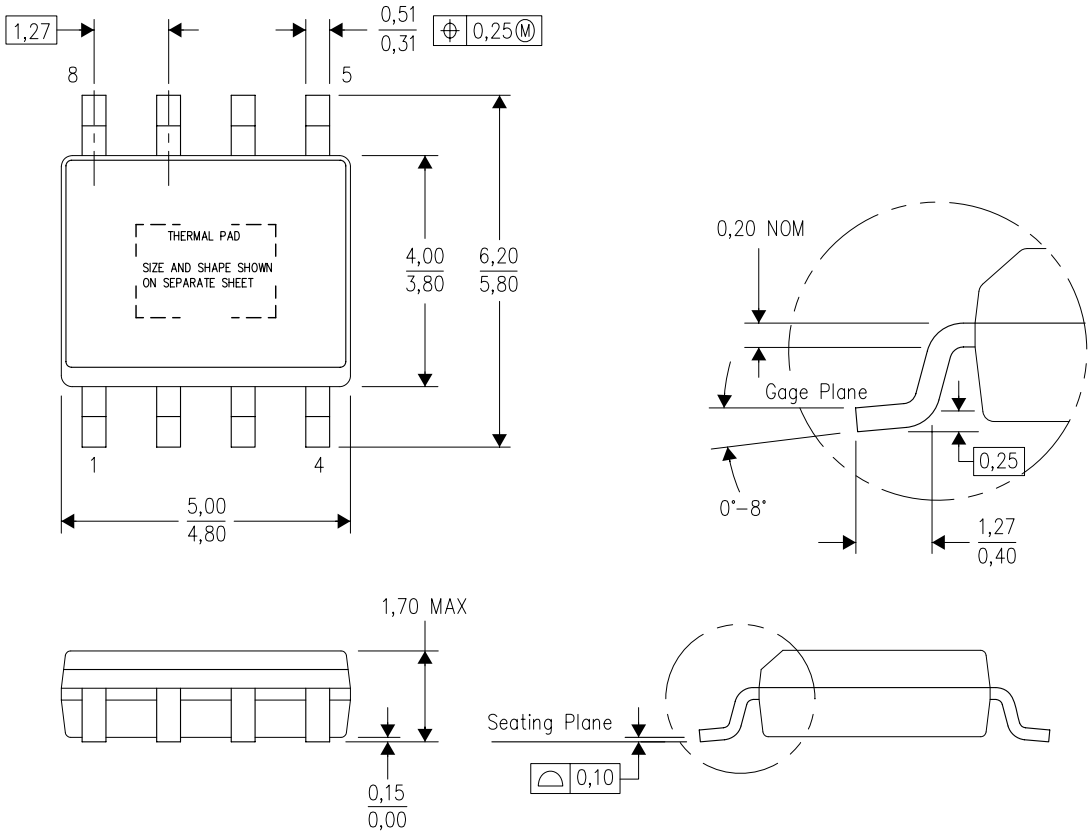
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LV14340DDAR	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LV14340DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

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