Application Report
SNVA722B–September 2014–Revised February 2015

# Inverting Applications Made SIMPLE with LM4600x and LM4360x

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**ABSTRACT**

We often require power sources with negative output voltages. There are many different ways to produce a negative output voltage from a positive input voltage. One option is a polarity-inverting buck-boost converter. The advantages of this topology are that it requires low component count and that it can be built with standard high-side regulator ICs such as those intended for buck regulators. The LM4360x and LM4600x synchronous family of SIMPLE SWITCHER® converters can be used in an inverting buck-boost topology to provide a regulated negative output voltage rail in the system.

This user guide will demonstrate the use of LM46002 in an inverting buck-boost application. The design accepts an input voltage of 15 V to 45 V and can provide an output voltage of -15 V capable of supplying a range of output current to the load up to 1 A.

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## 1 Introduction

The LM4360x and LM4600x SIMPLE SWITCHER® regulators are easy to use Wide $V_{IN}$ synchronous step-down DC-DC converters capable of delivering up to 3 A of load current from an input voltage of 3.5 V to 36 V, and up to 2 A for an input voltage of 60 V respectively. These converters provide very high efficiency, output accuracy and drop-out voltage in a very small solution size. An extended family in pin-to-pin compatible packages is available in 0.5 A and 1 A load current options.

The simplicity of the polarity-inverting buck-boost topology is one of its biggest advantages. The topology needs very few power stage components thereby reducing the cost and development complexity. Besides providing negative voltages in systems the polarity-inverting topology is very useful to power loads that do not depend on a polarity in reference to a system ground but are being supplied by an input voltage which might be higher or lower than the output voltage. A good example is powering a string of LEDs with a total voltage drop of 16V from a supply voltage in the range between 9 V and 30 V. In this example, the string of LEDs can accept a negative 16 V, since the LEDs may just be turned around by swapping the anode connection with the cathode connection. The polarity inverting topology can power the negative 16 V from positive 9 V of input voltage as well as from 30V of input voltage.

Compared to the buck and the boost topology, the inverting topology has the main energy storing element, the inductor, connected between the switch node and ground. In the buck topology the inductor is connected to the output node, in the boost topology the inductor is connected to the input node. The inductor always prevents current from changing instantaneously. Thus the inductor acts as part of a filter to reduce noise on a specific node. The polarity-inverting topology is noisy on the input side as well as on the output side. Noisy nodes require good capacitive filtering to reduce the ripple voltage. In the polarity-inverting topology, both, the input node as well as the output node require good low ESR bypassing capacitors to minimize voltage ripple and noise.

## 2 Board Specifications & Schematics

- $V_{IN}$ = 15 V to 45 V (LM46002)
- $V_{OUT}$ = -15 V. Refer to Section 7
- $I_{OUT}$ = 1 A.
- Four layer PCB: Inner layers are 35 µm (0.5 oz) copper and Outer layers are 70 µm (1 oz) copper.
- PCB measures 1.6 inches x 3.2 inches (40.64 mm x 81.28 mm) and is 62 mils (1.57 mm) thick of FR4 laminate material

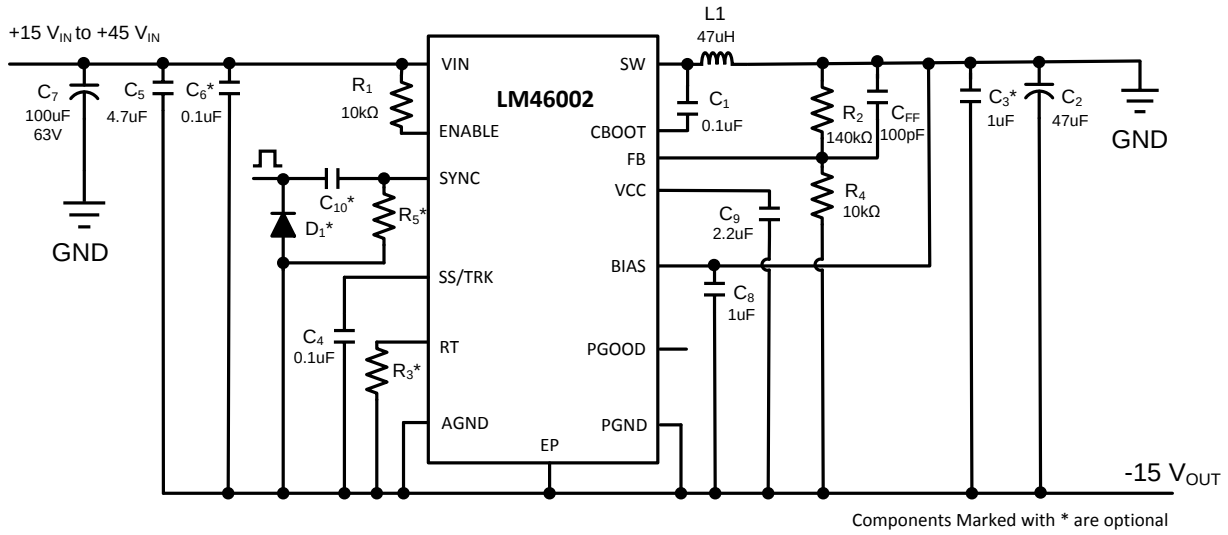



**Figure 1. Evaluation Board Schematic**

While this Application Report makes particular use of an output voltage of -15 V, this inverting application was also tested with -5 V and -12 V. Additionally the part can operate from -1 V to -28 V.

## 3 Board Connections

The board should be connected to a power supply across the $+V_{IN}$ and GND pins, and load connected between the $-V_{OUT}$ and GND pins. The input and output grounds in this application are shared. The PCB layout is designed to accommodate an external sync signal and is setup to operate at a default switching frequency of 500 kHz. Further layout guidelines and layout images are included below in the section Section 8.

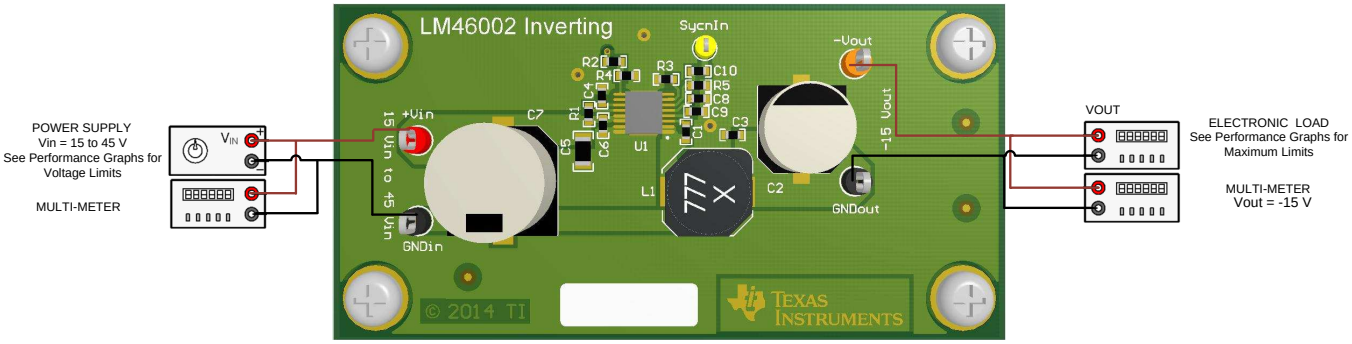



**Figure 2. Evaluation Board Picture**

**Table 1. Functionality of the Pins**

| Terminal Name | Description |
|---|---|
| +Vin | Input supply — Nominal operating range is from 15 V to 45 V for the LM46002. |
| GNDin | Power Ground for the Input. |
| -Vout | Output Voltage — Regulated at -15 V up to 1 A. Please refer to Section 5 |
| GNDout | Power Ground for the Load. |
| SyncIn | Synchronization is actuated through this pin. Please ensure that the Sync signal doesn't exceed the datasheet limits of 5.5 V. |

## 4 Optional Components

The inverting schematic shown in Figure 1 makes note of all options, however it is not necessary to populate the resistor R3, resistor R5 or the capacitor C10. Components that are optional are marked with an ' * ' in the schematic. The evaluation board has many options for input and output filtering. C3 has been installed to decrease high frequency noise at the output. Similarly, C6 has been installed to provide a high frequency bypass for the input current.

The sync pin in particular would need additional protection circuitry to ensure that datasheet limits are not violated. Specifically the amplitude of the sync signal with respect to IC ground must be inspected to avoid overstress.

For additional circuit considerations, see the *Applications* section of the *LM46002 2A SIMPLE SWITCHER® with 60V Maximum Input Voltage* (SNVSA13A).

For Enable toggling, see the *Enable Options* section of the *AN-2027 Inverting Applications for LMZ14203 Application Report* (SNVA425A).

# 5 Design Parameters

A buck converter can be re-purposed to generate a negative output voltage from a positive input source if the circuit is configured as an inverting buck-boost converter. The circuit design is quite simple, mentioned here are several key design points that will aid in your design. Throughout this design it is vital to remember, the ground of the device, including the exposed pad, should not be tied to system ground.

## 5.1 Input Voltage Range

The operating input voltage, $V_{IN(min)}$ of the power supply should be greater than the minimum device voltage, $V_{dev(min)}$. For the LM4600x, the $V_{dev(min)}$ is 3.5 V. The minimum input voltage requirement for this application is 15 V, thus, satisfying Equation 1.

$$V_{dev\,(\min)} \leq V_{IN} \leq V_{IN(\max)} \tag{1}$$

## 5.2 Output Voltage

The resulting negative output voltage is available at the device ground pin, so the effective voltage of the device is $V_{IN} + |V_{OUT}|$. It is also important that this difference not exceed the input-voltage rating of the device. For the LM4600x, the maximum input limit is 60 V.

$$V_{dev\,(\max)} \geq V_{IN(\max)} + |V_{OUT}| \tag{2}$$

Assuming $V_{OUT}$ is -15 V and using Equation 2, the maximum input voltage for the power supply could be as high as 45 V.

Use Equation 3 to determine top feedback resistor, R2, for the desired output voltage, set bottom feedback resistor, R4, to 10 kΩ and $V_{REF}$ to 1.011 V for the LM46002.

$$R2 = R4 \times \left(\frac{|V_{OUT}|}{V_{REF}} - 1\right) \tag{3}$$

Through calculation, R2 equals approximately 138 kΩ, we've chosen 140 kΩ for approximately $V_{OUT}$ = -15 V.

## 5.3 Input Capacitor

This application is stable with almost any combination of ceramic, polymer, tantalum, and aluminum capacitors. A bypass capacitor is a must from $V_{IN}$ to ground and from $V_{IN}$ to $V_{OUT}$ on the input. The bypass from $V_{IN}$ to $V_{OUT}$ is across the device voltage input and its rating must be carefully chosen.

The typical recommended value for the high frequency decoupling capacitor is 4.7 µF to 10 µF. A high-quality ceramic type X5R or X7R with sufficiency voltage rating is recommended. For this design, a 4.7 µF, X7R dielectric capacitor rated for 100 V is used for the input decoupling capacitor. The equivalent series resistance (ESR) is approximately 3 mΩ, and the current-rating is 3 A. Include a capacitor with a value of 0.1 µF for high-frequency filtering and place it as close as possible to the device pins.

For additional input capacitor considerations, see the *Detailed Design Procedure* section of the *LM46002 2A SIMPLE SWITCHER®* (SNVSA13A).

## 5.4 Output Capacitor

Ensure correct polarity of the output capacitor, as the output voltage is negative. The device is designed to be used with a wide variety of LC filters. It is generally desired to use as little output capacitance as possible to keep cost and size down. The output capacitor (s), $C_{OUT}$, should be chosen with care since it directly affects the steady state output voltage ripple, loop stability and the voltage over/undershoot during load current transients.

Please refer to the *Detailed Design Procedure Section 9.2.2.5* of the *LM46002 2A SIMPLE SWITCHER®* (SNVSA13A) for more details regarding output capacitor selection and stability requirements. Remember to substitute $V_{OUT}$ with the absolute value $|V_{OUT}|$ for Equations 19 and 20.

## 5.5 Output Current

The average inductor current is affected in this topology. In the buck configuration, the average inductor current equals the average output current because the inductor always supplies current to the load during both the on and off times of the control MOSFET. However, in the inverting buck boost configuration, the load is supplied with current only from the output capacitor and is completely disconnected from the inductor during the on time of the control MOSFET. During the off time, the inductor connects to both the output cap and the load.

The duty cycle for the typical buck converter is simply $V_{OUT}$ / $V_{IN}$ but the duty cycle for an inverting buck boost converter becomes:

$$D = \frac{|V_{OUT}|}{(\eta \times V_{IN}) + |V_{OUT}|} \quad (4)$$

The efficiency term, η, in Equation 4 adjusts the equations in this section for power conversion losses and yields a more accurate maximum output current result.

*Please note, the worst case scenario is given by the maximum duty cycle, $D_{MAX}$, and is calculated by using the minimum input voltage, $V_{IN\ (min)}$ substituted for input voltage, $V_{IN}$ in Equation 4. Assuming 15 V for $V_{IN}$ and a $V_{OUT}$ of -15 V, the maximum duty cycle, $D_{MAX}$, is 0.55 using an efficiency value, η of 80%.*

In the operation of a synchronous inverting buck-boost, when the high-side FET switch is on, the voltage seen across the inductor is $V_{IN}$ and the current ramps up at a rate of di/dt = $V_{IN}$/L. While the high-side FET is on, the necessary load current is provided by charge stored in the output capacitor.

During the Off state, this FET turns off and the inductor must reverse polarity to keep the inductor current continuous. The voltage across the inductor is approximately $V_{OUT}$, and the discharging rate of the inductor current is given by di/dt = –$V_{OUT}$/L. During this off time, the inductor will provide current to the load and at the same time replenish energy lost by the capacitor during the on time.

The average output current cannot exceed the LM4600x rated output, and hence the available load current is reduced by a factor of (1 – D). From the LM46002 datasheet, average inductor current is 2 A mentioned as typical value of valley current limit under Electrical Characteristics table.

For this design, knowing that the off time is (1 – D) of the switching period, the Output Current, $I_{OUT}$ is given by Equation 5:

$$I_{OUT} \leq (1 - D) \times I_{L(avg)} \quad (5)$$

where, $I_{L(avg)}$ is the rated average inductor current.

## 5.6 Inductor Selection

It is important to keep the inductor AC ripple current small for several reasons. The peak inductor current, which is defined as the average inductor current plus half of the peak-to-peak AC current, should be below the internal control circuit's current limit. The point at which the circuit operates in discontinuous conduction mode is also governed by the inductor AC ripple current.

Discontinuous operation mode, or DCM, occurs when the average current through the inductor is equal to half the peak-to-peak AC current. In general, this parameter limit is more severe than the preceding current limit.

The inductor ripple current contributes significantly to the output voltage ripple since the inductor transfers its energy to the capacitor and works together as a pair. Lower inductor ripple currents provide cleaner output voltages but if it becomes too low it will affect the signal to noise ratio detrimentally. This in turn might result in not enough inductor ripple for stable operation.

For any topology, there are significant differences between discontinuous and continuous mode operation. Designs that are stable in the discontinuous mode may become unstable when increased load current causes them to operate in the continuous mode, during which the feedback loop contains a right-half-plane zero.

The inductor inductance is calculated as:

$$\frac{V_{IN} \times D}{0.4 \times f_s \times I_{L(max)}} \leq L \leq \frac{V_{IN} \times D}{0.2 \times f_s \times I_{L(max)}} \quad (6)$$

Where,

**$\Delta I_L$ (A):** Peak to peak inductor ripple current and 0.4 or 40% at the highest and 0.2 or 20% as a bare minimum

**D:** Duty cycle

**$f_s$ (kHz):** Switching frequency

**L (µH):** Inductance of chosen inductor

**$V_{IN}$ (V):** Input voltage with respect to ground, instead of IC ground or $V_{OUT}$.

Table 3 provides several examples of the calculated maximum output currents for different output voltages (-5 V, -12 V and -15 V) based on an inductor value and switching frequency of 47 µH and 500 kHz, respectively. Increasing the inductance and/or input voltage allows higher output currents in the inverting buck boost configuration. The maximum output currents for the LM46002 in the inverting buck boost topology are frequently lower than 2 A due to the fact that the average inductor current is higher than that of a typical buck.

## 5.7 Feed-Forward Capacitor

The LM46002 is internally compensated and the internal R-C values are 400 kΩ and 50 pF respectively. Depending on the specific $|V_{OUT}|$ and frequency $F_S$, low phase margin is a possibility due to $C_{OUT}$ dominated by low ESR (ceramic type) capacitors. In transient testing low phase-margin may show up as an unstable design. To provide a phase boost an external feed-forward capacitor $C_{FF}$ can be added in parallel with $R_{FBT}$. $C_{FF}$ is chosen such that phase margin is boosted at the crossover frequency obtained in the absence of $C_{FF}$ and is given by Equation 7.

$$C_{FF} = \frac{\sqrt{R_{FBB} + R_{FBT}}}{2 \times \pi \times f_{x\_NO\_C_{FF}} \times R_{FBT} \times \sqrt{R_{FBB}}} \quad (7)$$

Where,

- $C_{FF}$ = Feed-forward capacitor
- $R_{FBT}$ = Upper feedback resistor
- $R_{FBB}$ = Lower feedback resistor
- $f_{X\_NO\_CFF}$ = System crossover frequency without the use of $C_{FF}$

The first and easiest method for $C_{FF}$ optimization is to use the simplified linear equation that estimates the value of $f_{X\_NO\_CFF}$. The linear approximation assumes that the output capacitor is of a ceramic type with very low ESR. The effect of ESR is not taken into consideration, and does not assume any parasitic pole frequencies occurring at higher frequencies. The linear approximation is different for every part in the LM4xx family of devices. The following equation applies to every device in the family:

$$f_{x\_NO\_C_{FF}} = \frac{K}{|V_{OUT}| \times (1 + D) \times C_{OUT}} \quad (8)$$

Where,

- D = Duty cycle calculated from Equation 4.

The corresponding values of the constant K for all the devices in the family can be obtained from the Table 2 as follows:

**Table 2. Device Specific Constant Values**

| DEVICE | CONSTANT VALUE (K) |
|---|---|
| LM43603 | 5.3 |
| LM43602 | 4.35 |
| LM43601 | 2.73 |
| LM43600 | 1.5 |
| LM46002 | 4.35 |
| LM46001 | 2.73 |
| LM46000 | 1.5 |

The result of the Equation 8 could then be used in Equation 7 to obtain the required $C_{FF}$ value. The second method to estimate the value of the parameter $f_{X\_NO\_CFF}$ is to use the downloadable PSPICE bode plot model. The model has been previously correlated against bench data for accuracy, and can plot the loop response.

The output current for three output voltages and component values for the same are displayed in Table 3.

**Table 3. Calculated Output Current Range and Component Values for Different $V_{OUT}$'s based on LM46002**

| Parameter | $V_{OUT}$ = -5 V | $V_{OUT}$ = -12 V | $V_{OUT}$ = -15 V |
|---|---|---|---|
| $f_s$ (kHz) | 500 | 500 | 500 |
| L (µH) | 47 | 47 | 47 |
| $V_{IN}$ (V) | 24 | 24 | 24 |
| η | 0.8 | 0.8 | 0.8 |
| D | 20.66% | 38.46% | 43.85% |
| $I_{OUT}$ (A) | 1.58 | 1.23 | 1.12 |
| $C_{OUT}$* (µF) | 150 | 47 | 33 |
| $C_{FF}$** (pF) | 910 | 820 | 750 |

**Please note $C_{OUT}$ value is after derating of the capacitors and rounded up to the closest available standard capacitor value.*

***Please note $C_{FF}$ value is based on an all ceramic design and will be lower depending on the ESR of the Output Capacitors. This is also the maximum value of $C_{FF}$ needed and rounded up to the closest available standard capacitor value.*

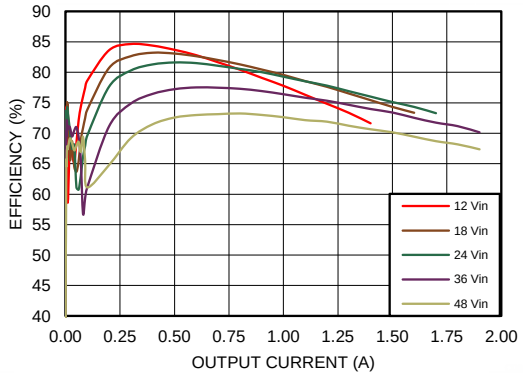
# 6 Bill of Materials

**Table 4. Evaluation Board Bill of Materials, $V_{IN}$ = 15 V to 45 V, $V_{OUT}$ = -15 V**

| Designator | Description | Case Size | Manufacturer | Manufacturer P/N | Quantity |
|---|---|---|---|---|---|
| U1 | SIMPLE SWITCHER ™ 3.5 V to 60 V 2 A Synchronous Step-Down Voltage Regulator | HTSSOP-16 | Texas Instruments | LM46002 | 1 |
| C1, C4, C6 | CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603 | 0603 | AVX | 06035C104KAT2A | 3 |
| C2 | CAP, Al Electrolytic, 47uF, 63V, 0.2Ohm ESR | SMT | SUNCON | 63CE47KX | 1 |
| C3, C8 | CAP, CERM, 1uF, 25V, +/-10%, X7R, 0603 | 0603 | TDK | C1608X7R1E105K080AB | 2 |
| C5 | CAP, CERM, 4.7uF, 100V, +/-10%, X5R, 1206 | 1206 | MuRata | GRM31CR71H475KA12 | 1 |
| C7 | CAP, Al Electrolytic, 100uF, 63V, 0.2Ohm ESR | SMT | SUNCON | 63CE100KX | 1 |
| C9 | CAP, CERM, 2.2uF, 6.3V, +/-10%, X5R, 0603 | 0603 | Kemet | C0603C225K9PACTU | 1 |
| Cff | CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603 | 0603 | AVX | 06035A101JAT2A | 1 |
| H1, H2, H3, H4 | Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead | Screw | B&F Fastener Supply | NY PMS 440 0025 PH | 4 |
| H5, H6, H7, H8 | Standoff, Hex, 0.5"L #4-40 Nylon | Standoff | Keystone | 1902C | 4 |
| L1 | Inductor, Shielded Drum Core, Ferrite, 47uH, 2.2A, 0.13 ohm, SMD | MSS1038 | Coilcraft | MSS1038-473MLB | 1 |
| R1, R4 | RES, 10.0k ohm, 1%, 0.1W, 0603 | 0603 | Vishay-Dale | CRCW060310K0FKEA | 2 |
| R2 | RES, 140k ohm, 1%, 0.1W, 0603 | 0603 | Vishay-Dale | CRCW0603140KFKEA | 1 |
| R5 | RES, 10.0k ohm, 1%, 0.1W, 0603 | 0603 | Vishay-Dale | CRCW060310K0FKEA | 1 |
| TP2 | Test Point, Multipurpose, Red, TH | Red Multipurpose Testpoint | Keystone | 5010 | 1 |
| TP3, TP4, TP5 | Test Point, Multipurpose, Black, TH | Black Multipurpose Testpoint | Keystone | 5011 | 3 |
| C10 | CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603 | 0603 | AVX | 06035A101JAT2A | 0 |
| R3 | RES, 10.0k ohm, 1%, 0.1W, 0603 | 0603 | Vishay-Dale | CRCW060310K0FKEA | 0 |
| TP1 | Test Point, Miniature, Yellow, TH | Yellow Miniature Testpoint | Keystone | 5004 | 0 |
| D1 | Diode, SMA, 100V, 1A | SMA | Vishay-Dale | ES1B | 0 |

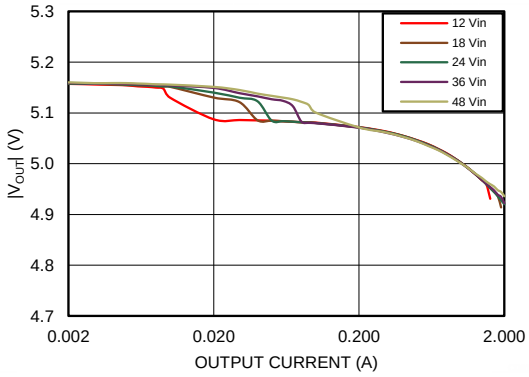
## 7 Performance Characteristics

Please refer to Table 4 for Bill of Materials for each $V_{IN}$ combination. Unless otherwise stated, application performance curves were taken at $T_A$ = 25 °C.



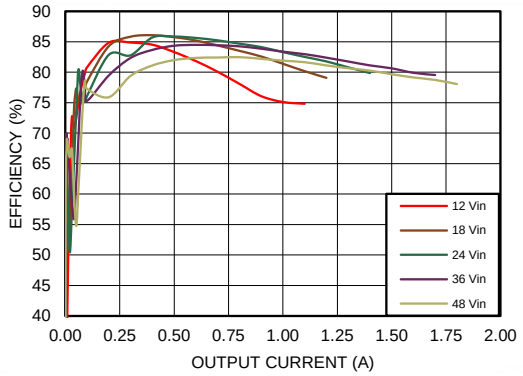

$V_{OUT}$ = -5 V $F_S$=500 kHz

**Figure 3. Efficiency (%)**



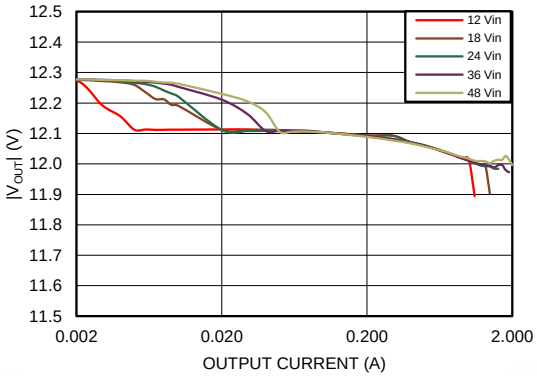

$V_{OUT}$ = -5 V $F_S$=500 kHz

**Figure 4. Output Regulation (V)**



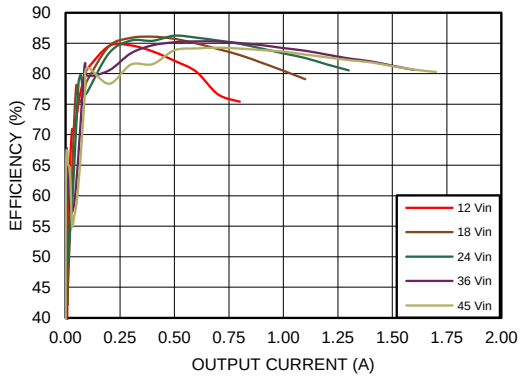

$V_{OUT}$ = -12 V $F_S$=500 kHz

**Figure 5. Efficiency (%)**



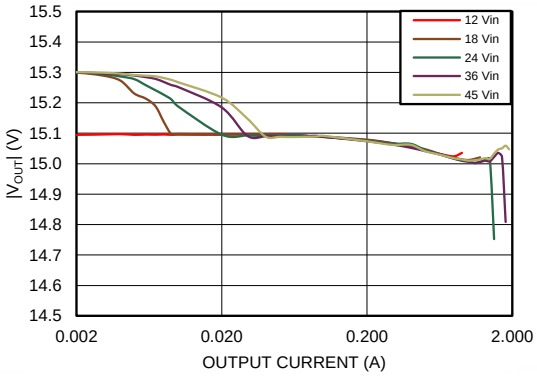

$V_{OUT}$ = -12 V $F_S$=500 kHz

**Figure 6. Output Regulation (V)**



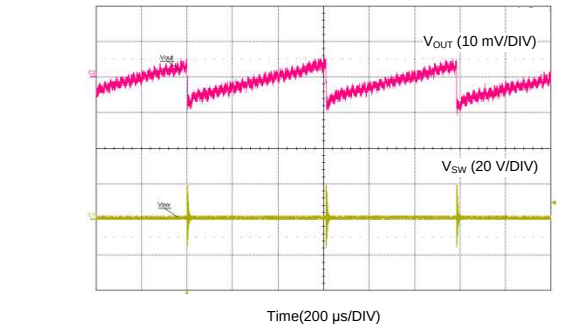

$V_{OUT}$ = -15 V $F_S$=500 kHz

**Figure 7. Efficiency (%)**



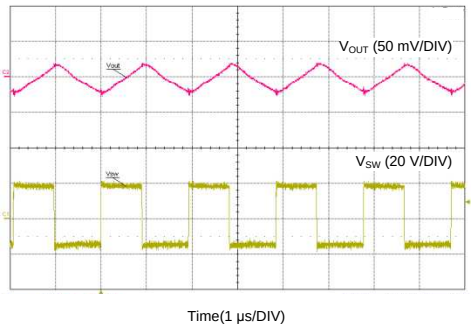

$V_{OUT}$ = -15 V $F_S$=500 kHz

**Figure 8. Output Regulation (V)**



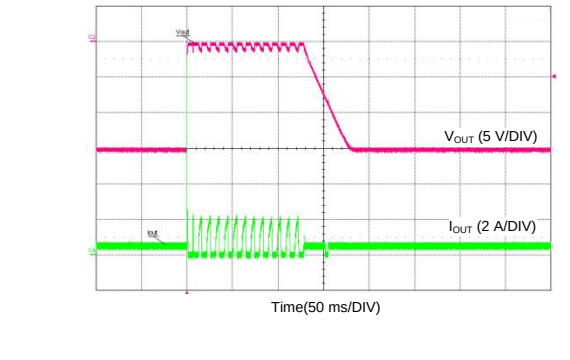

$V_{IN}$ = 18 V $V_{OUT}$ = -15 V

**Figure 9. Switching Operation and Output Ripple at No Load**



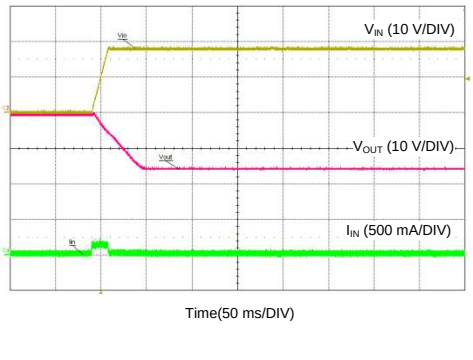

$V_{IN}$ = 18 V $V_{OUT}$ = -15 V $I_{OUT}$ = 500 mA

**Figure 10. Switching Operation and Output Ripple with Load**



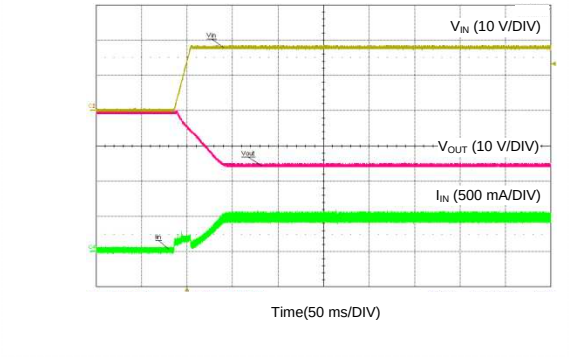

$V_{IN}$ = 18 V $V_{OUT}$ = -15 V $I_{OUT}$ = 500 mA

**Figure 11. Short-Circuit**



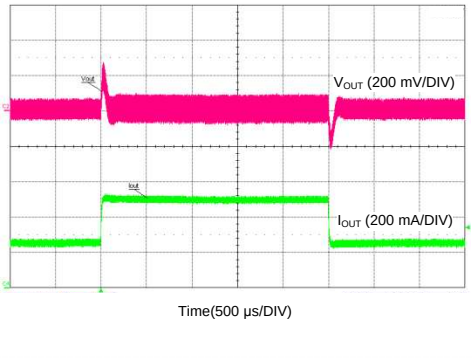

$V_{IN}$ = 18 V $V_{OUT}$ = -15 V

**Figure 12. Start-up at No Load**



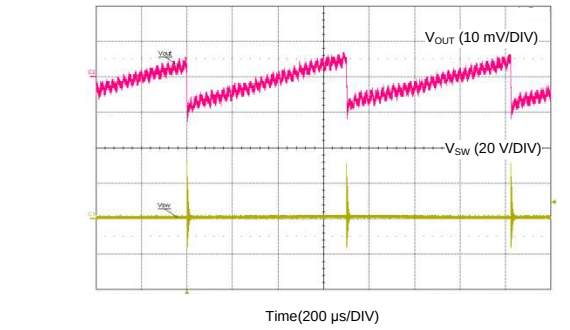

$V_{IN}$ = 18 V $V_{OUT}$ = -15 V $I_{OUT}$ = 500 mA

**Figure 13. Start-up into Load**



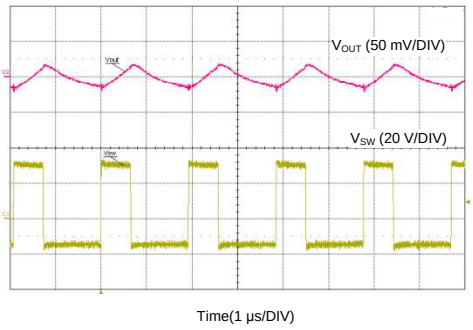

$V_{IN}$ = 18 V $V_{OUT}$ = -15 V $I_{OUT}$ = 0.25 A to 0.5 A

**Figure 14. Load Transient Response**



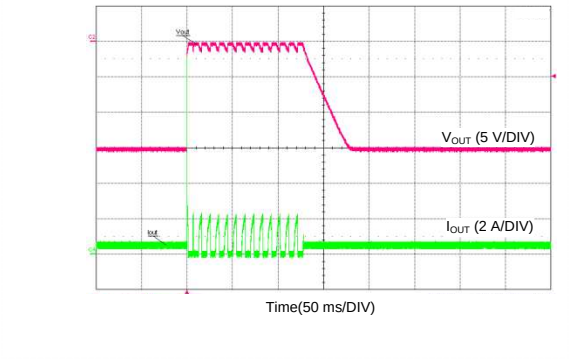

$V_{IN}$ = 30 V $V_{OUT}$ = -15 V

**Figure 15. Switching Operation and Output Ripple at No Load**



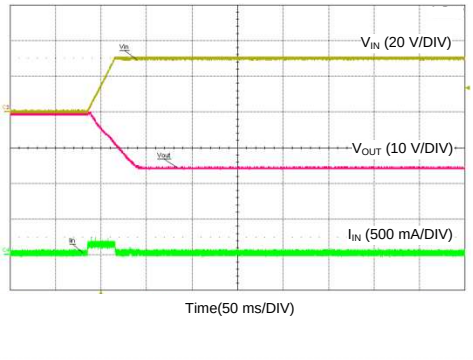

$V_{IN}$ = 30 V $V_{OUT}$ = -15 V $I_{OUT}$ = 500 mA

**Figure 16. Switching Operation and Output Ripple with Load**



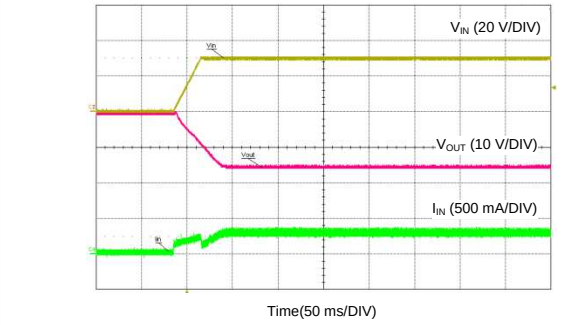

$V_{IN}$ = 30 V $V_{OUT}$ = -15 V $I_{OUT}$ = 500 mA

**Figure 17. Short-Circuit**



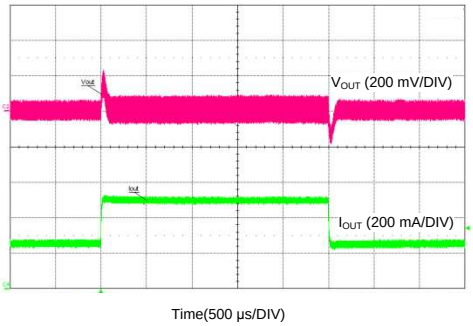

$V_{IN}$ = 30 V $V_{OUT}$ = -15 V

**Figure 18. Start-up at No Load**



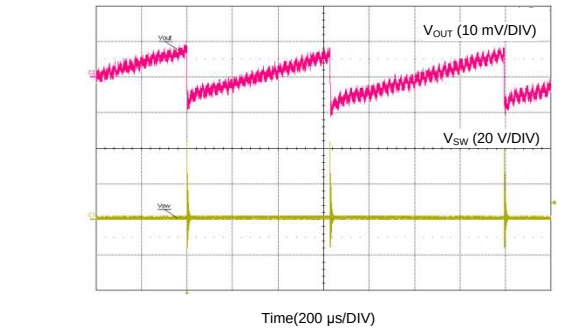

$V_{IN}$ = 30 V $V_{OUT}$ = -15 V $I_{OUT}$ = 500 mA

**Figure 19. Start-up into Load**



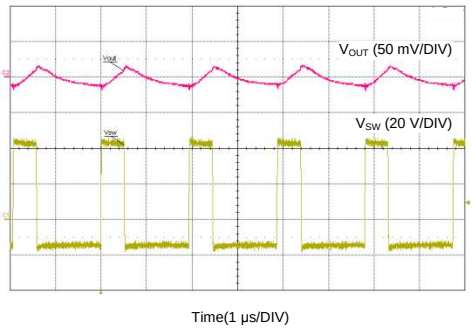

$V_{IN}$ = 30 V $V_{OUT}$ = -15 V $I_{OUT}$ = 0.25 A to 0.5 A

**Figure 20. Load Transient Response**



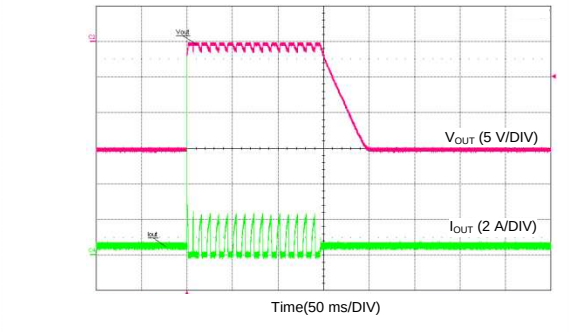

$V_{IN}$ = 42 V $V_{OUT}$ = -15 V

**Figure 21. Switching Operation and Output Ripple at No Load**



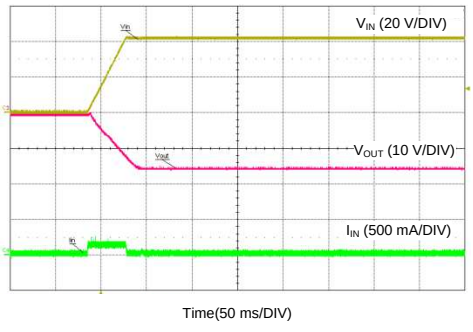

$V_{IN}$ = 42 V $V_{OUT}$ = -15 V $I_{OUT}$ = 500 mA

**Figure 22. Switching Operation and Output Ripple with Load**



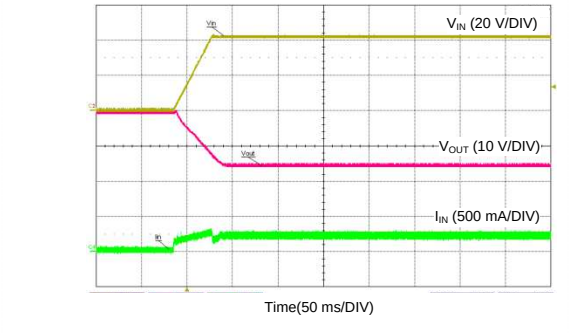

$V_{IN}$ = 42 V $V_{OUT}$ = -15 V $I_{OUT}$ = 500 mA

**Figure 23. Short-Circuit**



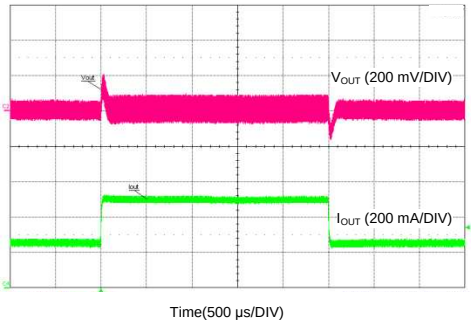

$V_{IN}$ = 42 V $V_{OUT}$ = -15 V

**Figure 24. Start-up at No Load**




$V_{IN}$ = 42 V $V_{OUT}$ = -15 V $I_{OUT}$ = 500 mA

**Figure 25. Start-up into Load**




$V_{IN}$ = 18 V $V_{OUT}$ = -15 V $I_{OUT}$ = 0.25 A to 0.5 A

**Figure 26. Load Transient Response**

## 8 PCB Layout Diagrams

Board layout is a critical aspect of SMPS design. The performance of an SMPS could be degraded by a poorly designed PCB. Even worse, a bad PCB layout may result in a malfunctioning converter. Due to the switching action in SMPS, large currents with fast transitions exist in the circuit. A current has to circulate through a loop and return to the source. If current transitions exist in a current loop, voltage spikes are going to be generated, v = L•(di/dt), where L is the self-inductance of the current loop and di/dt is the current transition rate. The self-inductance of a current loop is proportional to the area enclosed by it. The loops containing high di/dt current are the critical paths in SMPS PCB design. To reduce the voltage spikes and switching noises in an SMPS, the critical high di/dt paths should be identified and the area enclosed by them should be minimized.

Benefits of the LM4360x and LM4600x pin out include:

- All the converters in the LM4360x and LM4600x family are pin-to-pin compatible. PCB design can be easily scaled to different voltage and current levels.
- VIN and PGND pins are next to each other. The input capacitor can be placed as close as possible to the IC to minimize the high di/dt loop area. Noise generation from switching action is minimized.
- BOOT pin is next to SW pin, allowing CBOOT to be placed as close as possible to these two pins to minimize noise generated by high side FET driver.
- The SW node is on the opposite side of VIN and GND, instead of in between VIN and GND pins. Short and wide traces can be used to route VIN, GND to the input capacitor and SW to the inductor on the same layer as the IC. The SW node area, which contains high frequency currents, can be as small as possible.
- The sensitive FB pin is at the corner of the IC and far away from noisy pins. AGND pin is placed next to FB. This provides additional shielding. It also allows for resistor divider to be placed as close as possible to the FB and AGND pins, making the FB node really small and immune to noise.
- Internal compensation, current sensing, monitor and protection circuits. Circuit design and PCB layout are simplified.
- All external components can be placed and routed on the same layer as the IC. The other layers can be a full sheet of unbroken copper for the best heat dissipation and shielding but remember the exposed pad must be connected to $-V_{OUT}$.

Gerber and CAD files can be downloaded from the TI Designs portal linked from the main LM46002 product page.

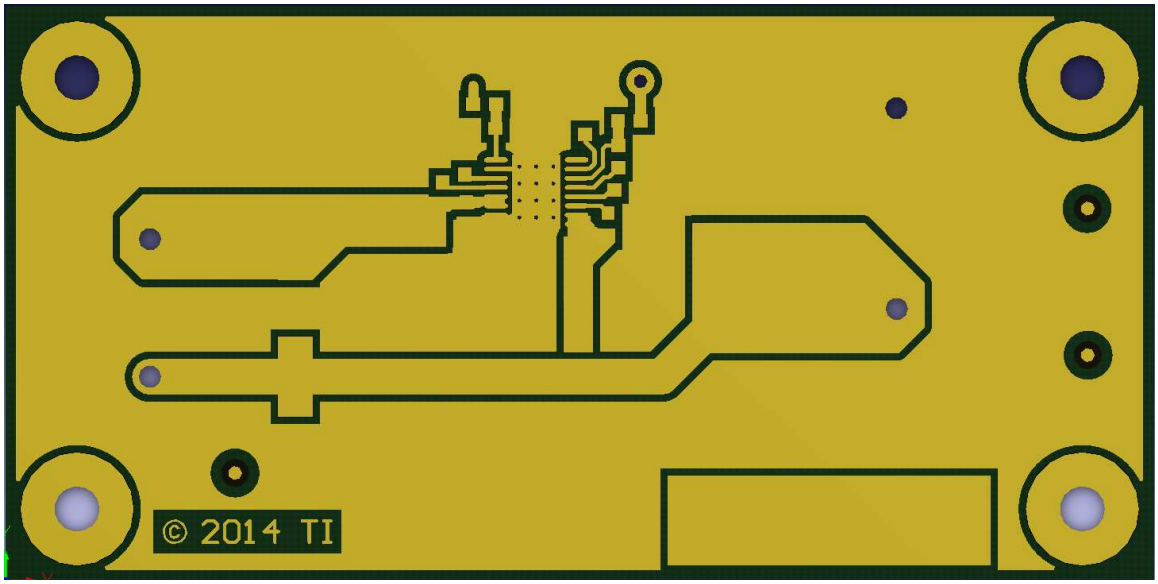



**Figure 27. Top Layer**

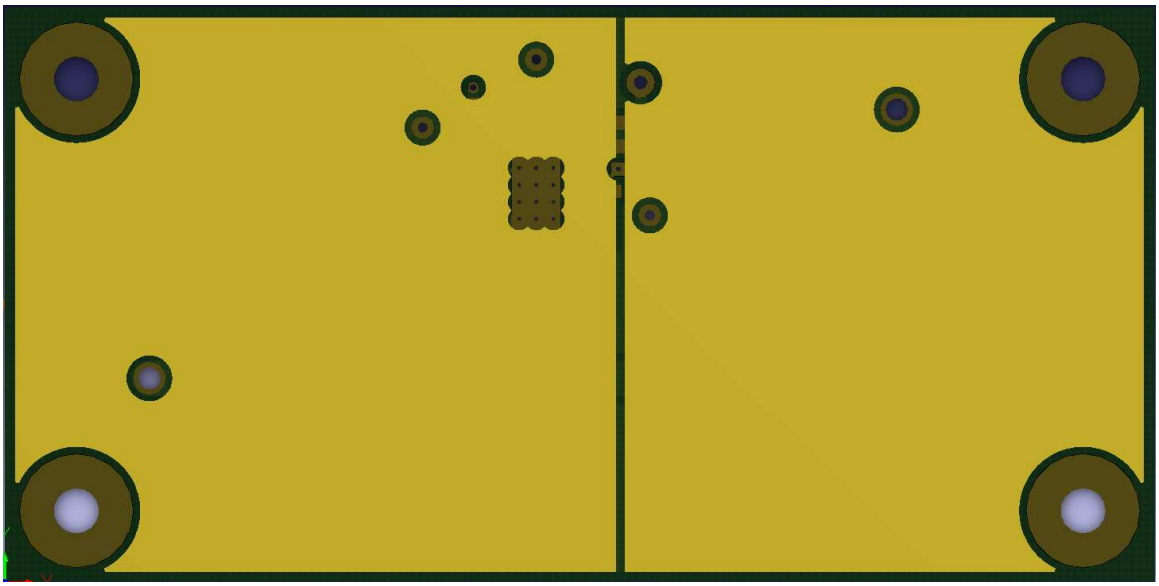


**Figure 28. Internal Layer I (Left Half is $V_{IN}$ and Right Half is Ground)**

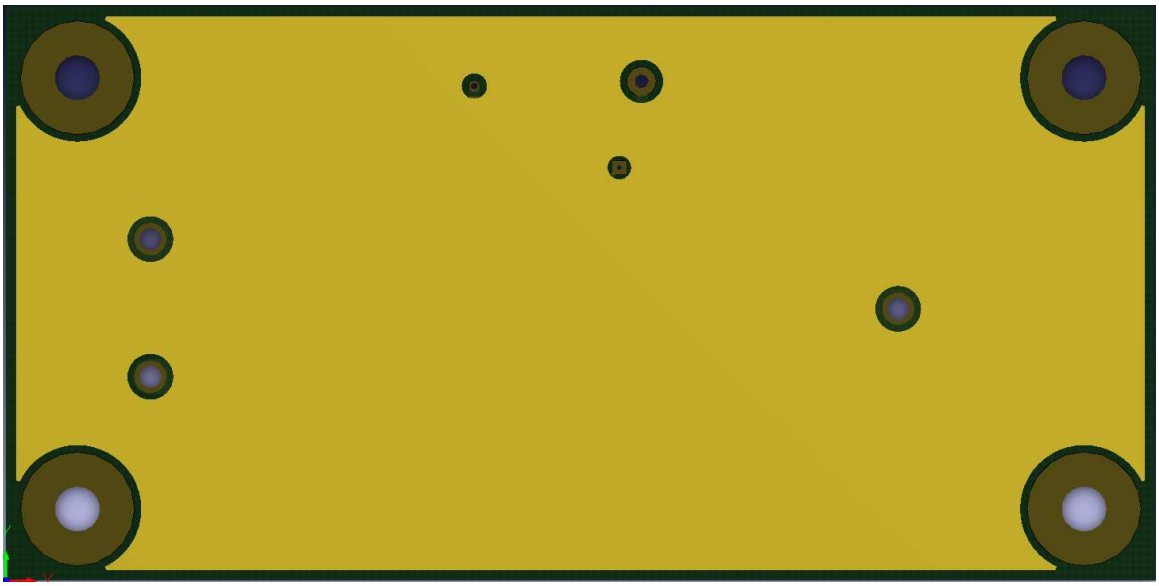


**Figure 29. Internal Layer II ($-V_{OUT}$)**

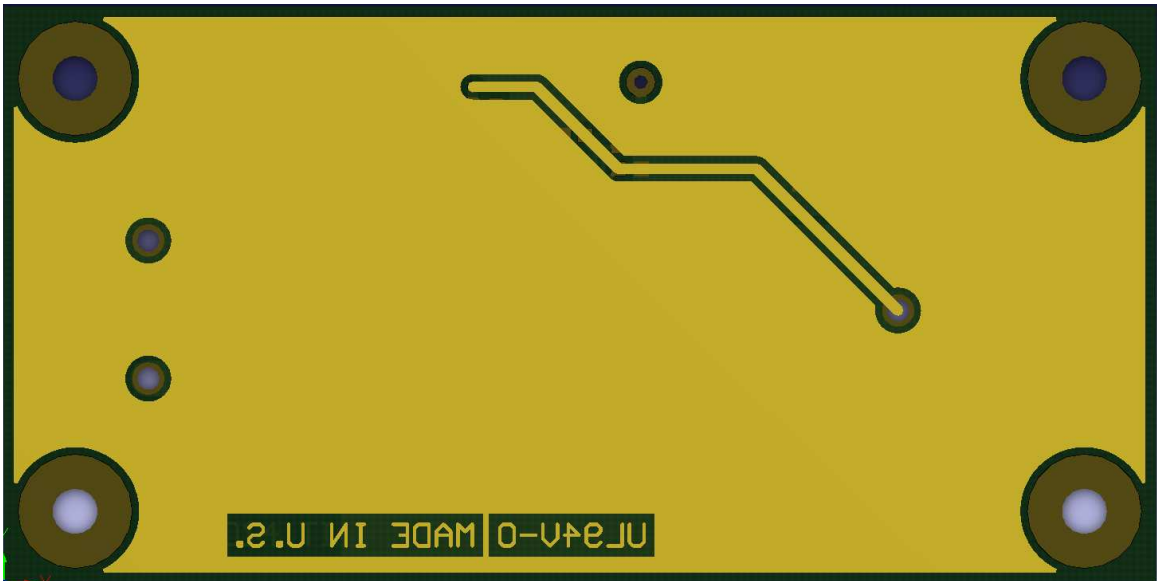



**Figure 30. Bottom Layer ($-V_{OUT}$ and Routing)**

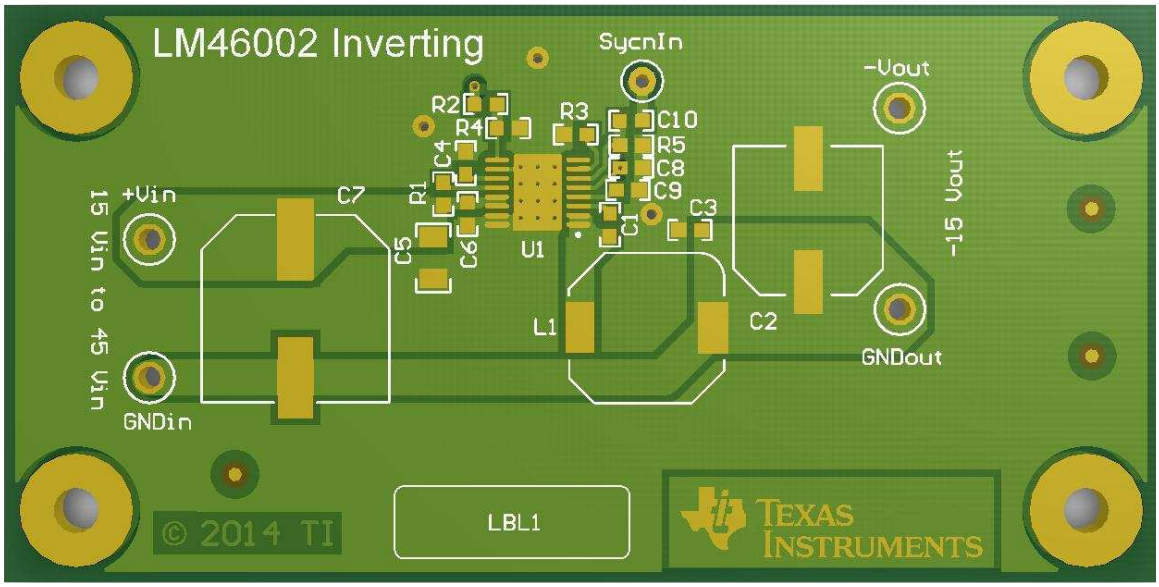



**Figure 31. Top Silkscreen**

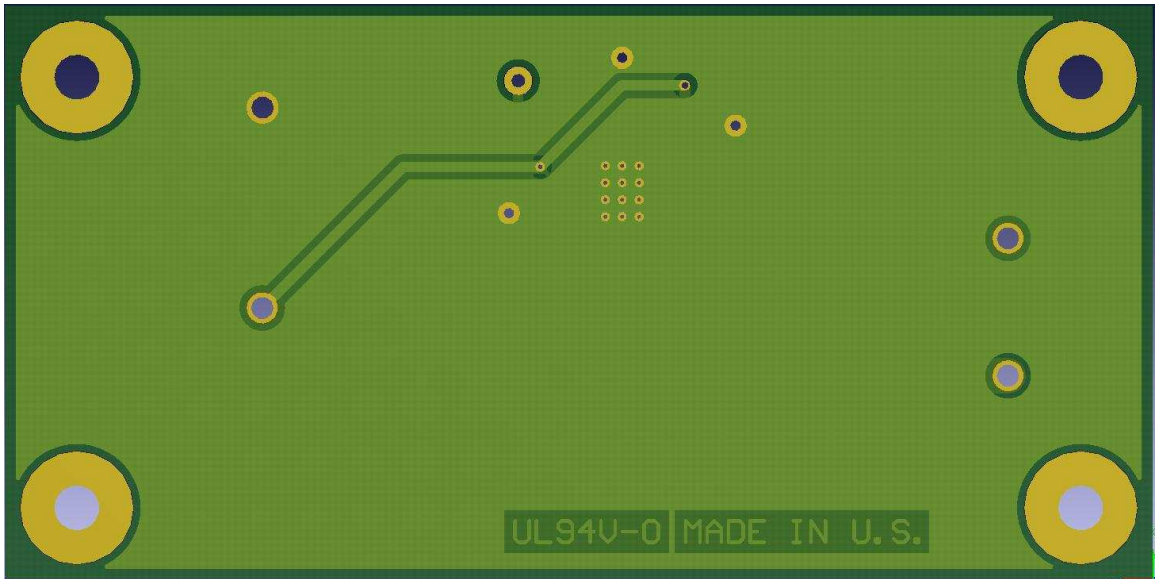



**Figure 32. Bottom Silkscreen**

## 9 Thermal Performance

Following best layout practices ensures optimal thermal performance of the IC as well. Please refer to Table 4 for Bill Of Materials for each $V_{IN}$ combination. Unless otherwise stated, Infrared Thermal Images were taken at $T_A$ = 25 °C.

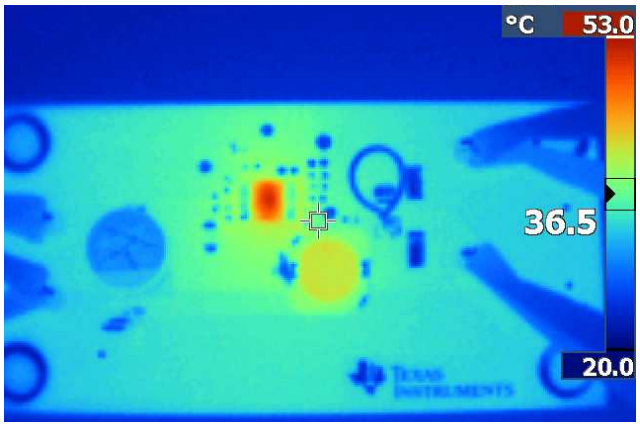



**Figure 33. Infrared Thermal Image (no airflow)**
**$V_{IN}$ = 18 V, $V_{OUT}$ = -15 V at 0.5 A**

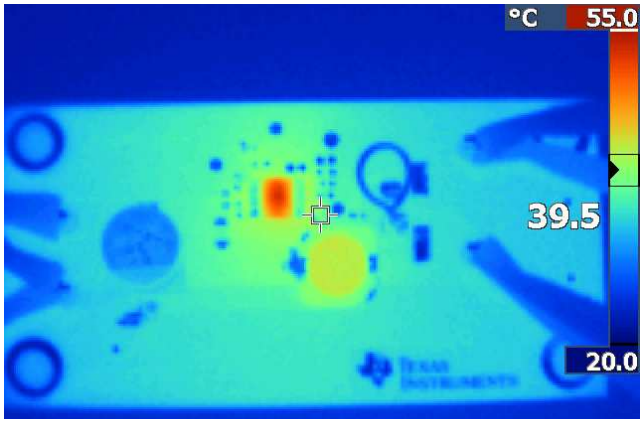



**Figure 34. Infrared Thermal Image (no airflow)**
**$V_{IN}$ = 30 V, $V_{OUT}$ = -15 V at 0.5 A**

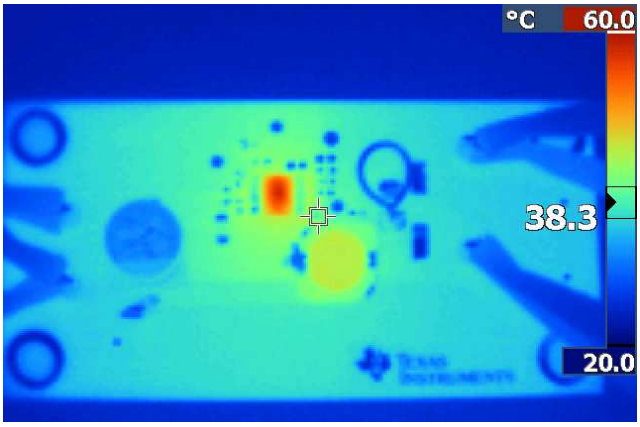



**Figure 35. Infrared Thermal Image (no airflow)**
**$V_{IN}$ = 42 V, $V_{OUT}$ = -15 V at 0.5 A**

# Revision History

| Changes from A Revision (September 2014) to B Revision | Page |
|---|---|
| • Changed image to reflect correct output capacitor polarity | 2 |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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