REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

NORTH
1 - ALERT
2 - DRDY
3 - FAULT
4 - CONV
5 - CELL6
6 - CELL6
7 - SCLK
8 - CS
9 - SDO
10 - SDI

CAUTION
HIGH VOLTAGE

INDIVIDUAL GROUND PLANES ARE NECESSARY FOR PROPER NOISE REJECTION AND STABILITY OF THESE CIRCUITS

NOTE: The ground reference per circuit block is unique
The most negative connection of CELL0 is the ground reference for each chip.

DO NOT connect ground references from different chips

Only the ground reference CELL0 of circuit 1 is safe to connect non-isolated test equipment grounds.

EXTERNAL POWER 5VDC @200mA

ALL RESISTERS 1% UNLESS NOTED

1 - POPULATE THESE COMPONENTS TO STACK SOUTH
USE 1K 0603 RESISTORS OR ADJUST AS NEEDED
2 - REMOVE THESE COMPONENTS TO STACK SOUTH
3 - REMOVE THESE COMPONENTS TO STACK NORTH
4 - POPULATE THESE COMPONENTS TO STACK NORTH
USE 1K 0603 RESISTORS OR ADJUST AS NEEDED

5 - THESE CAPACITORS ARE USED IN DESIGNS THAT HAVE HIGH NOISE LEVELS WHEN STACKING IC'S. USE 22pF - 100pF CAPS AS NEEDED (33pF 50V 0603 NPO 10% ARE THE DEFAULT CAPACITORS)

6 - LOCATE THESE RESISTORS CLOSE TO THE MOST NORTH IC
7 - LOCATE THESE RESISTORS CLOSE TO THE MOST SOUTH IC
8 - LOCATE THESE RESISTORS CLOSE TO THE MOST NORTH IC
9 - LOCATE THESE RESISTORS CLOSE TO THE MOST SOUTH IC

GROUND PLANE OF CIRCUIT 3
GROUND PLANE OF CIRCUIT 2

EXTEND THE GROUND PLANE UNDER THE SOUTH COMM LINES TO JUST BELOW THE NORTH COMM PINS OF THE CHIP BELOW

GROUND PLANE OF CIRCUIT 2
GROUND PLANE OF CIRCUIT 1

BQ76PL536A_CIRCUIT3 SHEET-4
BQ76PL536A_CIRCUIT2 SHEET-3
BQ76PL536A_CIRCUIT1 SHEET-2

ISOLATED CONTROLLER INTERFACE

ISOLATOR SHEET-5

USB GUI INTERFACE

CONTROLLER INTERFACE

FEET/Mounting holes

SOUTH
1 - ALERT
2 - DRDY
3 - FAULT
4 - CONV
5 - VSS
6 - VSS
7 - SCLK
8 - CS
9 - SDO
10 - SDI

CAUTION
HIGH VOLTAGE

COMPANY:	Texas Instruments		
TITLE:	bq76PL536AEVM-3 Stack Design <Code>		
DRAWN: GORDON VARNEY	DATED: 2/22/2012		
CHECKED: <Checked By>	DATED: <Checked Date>		
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>		
CODE:	SIZE: D	DRAWING NO: PWR004	REV: E3
SCALE: <Scale>	02/22/2012	SHEET:1 OF5	

SHEET 1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

ALL RESISTERS 1% UNLESS NOTED

** - Locate these components very close to U1.

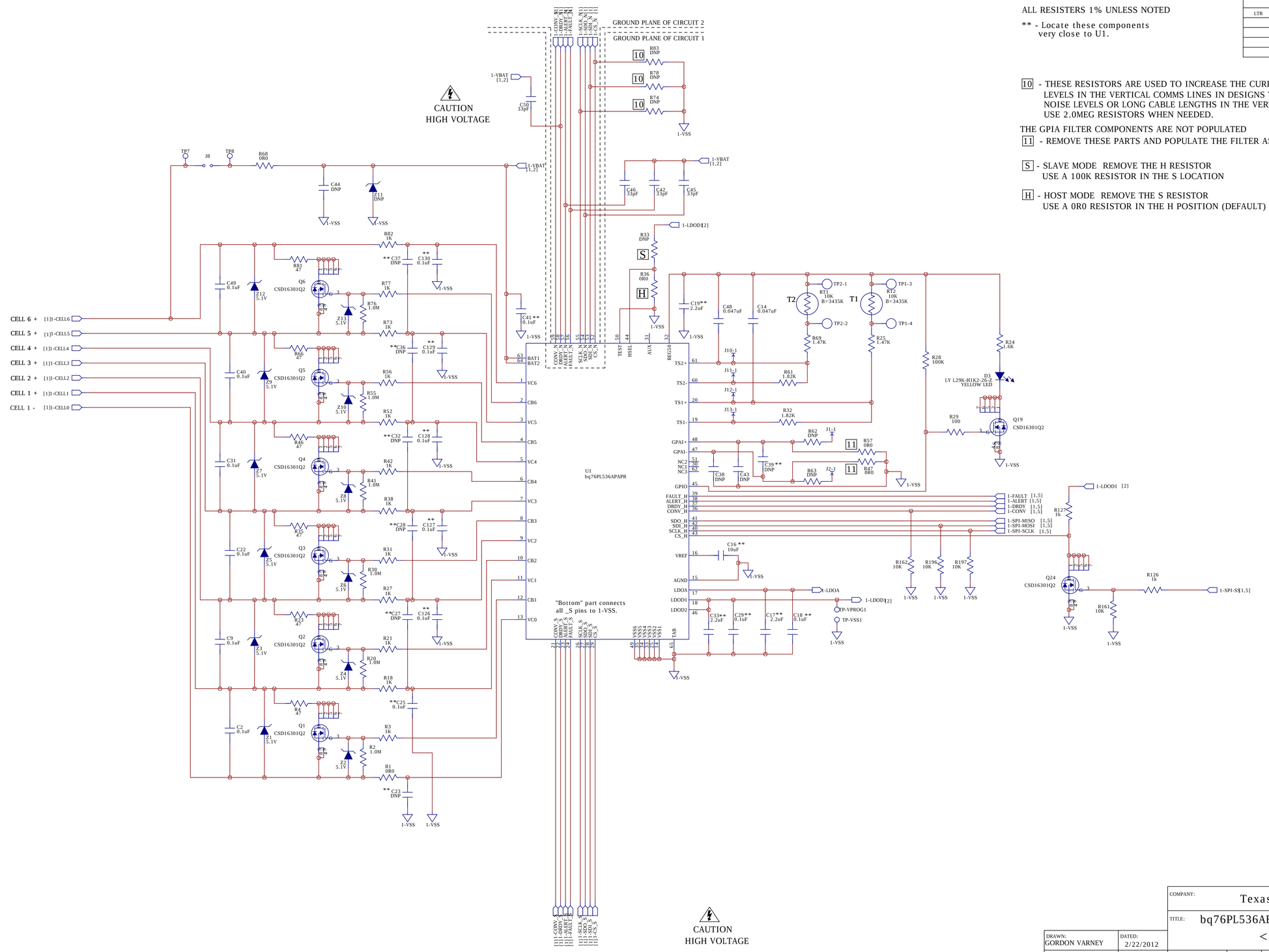
10 - THESE RESISTORS ARE USED TO INCREASE THE CURRENT LEVELS IN THE VERTICAL COMMS LINES IN DESIGNS THAT HAVE HIGH NOISE LEVELS OR LONG CABLE LENGTHS IN THE VERTICAL COMMS USE 2.0MEG RESISTORS WHEN NEEDED.

THE GPIA FILTER COMPONENTS ARE NOT POPULATED

11 - REMOVE THESE PARTS AND POPULATE THE FILTER AS NEEDED

S - SLAVE MODE REMOVE THE H RESISTOR USE A 100K RESISTOR IN THE S LOCATION

H - HOST MODE REMOVE THE S RESISTOR USE A 0R0 RESISTOR IN THE H POSITION (DEFAULT)



SHEET 2

DRAWN: GORDON VARNEY	DATED: 2/22/2012	COMPANY: Texas Instruments	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: bq76PL536AEVM-3 Stack Design <Code>	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE:	SIZE: D
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: CIRCUIT 1 PWR004	REV: E3
		SCALE: <Scale>	SHEET: 2 OF 5

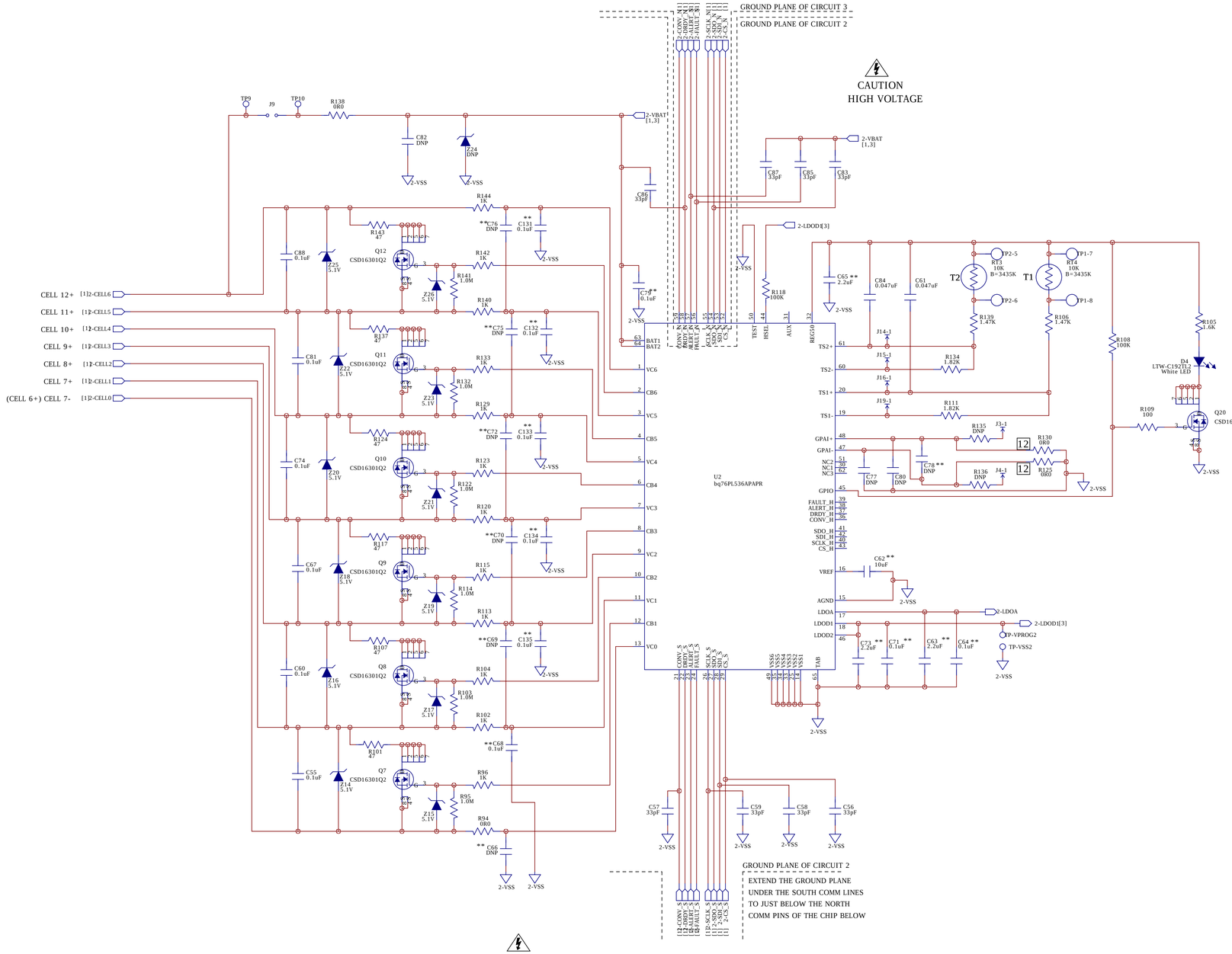
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

ALL RESISTERS 1% UNLESS NOTED

** - Locate these components very close to U2.

THE GPIA FILTER COMPONENTS ARE NOT POPULATED

12 - REMOVE THESE PARTS AND POPULATE THE FILTER AS NEEDED



SHEET 3

DRAWN: GORDON VARNEY	DATED: 2/22/2012	COMPANY: Texas Instruments	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: bq76PL536AEVM-3 Stack Design <Code>	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE:	SIZE: D
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: CIRCUIT 2 PWR004	REV: E3
		SCALE: <Scale>	SHEET: 3 OF 5

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

ALL RESISTERS 1% UNLESS NOTED

** - Locate these components very close to U3.

THE GPIA FILTER COMPONENTS ARE NOT POPULATED

13 - REMOVE THESE PARTS AND POPULATE THE FILTER AS NEEDED

14 - THIS RESISTOR IS USED TO INCREASE THE CURRENT LEVELS IN THE VERTICAL COMMS LINES IN DESIGNS THAT HAVE HIGH NOISE LEVELS OR LONG CABLE LENGTHS IN THE VERTICAL COMM PATHS. USE A 512K RESISTOR WHEN NEEDED

CAUTION
HIGH VOLTAGE

"Top" part connects all _N pins to VBAT of U3

U3
bq76PL536APAPR

GROUND PLANE OF CIRCUIT 3
EXTEND THE GROUND PLANE UNDER THE SOUTH COMM LINES TO JUST BELOW THE NORTH COMM PINS OF THE CHIP BELOW

CAUTION
HIGH VOLTAGE

SHEET 4

DRAWN: GORDON VARNEY	DATED: 2/22/2012	COMPANY: Texas Instruments	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: bq76PL536AEVM-3 Stack Design <Code>	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE:	SIZE: D
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: CIRCUIT 3 PWR004	REV: E3
SCALE: <Scale>		SHEET: 4 OF 5	

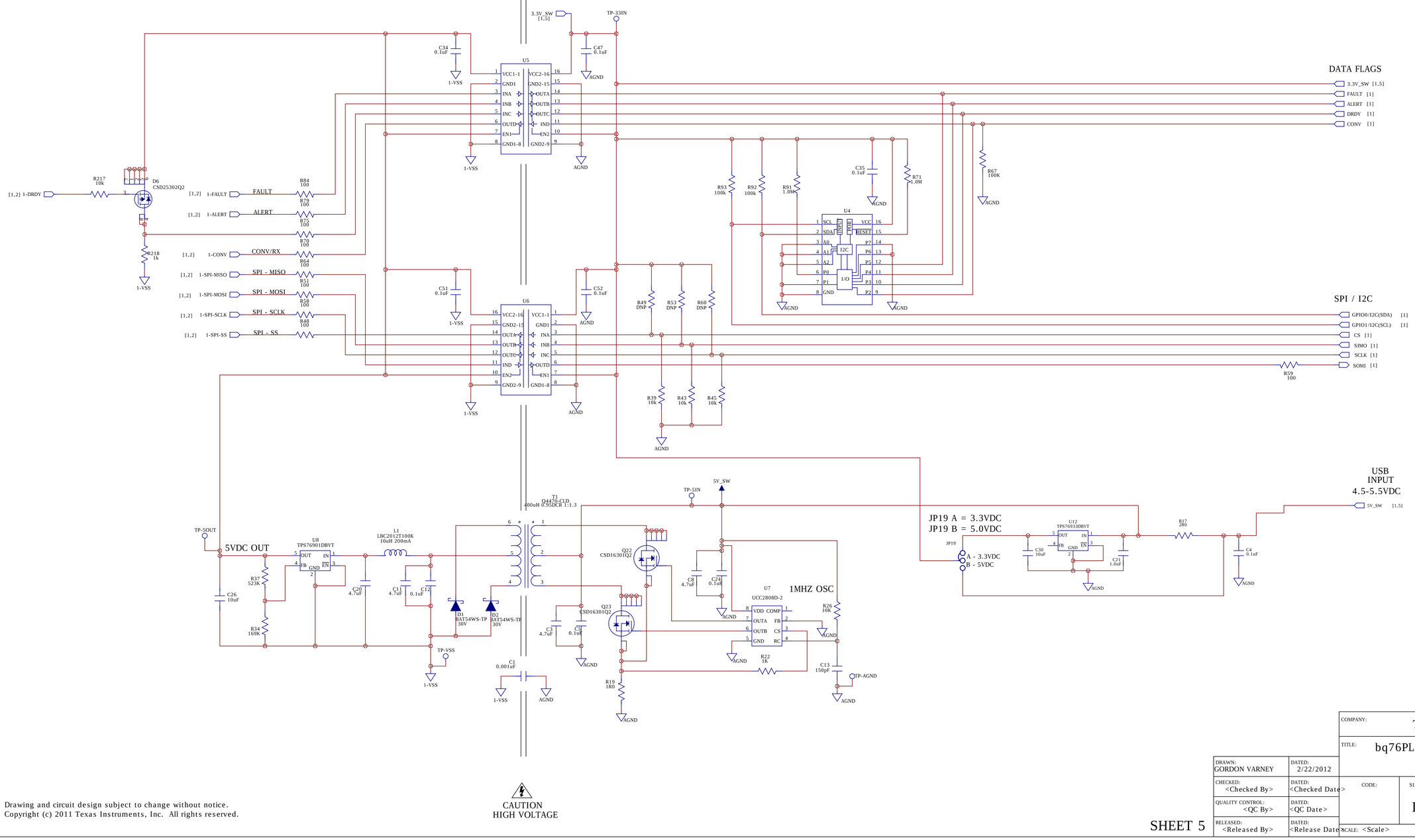
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

CAUTION
HIGH VOLTAGE

ISOLATION BOUNDRY
48 MIL ISOLATION REQUIRED

ALL RESISTERS 1% UNLESS NOTED

CAUTION: WHEN USING AN EXTERNAL MICROCONTROLLR PULL UP RESITORS CAN APPLY VOLTAGE TO THE MICRO WHEN THE MICRO IS POWERED DOWN.



Drawing and circuit design subject to change without notice.

CAUTION
HIGH VOLTAGE

SHEET 5

DRAWN: GORDON VARNEY	DATED: 2/22/2012	COMPANY: Texas Instruments	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: bq76PL536AEVM-3 Stack Design <Code>	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE:	SIZE: D
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: ISOLATOR PWR004	REV: E3
		SCALE: <Scale>	SHEET: 5 OF 5