

**Notes, Unless Otherwise Specified:**

1. Resistance Values are in Ohms.
2. Capacitance Values are in Microfarads.
3. Inductance Values are in Microhenries.
4. Highest Reference Designator used:
 

A. IC's	U26
B. Resistors	R70
C. Capacitors	C174
D. Inductors	L2
E. Transistors	--
F. LED	--
G. Crystals	Y3
H. Connectors/Headers	J4
I. Switches	SW1
J. Test Points	TP58
5. The following is the list of uninstalled parts:
6. All 0.1uF and 0.01uF caps are decoupling caps unless otherwise noted. They are shown on the page with ICs they should be placed near.
7. Board Properties:
  - A. Route to within 10% MANHATTAN Distance
  - B. 50 +/-5 Ohm Matched Impedance
  - C. Outer Layers 0.5 OZ Cu /W 0.5 OZ Au Plating
  - D. Inner Layer 1.0 OZ Cu
  - E. FR4 Board Material
  - F. Minimum Trace Width/Spacing 8 Mils
  - G. Minimum Via Size 12/24 Mils
  - H. Approximate Board Size 10 x 10 cm<sup>2</sup>
  - I. Layer Stackup:
    1. Top - Signal Routing
    2. Power Plane - Split Plane: +1.8V For DSP Core, +3.3V For DSP I/O
    3. Ground Plane - Split Plane: GND For Digital, AGND For Analog
    4. Bottom - Signal Routing


REV	Description	Date	Approved
A	Initial schematic ready for layout.	2005-12-8	

**Schematic Index:**

1. (Board Name) Notes and Contents
2. UART
3. CPLD&SRAM
4. AD
5. DA/DI/DO
6. POWER
7. Extern

Revision Status of Sheets

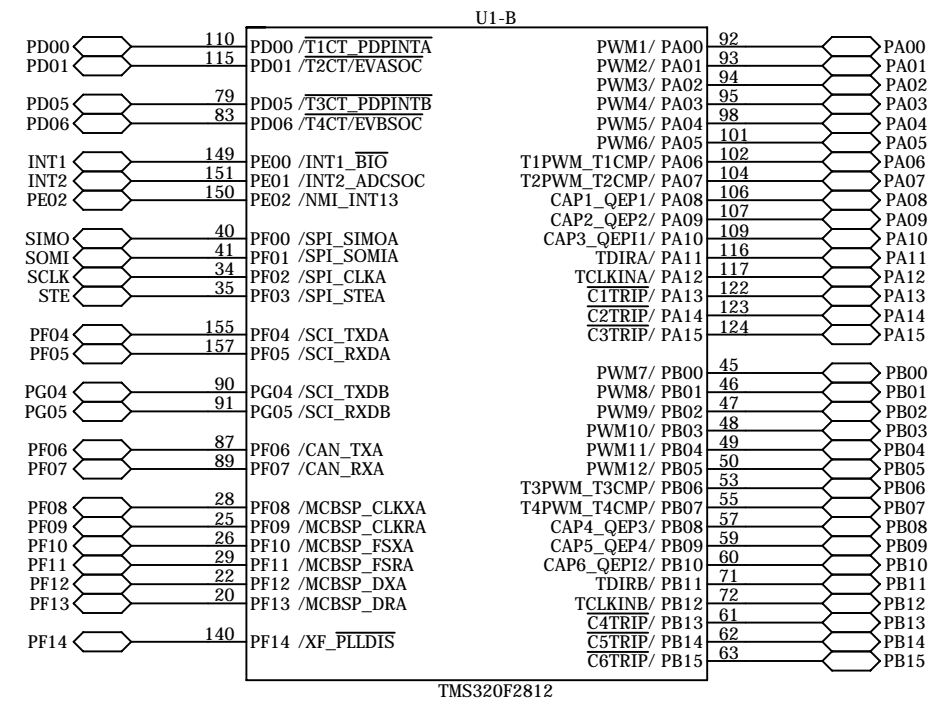
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REV															ENGR:	Date:	
SH															MGR:	Date:	
REV															QA:	Date:	
SH	8	9	10	11	12	13	14							MFG:	Date:		
REV															RLSE:	Date:	
SH	1	2	3	4	5	6	7	Application									

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Title:		SEED-DPS2812M	
Size:	B	Document No.:	7.820.108
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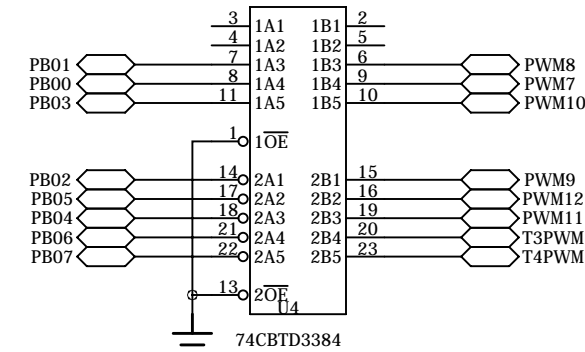
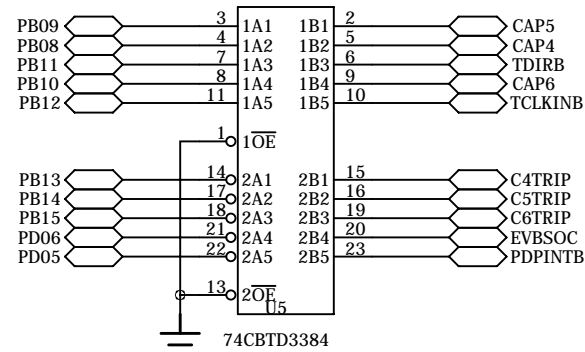
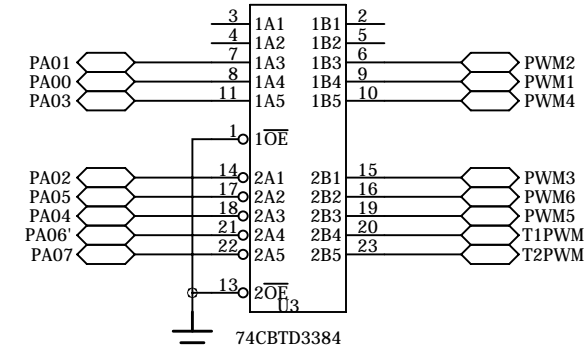
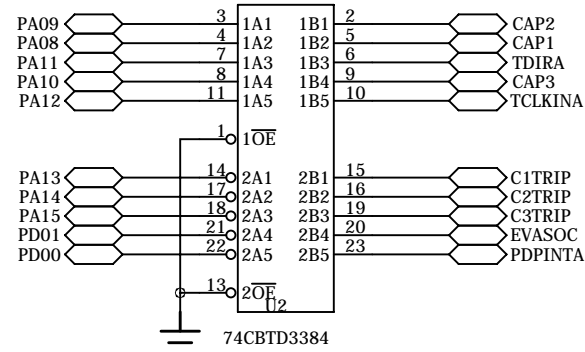
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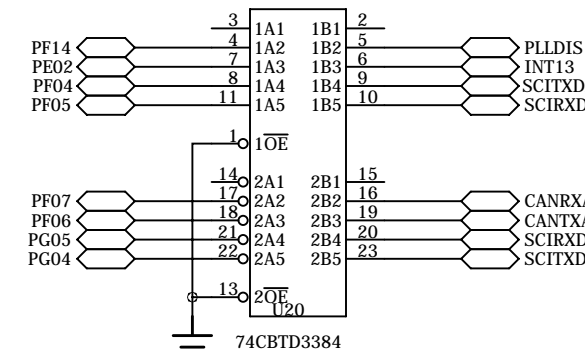
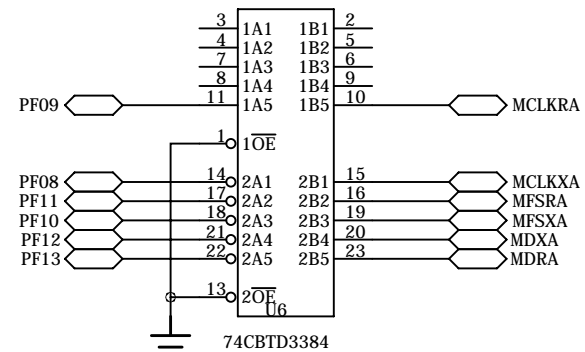
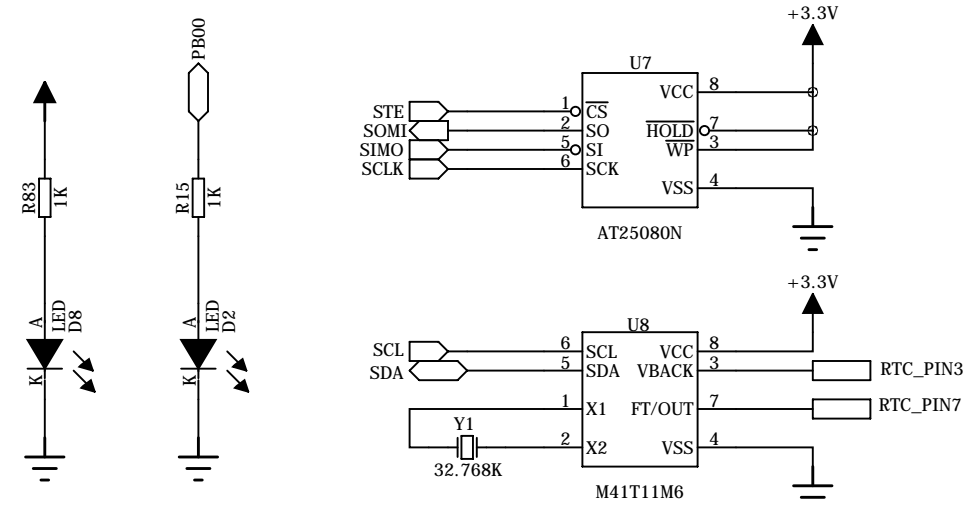
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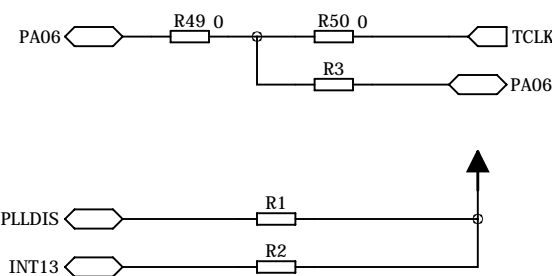
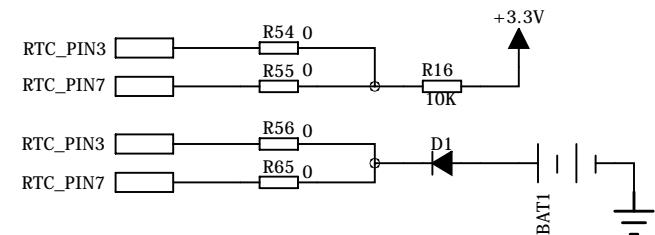
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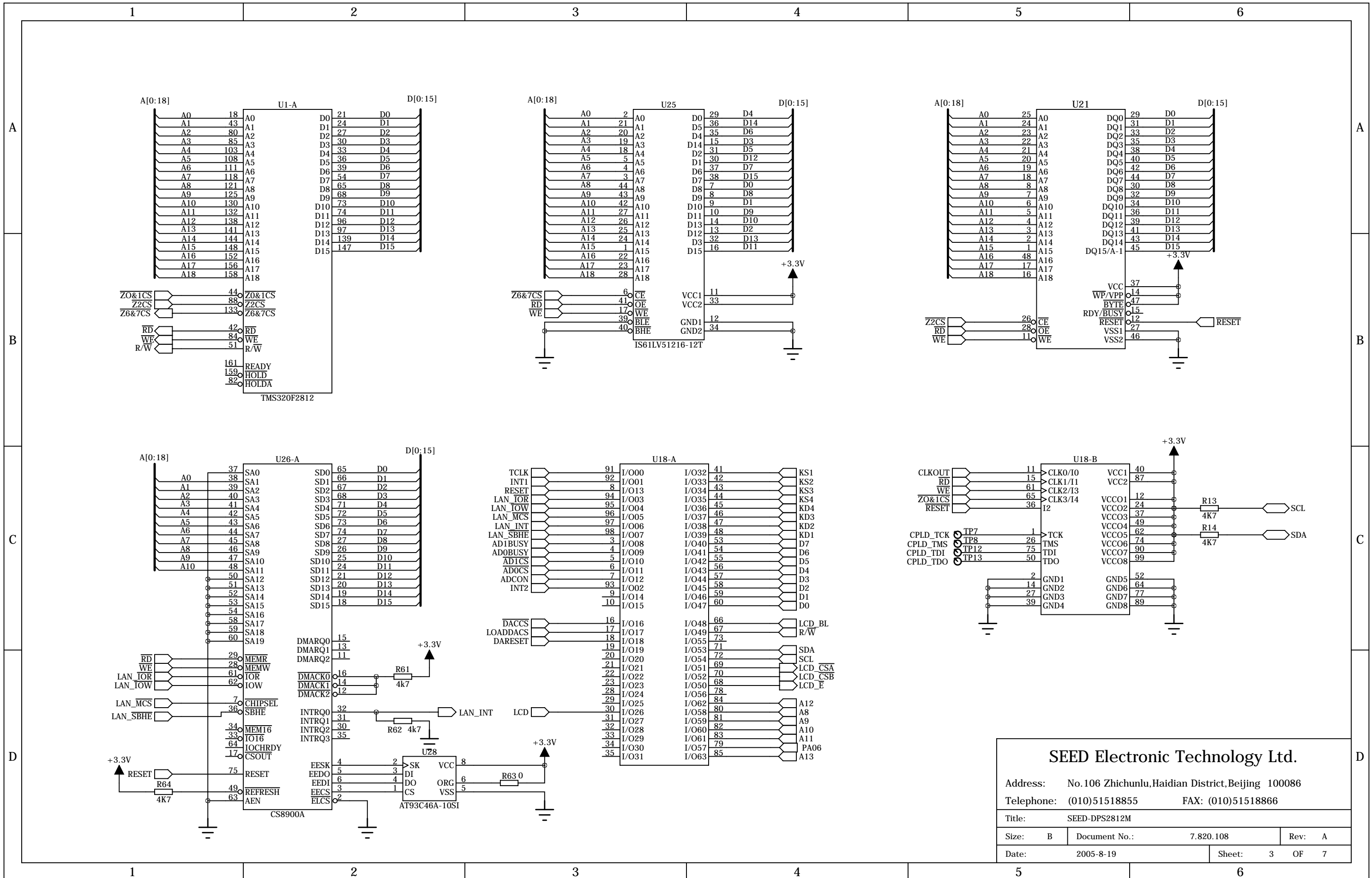
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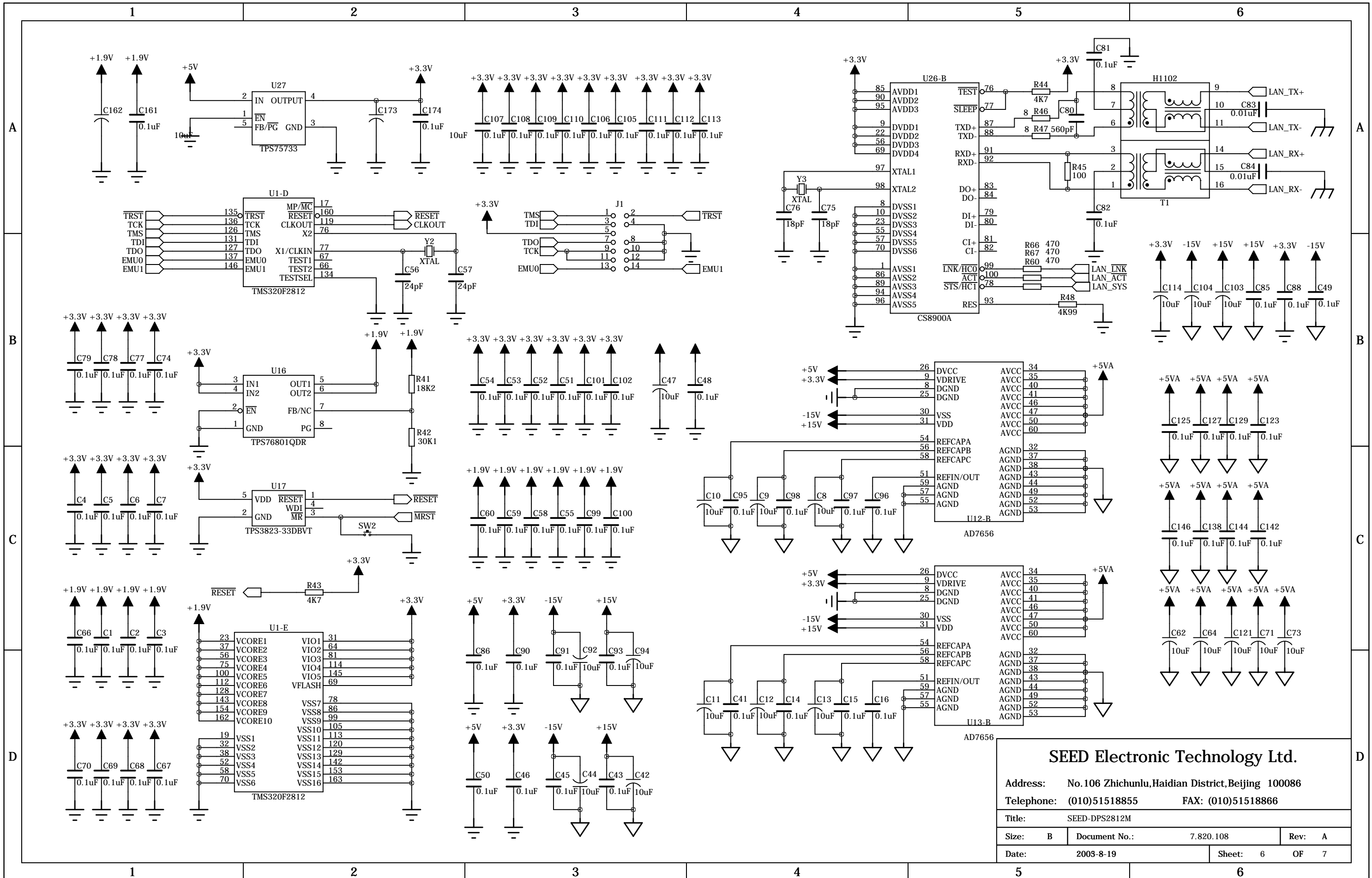


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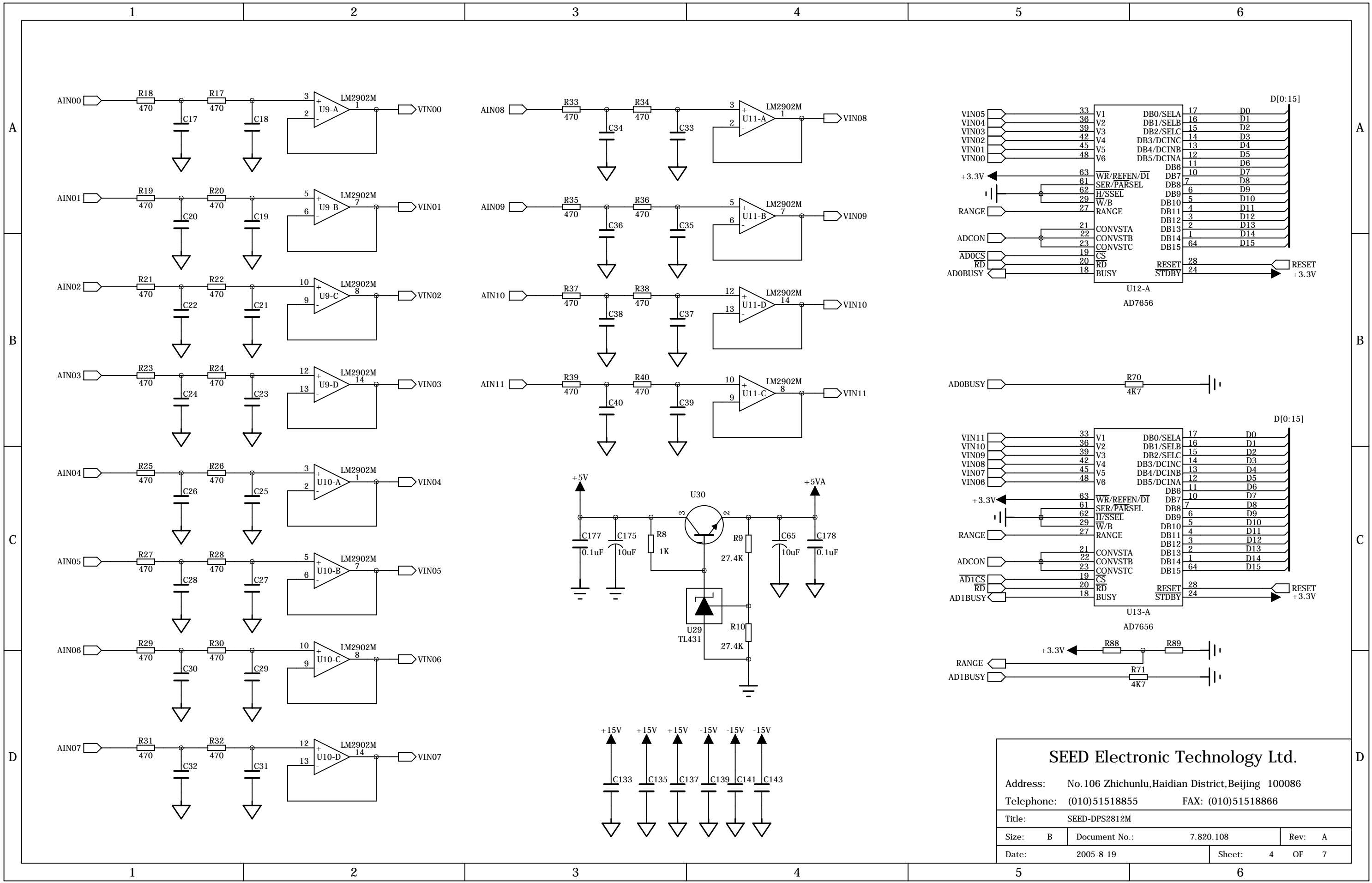


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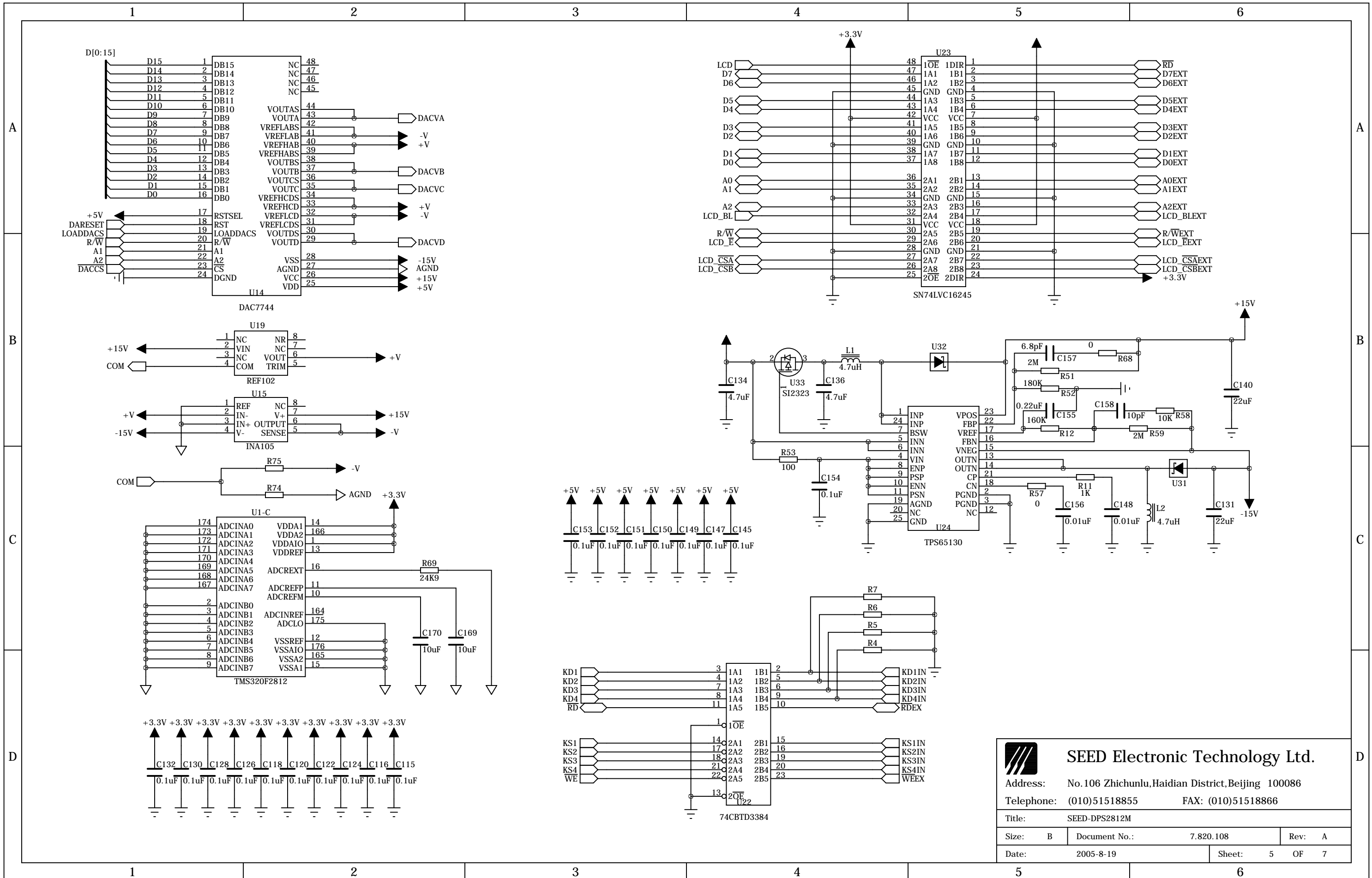
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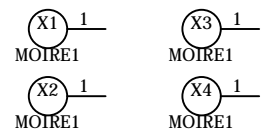
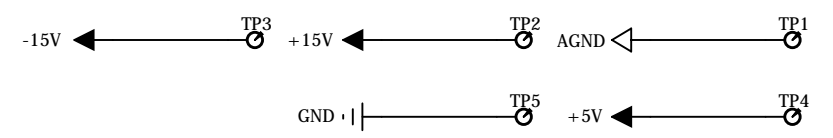
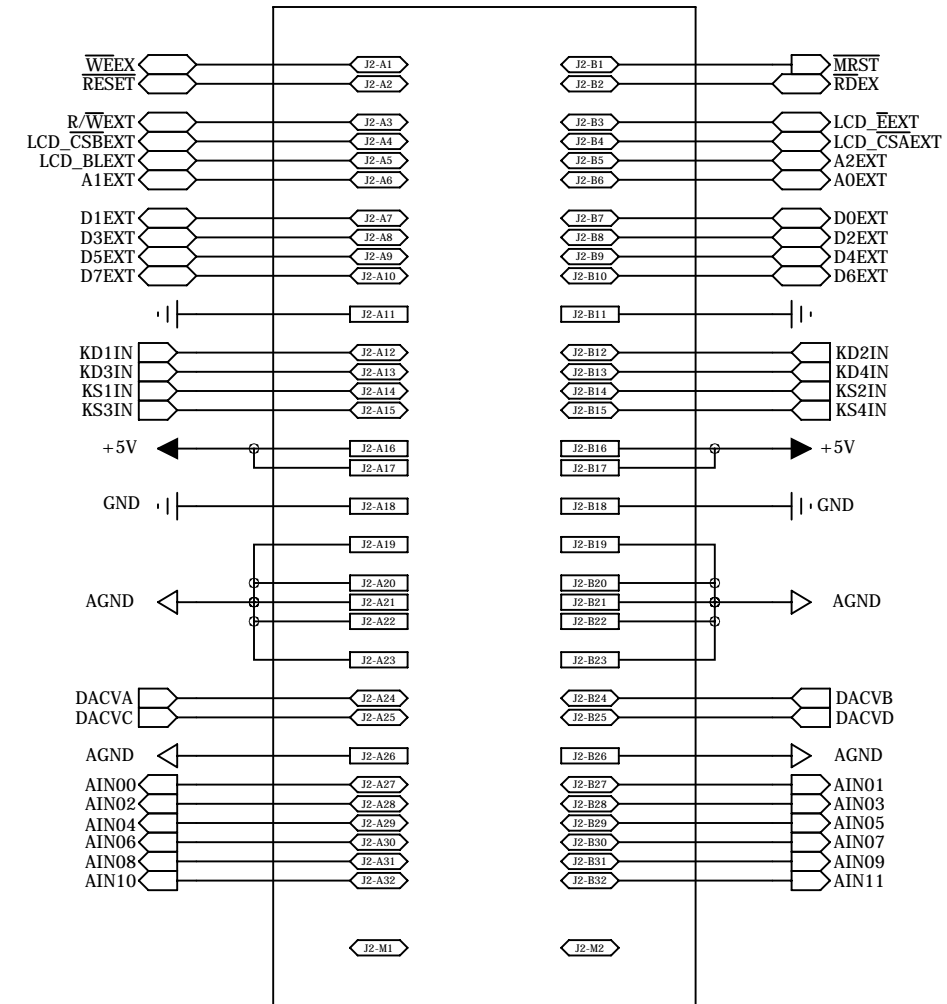
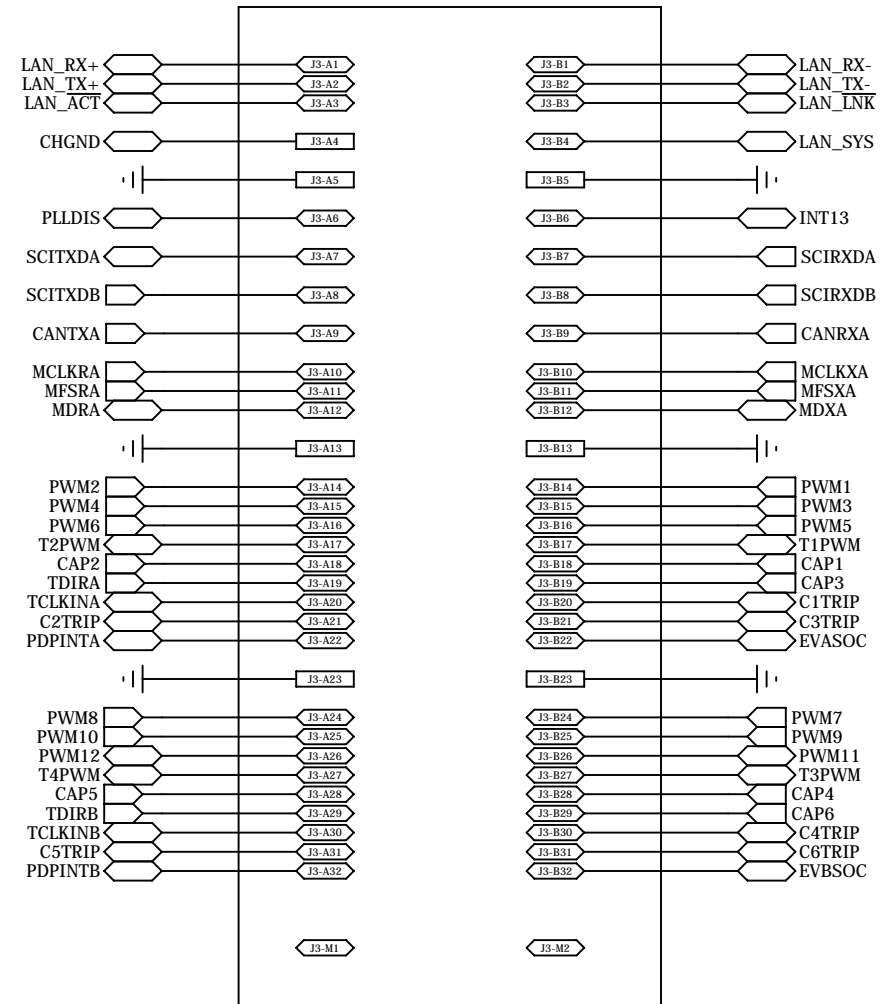
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