

# **AN-2292 Designing an Isolated Buck (Flybuck) Converter**

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## **ABSTRACT**

In many applications, one or more low-cost, simple to use, isolated power supplies working from input voltages up to 100V are needed. Traditional solutions use flyback converters to generate this bias supply. Flyback designs typically utilize asymmetric transformers turns ratios for primary and secondary power windings, with an optocoupler and reference, or an auxiliary winding for feedback regulation. Additionally, flyback converters need an elaborate compensation design for stability. This results in a tedious design process, bulky solution, with a higher component count and cost.

An isolated buck converter (flybuck) uses a synchronous buck converter with coupled inductor windings to create isolated outputs. Isolated converters utilizing flybuck topology use a smaller transformer for an equivalent power transfer as the transformer primary and secondary turns ratios are better matched. There is no need for an optocoupler or auxiliary winding as the secondary output closely tracks the primary output voltage, resulting in smaller solution size and cost.

This article presents the basic operating principle of an isolated buck converter. The operating current and voltage waveforms are explained and design equations are derived. The design example shows a step-by-step procedure for designing a practical two-output 3W isolated buck converter.

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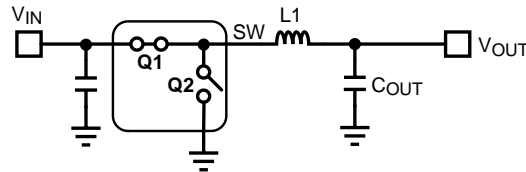
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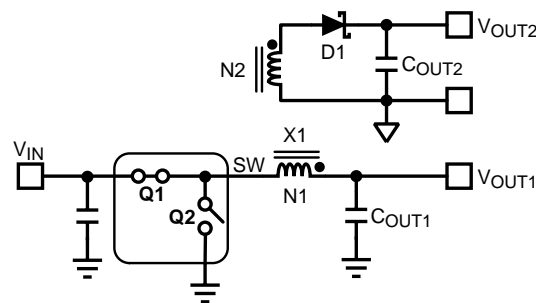
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## 1 Flyback Converter

An isolated buck converter, also known as flyback converter, is created by replacing the output filter inductor (L1) in a synchronous buck converter with a coupled inductor (X1) or flyback-type transformer, and rectifying the secondary winding voltage using a diode (D1) and a capacitor (C<sub>OUT2</sub>). The topology can be extended to any number of isolated secondary outputs. It also can be used to generate one or more inverting outputs.



1a) A Synchronous Buck Converter



1b) An Isolated Buck Converter (Fly-back)

**Figure 1. Creating an Isolated Buck Converter by Modifying a Synchronous Buck Converter**

The primary output voltage equation is identical to a buck converter and is given by [Equation 1](#):

$$V_{OUT1} = \frac{T_{ON}}{T_{ON} + T_{OFF}} V_{IN} = D \times V_{IN} \quad (1)$$

and the secondary output voltage is given by [Equation 2](#):

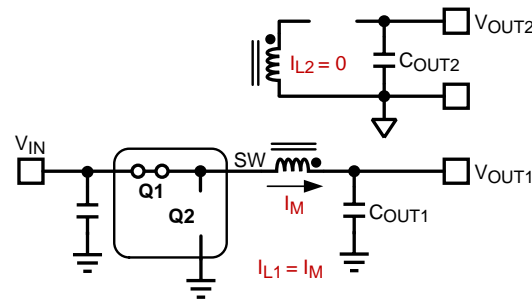
$$V_{OUT2} = \frac{N2}{N1} V_{OUT1} - V_F \quad (2)$$

where  $V_F$  is the forward voltage drop of the secondary rectifier diode, and  $N1$ ,  $N2$  are the number of turns in the primary and secondary windings, respectively. The secondary output ( $V_{OUT1}$ ) closely tracks the primary output voltage ( $V_{OUT1}$ ) without the need for additional transformer winding or an optocoupler for feedback across the isolation boundary.

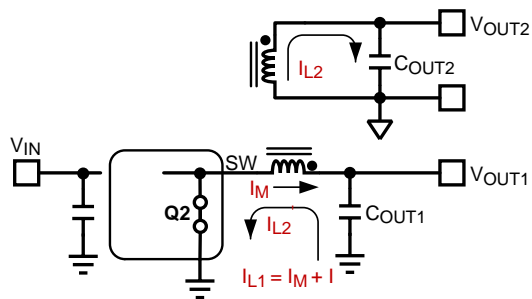
[Figure 2](#) shows the operating modes in an isolated configuration during  $T_{ON}$ , when the high-side buck switch is on; and  $T_{OFF}$ , when the low-side switch is on. Current in the two windings is also shown. During  $T_{ON}$ , the current in the secondary winding is zero as the secondary diode is reverse biased by a voltage equal to

$$V_{IN} \times \frac{N2}{N1} \quad (3)$$

The current in the primary winding is the same as the magnetizing current (similar to a buck converter inductor).



2a) TON (Q1: ON, Q2: OFF)



2b) TOFF (Q1: OFF, Q2: ON)

Figure 2. Isolated Buck Converter Switching Status

During TOFF, the current in the secondary winding is decided by the resonant tank formed by  $C_{OUT1}$ , the leakage inductance of the coupled inductor, and  $C_{OUT2}$ . The current in the primary winding is the sum of the magnetizing current (similar to a buck converter inductor current), and the reflected current from the secondary winding. These operating waveforms are shown in Figure 3.

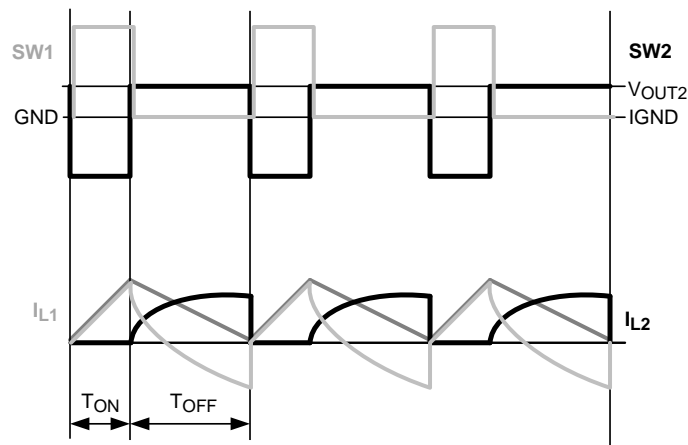


Figure 3. Isolated Buck Operating Waveforms

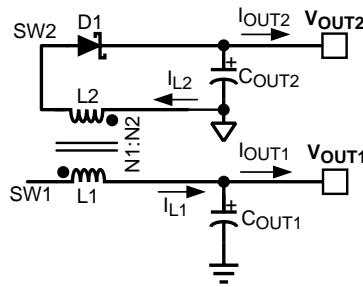
## 2 Maximum Output Current Equations

On a cycle-by-cycle average basis, the winding and output currents have the following relationship Figure 4.

$$I_{L1} = I_{OUT1} \tag{4}$$

and

$$I_{L2} = I_{OUT2} \quad (5)$$


**Figure 4. Isolated Buck Output Stage with Coupled Inductor**

The combined inductor current waveform ( $iL1 + iL2$ ), which is equal to the magnetizing current, is identical to a buck converter. The peak inductor and switch current during on-time is given by Equation 6:

$$i_{sw(peak)} = i_{L1(peak)} = I_{L1} + I_{L2} + \frac{\Delta I_{L1} + \Delta I_{L2}}{2} = I_{OUT1} + I_{OUT2} + \frac{\Delta I_{L1}}{2} \quad \text{电荷守恒:} \quad (6)$$

where we make use of the fact that during on-time (TON) there is no current in secondary winding. Therefore, the maximum total load current is given by Equation 7:

$$I_{OUT1} + I_{OUT2} = I_{LIM(MIN)} - \frac{\Delta I_{L1}}{2} \quad (7)$$

where the total load current is defined as the sum of the load currents at the two outputs. For turn-ratios ( $N2/N1$ ) not equal to unity,  $I_{OUT2}$  should be multiplied by the turn-ratio in Equation 7, shown here in Equation 8:

$$I_{OUT1} + I_{OUT2} \frac{N2}{N1} = I_{LIM(MIN)} - \frac{\Delta I_{L1}}{2} \quad (8)$$

The maximum peak-to-peak current ripple in the primary winding is given by Figure 5:

$$\Delta I_{L1} = \frac{(V_{IN(MAX)} - V_{OUT})}{L1 \times f_{SW}} \frac{V_{OUT}}{V_{IN(MAX)}} \quad (9)$$

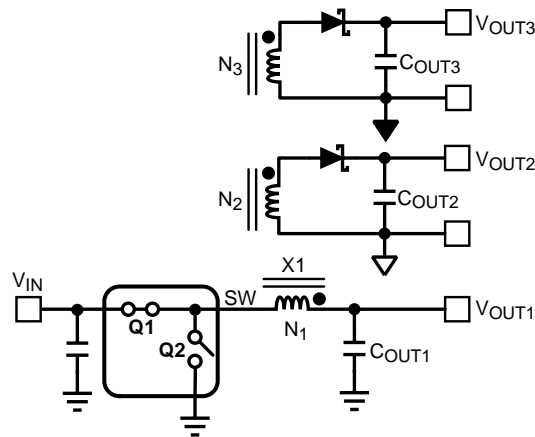

**Figure 5. Isolated Buck Regulator with Three Outputs**

Table 1 presents equations for non-equal turn-ratios and three windings (Figure 5). The generalization to any number of windings is straightforward.

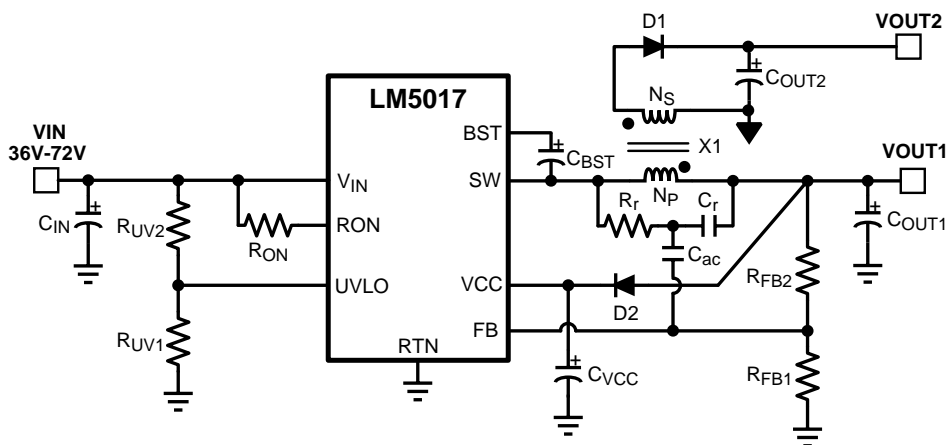
**Table 1. Isolated Buck Regulator Design Equations**

Description	Equations
Output Voltages	$V_{OUT1} = \frac{T_{ON}}{T_{ON} + T_{OFF}} V_{IN} = D \times V_{IN} \quad (10)$
	$V_{OUT2} = \frac{N2}{N1} V_{OUT1} - V_F \quad (11)$
	$V_{OUT3} = \frac{N3}{N1} V_{OUT1} - V_F \quad (12)$
Cycle-by-Cycle Average Quantities	$I_{L1} = I_{OUT1} \quad (13)$
	$I_{L2} = I_{OUT2} \quad (14)$
	$I_{L3} = I_{OUT3} \quad (15)$
Peak Currents in HS FET and Primary Winding	$i_{sw(peak)} = i_{L1(peak)} = I_{OUT1} + \frac{N2}{N1} I_{OUT2} + \frac{N3}{N1} I_{OUT3} + \frac{\Delta I_{L1}}{2} \quad (16)$
Primary Winding Peak-to-Peak Current Ripple	$\Delta I_{L1} = \frac{(V_{IN(MAX)} - V_{OUT})}{L1 \times f_{SW}} \frac{V_{OUT}}{V_{IN(MAX)}} \quad (17)$

### 3 Design Example

The design example illustrated in Figure 6 details the design procedure for a two-output isolated buck converter.

Design Specifications	
Input Voltage Range (V <sub>IN</sub> )	36V - 72V
Primary Output Voltage (V <sub>OUT1</sub> )	10V
Secondary Output Voltage (V <sub>OUT2</sub> )	10V
Primary Load Current (I <sub>OUT1</sub> )	100mA
Secondary Load Current (I <sub>OUT2</sub> )	200mA
Switching Frequency (f <sub>sw</sub> )	750kHz



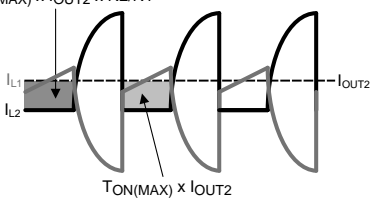
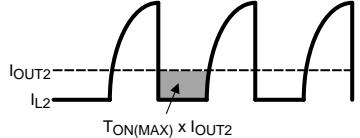
**Figure 6. Two Output Isolated Buck Reference Schematic**

In this example, we start with a standard two-output circuit using TI's 100 V synchronous buck regulator, LM5017, and calculate the component values. We begin with buck converter component calculations and qualify some of the steps for the isolated configuration. The calculation steps are listed in Table 2.

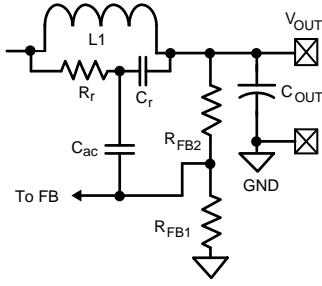
**Table 2. Component Calculation/Selection Steps for a Two-Output Isolated Buck**

Component Name	Calculation Steps	Selected Value/Rating
$R_{FB1}, R_{FB2}$	This parameter is selected by the user. Choose $R_{FB1}=1\text{k}\Omega$ $V_{OUT1} = 1.225\text{V} \times \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \quad (18)$ $\rightarrow R_{FB2} = \left(\frac{V_{OUT1}}{1.225} - 1\right) \times R_{FB1} = 7.16 \text{ k}\Omega \quad (19)$	1k $\Omega$ , 7.16k $\Omega$
$C_{VCC}$	Select a 1 $\mu\text{F}$ capacitor of 16V or higher rating as recommended in the LM5017 datasheet.	1 $\mu\text{F}$ , 16V
$C_{BST}$	Select a 0.01 $\mu\text{F}$ capacitor of 16V or higher rating, as recommended in the datasheet.	0.01 $\mu\text{F}$ , 16V
$C_{IN}$	Input capacitor should be large enough to limit the input voltage ripple $C_{IN} \geq \frac{I_{OUT(MAX)}}{8 \times f \times \Delta V_{IN}} \quad (20)$ Choosing a $\Delta V_{IN}=0.5\text{V}$ gives a minimum $C_{IN}=1.24\mu\text{F}$ . A standard value of 2.2 $\mu\text{F}$ is selected. Input capacitor should be rated for the maximum input voltage under all conditions.	2.2 $\mu\text{F}$ , 100V
$R_{ON}$	From datasheet, $f_{SW} = \frac{V_{OUT1}}{K \times R_{ON}} \quad (21)$ Where $K = 1 \times 10^{-10} \rightarrow R_{ON}=133 \text{ k}\Omega$	130k $\Omega$
$R_{UV1}, R_{UV2}$	UVLO resistors $R_{FB1}$ and $R_{FB2}$ set the UVLO threshold and hysteresis according to the following relationship: $V_{IN(HYS)} = I_{HYS} \times R_{UV2} \quad (22)$ and $V_{IN(UVLO, rising)} = 1.225\text{V} \times \left(\frac{R_{UV2}}{R_{UV1}} + 1\right) \quad (23)$ where $I_{HYS}=20\mu\text{A}$ . Setting UVLO hysteresis of 2.5V and UVLO rising threshold of 36V results in $R_{UV1}=4.42\text{k}\Omega$ ; and $R_{UV2}=125\text{k}\Omega$	4.42k $\Omega$ , 125k $\Omega$
X1	A coupled inductor or a flyback type transformer is required for this topology. Energy is transferred from primary to secondary when the synchronous switch of the buck is ON. Using Equation 16 for the peak inductor current equation in Table 1, the maximum inductor current ripple that can be tolerated is given by: $\Delta I_{L1} = (0.7 - I_{OUT1} - I_{OUT2} \times \frac{N2}{N1}) \times 2 = 0.8\text{A} \quad (24)$ Using Equation 17 for the peak-to-peak inductor current ripple equation, the minimum inductor value is given by: $L1 = \frac{(V_{IN(MAX)} - V_{OUT})}{\Delta I_{L1} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN(MAX)}} = 14.4 \mu\text{H} \quad (25)$ A higher value such as 22 $\mu\text{H}$ or 33 $\mu\text{H}$ for primary inductance can be selected to keep the primary winding and high-side switch current below the minimum peak current limit. For our design, a 33 $\mu\text{H}$ value is selected for primary inductance. For this chosen primary inductance, in the primary inductor current ripple during TON is Equation 26 $\Delta I_{L1} = \frac{(V_{IN(MAX)} - V_{OUT})}{L1 \times f_{SW}} \times \frac{V_{OUT}}{V_{IN(MAX)}} \quad (26)$ A 1:1 turns ratio is selected, resulting in Equation 27 $V_{OUT2} = \frac{N2}{N1} V_{OUT1} - V_F \approx 9.3\text{V} \quad (27)$	L1=33 $\mu\text{H}$ , 1:1 turns ratio
D1	The voltage across D1 when the high side buck switch is on is $V_{D1} = \frac{N2}{N1} V_{IN} \quad (28)$ For a $V_{IN,MAX}=72\text{V}$ , a 100V Schottky is selected.	100V, 1A DLFS1100-7

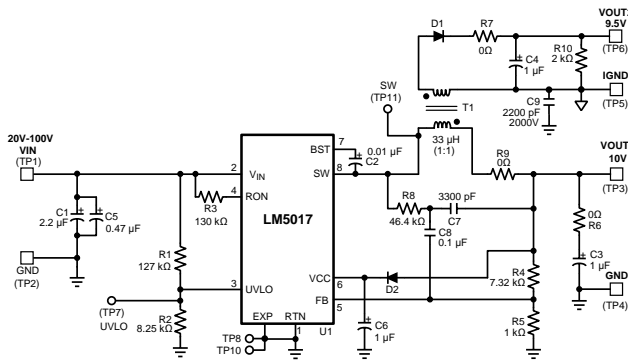
**Table 2. Component Calculation/Selection Steps for a Two-Output Isolated Buck (continued)**

Component Name	Calculation Steps	Selected Value/Rating
<p><math>C_{OUT1}</math></p>	<p>In a buck converter,</p> $\Delta V_{OUT} = \frac{\Delta I_{L1}}{8 \times f \times C_{OUT1}} \quad (29)$ <p>and therefore for an output voltage ripple of ~50mV gives, <math>C_{OUT1} = 1.16\mu\text{F}</math>. Selecting a standard value of <math>1\mu\text{F}</math> results in <math>\Delta V_{OUT} = 60\text{mV}</math> at <math>V_{IN} = 72\text{V}</math> and <math>\Delta V_{OUT} = 50\text{mV}</math> at <math>V_{IN} = 36\text{V}</math>. The figure below shows the primary winding current waveform (<math>I_{L1}</math>). The reflected secondary winding current adds to the primary winding current. Because of this the output voltage ripple is not the same as in a non-isolated buck converter. The output capacitor value calculated in Equation 29 should be used as the starting point. Actual optimization of output capacitor over the whole line/load range must be done experimentally. A better approximation of the primary output capacitor voltage ripple is given by Equation 30:</p> $\Delta V_{OUT1} = \frac{(I_{OUT2} \times \frac{N2}{N1}) \times T_{ON(MAX)}}{C_{OUT1}} \approx 75 \text{ mV} \quad (30)$  <p style="text-align: center;">Current Waveforms for <math>C_{OUT1}</math> Ripple Calculation (31)</p> <p>As can be seen from the primary inductor current waveform in the above figure, in case of low leakage, the primary winding current reverses immediately when the secondary winding starts conducting. Therefore, the reflected secondary winding current induced primary output ripple voltage is not phase-lagged with respect to the switch node waveform. Therefore, the reflected load current induced voltage ripple does not need to be compensated for with the ripple injection circuit. If lower output voltage ripple is required, a higher value should be selected for <math>C_{OUT1}</math> and/or <math>C_{OUT2}</math>.</p>	<p><math>1\mu\text{F}</math>, 25V, X7R</p>
<p><math>C_{OUT2}</math></p>	<p>A simplified waveform for secondary output current (<math>I_{OUT2}</math>) and the current in the secondary winding is shown in the figure below.</p>  <p style="text-align: center;">Secondary Current Waveforms for <math>C_{OUT2}</math> Ripple Calculation (32)</p> <p>The secondary output current (<math>I_{OUT2}</math>) is sourced by <math>C_{OUT2}</math> during one time <math>T_{ON}</math>. Ignoring the current transitions time in the secondary winding, the secondary output capacitor ripple voltage can be calculated using Equation 33:</p> $\Delta V_{OUT2} = \frac{I_{OUT2} \times T_{ON(MAX)}}{C_{OUT2}} \quad (33)$ <p>For a 1:1 transformer turns ratio the primary and secondary voltage ripple equations are identical. Therefore, <math>C_{OUT2}</math> is chosen to be equal to <math>C_{OUT1}</math> (<math>1\mu\text{F}</math>) to get comparable ripples on primary and secondary outputs. If lower output voltage ripple is required, a higher value should be selected for <math>C_{OUT1}</math> and/or <math>C_{OUT2}</math>.</p>	<p><math>1\mu\text{F}</math>, 25V, X7R</p>

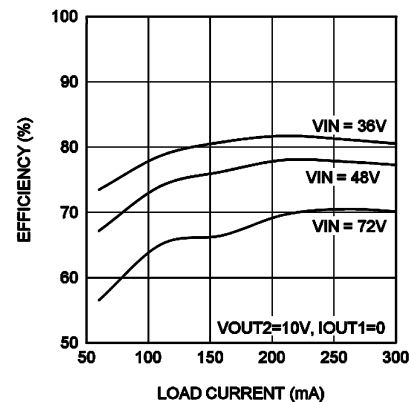
**Table 2. Component Calculation/Selection Steps for a Two-Output Isolated Buck (continued)**

Component Name	Calculation Steps	Selected Value/Rating
Rr, Cr, Cac	<p>Type III ripple circuit as described in the LM5017 datasheet is preferred for isolated configuration. Type I and Type II ripple circuits suffer from larger jitter as the reflected load current affects the feedback ripple. For a constant on time converter to be stable, the injected in-phase ripple should be larger than the capacitive ripple on C<sub>OUT1</sub>.</p>  <p style="text-align: center;">Type II Ripple Circuit (34)</p> <p>Using type III ripple circuit equations, the target ripple should be greater than the capacitive ripple generated at the primary output.</p> $C_r = 1000 \text{ pF}$ $C_{ac} = 0.1 \text{ }\mu\text{F}$ $R_r C_r \leq \frac{(V_{IN(MIN)} - V_{OUT}) \times T_{ON}}{50 \text{ mV}} \quad (35)$ <p>Resulting in Rr= 180kΩ. This is the borderline case of stable ripple. Half to a fourth of this resistance should be selected for sufficient margin for variations in TON, C<sub>OUT1</sub>, and other components. For this design Rr = 46.4kΩ; is selected for robust operation.</p>	46kΩ, 0805, 1000pF, 0.1μF (25V)
D2 (optional)	D2 is an optional diode connected between V <sub>OUT1</sub> and V <sub>CC</sub> regulator output. When V <sub>OUT1</sub> is > V <sub>CC</sub> the V <sub>CC</sub> supplied from V <sub>OUT1</sub> . This results in reduced losses in V <sub>CC</sub> regulator inside the IC.	20V, 50mA

The final schematic for the isolated power supply is shown in Figure 7. The experimental results for this circuit are presented in Figure 8, Figure 9, and Figure 10.



**Figure 7. Complete Schematic for an LM5017–Based Isolated Converter**



**Figure 8. Efficiency at 750 kHz, V<sub>OUT1</sub> = 10V**



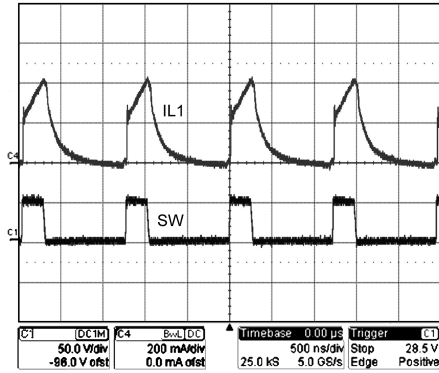


Figure 9. Steady State Waveform ( $V_{IN} = 48V$ ,  $I_{OUT1} = 100mA$ ,  $I_{OUT2} = 200mA$ )

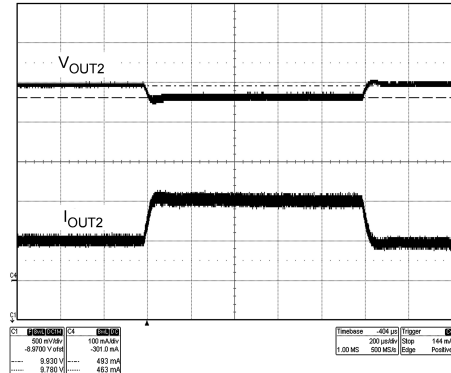


Figure 10. Step Load Response ( $V_{IN} = 48V$ ,  $I_{OUT1} = 0$ , Step Load on  $I_{OUT2} = 100mA$  to  $200mA$ ).

#### 4 Conclusions

An isolated buck converter (or flyback) converter was presented that does not require any additional winding or optocoupler for regulating an isolated output. The operating principle of the topology was also presented along with operating current and voltage waveforms. The relationship between the primary and the isolated output voltages and output currents were presented. We also developed design equations for estimating the peak primary switch current for specified load currents. The equations in this design can also be used to determine the maximum load current that the converter can provide for a given peak current limit. Simplified approximations for output voltage ripples were also presented. A detailed design procedure was presented for a 3W two-output isolated buck converter with a primary output and an isolated output using a 100V synchronous buck regulator IC.

An isolated buck converter can be used to replace a flyback converter for low-power isolated regulator applications with potential savings in complexity, number of components, and cost. Learn more about flyback converters on the Power Management website at [www.ti.com](http://www.ti.com).

#### 5 References

LM5017: 100V,600mA Constant On-Time Synchronous Buck Data Sheet ([SNVS783](#))

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Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
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