

Understanding the load-transient response of LDOs

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Advanced Analog Products

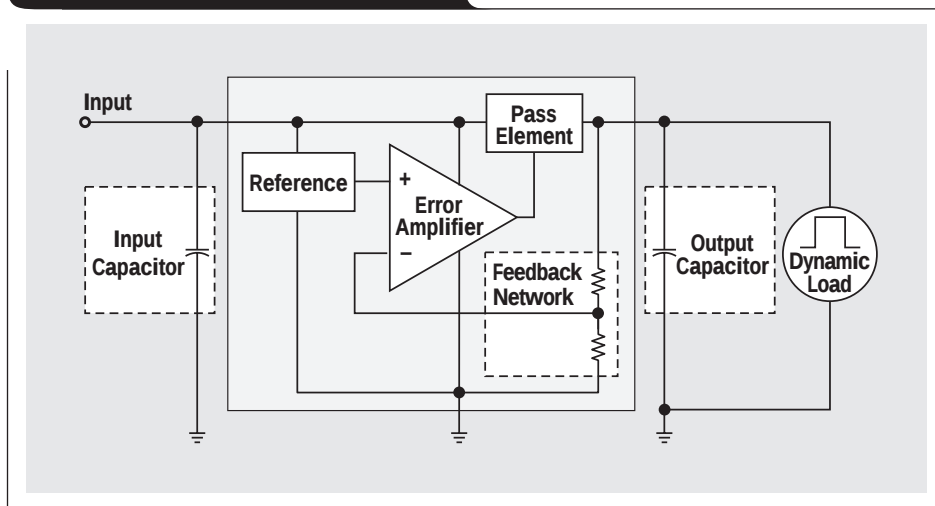
Introduction

Low-dropout linear regulators (LDOs) are commonly used to provide power to low-voltage digital circuits, where point-of-load regulation is important. In these applications, it is common for the digital circuit to have several different modes of operation. As the digital circuit switches from one mode of operation to another, the load demand on the LDO can change quickly. This quick change of load results in a temporary glitch of the LDO output voltage. Most digital circuits do not react favorably to large voltage transients. For the digital circuit designer, minimizing an LDO's transient response is an important task.

LDOs are available in a wide variety of output voltages and current capacities. Some LDOs are tailored to applications where a good response to a fast transient is important. The TPS751xx, TPS752xx, TPS753xx, and TPS754xx families of LDOs from Texas Instruments are examples of fast-transient-response LDOs. The TPS751xx and TPS753xx families are rated at 1.5 A of output current, while the TPS752xx and TPS754xx families can provide up to 2 A. All four families use PMOS pass elements to provide a low dropout voltage and low ground current. These devices come in a PowerPAD™ package that provides an effective way of managing the power dissipation in a TSSOP footprint.

Figure 1 shows the circuit elements of a typical LDO application. The main components within a monolithic LDO include a pass element, precision reference, feedback network, and error amplifier. The input and output capacitors are usually the only key elements of the LDO that are not contained in a monolithic LDO. There are a number of factors that affect the response of an LDO circuit to a load transient. These factors include the internal compensation of the LDO, the amount of output capacitance, and the parasitics of the output capacitor.

Figure 1. Typical LDO components



LDO compensation

The primary feedback loop of the LDO, consisting of the output capacitor, feedback network, error amplifier, and pass element, determines the LDO's frequency response. The unity gain crossover frequency and stability of the LDO circuit affect the overall transient response of the LDO.

The crossover frequency affects the settling time of the linear regulator circuit, where the settling time is the time elapsed from the initial onset of the load transient to the time where the output voltage returns to within a few percent of a steady-state value. A higher crossover frequency will decrease the duration of a transient condition. In most LDOs, the output capacitor and its associated equivalent series resistance (ESR) form a dominant pole in the loop response. Although larger output capacitors tend to decrease the magnitude of the transient response, they also tend to increase the settling time.

The stability of an LDO circuit can be assessed from the gain and phase margins of the loop response. A stable regulator will respond to a transient in a smooth, controlled manner, while an unstable or quasi-stable regulator will produce a more oscillatory transient response. Since the internal compensation of an LDO is fixed, only the output capacitor can be adjusted to insure stability. To assist in the proper selection of an output capacitor, LDO manufacturers typically provide limits on the acceptable values of capacitance and ESR.

This article was adapted from "Optimized LDO Response to Load Transients Requires the Appropriate Output Capacitor and Device Performance" by Brian King in the September 2000 issue of *PCIM Power Electronics Systems* by permission of Primedia's Intertec Publishing Group.

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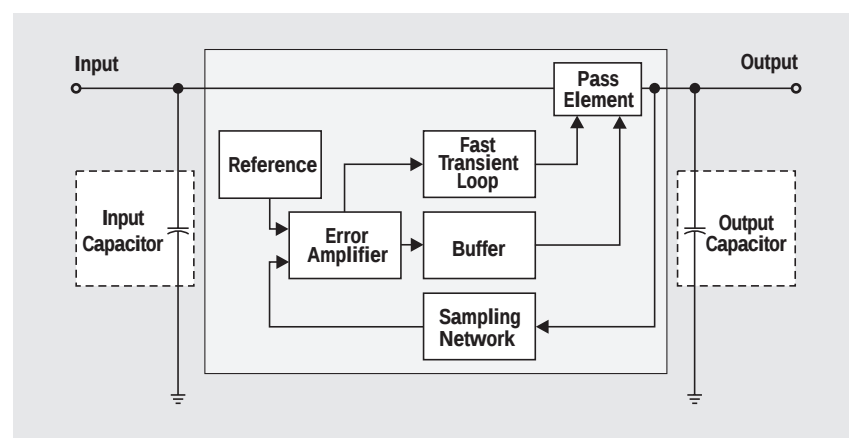
In addition to the main feedback loop, some LDOs contain a second feedback loop that allows the LDO to respond faster to large-output transients. This fast-transient loop basically bypasses the error amplifier stage and drives the pass element directly. A symbolic representation of an LDO with this secondary compensation is shown in Figure 2. By responding faster than the error amplifier compensation, LDOs that contain this loop are better able to minimize the effects of a load transient. The TPS751xx, TPS752xx, TPS753xx, and TPS754xx families of LDOs from Texas Instruments are examples of devices that contain this secondary loop.

Figures 3 and 4 show the transient response of a TPS75433 with a 100- μ F, 55-m Ω output capacitor to different load transients. The transient in Figure 3 transitions from no load to 250 mA, while the transient in Figure 4 steps from no load to 2 A. The 250-mA-load transient is not large enough to trigger the secondary loop. However, the response of the secondary feedback loop is clearly visible in the LDO response to the 2-A transient. If the secondary loop were not present, the voltage drop in Figure 4 would be much more severe.

Output capacitor

Since the LDO cannot respond instantaneously to a transient condition, there is some inherent delay time before the current through the pass element can be adjusted to accommodate the increased load current. During this delay time, the output capacitor is left to supply the entire transient current. Because of this, the amount of output capacitance and its associated parasitic elements greatly impact the transient response of the LDO circuit.

Figure 2. LDO with secondary loop for fast-transient response



The equivalent model of a typical capacitor is shown in Figure 5. All capacitors have an equivalent series resistance (ESR) and an equivalent series inductance (ESL). A number of factors affect the ESR and ESL values, such as the package type, case size, dielectric material, temperature, and frequency. The amount of capacitance, ESR, and ESL each affect the transient response in a different way.

To demonstrate the effects of the parasitics of the output capacitor, a test circuit was built by using a TPS75433 and an adjustable output capacitor model. The capacitor model was built using discrete components to model the ESL, ESR, and capacitance so that the effects of each parasitic element could be evaluated independently. Small valued air-core inductors were used to model the ESL. Low-inductance metal film resistors were used to model the ESR. The capacitance was modeled by combining multiple 10- μ F ceramic capacitors in parallel. The low ESL and low ESR of the ceramic capacitors make them good models of an ideal capacitor.

Figure 3. TPS75433 response to a 250-mA-load transient

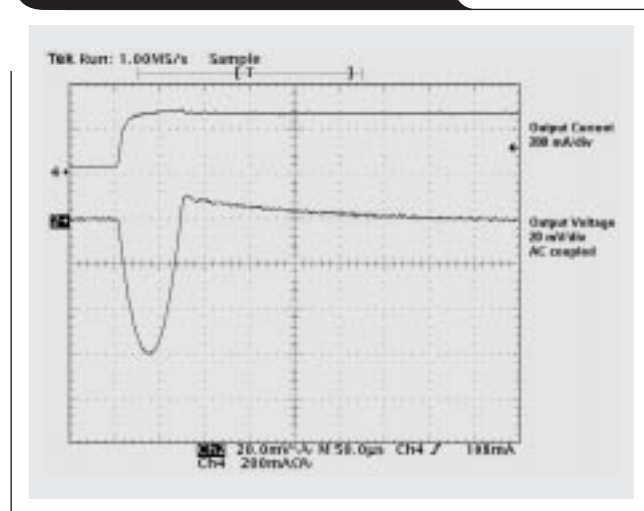
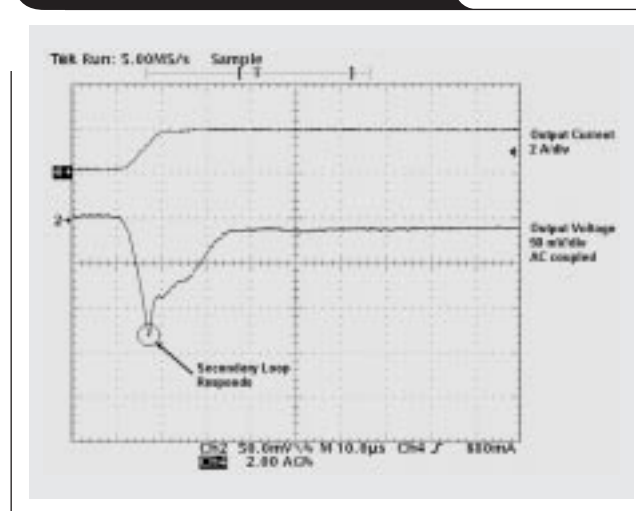


Figure 4. TPS75433 response to a 2-A-load transient



Equivalent series inductance

When a load transient occurs, the first factor that comes into play is the ESL. The transient response of various amounts of ESL is shown in Figure 6. The voltage across the ESL is equal to the product of the inductance and the rate of change of current. Initially, the ESL voltage is zero. During the rising edge of the current, a negative potential will appear across the ESL. Once the transient has reached its final value, the voltage across the ESL will return to zero. The net result is a negative voltage spike whose width is determined by the rise time of the transient and whose magnitude is determined by the slew rate of the transient step and the ESL value. The ESL value of capacitors is quite small. However, as the rate of change in current increases, the ESL-induced voltage may become bothersome. For this reason, it is a good idea to consider the ESL when selecting a capacitor for a fast-switching application, particularly if the load is sensitive to voltage spikes.

Since the parasitic inductance of PWB traces will add in series with the ESL, a good layout is key to minimizing the effects of ESL. The inductance of a trace is dependent upon the geometry of the layout. However, as a general rule, 10 nH to 15 nH are added for every inch of trace. Ideally, the input and output capacitors should be located as close as possible to the LDO. In addition, the entire LDO circuit should be located as close as possible to the load. Using planes for the LDO output and its return will also help to reduce the stray inductance.

Equivalent series resistance

The voltage across the ESR of a capacitor also adds to the transient response. The voltage across various amounts of ESR is shown in Figure 7. The ESR voltage is equal to the product of the capacitor current and the resistance. Before the transient, while there is no current flowing in the capacitor, the ESR voltage is zero. As the output capacitor begins to supply the transient current, the ESR voltage ramps down proportionally to the rise in load current. The voltage across the ESR remains at a steady value until the LDO begins to respond to the transient condition. After the LDO has responded to the transient, the entire load current is again supplied by the LDO, and the voltage drop across the ESR returns to zero. The resulting response is a negative pulse of voltage. The magnitude of the load transient and the amount of series resistance determine the magnitude of the ESR voltage pulse. The period of the voltage pulse is determined by the response time of the LDO and is significantly longer than the period of the ESL voltage spike. Because of the integrating nature of the LDO error amplifier, the LDO responds faster to larger dips in output voltage. Basically, a larger dip in output voltage generates a larger differential error voltage that causes the error amplifier to drive the pass element harder. Consequently, the LDO responds faster to larger voltage drops caused by larger ESR values. As a result, the period of the ESR-induced voltage droop decreases as the amount of ESR increases. From a transient point of view, it is desirable to minimize the amount of ESR. However, since the ESR and output capacitance form a dominant pole in the compensation of most LDOs, some finite amount of ESR is usually required to guarantee stability of the LDO.

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Figure 5. Equivalent capacitor model

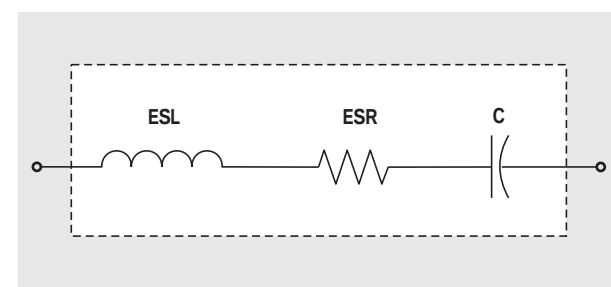


Figure 6. ESL load-transient response

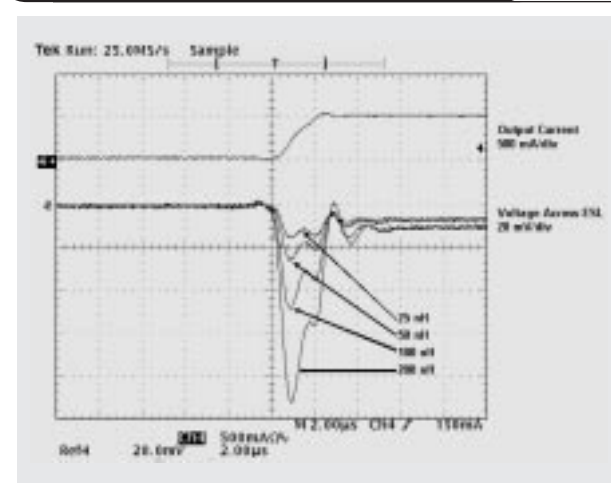
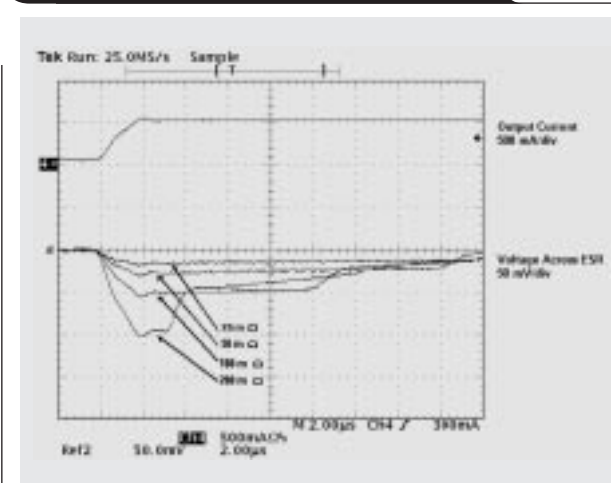


Figure 7. ESR load-transient response



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Bulk capacitance

The voltage across the actual output capacitance begins to decay as the capacitor supplies current to the transient load. The transient response of various amounts of output capacitance is shown in Figure 8. The rate of change of capacitor voltage is equal to the transient current divided by the capacitance. While the load is at its new value, the capacitor voltage decays at a constant rate until the LDO begins to respond. The larger voltage dip associated with a smaller capacitance value produces a larger error signal at the input of the error amplifier that causes the LDO to respond faster. Consequently, as the output capacitance is increased, the magnitude of the voltage dip decreases, while the period of the voltage dip increases. In order to minimize the output voltage dip, the amount of bulk capacitance must be increased.

The combined effect of the capacitance, ESL, and ESR is shown in Figure 9. In Figure 9, the capacitor consists of 200 μF of capacitance, 33 $\text{m}\Omega$ of ESR, and 100 nH of ESL. The actual response of a given capacitor will vary depending on the relative values of the ESR, ESL, and capacitance. The initial voltage spike during the rising slope of transient load will be less pronounced for capacitors with lower ESL values. Similarly, the voltage offset caused by the ESR will be smaller for smaller values of ESR, and the output voltage droop will be smaller for larger values of capacitance.

Capacitor technology

Although there are many types of capacitors, there are three that are most commonly used in LDO applications. These capacitor types include ceramic, aluminum electrolytic, and tantalum.

Ceramic capacitors offer a compact size, low cost, and very low ESR and ESL. Until recently, ceramics were limited to about 4.7 μF maximum. However, ceramics up to 22 μF recently have been introduced to the market. In situations where the low ESR of ceramics becomes a stability problem for the LDO, a low-value external resistor can be added in series with the capacitor.

Aluminum electrolytic capacitors are available in a wide range of capacitance values and case sizes. Because the loss of electrolyte over time limits the useful life of aluminum electrolytics, reliability can be a concern. The ESR of aluminum electrolytic capacitors is much higher than that of ceramic capacitors, but it decreases substantially as the voltage rating increases. In addition, aluminum electrolytic capacitors typically have more ESL than either ceramic or tantalum capacitors. However, the ESL of aluminum electrolytic capacitors usually is not large enough to cause concern. While the footprint areas of surface-mount electrolytics are comparable to ceramics, they tend to have taller profiles than their ceramic counterparts. However, since most LDO applications require a large amount of capacitance (more than 4.7 μF), aluminum electrolytics offer an attractive solution.

Tantalum capacitors offer a large capacitance in a compact size. The low ESR values of tantalums are well suited to LDO applications. The ESL of tantalum capacitors usually is higher than that of ceramic capacitors but less than that of aluminum electrolytic capacitors. As with aluminum electrolytic capacitors, the ESL usually is small enough not to cause concern in LDO applications. Most tantalum capacitors have an unsafe failure mode, which dictates that their operating voltage should be substantially less than their rated voltage (usually less than 50%.) Although tantalum capacitors are well suited to LDO applications, their popularity has skyrocketed in recent years, reducing availability and raising cost.

Design example

Consider a 3.3-V application that must be able to supply a load transient that transitions from no load to 1 A in 2 μs . Assume that the specifications do not allow the output voltage to drop below 3.0 V under any transient condition. First, an LDO must be selected that the designer feels can handle the output requirements. Given the high load rating and the transient requirements, a TPS75333 may be used, which provides 3.3 V at up to 1.5 A. From the TPS75333 data sheet, it can be seen that the minimum guaranteed output voltage is 3.234 V. Subtracting the 3.0-V output

Figure 8. Capacitance load-transient response

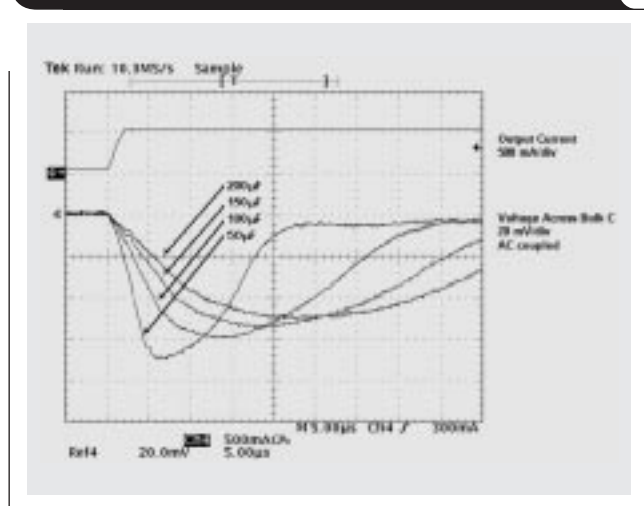
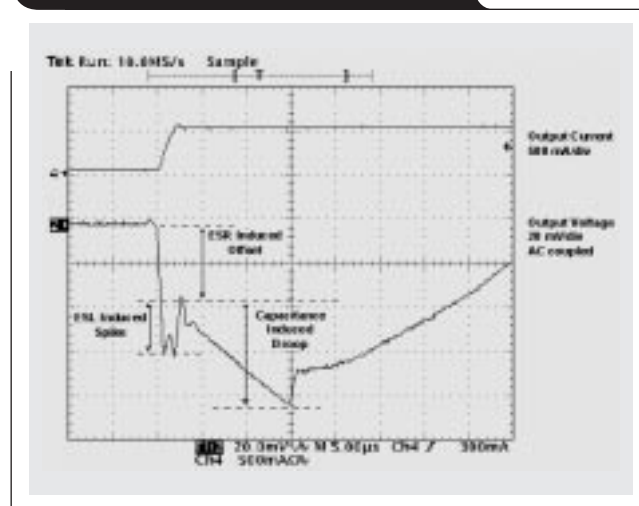


Figure 9. Total capacitor response



requirement from the minimum LDO voltage allows 234 mV for the transient.

Next, an output capacitor must be selected that, in conjunction with the TPS75333, will keep the output at an acceptable level. First, the ESL requirement must be checked. The maximum allowable ESL can be calculated as follows:

$$ESL_{\max} = V_{\text{dip}, \max} \times \frac{\Delta t_1}{\Delta I} = 234 \text{ mV} \times \frac{2 \mu\text{s}}{1 \text{ A}} = 466 \text{ nH}, \quad (1)$$

where $V_{\text{dip}, \max}$ is the maximum allowable voltage dip, Δt_1 is the current rise time, and ΔI is the stepped load change. In this example, as in most situations, the maximum allowable ESL is quite large and will not impact the capacitor selection.

Next, assume that the response time of the TPS75333 is going to be around 5 μs . Since LDO response times vary based on the ESR, capacitance, and the magnitude of the transient, this information typically is not published in the data sheets. Consequently, this assumption must be based on the evaluation or prior knowledge of the part. Having made this assumption, the voltage droop can be calculated for different capacitance values. The droop associated with the capacitance is given by

$$\Delta V_C = \frac{\Delta I \times \Delta t_2}{C} = \frac{1 \text{ A} \times 5 \mu\text{s}}{100 \mu\text{F}} = 50 \text{ mV}, \quad (2)$$

where C is the output capacitance and Δt_2 is the response time of the LDO. Assuming that 100 μF of output capacitance is needed, the associated voltage drop will be about 50 mV. Subtracting this 50 mV from the 234-mV allowable drop leaves 184 mV for the ESR voltage drop.

The maximum allowable ESR can now be calculated:

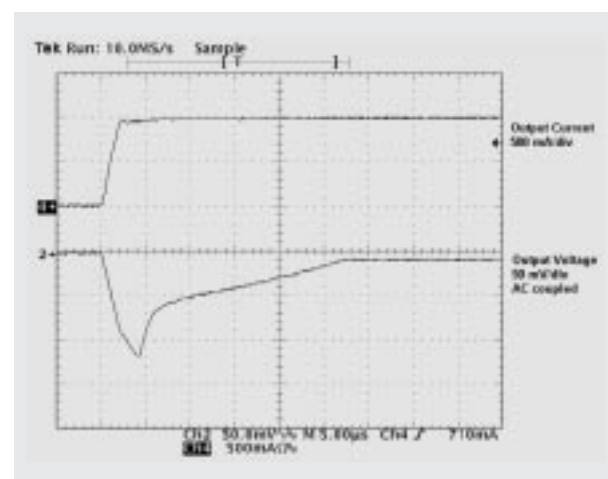
$$ESR_{\max} = \frac{\Delta V_{\text{ESR}, \max}}{\Delta I} = \frac{184 \text{ mV}}{1 \text{ A}} = 184 \text{ m}\Omega. \quad (3)$$

For the assumed 5- μs response time and 100- μF capacitance, the ESR should be less than 184 m Ω . There are numerous electrolytic and tantalum capacitors that meet this requirement. Selecting a 10-V, 100- μF tantalum with 55 m Ω of ESR should provide plenty of margin in meeting the specifications. The transient response for this example is shown in Figure 10. In fact, the output voltage droops about 120 mV, which is well within the specifications.

Summary

Selecting an LDO that is tailored to fast-transient loads is the first step in minimizing the effects of transients. Equally as important is the selection of the output capacitor. Understanding the load requirements and the behavior of the LDO and output capacitor can provide confidence in the design of a power distribution strategy. With this understanding, the designer can optimize a design for performance, board area, and cost.

Figure 10. Design example transient response



References

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Document Title

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Related Web sites

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