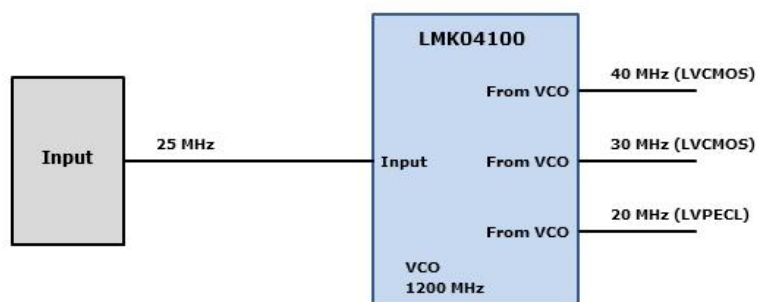


WEBENCH[®] Clock Architect

Project Report

Project: 4392296/2 Project 2 - [LMK04100]

Created: 6/7/15 8:12:16 PM



Block Diagram

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	20	Any	1
fixed1	30	Any	1
fixed2	40	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	Yes

Properties

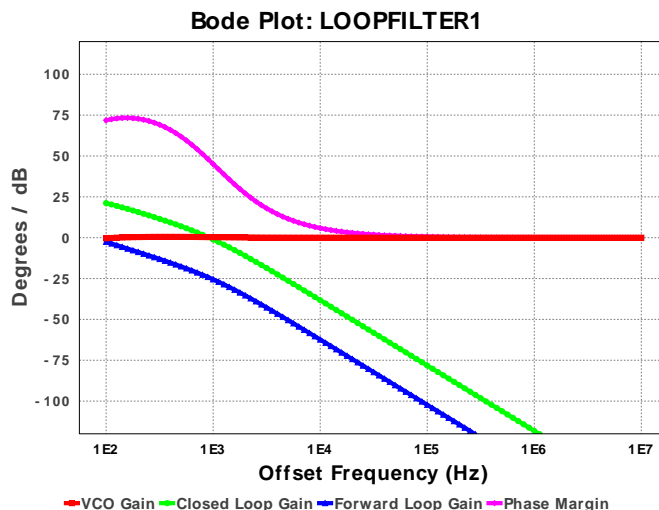
Name	Design Value
External Sources	none
Total BOM Cost	\$6.0
Total Current	218.5 mA
Total Footprint	49.0 mm ²



User ID = 4392296
 Design Id = 6
 Device = LMK04100
 Created = 6/7/15 8:12:16 PM

WEBENCH® Clock Design Report

Loop Filter: LOOPFILTER1



Preferences

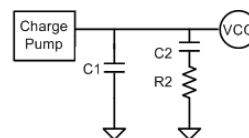
Name	Design Value
Filter Type	Passive
Filter Order	2nd Order
Op Amp Gain	1.00
Charge Pump Gain	0.08 mA
VCO Gain	0.002 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	80.00 MHz
Phase Det. Frequency	5.00 MHz

Parameters

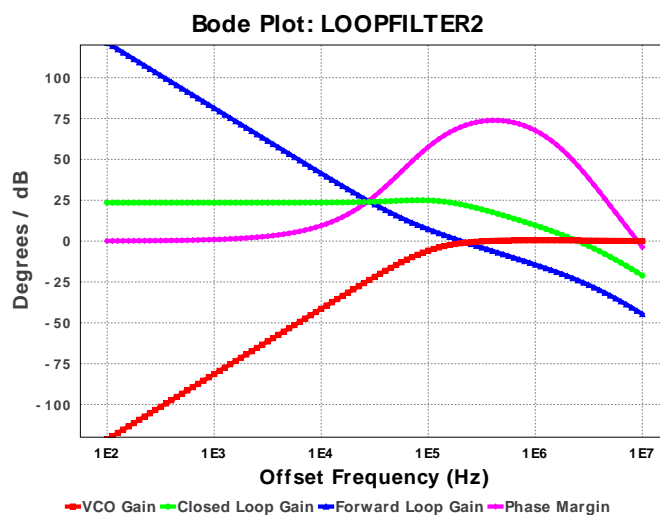
Name	Design Value	Forced	Actual Value
Loop Bandwidth	0.075 kHz	N	0.076 kHz
Phase Margin	70.00 deg	N	69.333 deg
T3/T1Ratio	0.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	0.245

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	3.30 nF	N	N
C2	150.00 nF	N	N
3. C3	Open	N	N
4. C4	Open	N	N
R2	47.00 kohms	N	N



Loop Filter: LOOPFILTER2



Preferences

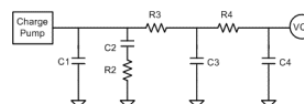
Name	Design Value
Filter Type	Passive
Filter Order	4th Order
Op Amp Gain	1.00
Charge Pump Gain	3.20 mA
VCO Gain	8.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	1200.00 MHz
Phase Det. Frequency	80.00 MHz

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	201.451 kHz	N	206.493 kHz
Phase Margin	70.00 deg	N	70.097 deg
T3/T1Ratio	50.00 %	N	13.406 %
T4/T3Ratio	50.00 %	N	0.00 %
Gamma	0.24	N	0.246

Loop Filter Components

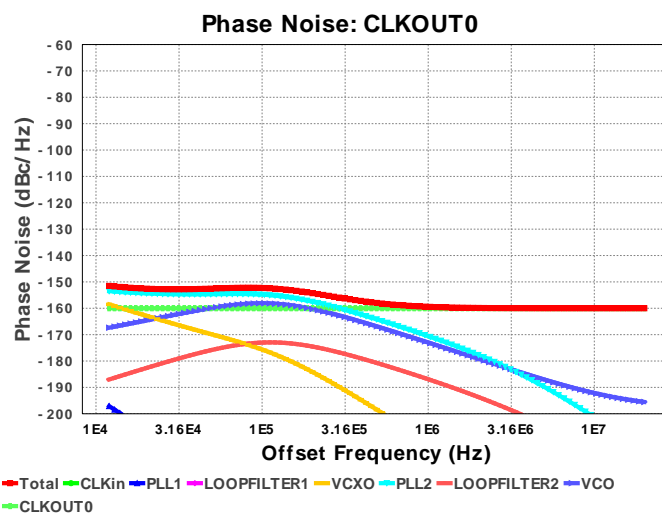
Name	Target Value	Fixed	Forced
C1	0.047 nF	N	N
C2	3.30 nF	N	N
3. C3	Open	Y	N
C4	0.01 nF	Y	N
R2	0.82 kohms	N	N
R3	0.60 kohms	Y	N
R4	0.20 kohms	Y	N



Output Block: CLKOUT0 as LVPECL output, 20.0 MHz

Integrated Noise Info

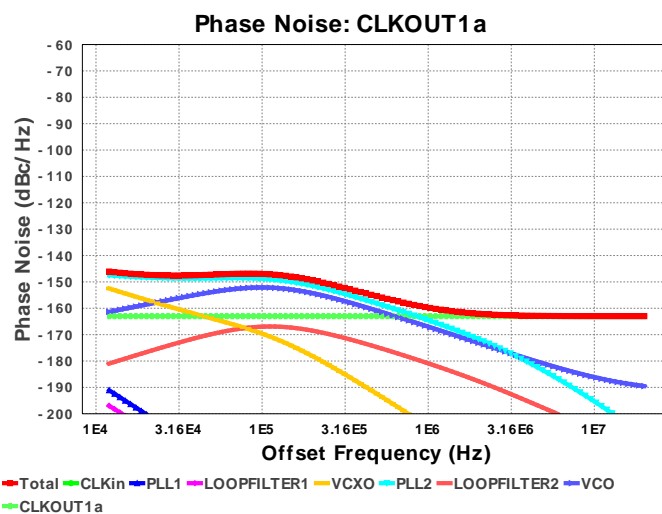
Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-159.698 dBc/Hz
RMS Jitter	520.965 fs
RMS Phase Error (deg)	0.004 deg
RMS Phase Error	0.065 mrad
EVM	0.007%
SNR	83.68 dB
Spur	-86.68 dBc
Jitter (Pk-Pk)	3714.742 fs
Jitter (Cycle to Cycle Pk)	7429.483 fs
Jitter (Cycle to Cycle RMS)	736.756 fs
A/D ENOB	13.615 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00



Output Block: CLKOUT1a as LVCMOS output, 40.0 MHz

Integrated Noise Info

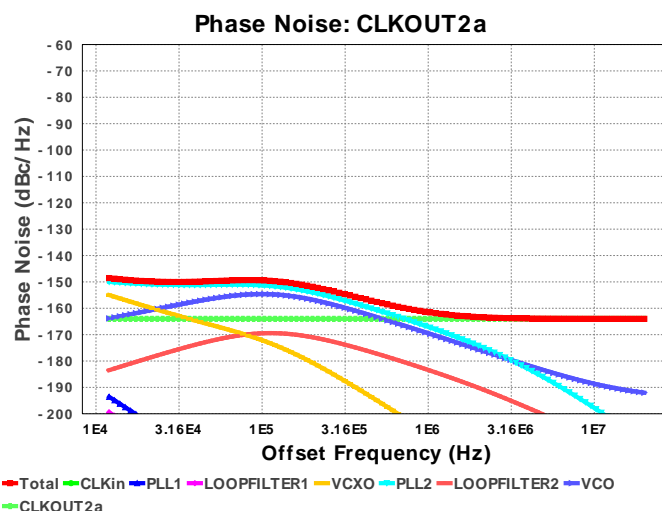
Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-161.026 dBc/Hz
RMS Jitter	223.547 fs
RMS Phase Error (deg)	0.003 deg
RMS Phase Error	0.056 mrad
EVM	0.006%
SNR	85.008 dB
Spur	-88.008 dBc
Jitter (Pk-Pk)	1593.998 fs
Jitter (Cycle to Cycle Pk)	3187.995 fs
Jitter (Cycle to Cycle RMS)	316.143 fs
A/D ENOB	13.835 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00



Output Block: CLKOUT2a as LVCMOS output, 30.0 MHz

Integrated Noise Info

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-162.515 dBc/Hz
RMS Jitter	251.089 fs
RMS Phase Error (deg)	0.003 deg
RMS Phase Error	0.047 mrad
EVM	0.005%
SNR	86.497 dB
Spur	-89.497 dBc
Jitter (Pk-Pk)	1790.389 fs
Jitter (Cycle to Cycle Pk)	3580.778 fs
Jitter (Cycle to Cycle RMS)	355.094 fs
A/D ENOB	14.083 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00



Texas Instruments' WEBENCH simulation tools attempt to recreate the performance of a substantially equivalent physical implementation of the design. Simulations are created using Texas Instruments' published specifications as well as the published specifications of other device manufacturers. While Texas Instruments does update this information periodically, this information may not be current at the time the simulation is built. Texas Instruments does not warrant the accuracy or completeness of the specifications or any information contained therein. Texas Instruments does not warrant that any designs or recommended parts will meet the specifications you entered, will be suitable for your application or fit for any particular purpose, or will operate as shown in the simulation in a physical implementation. Texas Instruments does not warrant that the designs are production worthy.

You should completely validate and test your design implementation to confirm the system functionality for your application prior to production.

Use of Texas Instruments' WEBENCH simulation tools is subject to [Texas Instruments' Site Terms and Conditions of Use](#). Prototype boards based on WEBENCH created designs are provided AS IS without warranty of any kind for evaluation and testing purposes and are subject to the terms of the [Evaluation License Agreement](#).