

# WEBENCH<sup>®</sup> Clock Architect

## Project Report

Project: 4211465/6 Project 6 - [LMK04906B]

Created: 6/7/15 8:16:54 PM

Block Diagram

## System Specification and Parameters

### Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	50	Any	1
fixed1	75	Any	1
fixed2	100	Any	1

### Options

Name	Design Value
Automatically Select Input Frequencies	No

### Properties

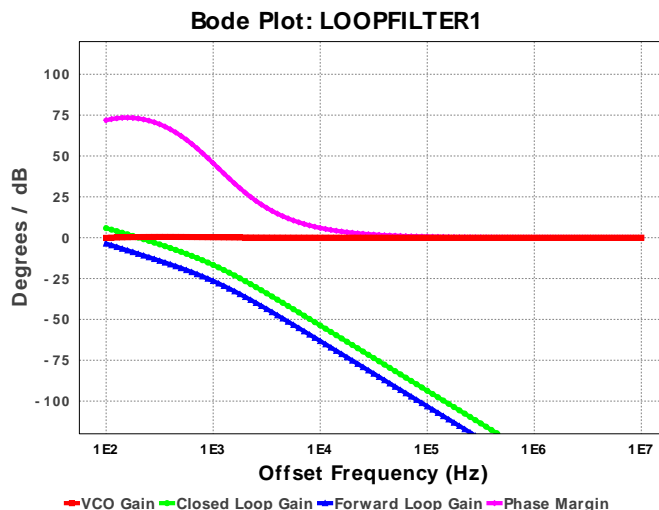
Name	Design Value
External Sources	none
Total BOM Cost	\$6.49
Total Current	262.0 mA
Total Footprint	81.0 mm <sup>2</sup>



User ID = 4211465  
 Design Id = 35  
 Device = LMK04906B  
 Created = 6/7/15 8:16:54 PM

## WEBENCH® Clock Design Report

Loop Filter: LOOPFILTER1



### Preferences

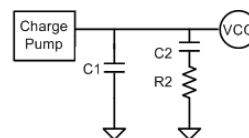
Name	Design Value
Filter Type	Passive
Filter Order	2nd Order
Op Amp Gain	1.00
Charge Pump Gain	1.60 mA
VCO Gain	0.002 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	75.00 MHz
Phase Det. Frequency	25.00 MHz

### Parameters

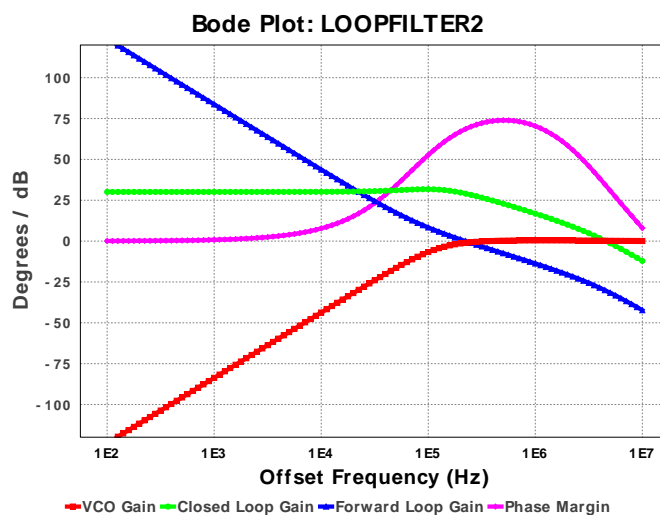
Name	Design Value	Forced	Actual Value
Loop Bandwidth	0.075 kHz	N	0.068 kHz
Phase Margin	70.00 deg	N	67.953 deg
T3/T1Ratio	0.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	0.192

### Loop Filter Components

Name	Target Value	Fixed	Forced
C1	390.00 nF	N	N
C2	18000.00 nF	N	N
3. C3	Open	N	N
4. C4	Open	N	N
R2	0.39 kohms	N	N



## Loop Filter: LOOPFILTER2



## Preferences

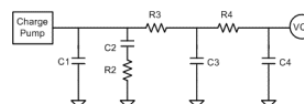
Name	Design Value
Filter Type	Passive
Filter Order	4th Order
Op Amp Gain	1.00
Charge Pump Gain	3.20 mA
VCO Gain	18.25 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	2400.00 MHz
Phase Det. Frequency	75.00 MHz

## Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	228.019 kHz	N	222.877 kHz
Phase Margin	70.00 deg	N	68.609 deg
T3/T1Ratio	50.00 %	N	7.394 %
T4/T3Ratio	50.00 %	N	24.608 %
Gamma	0.24	N	0.19

## Loop Filter Components

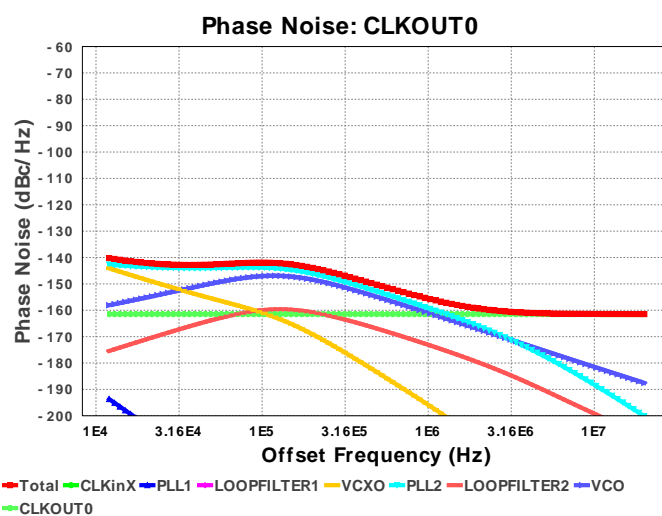
Name	Target Value	Fixed	Forced
C1	0.027 nF	N	N
C2	2.70 nF	N	N
C3	0.01 nF	Y	N
C4	0.01 nF	Y	N
R2	0.82 kohms	N	N
R3	0.20 kohms	Y	N
R4	0.20 kohms	Y	N



## Output Block: CLKOUT0 as LVCMOS output, 100.0 MHz

## Integrated Noise Info

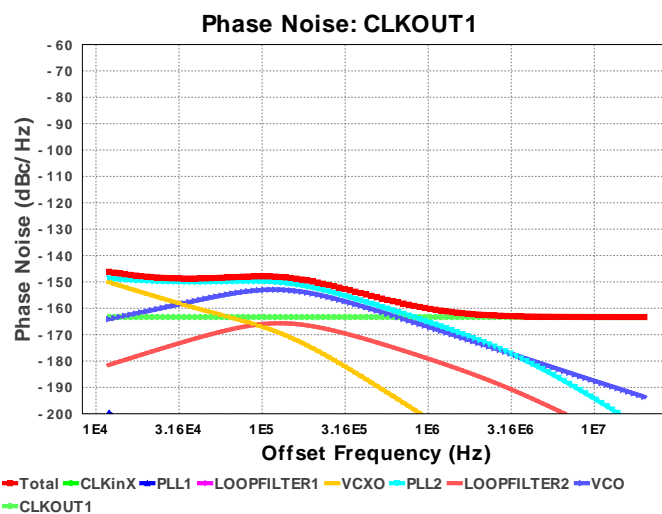
Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-157.668 dBc/Hz
RMS Jitter	131.62 fs
RMS Phase Error (deg)	0.005 deg
RMS Phase Error	0.083 mrad
EVM	0.008%
SNR	81.65 dB
Spur	-84.65 dBc
Jitter (Pk-Pk)	938.514 fs
Jitter (Cycle to Cycle Pk)	1877.027 fs
Jitter (Cycle to Cycle RMS)	186.138 fs
A/D ENOB	13.277 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00



## Output Block: CLKOUT1 as LVCMOS output, 50.0 MHz

## Integrated Noise Info

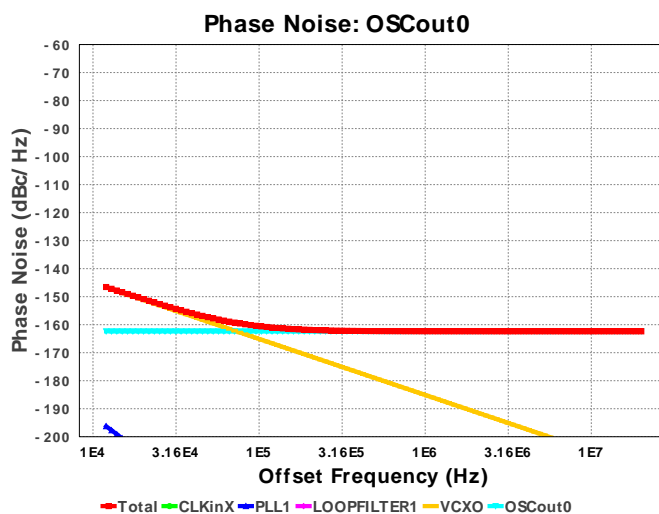
Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-161.465 dBc/Hz
RMS Jitter	170.025 fs
RMS Phase Error (deg)	0.003 deg
RMS Phase Error	0.053 mrad
EVM	0.005%
SNR	85.447 dB
Spur	-88.447 dBc
Jitter (Pk-Pk)	1212.363 fs
Jitter (Cycle to Cycle Pk)	2424.726 fs
Jitter (Cycle to Cycle RMS)	240.452 fs
A/D ENOB	13.908 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00



## Output Block: OSCout0 as LVCMOS output, 75.0 MHz

## Integrated Noise Info

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-162.291 dBc/Hz
RMS Jitter	103.061 fs
RMS Phase Error (deg)	0.003 deg
RMS Phase Error	0.049 mrad
EVM	0.005%
SNR	86.273 dB
Spur	-89.273 dBc
Jitter (Pk-Pk)	734.879 fs
Jitter (Cycle to Cycle Pk)	1469.759 fs
Jitter (Cycle to Cycle RMS)	145.751 fs
A/D ENOB	14.045 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00



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