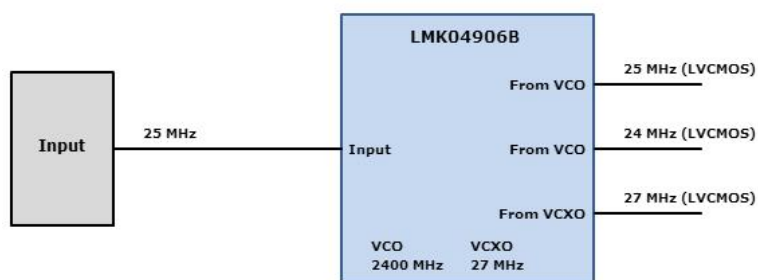


WEBENCH[®] Clock Architect

Project Report

Project: 4393327/3 Project 3 - [LMK04906B]

Created: 6/8/15 9:33:39 PM



Block Diagram

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	24	Any	1
fixed1	27	Any	1
fixed2	25	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	Yes

Properties

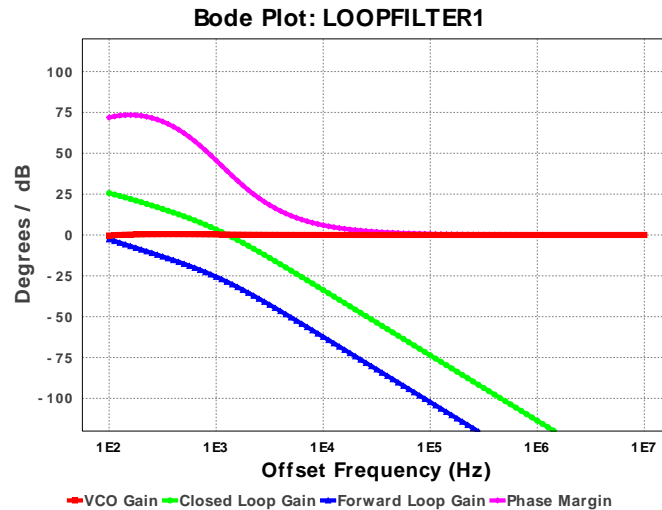
Name	Design Value
External Sources	none
Total BOM Cost	\$6.49
Total Current	262.0 mA
Total Footprint	81.0 mm ²



User ID = 4393327
 Design Id = 11
 Device = LMK04906B
 Created = 6/8/15 9:33:39 PM

WEBENCH® Clock Design Report

Loop Filter: LOOPFILTER1



Preferences

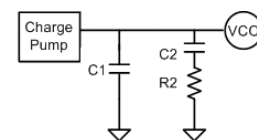
Name	Design Value
Filter Type	Passive
Filter Order	2nd Order
Op Amp Gain	1.00
Charge Pump Gain	1.60 mA
VCO Gain	0.002 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	27.00 MHz
Phase Det. Frequency	1.00 MHz

Parameters

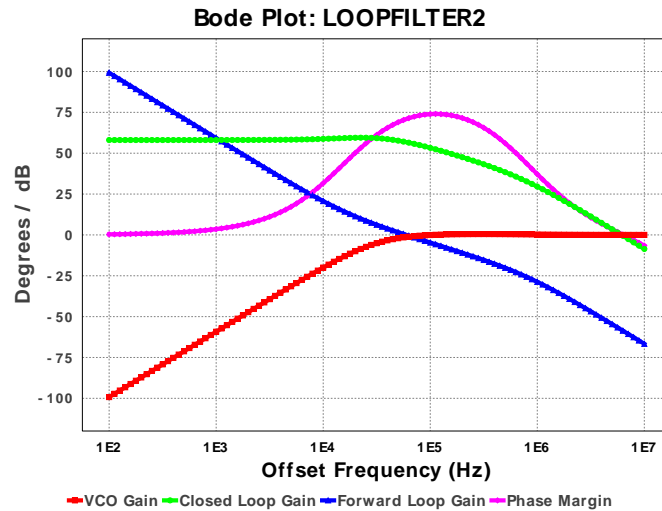
Name	Design Value	Forced	Actual Value
Loop Bandwidth	0.075 kHz	N	0.075 kHz
Phase Margin	70.00 deg	N	69.173 deg
T3/T1Ratio	0.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	0.232

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	39.00 nF	N	N
C2	1800.00 nF	N	N
3. C3	Open	N	N
4. C4	Open	N	N
R2	3.90 kohms	N	N



Loop Filter: LOOPFILTER2



Preferences

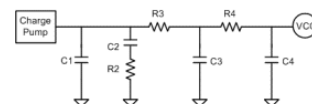
Name	Design Value
Filter Type	Passive
Filter Order	4th Order
Op Amp Gain	1.00
Charge Pump Gain	3.20 mA
VCO Gain	18.25 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	2400.00 MHz
Phase Det. Frequency	3.00 MHz

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	58.364 kHz	N	59.748 kHz
Phase Margin	70.00 deg	N	70.942 deg
T3/T1Ratio	50.00 %	N	1.234 %
T4/T3Ratio	50.00 %	N	29.161 %
Gamma	0.24	N	0.282

Loop Filter Components

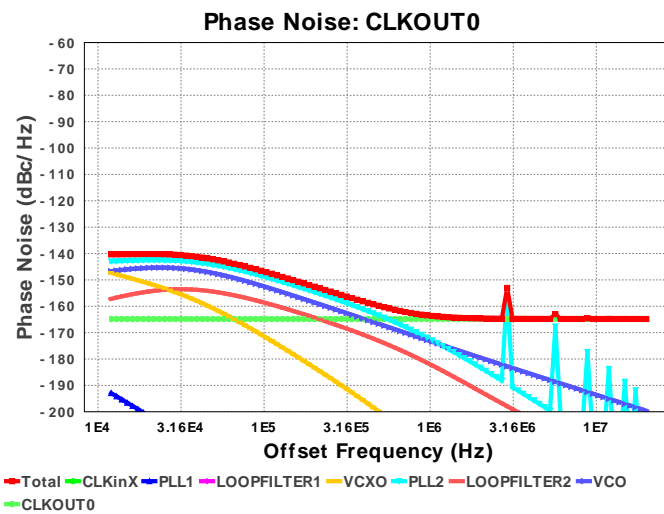
Name	Target Value	Fixed	Forced
C1	0.015 nF	N	N
C2	1.80 nF	N	N
C3	0.01 nF	Y	N
C4	0.01 nF	Y	N
R2	5.60 kohms	N	N
R3	0.20 kohms	Y	N
R4	0.20 kohms	Y	N



Output Block: CLKOUT0 as LVCMOS output, 25.0 MHz

Integrated Noise Info

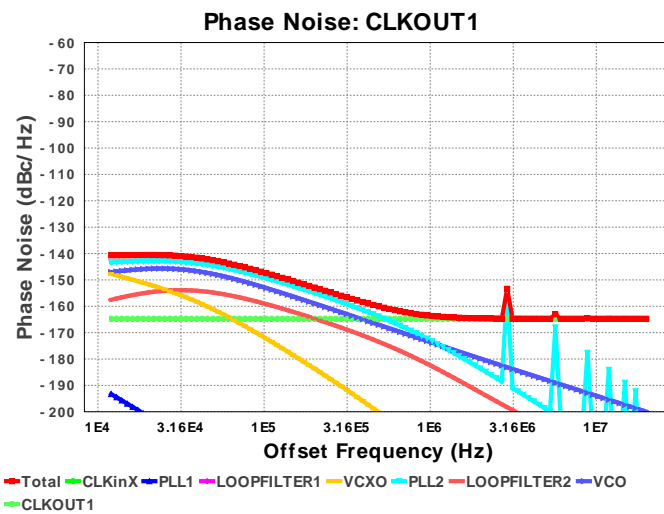
Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-161.407 dBc/Hz
RMS Jitter	342.31 fs
RMS Phase Error (deg)	0.003 deg
RMS Phase Error	0.054 mrad
EVM	0.005%
SNR	85.389 dB
Spur	-88.389 dBc
Jitter (Pk-Pk)	2440.842 fs
Jitter (Cycle to Cycle Pk)	4881.684 fs
Jitter (Cycle to Cycle RMS)	484.10 fs
A/D ENOB	13.899 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00



Output Block: CLKOUT1 as LVCMOS output, 24.0 MHz

Integrated Noise Info

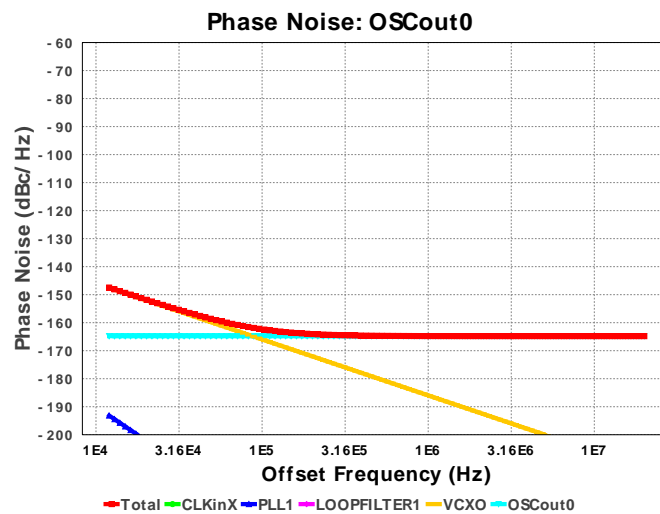
Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-161.561 dBc/Hz
RMS Jitter	350.317 fs
RMS Phase Error (deg)	0.003 deg
RMS Phase Error	0.053 mrad
EVM	0.005%
SNR	85.543 dB
Spur	-88.543 dBc
Jitter (Pk-Pk)	2497.936 fs
Jitter (Cycle to Cycle Pk)	4995.872 fs
Jitter (Cycle to Cycle RMS)	495.424 fs
A/D ENOB	13.924 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00



Output Block: OSCout0 as LVCMOS output, 27.0 MHz

Integrated Noise Info

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-164.677 dBc/Hz
RMS Jitter	217.519 fs
RMS Phase Error (deg)	0.002 deg
RMS Phase Error	0.037 mrad
EVM	0.004%
SNR	88.659 dB
Spur	-91.659 dBc
Jitter (Pk-Pk)	1551.02 fs
Jitter (Cycle to Cycle Pk)	3102.041 fs
Jitter (Cycle to Cycle RMS)	307.619 fs
A/D ENOB	14.442 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00



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