WEBENCH® Clock Architect

Project Report

Project: 4264827/1 Project 1 - [LMK03806B]
Created: 6/9/15 6:06:37 AM

Block Diagram

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	24	Any	1
fixed1	50	Any	1
fixed2	60	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	Yes

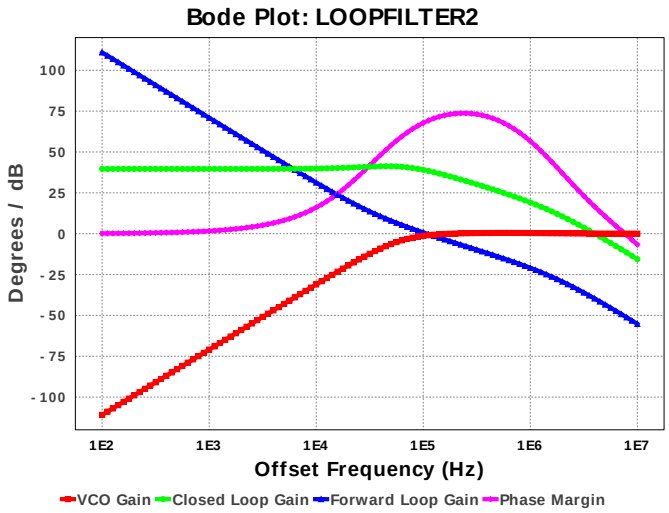
Properties

Name	Design Value
External Sources	none
Total BOM Cost	$7.95
Total Current	209.5 mA
Total Footprint	81.0 mm^2

User ID = 4264827
Design Id = 9
Device = LMK03806B
Created = 6/9/15 6:06:37 AM

WEBENCH® Clock Design Report

Loop Filter: LOOPFILTER2



Preferences

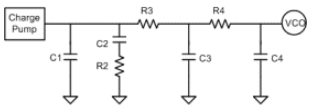
Name	Design Value
Filter Type	Passive
Filter Order	4th Order
Op Amp Gain	1.00
Charge Pump Gain	3.20 mA
VCO Gain	18.25 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	2400.00 MHz
Phase Det. Frequency	25.00 MHz

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	108.432 kHz	N	108.206 kHz
Phase Margin	70.00 deg	N	68.84 deg
T3/T1Ratio	50.00 %	N	4.27 %
T4/T3Ratio	50.00 %	N	19.31 %
Gamma	0.24	N	0.206

Loop Filter Components

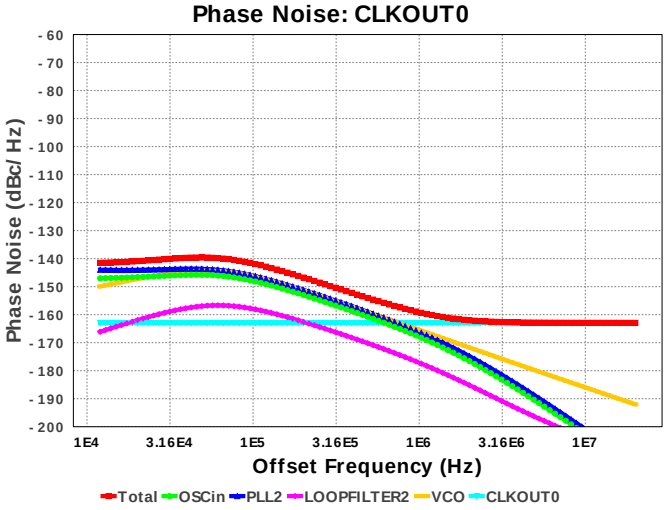
Name	Target Value	Fixed	Forced
C1	0.056 nF	N	N
C2	3.90 nF	N	N
C3	0.01 nF	Y	N
C4	0.01 nF	Y	N
R2	1.20 kohms	N	N
R3	0.20 kohms	Y	N
R4	0.20 kohms	Y	N



Output Block: CLKOUT0 as LVCMOS output, 60.0 MHz

Integrated Noise Info

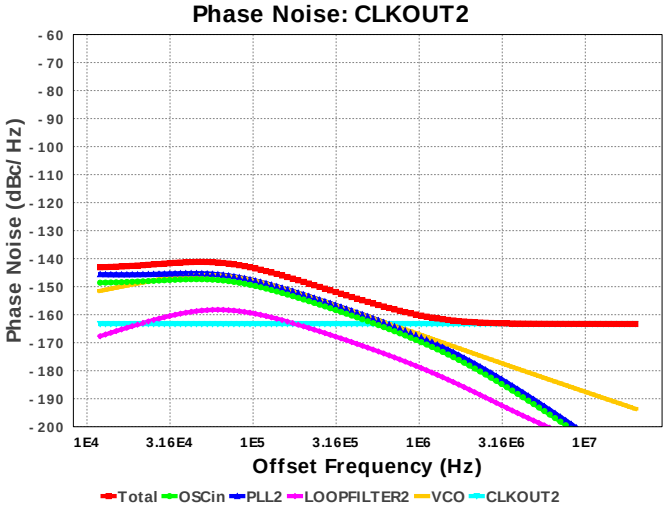
Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-158.881 dBc/Hz
RMS Jitter	190.779 fs
RMS Phase Error (deg)	0.004 deg
RMS Phase Error	0.072 mrad
EVM	0.007%
SNR	82.863 dB
Spur	-85.863 dBc
Jitter (Pk-Pk)	1360.352 fs
Jitter (Cycle to Cycle Pk)	2720.704 fs
Jitter (Cycle to Cycle RMS)	269.803 fs
A/D ENOB	13.479 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00



Output Block: CLKOUT2 as LVCMOS output, 50.0 MHz

Integrated Noise Info

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-159.95 dBc/Hz
RMS Jitter	202.417 fs
RMS Phase Error (deg)	0.004 deg
RMS Phase Error	0.064 mrad
EVM	0.006%
SNR	83.932 dB
Spur	-86.932 dBc
Jitter (Pk-Pk)	1443.335 fs
Jitter (Cycle to Cycle Pk)	2886.669 fs
Jitter (Cycle to Cycle RMS)	286.261 fs
A/D ENOB	13.656 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00



Output Block: CLKOUT4 as LVCMOS output, 24.0 MHz

Integrated Noise Info

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-163.364 dBc/Hz
RMS Jitter	284.645 fs
RMS Phase Error (deg)	0.002 deg
RMS Phase Error	0.043 mrad
EVM	0.004%
SNR	87.346 dB
Spur	-90.346 dBc
Jitter (Pk-Pk)	2029.662 fs
Jitter (Cycle to Cycle Pk)	4059.323 fs
Jitter (Cycle to Cycle RMS)	402.549 fs
A/D ENOB	14.224 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00