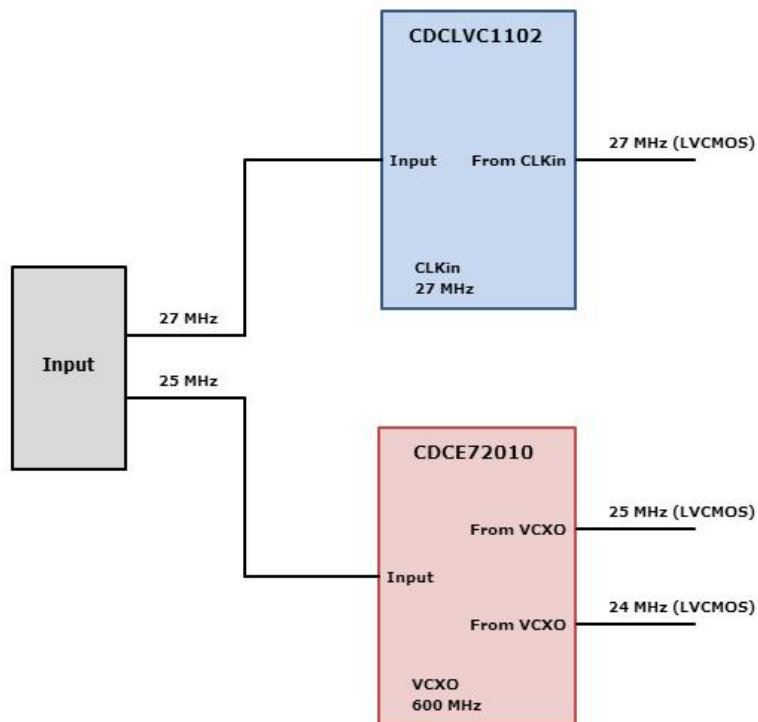


WEBENCH[®] Clock Architect

Project Report

Project: 4387412/2 Project 2 - [CDCLVC1102, CDCE72010]
 Created: 6/9/15 6:26:29 PM



Block Diagram

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	24	Any	1
fixed1	27	Any	1
fixed2	25	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	Yes

Properties

Name	Design Value
External Sources	none

Name	Design Value
Total BOM Cost	\$11.35
Total Current	294.0 mA
Total Footprint	101.0 mm ²



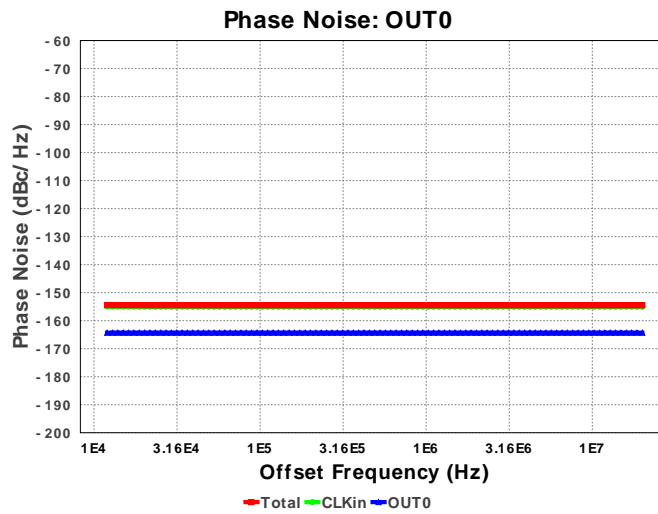
User ID = 4387412
Design Id = 8
Device = CDCLVC1102
Created = 6/9/15 6:26:29 PM

WEBENCH® Clock Design Report

Output Block: OUT0 as LVCMOS output, 27.0 MHz

Integrated Noise Info

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-154.518 dBc/Hz
RMS Jitter	700.615 fs
RMS Phase Error (deg)	0.007 deg
RMS Phase Error	0.119 mrad
EVM	0.012%
SNR	78.50 dB
Spur	-81.50 dBc
Jitter (Pk-Pk)	4995.732 fs
Jitter (Cycle to Cycle Pk)	9991.463 fs
Jitter (Cycle to Cycle RMS)	990.819 fs
A/D ENOB	12.754 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00





User ID = 4387412
Design Id = 9
Device = CDCE72010
Created = 6/9/15 6:26:29 PM

WEBENCH® Clock Design Report

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