



# WEBENCH<sup>®</sup> Clock Architect

## Project Report

Project: 4398736/1 Project 1 - [CDCLVC1103, LMX2571, LMK04100]  
Created: 6/15/15 5:56:45 AM

Block Diagram

## System Specification and Parameters

### Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	24	Any	1
fixed1	27	Any	1
fixed2	25	Any	1
fixed_2	150	Any	1

### Options

Name	Design Value
Automatically Select Input Frequencies	No

### Properties

Name	Design Value
External Sources	none
Total BOM Cost	\$11.55
Total Current	205.75 mA
Total Footprint	105.0 mm <sup>2</sup>



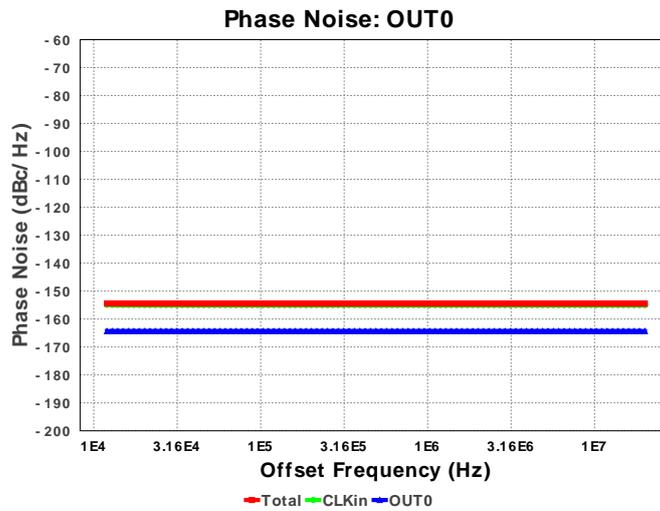
User ID = 4398736  
Design Id = 4  
Device = CDCLVC1103  
Created = 6/15/15 5:56:45 AM

## WEBENCH® Clock Design Report

## Output Block: OUT0 as LVCMOS output, 25.0 MHz

## Integrated Noise Info

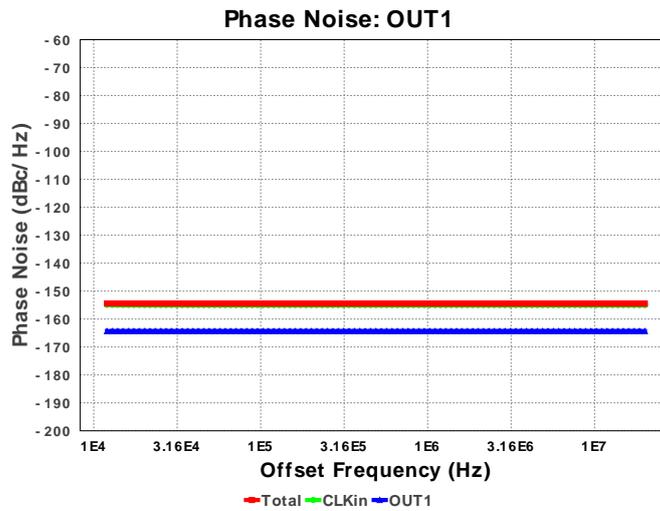
Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-154.518 dBc/Hz
RMS Jitter	756.664 fs
RMS Phase Error (deg)	0.007 deg
RMS Phase Error	0.119 mrad
EVM	0.012%
SNR	78.50 dB
Spur	-81.50 dBc
Jitter (Pk-Pk)	5395.39 fs
Jitter (Cycle to Cycle Pk)	10790.78 fs
Jitter (Cycle to Cycle RMS)	1070.085 fs
A/D ENOB	12.754 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00



## Output Block: OUT1 as LVCMOS output, 25.0 MHz

## Integrated Noise Info

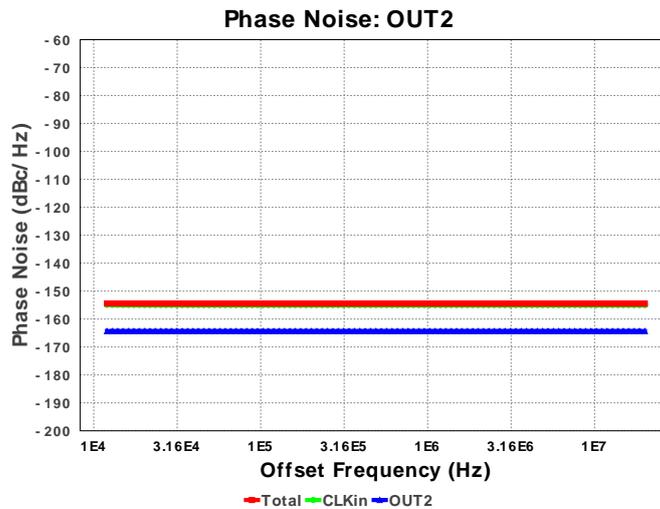
Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-154.518 dBc/Hz
RMS Jitter	756.664 fs
RMS Phase Error (deg)	0.007 deg
RMS Phase Error	0.119 mrad
EVM	0.012%
SNR	78.50 dB
Spur	-81.50 dBc
Jitter (Pk-Pk)	5395.39 fs
Jitter (Cycle to Cycle Pk)	10790.78 fs
Jitter (Cycle to Cycle RMS)	1070.085 fs
A/D ENOB	12.754 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00



## Output Block: OUT2 as LVCMOS output, 25.0 MHz

## Integrated Noise Info

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-154.518 dBc/Hz
RMS Jitter	756.664 fs
RMS Phase Error (deg)	0.007 deg
RMS Phase Error	0.119 mrad
EVM	0.012%
SNR	78.50 dB
Spur	-81.50 dBc
Jitter (Pk-Pk)	5395.39 fs
Jitter (Cycle to Cycle Pk)	10790.78 fs
Jitter (Cycle to Cycle RMS)	1070.085 fs
A/D ENOB	12.754 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00





User ID = 4398736  
Design Id = 5  
Device = LMX2571  
Created = 6/15/15 5:56:45 AM

## WEBENCH® Clock Design Report



User ID = 4398736  
Design Id = 6  
Device = LMK04100  
Created = 6/15/15 5:56:45 AM

## WEBENCH® Clock Design Report

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**You should completely validate and test your design implementation to confirm the system functionality for your application prior to production.**

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