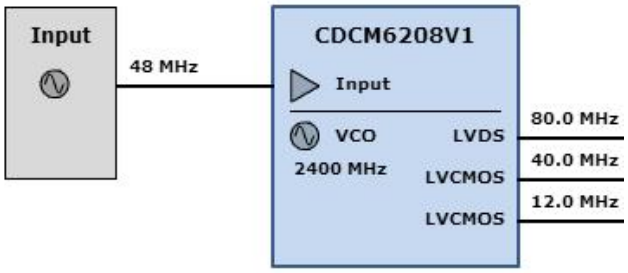
WEBENCH® Clock Architect

Project Report

Project: 4368542/2 Project 2 - [CDCM6208V1]
Created: 7/30/15 6:40:30 PM



Block Diagram

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	80	Any	1
fixed1	40	Any	1
fixed2	12	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	No

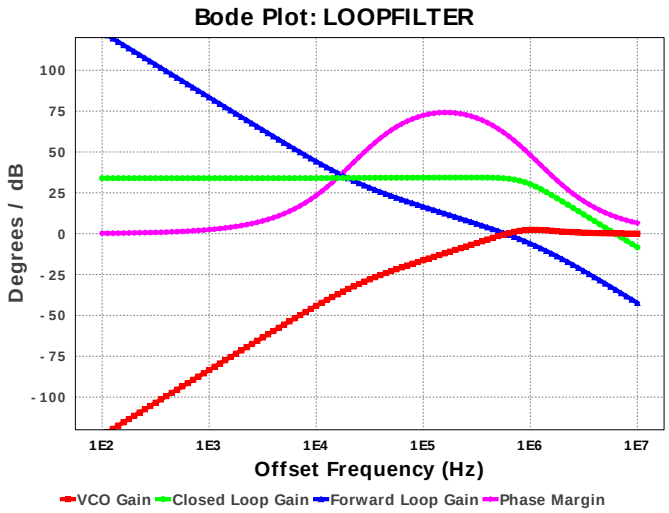
Properties

Name	Design Value
External Sources	none
Total BOM Cost	$5.2
Total Current	132.5 mA
Total Footprint	49.0 mm^2

User ID = 4368542
Design Id = 10
Device = CDCM6208V1
Created = 7/30/15 6:40:30 PM

WEBENCH® Clock Design Report

Loop Filter: CDCM6208V1 LOOPFILTER



Preferences

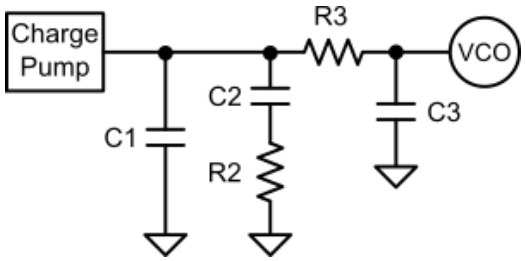
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	2.50 mA
VCO Gain	185.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	2400.00 MHz
Phase Det. Frequency	48.00 MHz

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	542.733 kHz	N	587.929 kHz
Phase Margin	65.00 deg	N	61.122 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	9.50	N	13.086

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	Open	N	N
C2	15.00 nF	N	N
C3	0.242 nF	Y	N
C4	Open	Y	N
R2	0.47 kohms	N	N
R3	0.10 kohms	Y	N



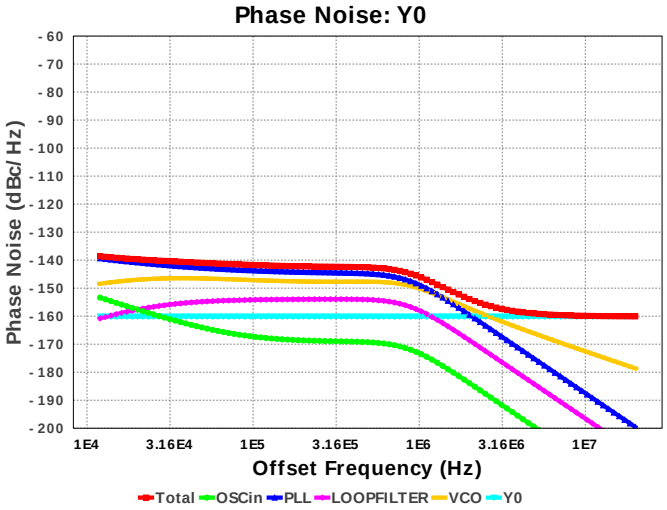
Output Block: CDCM6208V1 Y0 as LVDS output, 80.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-153.784 dBc/Hz
RMS Jitter	257.29 fs
RMS Phase Error (deg)	0.007 deg
RMS Phase Error	0.129 mrad
EVM	0.013%
SNR	77.766 dB
Spur	-80.766 dBc
Jitter (Pk-Pk)	1834.606 fs
Jitter (Cycle to Cycle Pk)	3669.213 fs
Jitter (Cycle to Cycle RMS)	363.863 fs
A/D ENOB	12.632 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	Y0
12 kHz	-138.63	-153.37	-139.35	-160.76	-148.4	-160.12
100 kHz	-141.72	-167.28	-143.67	-154.17	-147.12	-160.12
20000 kHz	-160.06	-223.88	-199.56	-208.61	-178.63	-160.12



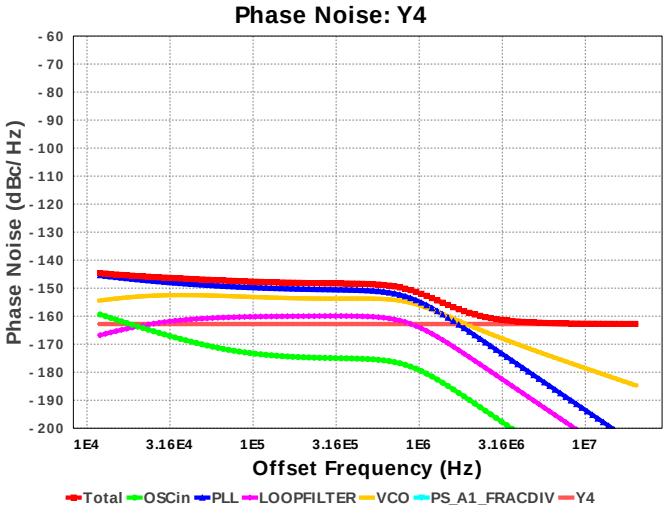
Output Block: CDCM6208V1 Y4 as LVCMOS output, 40.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-158.769 dBc/Hz
RMS Jitter	289.889 fs
RMS Phase Error (deg)	0.004 deg
RMS Phase Error	0.073 mrad
EVM	0.007%
SNR	82.751 dB
Spur	-85.751 dBc
Jitter (Pk-Pk)	2067.052 fs
Jitter (Cycle to Cycle Pk)	4134.105 fs
Jitter (Cycle to Cycle RMS)	409.965 fs
A/D ENOB	13.46 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	PS_A1_FRACDIV	Y4
12 kHz	-144.62	-159.39	-145.37	-166.78	-154.42	-1000	-162.8
100 kHz	-147.67	-173.3	-149.69	-160.19	-153.14	-1000	-162.8
20000 kHz	-162.77	-229.9	-205.58	-214.63	-184.65	-1000	-162.8



Output Block: CDCM6208V1 Y5 as LVCMOS output, 12.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-162.24 dBc/Hz
RMS Jitter	647.97 fs
RMS Phase Error (deg)	0.003 deg
RMS Phase Error	0.049 mrad
EVM	0.005%
SNR	86.222 dB
Spur	-89.222 dBc
Jitter (Pk-Pk)	4620.345 fs
Jitter (Cycle to Cycle Pk)	9240.691 fs
Jitter (Cycle to Cycle RMS)	916.368 fs
A/D ENOB	14.037 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	PS_A2_FRACDIV	Y5
12 kHz	-154.45	-169.85	-155.83	-177.24	-164.87	-1000	-162.8
100 kHz	-156.95	-183.76	-160.15	-170.65	-163.6	-1000	-162.8
20000 kHz	-162.8	-240.36	-216.04	-225.08	-195.11	-1000	-162.8