TEXAS INSTRUMENTS

bq80201A

Cool-GG Programmable Battery Management IC

Data Manual

May 2005 ***PMP - Portable Power***

SLVS498A

Contents

List of Figures

List of Tables

1 Introduction

1.1 Features

- **Powerful Low-Power 8-Bit RISC CPU Core**
- **Operating at Up to 4-MHz Clock Frequency**
- **Flexible Memory Architecture**
  - **16k x 22 Program Flash EPROM**
  - **4k x 22 Program Mask ROM**
  - **1k x 8 Data Flash EPROM**
  - **756 x 8 Data RAM**
- **Three Reduced Power Modes (Typical battery pack operating range conditions)**
  - **Low Power: < 300 μA**
  - **Sleep: < 8 μA**
  - **Hibernate: < 1.4 μA**
- **High-Accuracy Analog Front End With Two Independent ADCs**
  - **High-Resolution Integrator for Coulomb Counting—Better Than 3nVh Resolution**
  - **Coulomb Counter Self-Calibration Reduces Offset to Less Than 1 μV**
  - **15-Bit Delta-Sigma ADC With a 12-Channel Multiplexer for Voltage, Current, and Temperature Measurements**
- **Clock Source From Either an Accurate Internal Oscillator or External Crystal**
- **Internal Clock Synthesizer Generates Frequencies up to 4 MHz From a Single Crystal Input—Reduces Component Count**
- **Integrated Flash Memory Eliminates Need for External EEPROM**
- **24 Memory-Mapped I/O Pins**
- **Supports Two Serial Communication Protocols**
  - **Two-Wire SMBus v1.1 Interface**
  - **Single-Wire HDQ Interface**
- **Packages: 38-Pin TSSOP (DBT) and 36-Pin QFN (RTT)**
- **Complete Integrated Development Environment**

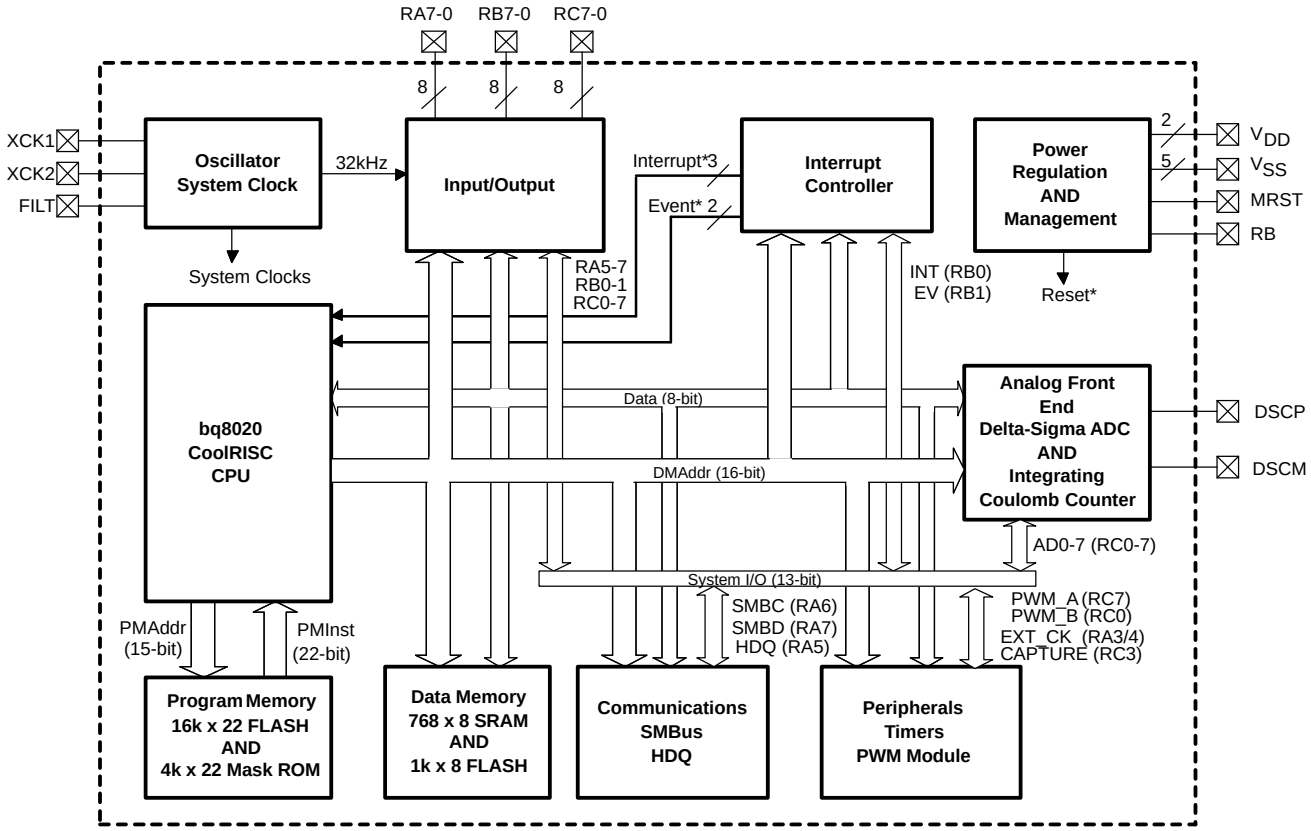
1.2 Applications

- **Battery Management**
- **Gas Gauges**

1.3 Description

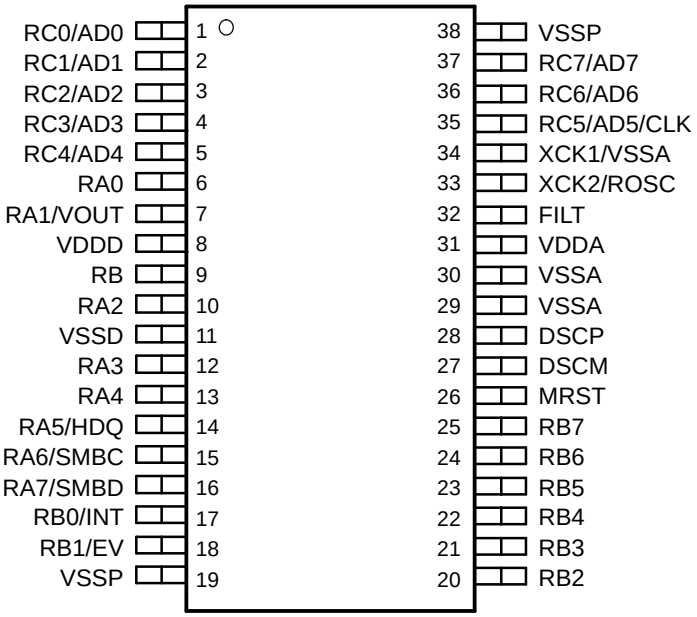
The Texas Instruments bq80201A Cool-GG™ programmable battery management IC is one of a series of advanced, high-performance, reduced instruction-set CPU (RISC) integrated circuits for battery management and gas-gauge applications. In a single CMOS IC, the bq80201A combines high-accuracy analog measurement capabilities with a low-power high-speed RISC processor, integrated flash memory and an array of peripheral and communication ports. The program flash EPROM allows fast development of custom implementations, and the low-power analog peripherals improve accuracy beyond discrete implementations. In its 38-pin TSSOP or 36-pin QFN packages, the bq80201A can implement a variety of functions in a small PCB area.

1.4 Functional Block Diagram

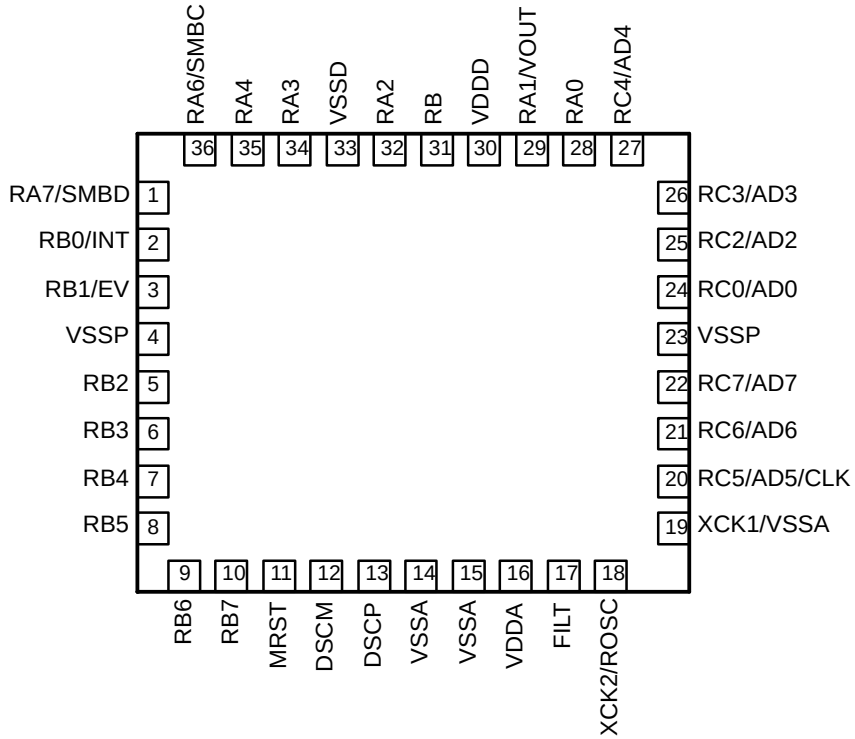


1.5 Terminal Assignments

DBT PACKAGE
(TOP VIEW)



RTT PACKAGE
(TOP VIEW)



1.6 Terminal Functions

TERMINAL NAME	TSSOP	QFN	I/O(1)	DESCRIPTION
DSCM	27	12	IA	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between DSCP and DSCM. DSCM can also be selected as an input to the over-sampled ADC.
DSCP	28	13	IA	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between DSCP and DSCM. DSCP can also be selected as an input to the over-sampled ADC.
FILT	32	17	IA	Analog pin connected to the external PLL loop filter components.
MRST	26	11	I	Master reset input pin that forces the device into reset when held high. Must be held low for normal operation.
RA0	6	28	I/OD	Port A.0 digital open-drain I/O pin
RA1/VOUT	7	29	I/O	Port A.1 digital push-pull I/O pin with pull-up capable of driving power for an external device
RA2	10	32	I/OD	Port A.2 digital open-drain I/O pin
RA3	12	34	I/OD	Port A.3 digital open-drain I/O pin
RA4	13	35	I/OD	Port A.4 digital open-drain I/O pin
RA5/HDQ	14	N/A	I/OD	Port A.5 digital open-drain I/O pin or one-wire DQ/HDQ serial communication pin
RA6/SMBC	15	36	I/OD	Port A.6 digital open-drain I/O pin or SMBus clock pin
RA7/SMBD	16	1	I/OD	Port A.7 digital open-drain I/O pin or SMBus data pin
RB	9	31	P	RAM backup pin to provide backup potential to the internal DATA RAM if VCC is momentarily shorted, by using a capacitor attached between RB and VSS(2)
RB0/INT	17	2	I/OD	Port B.0 digital open-drain I/O pin or selectable as a configurable external processor interrupt.
RB1/EV	18	3	I/OD	Port B.1 digital open-drain I/O pin or selectable as a configurable external event input to wake the controller from a halt state.
RB2	20	5	I/OD	Port B.2 digital open-drain I/O pin
RB3	21	6	I/OD	Port B.3 digital open-drain I/O pin
RB4	22	7	I/OD	Port B.4 digital open-drain I/O pin
RB5	23	8	I/OD	Port B.5 digital open-drain I/O pin
RB6	24	9	I/OD	Port B.6 digital open-drain I/O pin
RB7	25	10	I/OD	Port B.7 digital open-drain I/O pin
RC0/AD0	1	24	I/O	Port C.0 digital push-pull I/O pin or selectable as an input, AD0, to the oversampled ADC
RC1/AD1	2	N/A	I/O	Port C.1 digital push-pull I/O pin or selectable as an input, AD1, to the oversampled ADC
RC2/AD2	3	25	I/O	Port C.2 digital push-pull I/O pin or selectable as an input, AD2, to the oversampled ADC
RC3/AD3	4	26	I/O	Port C.3 digital push-pull I/O pin or selectable as an input, AD3, to the oversampled ADC
RC4/AD4	5	27	I/O	Port C.4 digital push-pull I/O pin or selectable as an input, AD4, to the oversampled ADC
RC5/AD5/CLK	35	20	I/O	Port C.5 digital push-pull I/O pin or selectable as an input, AD5, to the oversampled ADC or a 32-kHz square-wave output
RC6/AD6	36	21	I/O	Port C.6 digital push-pull I/O pin or selectable as an input, AD6, to the oversampled ADC
RC7/AD7	37	22	I/O	Port C.7 digital push-pull I/O pin or selectable as an input, AD7, to the oversampled ADC
VDDA	31	16	P	Positive supply for analog circuitry. VDDA and VDDD must be driven to the same potential.
VDDD	8	30	P	Positive supply for digital circuitry and I/O pins. VDDD and VDDA must be driven to the same potential.
VSSA	30,29	14,15	P	Negative supply for analog circuitry. VSSA, VSSD, and VSSP must be driven to the same potential.
VSSD	11	33	P	Negative supply for digital circuitry. VSSA, VSSD, and VSSP must be driven to the same potential.
VSSP	19, 38	4,23	P	Negative supply for output circuitry. VSSA, VSSD, and VSSP must be driven to the same potential.
XCK1/VSSA	34	19	I	32.768 kHz crystal oscillator input pin or connected to VSSA if the internal oscillator is used
XCK2/ROSC	33	18	O	32.768 kHz crystal oscillator output pin or connected to a 100k, 50 ppm or better resistor if the internal oscillator is used

(1) I = Input, IA = Analog input, I/O = Input/output, I/OD = Input/Open-drain output, O = Output, OA = Analog output, P = power
(2) VSS refers to the common mode of VSSA and VSSD.

2 Specifications

2.1 Absolute Maximum Ratings

Over Operating Free-Air Temperature (unless otherwise noted)(1)

		UNIT
	Supply voltage range, V_{DD} relative to V_{SS}(2)	–0.3 V to 4.1 V
	Open-drain I/O pins, $V_{(IOD)}$ relative to V_{SS}(2)	–0.3 V to 6 V
	Input voltage range to all other pins, V_I relative to V_{SS}(2)	–0.3 V to V_{DD} + 0.3 V
T_A	Operating free-air temperature range	–20°C to 85°C
T_{stg}	Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{DD} refers to the common node of V_{DDA} and V_{DDD}. V_{SS} refers to the common node of V_{SSA} and V_{SSD}.

2.2 Electrical Characteristics

T_A = –20°C to 85°C, 3 V to 3.6 V (unless otherwise noted); Typical Values at T_A = 25°C and V_{DD} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(DDD)}$	Digital supply voltage range		3	3.3	3.6	V
$V_{(DDA)}$	Analog supply voltage range		3	3.3	3.6	V
$I_{(DDD)}$	Digital supply current	Normal (1)		2.0	3.5	mA
		Normal (V_{DD} = 3.3 V, T_A≤ 60°C(1)			2.5	
		Low power (2)		60	85	µA
		Low power (V_{DD} = 3.3 V, T_A≤ 60°C (2)			67	
		Sleep(3)		0.4	3.5	
		Sleep (V_{DD} = 3.3 V, T_A≤ 60°C(3)			1.1	
		Hibernate(4)(5)		0.01	3.0	
		Hibernate (V_{DD} = 3.3 V, T_A≤ 60°C(4)(5)			0.6	
$I_{(DDA)}$	Analog supply current	Normal(1)		200	300	µA
		Normal (V_{DD} = 3.3 V, T_A≤ 60°C(1)			235	
		Low power(2)		175	250	
		Low power (V_{DD} = 3.3 V, T_A≤ 60°C (2)			207	
		Sleep (3)		6.0	8.0	
		Sleep (V_{DD} = 3.3 V, T_A≤ 60°C(3)			6.9	
		Hibernate(4)(5)		0.4	0.8	
		Hibernate (V_{DD} = 3.3 V, T_A≤ 60°C(4)			0.7	
I(DDPOR)	Power on reset current	V(DD) < V(POR(5)		0.2	1.0	µA
		V(DD) < V(POR) (V_{DD} = 3.3 V, T_A≤ 60°C(5)			0.8	

(1) CPU executing test code. No flash programming or erase operation . ADC and CC operating. VOUTEN = 0.
(2) Internal oscillator, PLL circuits active (PLL_EN=1, OSC_EN=1) CC operating. CPU halted.
(3) Internal oscillator circuit active, PLL is off (PLL_EN=0, OSC_EN=1) CPU halted.
(4) Internal oscillator and PLL are off. (PLL_EN=0, OSC_EN=0). CPU halted.
(5) $I_{(DDPOR)} = I_{(DDD)} + I_{(DDA)}$

2.2.1 Power-On Reset (see Figure 2-6)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT-}	Negative-going voltage input		2.1	2.3	2.5	V
V_{hys}			50	125	200	mV

2.2.2 General Purpose Digital Inputs and Outputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage low				0.8	V
V_{OH}	Output voltage high(1)	I_L = –0.5 mA	V_{DD}–0.5			V
V_{OL}	Low-level output voltage	I_L = 0.5 mA			0.4	V
C_I	Input capacitance			5		pF
I_{OL}	Low-level output current	Open drain outputs, VOL = 0.4 V			10	mA
$I_{(VOUT)}$	VOUT source current	VOUT active, VOUT = V_{DD}– 0.6 V	–5			mA
$I_{lkg(VOUT)}$	VOUT leakage current	VOUT inactive	–0.2		0.2	µA
I_{lkg}	Input leakage current				1	µA

(1) RC[0:7] bus

2.2.3 ADC

Unless otherwise noted, the specification limits are valid at both slow and fast modes as well as internal and external reference.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range	Internal V_{ref}	–0.3		1	V
	External V_{ref}	–0.3		0.8 x VDDA	
Conversion time	FAST = 0		31.5		ms
	FAST = 1		2.0		
Resolution (no missing codes)	FAST = 0	16			bits
Effective resolution	FAST = 0	14	15		bits
	FAST = 1	9	10		
Input referred noise	FAST = 0		20		µVrms
	FAST = 1		375		
Integral nonlinearity	FAST = 0, –0.1 V to 0.8 x V_{ref}		±0.004	±0.010	%FSR (1)
	FAST = 0, –0.3 V to –0.1 V		±0.040		
	FAST = 1, –0.1 V to 0.8 x V_{ref}		±0.020	±0.040	
	FAST = 1, –0.3 V to –0.1 V		±0.042		
Offset error(2)	FAST = 0		100	250	µV
Offset error drif (2)	FAST = 0, 25°C to 85°C typical		1.3	4.0	µV/°C
Full-scale error (3)			±0.1%		
Full-scale error drift	FAST = 0, 25°C to 85°C typical		50		PPM/°C
Effective input resistance (4)		8			MΩ

(1) Full-scale reference
(2) Post-calibration performance
(3) Uncalibrated performance. This gain error can be eliminated with external calibration.
(4) The A/D input is a switched-capacitor input. Since the input is switched, the effective input resistance is a measure of the average resistance.

2.2.4 Coulomb Counter

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		–0.25		0.25	V
Conversion time	Single conversion		250		ms
Effective resolution	Single conversion	15			bits
Noise	Single conversion		5		µVrms
Integral nonlinearity	–0.1 V to 0.25 V		±0.004	±0.019	%FSR
	–0.25 V to –0.1 V		±0.007		
Offset error (1)			1		µV
Offset error drift (1)	25°C to 85°C typical		0.4	0.7	µV/°C
Full-scale error (2)(3)			±0.25%		
Full-scale error drift	25°C to 85°C typical		150		PPM/°C
Effective input resistance (4)		2.5			MΩ

(1) Post-calibration performance
(2) Reference voltage for the coulomb counter is typically V_{ref}/3.969 at V_{DD} = 3.3 V, T_A = 25°C.
(3) Uncalibrated performance. This gain error can be eliminated with external calibration.
(4) The CC input is a switched capacitor input. Since the input is switched, the effective input resistance is a measure of the average resistance.

2.2.5 Temperature Sensor (see Figure 2-7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TEMP)}$	Temperature sensor voltage (1)			–2.1		mV/°C

(1) -55.6 LSB/°C

2.2.6 Voltage Reference (see Figure 2-8)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage		1.219	1.225	1.231	V
Output voltage drift	T_A over 50°C		57		PPM/°C
	T_A below 50°C		40		

2.3 PLL Switching Characteristics

T_A = –20°C to 85°C, 3 V to 3.6 V (unless otherwise noted); Typical Values at T_A = 25°C and V_{DD} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(sp)}$	Start-up time (1)	±0.5% frequency error		2.0	5.0	ms

(1) The frequency error is measured from the trimmed frequency of the internal system clock which is 128 x oscillator frequency, nominally 4.194 MHz.

2.3.1 External Crystal Oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(exo)}$	Frequency error (1)	12.5 pF crystal	-0.025%		0.025%	
$t_{(sxo)}$	Start-up time (2)				200	ms

(1) The frequency error is measured from 32768 Hz.
(2) The startup time is defined as the time it takes for the oscillator output frequency to be ±1%.

2.3.2 Internal Crystal Oscillator (see Figure 2-1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(eio)}$	Frequency error (1)	ROSC = 100 kΩ	–2%	0.25%	2%	
$f_{(dio)}$	Frequency drift (2)	ROSC = 100 kΩ, T_A = 0°C to 50°C	–1%		1%	
$t_{(sio)}$	Start-up time (3)				250	µs

(1) The frequency error is measured from 32768 Hz, and does not incorporate additional offset due to PCB layout or component selection.
(2) The frequency drift is measured from the trimmed frequency at V_{DD} = 3 V, T_A = 25°C.
(3) The startup time is defined as the time it takes for the oscillator output frequency to be ±2%.

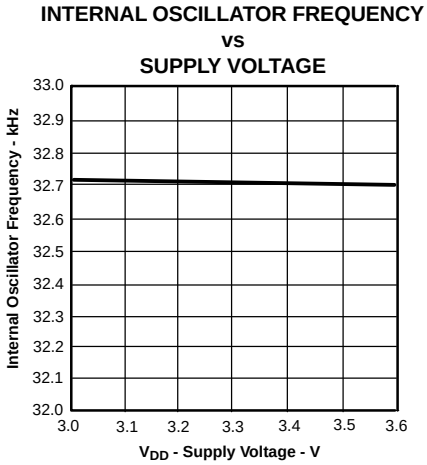


Figure 2-1. Internal Oscillator Frequency vs Supply Voltage

2.4 Data Flash Memory Switching Characteristics

Over Recommended Operating Temperature and Supply Voltage; Typical Values at T_A = 25°C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention	Assured by design. Not production tested.	10			Years
	Flash programming write-cycles		20k			Cycles
$t_{(ROWPROG)}$	Row programming time				2	ms
$t_{(MASSERASE)}$	Mass-erase time				200	ms
$t_{(PAGEERASE)}$	Page-erase time				10	ms
$I_{(DDPROG)}$	Flash-write supply current			8	15	mA
$I_{(DDERASE)}$	Flash-erase supply current			8	15	mA

2.4.1 Register Backup

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(RB)}$	RB data-retention input current	VRB > 2.0 V, V_{DD} < VIT		10	100	nA
		VRB > 2.0 V, V_{DD} < VIT, T_A = 0°C to 50°C		10	50	
$V_{(RB)}$	RB data-retention input voltage (1)		1.3			V

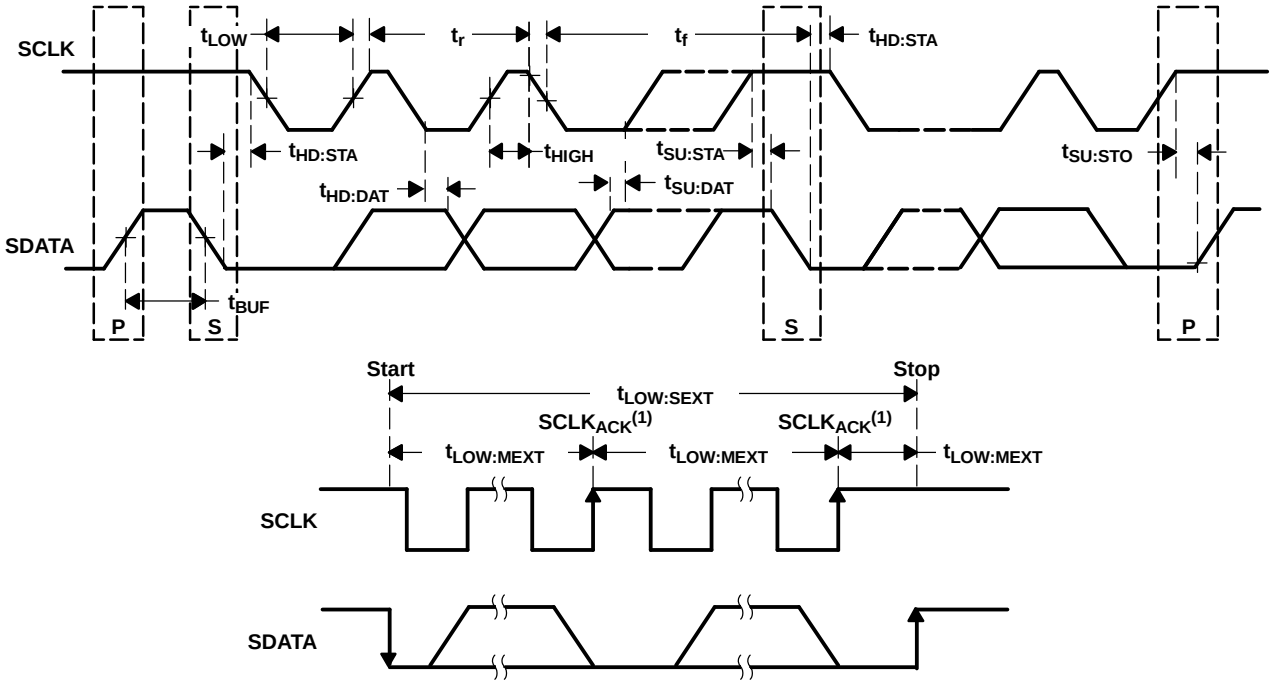
(1) Assured by design. Not production tested.

2.5 SMBus Timing Characteristics

T_A = –20°C to 85°C, 3.0 V < V_{CC} < 3.6 V; Typical Values at T_A = 25°C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		100	kHz
f_{MAS}	SMBus master clock frequency	Master mode, No clock low slave extend		51.2		kHz
t_{BUF}	Bus free time between start and stop (see Figure 2-2)		4.7			µs
$t_{HD:STA}$	Hold time after (repeated) start (see Figure 2-2)		4.0			µs
$t_{SU:STA}$	Repeated start setup time (see Figure 2-2)		4.7			µs
$t_{SU:STO}$	Stop setup time (see Figure 2-2)		4.0			µs
$t_{HD:DAT}$	Data hold time (see Figure 2-2)	Receive mode	0			ns
		Transmit mode	300			
$t_{SU:DAT}$	Data setup time (see Figure 2-2)		250			ns
$t_{TIMEOUT}$	Error signal/detect (see Figure 2-2)	See (1)	25		35	µs
t_{LOW}	Clock low period (see Figure 2-2)		4.7			µs
t_{HIGH}	Clock high period (see Figure 2-2)	See (2)	4.0		50	µs
$t_{LOW:SEXT}$	Cumulative clock low slave extend time	See (3)			25	µs
$t_{LOW:MEXT}$	Cumulative clock low master extend time (see Figure 2-2)	See (4)			10	µs
t_f	Clock/data fall time	See (5)			300	ns
t_r	Clock/data rise time	See (6)			1000	ns

(1) The bq80201A times out when any clock low exceeds $t_{TIMEOUT}$
(2) t_{HIGH}, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction involving bq80201A that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0]=0).
(3) $t_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) $t_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.
(5) Rise time t_r = ($V_{IL(max)}$ - 0.15) to ($V_{IH(min)}$ + 0.15)
(6) Fall time t_f = 0.9V_{DD} to ($V_{IL(max)}$ - 0.15)



(1) $SCLK_{ACK}$ is the acknowledge-related clock pulse generated by the master.

Figure 2-2. SMBus Timing Diagram

2.6 HDQ Timing Characteristics

Figure 2-3 through Figure 2-5 are timing diagrams for the bq80201A.

T_A = –20°C to 85°C, 3.0 V < V_{CC} < 3.6 V; Typical Values at T_A = 25°C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{c(CYCH)}$	Cycle time, host to bq80201A (write)	See Figure 2-4	190			µs
$t_{c(CYCB)}$	Cycle time, bq80201A to host (read)	See Figure 2-5	190	205	250	µs
$t_{h(STRH)}$	Start hold time, host to bq80201A (write)	See Figure 2-4	5			ns
$t_{h(STRB)}$	Start hold time, host to bq80201A (read)	See Figure 2-5	32			µs
$t_{su(DSU)}$	Data setup time	See Figure 2-4			50	µs
$t_{su(DSUB)}$	Data setup time	See Figure 2-5			50	µs
$t_{h(DH)}$	Data hold time	See Figure 2-4	100			µs
$t_{(DV)}$	Data valid time	See Figure 2-5	80			µs
$t_{su(SSU)}$	Stop setup time	See Figure 2-4			145	µs
$t_{su(SSUB)}$	Stop setup time	See Figure 2-5			145	µs
$t_{(RSPS)}$	Response time, bq80201A to host		190		320	µs
$t_{(B)}$	Break time	See Figure 2-3	190			µs
$t_{(BR)}$	Break recovery time	See Figure 2-3	40			µs

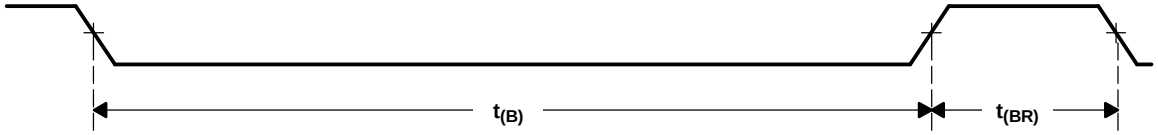


Figure 2-3. HDQ Break Timing

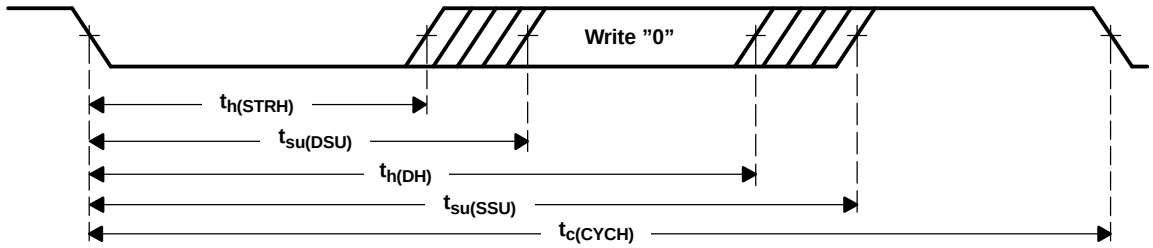


Figure 2-4. HDQ Host to bq8012

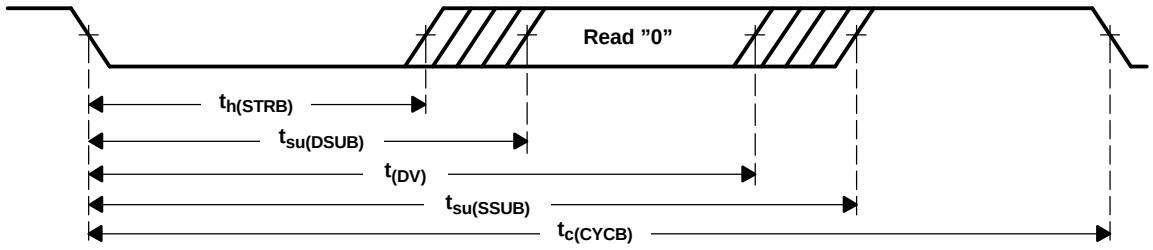


Figure 2-5. HDQ bq8012 to Host

2.7 Typical Characteristics

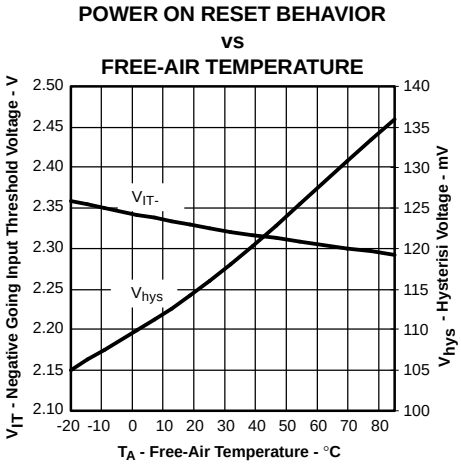


Figure 2-6. Power On Reset Behavior vs Free-Air Temperature

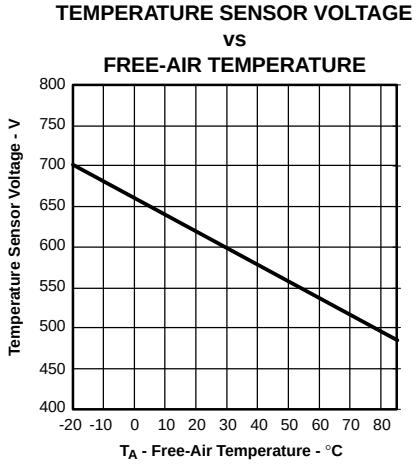


Figure 2-7. Temperature Sensor Voltage vs Free-Air Temperature

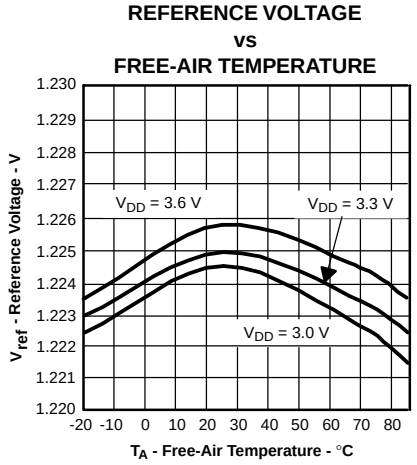


Figure 2-8. Reference Voltage vs Free-Air Temperature

3 General Operation Overview

The bq80201A functional block diagram outlines the major components within the IC. Together with the flash-based firmware, the bq80201A performs the necessary calculations and control for a fully functional battery management system. Each of the major component blocks within the bq80201A is outlined below.

3.1 RISC Processor

The bq80201A's flexible architecture allows easy development of numerous battery-management solutions. Based on a RISC processor featuring a Harvard architecture, the bq80201A operates at frequencies up to 4 MHz. The clock frequency is synthesized from an on-chip oscillator or a low-cost 32-kHz crystal. Using a three-stage instruction pipeline, the RISC processor can execute one instruction every clock cycle. With a 22-bit instruction width, the bq80201A can manipulate complex data with a single line of code.

3.2 Data and Program Memory

To improve performance and reduce operating power, the bq80201A uses separate data and program memory address buses, providing ample program and data-storage capability. This feature also allows for future memory expansion of the bq80201A family without affecting existing programs.

The bq80201A provides 768 bytes of data RAM on three 256-byte pages and another 1024 bytes of flash EPROM on another four 256-byte pages. The flash EPROM is available to store user specific static data, such as serial numbers and system operational data, without modifying the program memory. The bq80201A provides flexible instruction memory for implementing a wide-variety of battery management functions. For better flash EPROM utilization, the bq80201A instruction memory is separated into two blocks. The first block is a 16k x 22 flash EPROM for custom user programs and the second block is a 4k x 22 mask ROM containing common programs such as the math and battery-management libraries, communication, and power-on reset routines. Refer to the bq80201A Mask ROM description for further details.

In addition, the 768 bytes of general-purpose SRAM can be powered by the RB pin of the bq80201A if power is lost. Typically, a capacitor provides the necessary voltage to the cells during inadvertent momentary power loss. The RB pin can also be connected to a battery cell to provide power to the data RAM for longer periods. The RB pin operating current is less than 50 nA.

Figure 3-1 and Figure 3-2 outline the bq80201A memory maps and shows the address location of the internal registers. Further details about the bq80201A registers are in the register description section and Figure 3-1, bq80201A register and peripheral map.

3.3 Analog Front End

The bq80201A features a precision analog front-end ideal for battery monitoring and capacity measurement applications. Two analog-to-digital converters (ADCs) and a 12-channel multiplexer are available, allowing program flexibility. The first ADC is an integrating converter designed specifically for coulomb counting. The converter resolution is a function of how many samples are integrated: 16 samples for 2.5-μV resolution. For example, 9.3 μV can be resolved after a single 250-ms conversion. Therefore, a 10-μV signal is resolved in approximately 1 seconds. The second converter is a 15-bit delta sigma ADC for general-purpose measurements. This converter can be connected to one of eight multiple-purpose I/O pins, an internal temperature sensor, the current sense inputs, or the negative power supply. The 15-bit mode has a conversion time of 32 ms and the 10-bit mode has a conversion time of 2 ms. In either mode, a full 24 bits are returned from the converter for better averaging capability.

3.4 I/O and Specialized Functions

The bq80201A provides a total of 24 memory-mapped I/O lines in three ports (A, B, C). These ports are used for data conversion, communication, external-device power interface, external interrupt or wake, and general-purpose control functions.

The bq80201A provide two hardware communications ports. The first is the two-wire SMBus interface (SMBC and SMBD, dual function with RA6 and RA7). Together with the proper firmware, it is compatible with the SMBus v1.1 protocol supporting packet error check (PEC) if enabled. The second communications port is the single-wire HDQ serial interface (dual function with RA5). This pin can be made to support HDQ8 (8-bit) or HDQ16 (16-bit) protocols found on other bq gas gauge and battery management devices.

VOUT (Dual function with RA1) is a switch power supply of up to 5 mA to an external device under bq80201A firmware control. This power supply reduces the system implementation requirements for powering devices external to the bq80201A and eliminates wasting the additional power when the external device is not needed.

Clock out (32.768-kHz output) is dual-functioned with RC5. The 32.768-kHz output can be used to provide an accurate time-base to external devices such as a lithium-ion protector IC, without the cost of generating a new clock. The 32-kHz clock within the bq80201A simplifies the implementation.

The interrupt pin (dual function with RB0) provides a hardware means of interrupting the bq80201A during operation. The event pin (dual function with RB1) provides a hardware means of waking the bq80201A during sleep or hibernate modes. The inputs, if enabled, signal the CPU to resume from a HALT state and/or service an interrupt.

Further information about the specialized port functions is given in the bq80201A device pin-out and pin descriptions. Specialized function usage is detailed in the register map and register details section.

An internal temperature sensor is available on the bq80201A to reduce the cost, power, and size of the external components necessary to measure temperature. Scaled to -58.6 LSB/°C in the ADC data registers, the internal temperature sensor is ideal for determining pack temperature during storage and the IC temperature during operations.

3.5 Power Consumption

The bq80201A core running from the mask ROM is capable of 1,700 MIPS/watt in a 3-V system. Combined with other very low power analog peripherals, the bq80201A is ideal for embedded battery-management applications. The bq80201A also provides three reduced-power modes for additional power savings. In the low-power mode, the CPU is halted but the PLL and clock oscillator are still operating. In the sleep mode, the CPU is halted, the PLL is off, and the clock oscillator is running. In this mode, the current is less than 4.5 μA during crystal operation, and less then 10 μA in when utilizing internal oscillator. In the hibernate mode, the CPU is halted, and both the PLL and clock oscillator are turned off, reducing the current to less than 1 μA.

3.6 Mask ROM Functions

The bq80201A default-state is with the flash EPROM erased to all 1s. Upon powering up the bq80201A for the first time, the initialization routine is executed from the mask ROM. After initialization, the bq80201A defaults as an SMBus slave (address 16h). From this point, the flash instruction memory may be programmed. Once the flash programming is complete and the proper commands initiated, the bq80201A executes its program from the flash memory. During normal operation, the library commands in the mask ROM are still available for use.

3.7 Memory Map

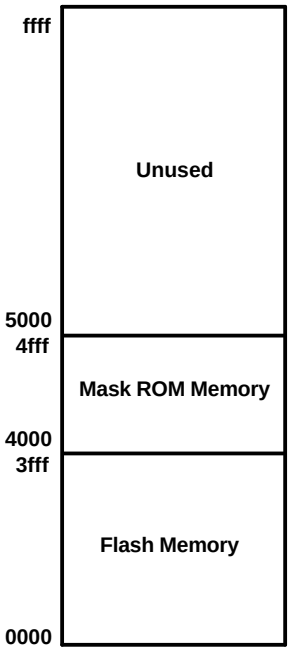


Figure 3-1. Program Memory Register Map

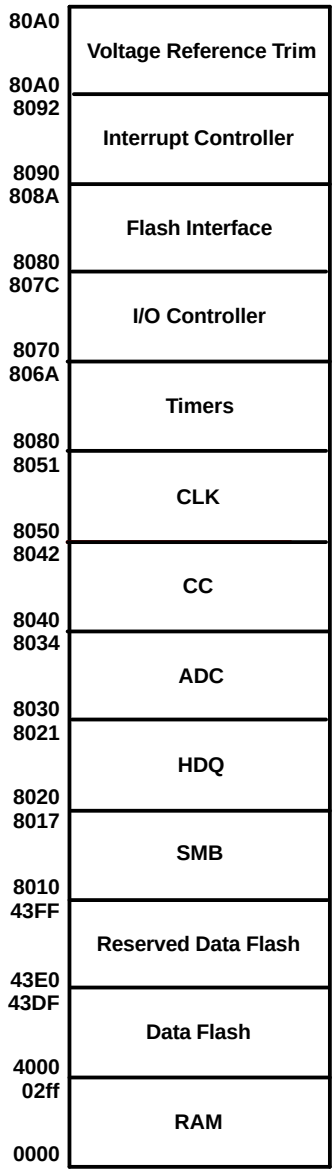


Figure 3-2. Data Memory Map

Table 3-1. bq80201A Register and Peripheral Map

Address	Symbol	Name	Read/ Write	Bit fields							
				7 (MSB)	6	5	4	3	2	1	0 (LSB)
8010h	SMBMA	SMBus master mode	Write	SMBMA7	SMBMA6	SMBMA5	SMBMA4	SMBMA3	SMBMA2	SMBMA1	R/W_B
8011h	SMBDA	SMBus data	R/W	SMBD7	SMBD6	SMBD5	SMBD4	SMBD3	SMBD2	SMBD1	SMBD0
8012h	SMBACK	SMBus acknowledge	Write	—	—	—	—	—	—	—	ACK
8013h	SMBSTA	SMBus status	Read	BUS_LOW	D_REQ	D_RDY	SA_RDY	NACKED	BUS_FREE	UNIT_BUSY	MASTER
8014h	SMBCTL	SMBus control	R/W	NC_SMB	BLI_EDGE	BLI_EN	PEC_DIS	BFI_EN	SMB_RST	ISOLATE	SA_EN
8015h	SMBPEC	SMBus packet error check	R/W	—	—	—	—	—	PEC_SND	PEC_CHK	PEC_VLD
8016h	SMBTAR	SMB target slave address	R/W	SMBT7	SMBT6	SMBT5	SMBT4	SMBT3	SMBT2	SMBT1	SMBT0
8017h	SMBBUSLO	SMB Bus Low		—	—	—	—	—	BUSLO_2	BUSLO_1	BUSLO_0
8020h	HDQSTA	HDQ register status	Read	—	—	—	—	HDQ_DRQ	HDQ_DRDY	SBIT_IN	DATA_IN
8021h	HDQOUT	HDQ output control register	R/W	—	—	—	—	—	—	SBIT_OUT	DATA_OUT
8030h	ADCTL0	ADC control register 0	R/W	CONV	VRVDD	ADC_ON	FAST	CHAN3	CHAN2	CHAN1	CHAN0
8031h	ADCTL1	ADC control register 1	Read	—	—	—	—	—	—	—	AD_DRDY
8032h	ADHI	ADC data register hi byte	Read	ADR23	ADR22	ADR21	ADR20	ADR19	ADR18	ADR17	ADR16
8033h	ADMID	ADC data register mid byte	Read	ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
8034h	ADLO	ADC data register low byte	Read	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
8040h	CCCTL	Coulomb counter control register	R/W	—	—	—	—	—	—	CC_ON	CC_CAL
8041h	CCHI	Coulomb counter data high byte	Read	CCR15	CCR14	CCR13	CCR12	CCR11	CCR10	CCR9	CCR8
8042h	CCLO	Coulomb counter data low byte	Read	CCR7	CCR6	CCR5	CCR4	CCR3	CCR2	CCR1	CCR0
8050h	CLK	Clock control register	R/W	—	—	DG1	DG0	**Reserved**	OSC_NG	OSC_EN	PLL_EN
8051h	OSC_TRIM	Oscillator trim control	R/W	OTRIM7	OTRIM6	OTRIM5	OTRIM4	OTRIM3	OTRIM2	OTRIM1	OTRIM0
8060h	TMRCTLW	Timer control register	R/W	—	—	—	—	WDF	WDEN	WKEN	WDRST
8061h	TMRPERW	Timer program register	R/W	PERW7	PERW6	PERW5	PERW4	PERW3	PERW2	PERW1	PERW0
8062h	TMRCTLA	Timer A control	R/W	—	TM16	TMA_ON	TMA_EXT	TMA_ISRC	TMA_EDG	TMA_PS1	TMA_PS0
8063h	TMRCTLB	Timer B control	R/W	PWB1	PWB0	TMB_ON	TMB_EXT	TMB_ISRC	TMB_EDG	TMB_PS1	TMB_PS0
8064h	TMRCTLC	Timer C control	R/W	PWA1	PWA0	MODE_2	MODE_1	MODE_0	CAP_EDG	CAP_PS1	CAP_PS0
8065h	TMRPERA	Timer A period	R/W	PERA7	PERA6	PERA5	PERA4	PERA3	PERA2	PERA1	PERA0
8066h	TMRPERB	Timer B period	R/W	PERB7	PERB6	PERB5	PERB4	PERB3	PERB2	PERB1	PERB0
8067h	TMRPWA	Timer A PWM	R/W	PWA9	PWA8	PWA7	PWA6	PWA5	PWA4	PWA3	PWA2
8068h	TMRPWB	Timer B PWM	R/W	PWB9	PWB8	PWB7	PWB6	PWB5	PWB4	PWB3	PWB2
8069h	TMRPGMA	Timer A program	R/W	PGMA7	PGMA6	PGMA5	PGMA4	PGMA3	PGMA2	PGMA1	PGMA0
806Ah	TMRPGMB	Timer B program	R/W	PGMB7	PGMB6	PGMB5	PGMB4	PGMB3	PGMB2	PGMB1	PGMB0
8070h	RA_OUT	RA output register	R/W	RAOUT7	RAOUT6	RAOUT5	RAOUT4	RAOUT3	RAOUT2	RAOUT1	RAOUT0
8071h	RB_OUT	RB output register	R/W	RBOUT7	RBOUT6	RBOUT5	RBOUT4	RBOUT3	RBOUT2	RBOUT1	RBOUT0
8072h	RC_OUT	RC output register	R/W	RCOUT7	RCOUT6	RCOUT5	RCOUT4	RCOUT3	RCOUT2	RCOUT1	RCOUT0
8073h	RA_IN	Status of RA register inputs	Read	RAIN7	RAIN6	RAIN5	RAIN4	RAIN3	RAIN2	RAIN1	RAIN0
8074h	RB_IN	Status of RB register inputs	Read	RBIN7	RBIN6	RBIN5	RBIN4	RBIN3	RBIN2	RBIN1	RBIN0
8075h	RC_IN	Status of RC register inputs	Read	RCIN7	RCIN6	RCIN5	RCIN4	RCIN3	RCIN2	RCIN1	RCIN0
8076h	RA_IEN	Enable RA input register	R/W	RAIEN7	RAIEN6	RAIEN5	RAIEN4	RAIEN3	RAIEN2	RAIEN1	RAIEN0
8077h	RB_IEN	Enable RC input register	R/W	RBIEN7	RBIEN6	RBIEN5	RBIEN4	RBIEN3	RBIEN2	RBIEN1	RBIEN0
8078h	RC_IEN	Enable RC input register	R/W	RCIEN7	RCIEN6	RCIEN5	RCIEN4	RCIEN3	RCIEN2	RCIEN1	RCIEN0
8079h	IOCTL	IO control register	R/W	32K_OUT	PWMA_EN	PWMB_EN	XEVEN	XINTEN	SMBEN	HDQEN	VOUTEN
807Ah	**Reserved**										
807Bh	**Reserved**										
807Ch	RC_PUP	RC pullup register	R/W	RCPUP7	RCPUP6	RCPUP5	RCPUP4	RCPUP3	RCPUP2	RCPUP1	RCPUP0
8080h	**Reserved**										
8081h	**Reserved**										
8082h	**Reserved**										
8083h	**Reserved**										
8084h	**Reserved**										

Table 3-1. bq80201A Register and Peripheral Map (continued)

Address	Symbol	Name	Read/ Write	Bit fields							
				7 (MSB)	6	5	4	3	2	1	0 (LSB)
8085h	**Reserved**										
8086h	**Reserved**										
8087h	**Reserved**										
8088h	**Reserved**										
8089h	**Reserved**										
808Ah	**Reserved**										
8090h	PFLAG	Peripheral flag register	R/W	SMBF	HDQF	ADF	CCF	TIMF	WKF	TMAF	TMBF
8091h	PIE	Peripheral interrupt enable	R/W	SMBIE	HDQIE	ADIE	CCIE	TIMIE	WKEVE	TMAIE	TMBIE
8092H	PCTL	Peripheral control	R/W	—	—	—	—	—	—	XIN_EDG	XEV_EDG
80a0h	VTRIM	Voltage reference trim	R/W	—	—	VTRIM5	VTRIM4	VTRIM3	VTRIM2	VTRIM1	VTRIM0

4 System Management Bus (SMBus) Peripheral and Operation Interface

The bq80201A system management bus peripheral (SMB) implements the two-wire bidirectional interface and protocol specified in the system management bus v1.1 specification. The SMB peripheral interfaces to the bq80201A CPU via interrupts or register polling. This peripheral can transmit and receive data as either an SMBus master or SMBus slave. The slave address for the bq80201A can be configured to respond automatically to a single slave address, or to multiple addresses if programmed into the bq80201A firmware.

The SMBus interface to the bq80201A CPU consists of seven registers and four possible types of interrupts.

4.1 SMB Interrupts

D_RDY (Data Ready): This indicates that serial data have been received and are available to be read by the bq80201A CPU. This interrupt is asserted before the SMBus acknowledge clock (ACK clock is stretched).

D_REQ (Data Request): This indicates that the SMB peripheral is ready for data to be sent on the SMBus. The bq80201A CPU must supply these data via a register write. This interrupt is asserted after previous ACK clock (clock after previous ACK is stretched).

BUS_FREE: This indicates that the SMBus is not active.

SA_RDY (Slave Address Ready): This indicates that a slave address has been received and must be checked by the bq80201A CPU to determine whether the SMB peripheral acknowledges the address. While this event is not typical for SMBus peripherals, this interrupt allows the bq80201A to respond to multiple slave addresses if necessary. The interrupt occurs before ACK clock (ACK clock is stretched).

4.2 Operating as a Slave

Automatic acknowledgement of a slave address requires SA_EN to be set to 0 in the SMB control register (8014h). In this mode, the SMB peripheral monitors the SMBus pins, watching for the slave address programmed in SMBTAR register. When this address has been received, the SMB peripheral ACKs the address and prepare to receive the ensuing command byte. If SA_EN is set to 1, firmware is required to examine the address and determine whether to ACK the address. After this command byte has been received, D_RDY is asserted, signaling the CPU that a command has been successfully received and is available to be read from SMBDA. The CPU must then decode this command and decide whether to ACK or NACK the command by writing to the SMBACK register (8012h), clearing D_RDY. For valid commands that may be either reads or writes, the CPU cannot determine whether to prepare to send data or receive it at this point. To determine whether the command is an SMB read or write:

- If the next SMBus activity consists of a repeated start followed by the repeated target address with LSB = 1, the transaction is a slave read. The SMB ACKs the repeated address and assert D_REQ, signaling the CPU that a slave read is in progress.
- If a repeated start is not received, the SMB is prepared to continue receiving data. Upon reception of eight more bits of data, D_RDY is asserted, signaling the CPU that a slave write is in progress.

4.2.1 For a Slave Read

In response to D_REQ, the CPU must write the required data to the SMBDA register (8011h), clearing D_REQ.

NOTE

The only way to abort the transaction at this point is to not clear D_REQ, causing the SMB to eventually time-out the SMBus and reset.

Upon each succeeding assertion of D_REQ, the status of the master's ACK or NACK of the preceding transmitted byte is checked by reading the NACKED bit. Ordinarily the final data byte is NACKed by the master, indicating the master is finished receiving data. If the expected final data byte is ACKed by the master, this indicates a PEC byte is to be sent. In this case, the PEC_SND bit in the SMBPEC register (8014h) is set in response to D_REQ. This setting clears D_REQ and instruct the SMB peripheral to send a PEC byte; SMBDA should not be written. In response to the final D_REQ with NACKED = 1, the CPU should write a 0 to SMBACK to clear D_REQ.

4.2.2 For a Slave Write

The SMB peripheral is receiving data sent from the master. After each byte of received data, D_RDY is asserted, signaling the CPU that the data byte is ready to be read from SMBDA. The CPU needs to ACK or NACK the byte by writing to SMBACK register, clearing D_RDY. If a data byte is to be checked as a PEC byte, the PEC_VLD bit in the SMBPEC register is checked after assertion of the final D_RDY and before writing the final ACK (or NACK).

4.3 Operating as a Master

The CPU must first verify that the SMBus is not currently active. Verification is by either polling the BUS_FREE bit in the SMBSTA register or setting the BFI_EN bit in the SMBCTL register. Once the bus is verified inactive, the CPU may then write the address of the slave device it wishes to communicate with to the SMBMA register. If the transaction is a read from the slave, the LSB of this register is written as a 1. Otherwise, if the transaction is a write to the slave, the LSB is written as a 0.

After transmitting the slave address, the SMB peripheral asserts a D_REQ. Then, successful acknowledgment of the address by the slave is indicated by the bit NACKED = 0. If NACKED = 1, the CPU may abort the transaction by writing a 0 to SMBACK. This action clears D_REQ and a stop condition is sent to free the bus. Otherwise, with NACKED = 0, the transaction is continued with the CPU writing the required SMBus command to SMBDA. This clears D_REQ and instruct the SMB peripheral to send the contents of SMBDA on the SMBus. D_REQ is asserted again after the command has been ACKed or NACKed by the slave. If ACKed, the next step is dependent on the LSB of SMBMA.

4.3.1 SMBMA Register for an LSB = 1: (R/W_B = 1), Master Read

D_REQ is cleared by writing a 1 to SMBACK, causing the SMB peripheral to send a repeated start followed by the repeated SLAVE address with its LSB = 1. This repeated address is ACKed or NACKed by the slave, and is verified by reading the NACKed bit after the next assertion of D_REQ. The D_REQ is cleared by writing a 1 to SMBACK. Then data are sent to the SMB peripheral from the slave device. After each byte of received data, D_RDY is asserted signaling the CPU that the data bit is ready to be read from SMBDA. The CPU then ACKs or NACKs the byte by writing to SMBACK, clearing D_RDY. If a data byte is to be checked as a PEC byte, the PEC_VLD bit is checked after assertion of the final D_RDY and before writing the final NACK. The final data byte to be read, or the PEC byte, is NACKed, which signals the SMB to end the master read and send a stop.

4.3.2 SMBMA Register for an LSB = 0: (R/W_B = 0), Master Write

D_REQ signals the request for data to be sent to the slave and is cleared by writing the requested data to the SMBDA register. Upon each assertion of D_REQ, the status of the slave's ACK or NACK of the preceding byte is checked by reading the NACKED bit. If a PEC byte is to be sent, PEC_SND is set in response to the D_REQ preceding the byte to be considered a PEC byte. Writing to PEC_SND clears D_REQ; the SMBDA register should not be written. If no more data are to be sent, the CPU should write a 0 to the SMBACK register in response to the final D_REQ, which clears D_REQ and sends a stop.

4.4 SMB Register Details (address 8010h-8017h)

The following is a description of the SMBus registers.

4.4.1 SMB (address 8010h):SMBus Master Address Register

A write to this register by the CPU initiates an SMBus master transaction, sets the desired SLAVE address, and signifies the type of SMB master transaction.

	SMBMA Register (Address 8010h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SMBMA7	SMBMA6	SMBMA5	SMBMA4	SMBMA3	SMBMA2	SMBMA1	R/W_B
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

SMBMA7-1 (bit 7:1): The SMB address of the slave device to be accessed in master mode.

R/W_B (bit 0): SMB master-mode direction control bit. This bit controls the direction of the master-mode transaction

1 = Master-mode read transaction from slave

0 = Master-mode write transaction to slave

4.4.2 SMBDA (address 8011h): SMBus Data Register

This is the register the CPU uses to transmit data to or receive data from the SMBus where SMBD0 is the LSB and SMBD7 is the MSB.

	SMBDA Register (Address 8011h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SMBD7	SMBD6	SMBD5	SMBD4	SMBD3	SMBD2	SMBD1	SMBD0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

4.4.3 SMBACK (address 8012h): SMBus Acknowledge Register

This register is used by the CPU to ACK/NACK the previously received data, to send stop condition in master mode, or to reset the SMB engine in response to errors detected on the SMBus.

	SMBACK REGISTER (ADDRESS 8012h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	—	—	ACK
Access	—	—	—	—	—	—	—	W
Reset	—	—	—	—	—	—	—	0

Reserved (bits 7:1): Do not use.

ACK (bit 0): Acknowledge bit.

1 = Acknowledge previous data, send ACK

0 = Do not acknowledge previous data, send NACK and reset; send stop if in master mode

4.4.4 SMBSTA (address 8013h): SMBus Status Register

This read-only register reports the status of the SMBus peripheral and SMBus interface.

	SMBSTA REGISTER (ADDRESS 8013h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BUS_LOW	D_REQ	D_RDY	SA_RDY	NACKED	BUS_FREE	UNIT_BUSY	MASTER
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

BUS_LOW (bit 7): SMBus Low bit. Indicates current state of BUS_LOW flag.

1 = BUS_LOW asserted, indicating a bus low timeout had occurred

0 = BUS_LOW not asserted

D_REQ (bit 6): Data request bit. This bit indicates current state of D_REQ interrupt.

1 = D_REQ asserted

0 = D_REQ not asserted

D_RDY (bit 5): Data ready bit. This bit indicates current state of D_RDY interrupt.

1 = D_RDY asserted

0 = D_RDY not asserted

SA_RDY (bit 4): Slave address ready bit. This bit indicates current state of SA_RDY interrupt.

1 = SA_RDY asserted

0 = SA_RDY not asserted

NACKED (bit 3): Not acknowledged bit. This bit indicates state of previously sent data's acknowledgment by the destination device (also indicates lost arbitration as a master).

1 = Previous data NACKed, or SMB has lost arbitration while operating as a master

0 = Previous data successfully ACKed

BUS_FREE (bit 2): Bus free bit. This bit indicates active state of the SMBus.

1 = SMBus inactive

0 = Activity detected on the SMBus

UNIT_BUSY (bit 1): SMB peripheral busy bit. This bit indicates active state of SMB engine.

1 = SMB engine processing an SMBus transaction as either a master or slave

0 = SMB engine idle

MASTER (bit 0): Master bit. This bit indicates whether or not the SMB engine is currently operating as an SMBus master.

1 = SMB engine has successfully attained master mode

0 = SMB engine is not currently operating as an SMBus master

4.4.5 SMBCTL (address 8014h): SMBus Control Register

This read-write register controls the operation of the SMBus peripheral.

	SMBCTL REGISTER (ADDRESS 8014h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	NC_SMB	BLI_EDGE	BLI_DIS	PEC_DIS	BFI_EN	SMB_RST	ISOLATE	SA_EN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

NC_SMB (bit 7): SMBus high time timeout disable bit. This is bit is used to disable the SMBus high time timeout in systems that may not conform to SMBus specifications.

1 = SMBus high time timeout disabled

0 = SMBus high time timeout enabled, conforms to SMBus specifications

BLI_EDGE (bit 6): Bus low interrupt polarity bit. This bit determines whether to generate an interrupt when BUS_LOW goes active, or when BUS_LOW goes inactive. BLI_EN must be set to trigger a bus low interrupt. BLI_EDGE should only be set if BUS_LOW is already active.

1 = If BLI_EN=1, generates an interrupt when BUS_LOW goes inactive.

0 = If BLI_EN=1, generates an interrupt when BUS_LOW goes active.

BLI_EN (bit 5): Bus low interrupt enable bit. This bit is used to enable SMB bus low timeout detection, and will generate an SMB interrupt if the SMBus clock and data lines have both been low for a time exceeding the programmable SMB bus low timeout (SMBBUSLO register, default=2s). This bit can be used to implement the charger broadcast re-enable function as described in the Smart Battery Data specification.

1 = Enable SMB bus low detection.

0 = Disable SMB bus low detection.

PEC_DIS (bit 4): Packet error checking engine disable bit. This bit disables PEC engine to conserve power if PEC checking or generation is not required.

1 = PEC engine disabled

0 = PEC engine enabled

BFI_EN (bit 3): Bus free interrupt enable bit. This bit enables interrupt when BUS_FREE is set.

1 = Assert interrupt in response to BUS_FREE assertion

0 = Mask assertion of interrupt in response to BUS_FREE assertion; BUS_FREE must be polled to determine active state of SMBus

SMB_RST (bit 2): SMB engine software reset bit.

1 = Reset SMB engine

0 = SMB normal operation

ISOLATE (bit 1): SMBus isolation bit. This bit isolates SMB peripheral from SMBus.

1= Disconnect SMB peripheral from SMBus

0 = SMB normal operation

SA_EN (bit 0): Slave address detection enable bit. This bit enables assertion of SA_RDY to allow the device to respond to multiple slave addresses.

1 = SA_RDY asserted in response to any slave address detected on SMBus; CPU required to ACK or NACK address via SMBACK

0 = SMB normal operation; SMB engine ACKs address programmed in SMBTAR without CPU intervention

4.4.6 SMBPEC (address 8015h): SMBus Packet Error Check Register

This register manages the PEC generation and control for SMBus transactions.

	SMBPEC REGISTER (ADDRESS 8015h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	PEC_SND	PEC_CHK	PEC_VLD
Access	—	—	—	—	—	R/W	R/W	R/W
Reset	—	—	—	—	—	0	0	0

Reserved (bits 7:3): Do not use.

PEC_SND (bit 2): PEC send bit. This bit instructs SMB engine to send calculated PEC byte of previously transmitted SMBus data; it is set in response to a DATA_REQ assertion.

1 = Send PEC byte (cleared by hardware)

0 = Do not send PEC byte

PEC_CHK (bit 1): PEC check bit. This bit instructs SMB engine to expect calculated PEC byte of previously transmitted SMBus data, or successful non-PEC termination of proceeding transaction; it is set in response to a D_RDY assertion.

1 = Check PEC byte (cleared by hardware)

0 = Do not check PEC byte

PEC_VLD (bit 0): PEC valid bit. This bit indicates validity of previously received PEC byte or successful non-PEC termination of previous SMBus transaction; it is read only in response to a D_RDY assertion.

1 = PEC byte was valid or a valid stop was received for a non-PEC transaction

0 = PEC byte was not valid

4.4.7 SMBTAR (address 8016h): SMBus Target Slave Register

This register contains the slave address that the SMB engine responds to where SMT0 is the LSB and SMT7 is the MSB.

	SMBTAR REGISTER (ADDRESS 8016h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SMT7	SMT6	SMT5	SMT4	SMT3	SMT2	SMT1	SMT0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

4.4.8 SMBBUSLO (address 8017h): SMBus Bus Low Timeout Program Register

This register is used to adjust the length of time before an SMB bus low timeout violation occurs.

NOTE
Adjusting this register from the default value will violate theSMBus spec for BUS LOW timeout.

	SMBUSLO REGISTER (ADDRESS 8017h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	BUSLO2	BUSLO1	BUSLO0
Access	—	—	—	—	—	R/W	R/W	R/W
Reset	—	—	—	—	—	1	0	0

Reserved (bits 7:3): Do not use.

BUSLO[2:0]: SMBus bus low timer select. These bits select timeout period for BUS_LOW to be asserted:

000 = never.
001 = 0.5 s.
010 = 1.0 s.
011 = 1.5 s.
100 = 2.0 s (default reset value).
101 = 2.5 s.
110 = 3.0 s.
111 = 3.5 s.

5 HDQ Single-Pin Serial Interface Peripheral

The HDQ serial interface peripheral may be used to implement a single-wire serial interface. For flexibility, the HDQ peripheral performs all bit-framing for the transmission and reception of data and BREAK signals. Since this peripheral is a bit engine, all command and data formatting is a function of the user firmware offering maximum flexibility. The user firmware is required to format the received bits in a timely fashion and to transmit data bits out in the correct cycle time and format. The engine may be set up for interrupt driven operation, or polling may be used to determine peripheral status.

The HDQ interface is an asynchronous return-to-one protocol where a processor sends the command code to the bq80201A. With HDQ, the least significant bit (LSB) of a data byte (command) or word (data) is transmitted first. Note that the RA5/HDQ pin is open drain and requires an external pullup resistor. The 8-bit command code consists of two fields: the 7-bit HDQ command code (bits 0-6) and the 1-bit R/W field (MSB bit 7). The R/W field directs the bq80201A either to

- Store the next 8 or 16 bits of data to a specified register or
- Output 8 or 16 bits of data from the specified register

The HDQ peripheral can transmit and receive data as either an HDQ master or slave.

The return-to-one data bit frame of HDQ consists of three distinct sections. The first section is used to start the transmission by either the host or by the bq80201A taking the HDQ pin to a logic-low state for a time $t_{(STRH,B)}$. The next section is for data transmission, where the data are valid for a time $t_{(DSU)}$, after the negative edge used to start communication. The data are held until a time $t_{(DV)}$, allowing the host or bq80201A time to sample the data bit. The final section is used to stop the transmission by returning the HDQ pin to a logic-high state by at least a time $t_{(SSU)}$, after the negative edge used to start communication. The final logic-high state is held until the end of $t_{(CYCH,B)}$, allowing time to ensure the transmission was stopped correctly. The timing for data and break communication are given in the HDQ characteristics section.

HDQ serial communication is normally initiated by the host processor sending a break command to the bq80201A. A break is detected when the HDQ pin is driven to a logic-low state for a time $t_{(B)}$ or greater. The HDQ pin should then be returned to its normal ready high logic state for a time $t_{(BR)}$. The bq80201A is now ready to receive information from the host processor.

The HDQ peripheral is enabled by setting HDQEN=1 in the IOCTL register. HDQIE (bit 6 of the PIE register) and GIE (bit 5 of the internal CPU status register) must be set to a logic one for HDQ interrupt processing occur [address vector (3h)]. Refer to the interrupt processing section for more information about setting HDQIE and GIE. An HDQ interrupt (HDQF=HDQIE=GIE=1) is generated by the receiving valid data, a break condition or when the HDQ engine has finished transmitting and is ready to accept more data for transmission.

Data bits transmitted to the bq80201A are read via the HDQSTA register. The HDQ_DRDY bit is asserted by incoming data. Valid data are assumed when HDQ_DRDY=SBIT_IN=1. The data bit, DATA_IN, is stored allowing further command or data processing by the bq80201A. When HDQ_DRDY=1 and SBIT_IN=0, a BREAK or communication collision is assumed and the communication process restarted.

Data bits are output via the HDQOUT register. The first bit in a transmission may be sent by writing the appropriate data and stop bit to the DATA_OUT and SBIT_OUT bits, respectively. Subsequent data are sent after HDQ_DREQ is asserted, signifying that the transmission of the previous data is complete. A BREAK is transmitted by writing DATA_OUT=SBIT_OUT=0.

5.1 HDQSTA (address 8020h): HDQ Input and Interrupt Control Register

This register manages the HDQ interface and control status.

	HDQSTA REGISTER (ADDRESS 8020h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	HDQ_DRQ	HDQ_DRDY	SBIT_IN	DATA-IN
Access	—	—	—	—	R	R	R	R
Reset	—	—	—	—	—	—	—	—

Reserved (bit 7:4): Do not use.

HDQ_DRQ (bit 3): HDQ data request bit. Indicates current state of HDQ_DREQ when read

1 = HDQ_DREQ asserted

0 = HDQ_DREQ not asserted

HDQ_DRDY (bit 2): HDQ data request ready bit. Indicates current state of HDQ_cleared when read

1 = HDQ_DRDY asserted

0 = HDQ_DRDY not asserted

SBIT_IN (bit 1): HDQ stop bit In. Value of stop bit read from HDQ

1 = Stop bit equals 1

0 = Stop bit equals 0 (a break was received if DATA_IN=0)

DATA_IN (bit 0): HDQ data in. Value of data bit read from HDQ

1 = HDQ data in equals 1

0 = HDQ data in equals 0

5.2 HDQOUT (address 8021h): HDQ Output Control Register

This register manages the HDQ output control.

	HDQOUT REGISTER (ADDRESS 8021h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	—	SBIT_OUT	DATA_OUT
Access	—	—	—	—	—	—	R/W	W
Reset	—	—	—	—	—	—	—	—

SBIT_OUT (**bit 1):** HDQ stop bit out value of stop bit to be transmitted on bus

Reserved (bits 7:2): Do not use.

1 = Send a stop bit of 1

0 = Send a stop bit of 0 (sends a break if DATA_OUT=0)

DATA_OUT (bit 0): HDQ data out. Value of data bit to be transmitted on bus

1 = Send a 1

0 = Send a 0

6 Analog-to-Digital Converter (ADC) Operation

The ADC peripheral on the bq80201A consists of an analog multiplexer and a delta-sigma converter. The multiplexer can be configured to connect one of twelve different signals to the converter. For low-power operating modes, the ADC can be turned off under software control. Typical operation requires only a single write to the ADCTL0 register to simultaneously configure the ADC and issue a convert command.

Configuring the ADC includes enabling the peripheral (ADC_ON) and selecting the desired voltage referenced (VRVDD), filter length (FAST), and multiplexer channel (CHAN3:CHAN0). The conversion starts on the rising edge of CONV. CONV must be held high until the conversion is complete and data has been read from ADC data registers (ADHI:ADMID:ADLO). The ADC_DRDY bit (bit 0 in ADCTL1 register) is asserted upon completion of a conversion, signaling that valid data is available in the ADC data registers. The ADF flag bit in the PFLAG register is also asserted when ADC_DRDY goes to a one. An interrupt may be generated on the rising edge of ADC_DRDY; see theinterrupt timer section 8.6.1 for details.

CONV must be set to a zero before performing additional conversions. This clears ADC_DRDY, resets the ADC data registers to 800000h, and resets the converter. Once CONV is cleared, the converter is ready to perform additional conversions, or for the setup to change. The data in the ADC data registers is stored in 2s complement format. Full scale (7FFFFFh) is referred to the reference voltage (V_{ref}), typically 1.225 V when using the internal reference; or V_{DD} using the external reference. Even though the effective number of bits for a single conversion is 10 bits when FAST=1, and 15 bits when FAST=0, a 24-bit result is provided. Better resolution is obtained by averaging this 24-bit result across multiple conversions. If 16-bit accuracy is sufficient, reading ADLO is not necessary and should be skipped to simplify mathematical computation. To save power, the converter may be turned off by setting ADC_ON to a zero.

NOTE

For the specified accuracy, the ADC input range is limited to 80% of the ADC voltage reference input, either V_{DD} or internal V_{ref}.

6.1 ADCTLO (address 8030h): ADC Control Register

This is one of the ADC peripheral control registers.

	ADCTL0 REGISTER (ADDRESS 8030h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CONV	VRVDD	ADC_ON	FAST	CHAN3	CHAN2	CHAN1	CHAN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

CONV (bit 7): Convert command bit. This bit is used to start a conversion.

1 = Conversion started on the rising edge of CONV; CONV is held high until after valid data are read from ADLO and ADHI (ADC_DRDY =1)

0 = ADC held in reset; ADC_DRDY =0 and ADLO = 00h, ADHI = 80h

VRVDD (bit 6): Voltage reference selection bit. This bit selects which voltage reference (either VDD or internal V_{ref}) is used by the ADC.

1 = Selects VDD as the ADC reference voltage for ratiometric conversions

0 = Selects the internal VREF as the ADC reference voltage

ADC_ON (bit 5): ADC power control bit. This bit powers the ADC and the multiplexer.

1 = ADC power is on

0 = ADC power off and the multiplexer input impedance high

FAST (bit 4): Filter length selection bit. This bit selects between the 512 or 8192 length digital filter.

1 = 512 length decimation filter. Conversion time is 1.95 ms.

0 = 8192 length decimation filter. Conversion time is 31.25 ms.

CHAN3-CHAN0 (bit 3-0): Channel selection bits. These bits select which of twelve multiplexer inputs is converted.

CHAN3-CHAN0	ADC INPUT CHANNEL
0000	RC0
0001	RC1
0010	RC2
0011	RC3
0100	RC4
0101	RC5
0110	RC6
0111	RC7
1000	DSCP
1001	DSCM
1010	VTEMP
1011	Reserved
1100	Reserved
1101	Reserved
1110	Reserved
1111	VSSA

6.2 ADCTL1 (address 8031h): ADC Control Register 1

This register signals when data are ready from the ADC peripheral.

	ADCTL1 REGISTER (ADDRESS 8031h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	—	—	ADC_DRDY
Access	—	—	—	—	—	—	—	R
Reset	1	0	0	0	0	0	0	0

Reserved (bits 7:1): Do not use.

ADC_DRDY (bit 0): Data ready flag. This read-only bit signals when valid data are ready in ADLO and ADHI.

1 = Valid data are ready

0 = Conversion in progress or ADC held in reset, ADC_DRDY goes low on the falling edge of CONV

6.3 ADHI, ADMID, ADLO (address 8032h, 8033h, 8034h): ADC Data Registers

These store the result of the ADC data after conversion is complete. ADR0 is the LSB and ADR23 is the MSB.

	ADHI REGISTER (ADDRESS 8032h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ADR23	ADR22	ADR21	ADR20	ADR19	ADR18	ADR17	ADR16
Access	R	R	R	R	R	R	R	R
Reset	1	0	0	0	0	0	0	0

	ADMID REGISTER (ADDRESS 8033h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
Access	R	R	R	R	R	R	R	R
Reset	0	01	0	0	0	0	0	0

	ADL0 REGISTER (ADDRESS 8034h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

7 Coulomb Counter Operation

The coulomb counter peripheral is a single-channel, over-sampled converter with continuous sampling and is optimized for tracking charge and discharge activity of a rechargeable battery. The coulomb counter (CC) in normal operation is configured to convert the differential voltage across pins DSCP and DSCM. The coulomb counter design allows the integration of successive samples with no loss or corruption of data. This integration further reduces quantization error over time, thereby increasing system resolution. The coulomb counter can be turned on or off under firmware control, enabling greater power efficiency.

Coulombs are counted by integrating the voltage across a sense resistor placed in series with the negative terminal of a battery. After a power-on reset, the default state of the CC peripheral is off. The CC peripheral is enabled by setting the CC_ON bit to one in the CCCTL register. The CC inputs, DSCP and DSCM, are configured for normal operation by writing CC_CAL to a zero in the CCCTL register. The conversions begins automatically after CC_ON is set to a one. The converter asserts the CCF flag bit in the PFLAGS register once every 250 ms. An interrupt is generated when CCF is set, assuming CCIE = PIE = GIE = 1. CCLO and CCHI are then read and CCF cleared before another 250 ms have elapsed, avoiding corruption or data loss when the registers are updated following the next conversion.

The data in CCHI-CCLO are stored in 2's complement format. Full scale (7FFFh) is referred to approximately V_{ref} divided by four (typically 3.969). For a typical V_{ref} of 1.225 V, full scale is 308.64 mV. The allowable range of voltages for DSCP and DSCM is -0.25 V to 0.25 V. The differential voltage between DSCP and DSCM is limited to less than 0.25 V. The least significant bit (LSB) for a single conversion is 9.4 μV or 0.651 nVh. The charge LSB can be determined by dividing 0.654 nVh by the value of the sense resistor. Resolution is improved by summing (integrating) consecutive samples since no information is lost between conversions.

Calibration cycles can be performed at any time. To perform calibration if the coulomb counter is off, set CC_CAL and CC_ON to one. If the coulomb counter is on, and the conversion result is desired, wait until the conversion is complete and then read the data in CCLO and CCHI. After the data are read, turn the coulomb counter off by writing CC_ON to zero. This ensures that the converter is reset, and another calibration cycle can then be performed by setting CC_CAL and CC_ON to one. If the coulomb counter is on and the conversion result is not wanted, simply turn off the coulomb counter by writing CC_ON to zero. Calibrations are then performed by setting CC_CAL and CC_ON to one. Averaging of successive conversion results improves the offset resolution and better cancels the offset. One of several offset cancellation algorithms is chosen, depending upon the required performance and operating conditions.

After exiting sleep mode, it is not necessary to wait for the PLL frequency to settle, to start a coulomb-counter conversion. A conversion can start immediately after waking from sleep. For dc inputs, a conversion error less than one LSB can be achieved. However, if greater accuracy is required, wait until the PLL settles before initiating a conversion. When a conversion starts while the PLL is settling, the conversion time is slightly longer than 250 ms.

To save power, turn the converter off by setting CC_ON to a logic zero.

7.1 CCCTL (address 8040h): Coulomb Counter Control Register

This register controls the CC peripheral.

	CCCTL REGISTER (ADDRESS 8040h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	—	CC_ON	CC_CAL
Access	—	—	—	—	—	—	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Reserved (bits 7:2): Do not use.

CC_ON (bit1): Coulomb counter enable. This bit enables power to the coulomb counter peripheral.

1 = Coulomb counter power turned on

0 = Coulomb counter power turned off and DSCP and DSCM inputs are high-impedance state

CC_CAL (bit0): Coulomb counter calibration input control bit. This bit controls the differential input to the coulomb counter.

1 = Both inputs to the coulomb counter driven from DSCM for calibration

0 = Coulomb counter inputs driven differentially from pins DSCP and DSCM for normal operation

7.2 CCHI, CCLO (address 8041h, 8042h): Coulomb Counter Data Register

Coulomb counter register pair stores the result of the coulomb counter operation in two 8-bit registers, CCLO and CCHI, in 2s complement format where CCR0 is the LSB and CCR15 is the MSB.

	CCHI REGISTER (ADDRESS 8041h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CCR15	CCR14	CCR13	CCR12	CCR11	CCR10	CCR9	CCR8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

	CCLO REGISTER (ADDRESS 8042h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CCR7	CCR6	CCR5	CCR4	CCR3	CCR2	CCR1	CCR0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

8 PLL Clock Generator Peripheral

The PLL clock generator peripheral contains all of the necessary circuitry to generate the internal clocks for the bq80201A. The peripheral is composed of a crystal oscillator, Phase-locked-loop (PLL), and nonoverlapping clock circuit. The nominal clock frequency used by the bq80201A is 4.194 MHz, while the analog circuitry is clocked at 262.144 kHz. The peripheral also provides a 1.049-MHz clock for the SMB engine and a 32.768-kHz clock for the internal timers.

8.1 Oscillator Operation

The 32 kHz clock is generated from either a crystal oscillator or internal oscillator. On power-up the bq80201A automatically determines if an external bias resistor is present for the internal oscillator. If this resistor is present, the IC configures itself to run off of the internal oscillator. If a crystal is attached to the device instead of the internal oscillator bias resistor, the IC configures itself to run off the crystal oscillator. The configuration circuitry automatically powers off the unused oscillator circuit to save power.

Since the internal oscillator frequency is a function of the bias resistor, its value and drift performance are critical. It is recommended to use a value of 100 kΩ with a tolerance of 0.1% and a drift of 50 ppm/C or less.

The crystal oscillator is used with a 12.5-pF crystal. On-chip load capacitance of 12 pF is provided on XCK1 and XCK2. For greater frequency accuracy, additional off-chip capacitance may be added. However for most fuel gauging applications the extra capacitance is not necessary.

For the most accurate analog performance, using an external crystal is recommended.

The internal oscillator is trimmed at the factory using the OSC_TRIM register (0x8051). The factory determined value for this register is stored in nonvolatile reserved data flash and is loaded when the device is booted. Changing the value in the OSC_TRIM register may cause the device to fail.

8.2 PLL Clock Generator Operation

The CLK register control bits are reset during a POR or MRST. During a POR or MRST, the clock peripheral enters a low-power state and after the reset, the clock control bits are set to ensure that the clock is enabled. A watchdog reset is treated differently. If a watchdog reset occurs, the PLL_EN bit is set to a logic one. A watchdog reset does not affect the OSC_EN control bit.

To enter sleep (turn off PLL), 0x02 is written to address 0x8050. To enter hibernate (turn off PLL and oscillator), 0x00 is written to address 0x8050. In order to prevent the device from hanging after the register is written, the PLL and oscillator are not actually powered off until a halt instruction is executed.

Because the CPU is halted, waking the part from sleep mode is accomplished through communication on the HDQ or SMB pins, an external event or interrupt, or an internal interrupt. Since all of the clocks on the device are off during hibernate, external pins are the only available means to enable the clocks. Specifically, the HDQ, SMBC, SMBD, EV, and INT pins can be used to power up both the oscillator and PLL. If there is an external event or interrupt, or if there is communication on the HDQ or SMB pins, the oscillator and PLL are both enabled. Any communication with the part while the clocks are off only serves to wake up the device. Until the clocks become valid, data cannot be received by the part.

When the device is waking from sleep, if there is a valid SMB start condition during the first 4 ms, the SMBus holds the SMB clock line low until the PLL frequency has stabilized. 4 ms after the PLL is enabled, the frequency is stable, and SMB communication occurs.

When the device is waking from hibernate, until the oscillator begins to provide clocks, the SMBus will NACK any communication. Once the oscillator begins to clock, the SMBus behaves as if it is waking from sleep. I.e., for 4 mS after the oscillator begins to clock, if there is a valid SMB start condition, the SMBus holds the SMB clock line low until the PLL frequency has stabilized.

The PLL requires the addition of an external loop filter. The components are a 62-kΩ resistor in series with a 2.2-nF capacitor; the series combination is shunted by a 150-pF capacitor. When the PLL is powered off, the bq80201A requires approximately 1.5 ms to 4 ms to stabilize the PLL when it is re-enabled.

8.3 Oscillator Health Monitor

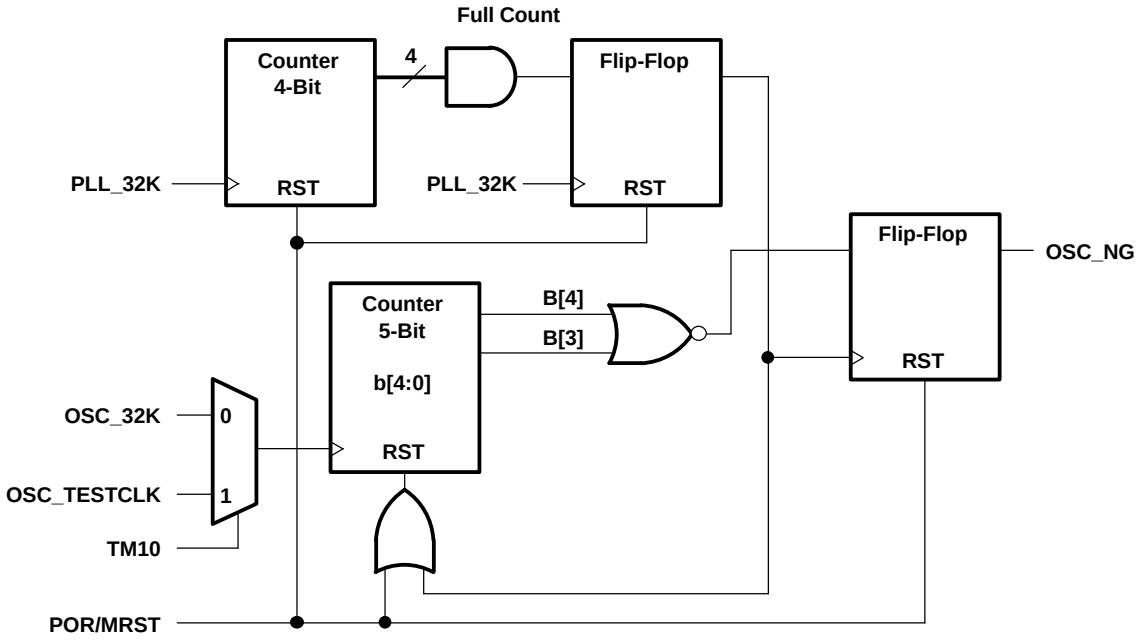


Figure 8-1. Oscillator Health Monitor Diagram

8.3.1 Hardware Description

The oscillator health monitor determines if the crystal oscillator or internal oscillator is functioning. This is a gross detection and is not an indication of performance. The output of the circuit is OSC_NG, which is set when the oscillator is determined to be nonfunctional. This register bit is read only and is cleared when the oscillator becomes functional. The address of the register is 0x8050h.

The inputs to the circuit are PLL_32K, which is the VCO divided down clock from the PLL, or OSC_32K, which is the internal or crystal oscillator (whichever is selected by the auto-detect circuit), and OSC_TESTCLK, which is an input clock on pin RC0 when tm10 is high. The circuit is reset by POR or MRST.

The circuit operates as follows. It compares the number of PLL_32K clocks to the number of OSC_32K clocks. The OSC_NG bit is set if OSC_32K < 8 or OSC_32K > 31 for 16 pll_32k clocks. If the 5-bit counter wraps, the OSC_NG bit is cleared when OSC_32K > 39. Hence the gross nature of the detection. This is acceptable since in the case of a missing or broken crystal or external resistor, the oscillation frequency should be zero or extremely low.

During power-on, or whenever the oscillator is powered up (exit hibernation), the OSC_NG bit is set until the oscillator starts and is stabilized. Once the oscillator has stabilized, OSC_NG clears if the oscillator is functional.

8.3.2 Reset De-Glitch Operation

Integrated into the Power-On Reset (POR) and Master Reset (MRST) circuitry is a programmable delay filter, intended to mask erroneous reset pulses due to external supply transients, or noise coupled into the Master Reset pin. Three delay times are available by setting the control bits DG1:0, while the default setting is no de-glitch delay filter (DG1:0 = 00). When the de-glitch circuitry is enabled, the POR or MRST signal must be active long enough to exceed the listed delay times to trigger a valid reset. However, a reset is not ensured unless the POR or MRST signal is active for two times the listed delay time, due to the sampling nature of the circuit.

8.4 CLK (Address 8050h): Clock Register

This register contains the clock configuration bits for the bq80201A.

Name	RSVD	RSVD	DG1	DG0	RSVD	OSC_NG	OSC_EN	PLL_EN
Access	R	R	R	R	R	R	R/W	R/W
DURING RESET	0	0	0	0	0	0	0	0
AFTER RESET	0	0	0	0	0	NA	1	1
During and After WDRST	NA	NA	NA	NA	NA	NA	Prior State	1
WAKE	0	0	0	0	0	NA	1	1

RSVD The RSVD bits are reserved for future revisions.

DG1:0 POR and MRST de-glitch filter control bits. These bits select the minimum filter delay time for the Power-On Reset and Master Reset signals. Programmable minimum delay times are as follows:

00 = No de-glitch filter, applied to POR and MRST.
01 = POR delay = 238 ns, MRST delay = 3.8 µs.
10 = POR delay = 3.8 µs, MRST delay = 61 µs.
11 = POR delay 61 µs, MRST delay = 3.9 ms.

OSC_NG Indication of the gross functionality of the internal or crystal oscillator. Can be used to determine if a crystal is broken.

1 = Oscillator is potentially malfunctioning.
0 = Oscillator is functioning.

OSC_EN The OSC_EN bit powers up the crystal or internal oscillator circuitry.

1 = Crystal or internal oscillator is turned on.
0 = Crystal or internal oscillator is turned off when a halt is issued by the microprocessor.

PLL_EN PLL power control bit. This bit enables power to the PLL. This signal is also used to control power to the bias circuitry. When the PLL is enabled, it takes 3.9 ms until the 1.049-MHz clock comes up (this assumes that the crystal oscillator has been on).

1 = The PLL is turned on.
0 = The PLL is turned off when a halt is issued by the microprocessor.

8.5 OSC_TRIM REGISTER (ADDRESS: 8051H)

Name	OTRIM7	OTRIM6	OTRIM5	OTRIM4	OTRIM3	OTRIM2	OTRIM1	OTRIM0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

OTRIM(7:0) Trim values used to calibrate the internal oscillator.

8.6 Timers

There are five timers on the device: an interrupt timer, a bus-low timer, a watchdog timer, and two general-purpose 8-bit timer/counter modules—Timer A and Timer B. The reference oscillator operates the interrupt, bus-low, and watchdog timers, so if the reference oscillator is disabled, these timers do not function. The interrupt timer provides a method to schedule tasks via processor interrupts. The bus-low timer is used to detect when the battery pack has been removed from the system. The watchdog timer provides a method for processor reset if processor execution becomes errant. Timer A and Timer B primarily serve as the time-base for the capture/compare/PWM modules. The PWM mode is intended to provide external charger control functionality, by establishing charge current and charge voltage set points.

8.6.1 Interrupt Timer

The interrupt timer is free-running and has a period of 7.8125 ms. When the TIMIE bit (bit 3) is enabled in the PIE register, the interrupt controller requests interrupt servicing at every interrupt timer clock period.

8.6.2 Bus-Low Timer

The bus-low timer is also free-running and is used in conjunction with bus-monitoring circuitry to determine if the battery has been removed from the system for more than two seconds. The sample period of the bus-low timer is 125 ms. The interrupt timer and the bus-low timer are reset by any reset event (POR, MRST, or watchdog reset). The bus-low timer is selectable: none, 0.5, 1.0, 1.5, 2.0, 2.5, 3.0, 3.5 using BUSLO[2:0] in the SMBBUSLO register (0x8017).

8.6.3 Watchdog and Wake Timer

The watchdog timer provides a method for periodic system reset in the case of errant processor execution. If the WDEN bit in the timer control register is set, and the value in the 16 bit count-up watchdog counter equals the value in the timer program register (concatenated with FFh in the lower byte), a LEVEL 1 reset is generated.

8.6.4 TMRCTLW - Timer Control Register (Address: 8060h)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	RSVD	RSVD	RSVD	RSVD	WDF	WDEN	WKEN	WDCRST
Access	R	R	R	R	R/W	R/W	R/W	R/W
After WD RST	0	0	0	0	1	0	0	0
During Other RESET	0	0	0	0	0	0	0	1
After Other RESET	0	0	0	0	0	0	0	0

RSVD The RSVD bits are reserved and must not be modified by firmware to ensure compatibility with future silicon revisions. These bits are forced to a logic zero.

WDF The WDF bit (bit 3) indicates a watchdog reset has occurred

1 = The watchdog reset enabled
0 = The watchdog reset disabled

WDEN The WDEN bit (bit 2) enables the watchdog timer reset circuit

1 = The watchdog reset enabled
0 = The watchdog reset disabled

WKEN The WKEN bit (bit 1) enables the wake timer signal.

1 = The timer issues a wake signal.
0 = No wake signal is provided.

WDCRST The WDCRST bit (bit 0) clears both the watchdog and wake counter, and must be periodically set by firmware to avoid a watchdog reset. This bit is automatically cleared by the watchdog circuitry after the internal watchdog counter is reset.

1 = The watchdog counter is reset
0 = Watchdog counting if enabled

If the bq80201A enters hibernation mode (the reference oscillator is stopped), the registers are preserved throughout hibernation if VDD is above minimum operating voltage, and remain in this state when the bq80201A exits hibernation. If WDEN is high, the watchdog counter is stopped when the reference oscillator is stopped. It resumes counting from the previous point when the reference oscillator starts again.

8.6.5 TMRPERW - Watchdog and Wake Timer Program Register (Address: 8061h)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	PERW7	PERW6	PERW5	PERW4	PERW3	PERW2	PERW1	PERW0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

The timer program register sets the wake and watchdog reset time. The minimum wake time is 3.90625 ms when the register is set to 01h. The maximum wake time is 996.09 ms when the program register is set to FFh. The program register allows the user to program the time between the minimum and maximum values in 3.90625 ms steps. The wake and watchdog timer is disabled when TMRPERW is set to 00h. The program register also sets the watchdog reset time to twice the wake time. Therefore, the minimum watchdog reset time is 7.8125 ms and the maximum reset time is 1.9922 seconds. The programming step size is 7.8125 ms.

The watchdog timer can also be programmed to provide a wake signal, which is a processor event to allow the cpu to resume from the HALT state. The wake time is always one-half of the watchdog time.

Clearing the watchdog timer clears both the watchdog reset signal and the wake signal. The timer control and program registers are only reset by the LEVEL 0 RESET (POR and MRST). The LEVEL 1 RESET (watchdog timer reset) has no effect on these registers. The timer program register does not count down when the wake or watchdog timers are enabled. When programmed, the timer register will maintain its value unless reprogrammed or a LEVEL 0 RESET has occurred.

Since both the wake signal and watchdog reset are operated from the same counter, care must be used when enabling each signal. Enabling one signal while the other signal is already enabled does not reset the state of the counter. To ensure proper operation in this situation the user should clear the counter before enabling the second signal. Clearing can be accomplished by writing 0 to both WDEN and WKEN bits in the TMR_CNTL register followed by setting both enable bits to 1.

8.6.6 Timer A and Timer B

Timer A and Timer B are 8-bit timers, each with a 2-bit prescaler. Figure 8-2 shows the block diagram for Timers A and B. TMRPGMA and TMRPGMB are read/write registers, cleared on any LEVEL 0 or LEVEL 1 RESET. The prescaler option allows TMRPGMA and TMRPGMB to increment at rates: 1:1, 1:2, 1:4, or 1:16, selected by the control bits TMA_PS1:0 (TMRCTLA<1:0>) and TMB_PS1:0 (TMRCTLB<1:0>). The respective prescaler counters are cleared when:

- The Timer Program Register (TMRPGMA or TMRPGMB) is written.
- The Timer Control Register (TMRCTLA or TMRCTLB) is written.
- Any LEVEL 0 or LEVEL 1 reset occurs.

NOTE

The timer program registers (TMRPGMA, TMRPGMB) are not cleared when the timer control registers (TMRCTLA or TMRCTLB) are written.

The input clock source is selectable between the internal system clock (4.194 MHz), the reference oscillator (32.768 kHz), or an external clock source applied on the port pin RA2. The control bits TMA_EXT:TMA_ISRC (TMRCTLA<4:3>) and TMB_EXT:TMB_INT (TMRCTLB<4:3>) select the clock input to the timers. When the clock source is an external clock, either the rising or falling edge is selected to increment the timer modules, using the control bits TMA_EDG (TMRCTLA<2>) and TMB_EDG (TMRCTLB<2>).

Timer A and Timer B are configured to operate as a single 16 bit timer using the control bit TM16 (TMRCTLA<6>). In this mode, TMRPERB becomes the high byte, with TMRPERA serving as the low byte. Only the Timer A configurations for the clock source and prescaler value are used in 16-bit timer mode; Timer B configurations, TMRCTLA<4:0>, are ignored. PWM mode is not useable if TM16 is set.

In normal mode, Timer A and Timer B begin counting from an initial value read from their respective program registers, TMRPGMA and TMRPGMB. Two 8-bit period registers, TMRPERA and TMRPERB, are compared to their respective timer program registers (TMRPGMA & TMRPGMB) on each successive timer increment, until a respective match occurs. The respective timer register is reset to 00h on the next increment cycle. TMRPERA and TMRPERB are read/write registers, initialized to FFh upon LEVEL 0 or LEVEL 1 RESET. The match outputs of the period registers are latched in bits TMAF and TMBF (PFLAG<1:0>) and can be configured to generate an interrupt,.

To minimize power consumption, Timer A and Timer B are turned off through control bits TMA_ON (TMRCTLA<5>) and TMB_ON (TMRCTLB<5>).

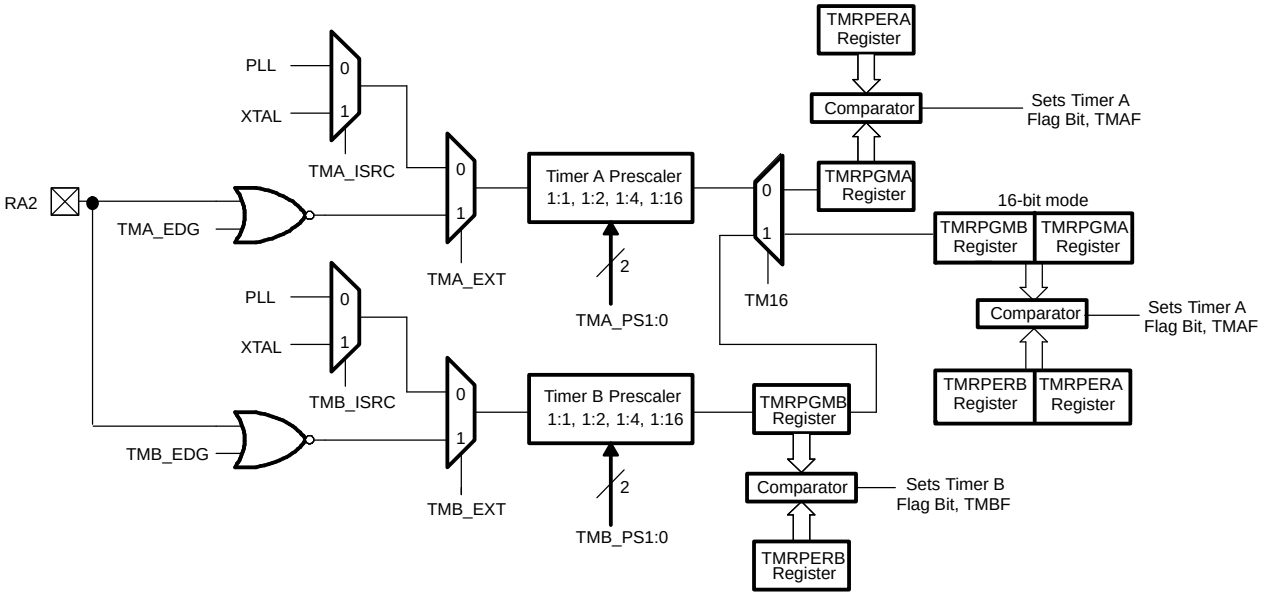


Figure 8-2. Timer A/B Block Diagram

8.6.7 TMRCTLA—Timer A Control Register (Address: 8062h)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	RSVD	TM16	TMA_ON	TMS_EXT	TMA_ISRC	TMS_EDG	TMS_PS1	TMA_PS0
Access	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	—	0	0	0	0	0	0	0

RSVD The RSVD bits are reserved for future use.

TM16 16-bit Timer mode. TMRA:TMRB represent a single 16-bit timer result.

1 = 16-bit timer mode enabled.
0 = 16-bit mode disabled.

TMA_ON Timer A On bit. This bit enables the Timer A.

1 = Timer A on.
0 = Timer A off.

TMA_EXT Timer A external clock select. This bit enables the clock input through port pin RA3.

1 = External clock input enabled.
0 = External clock input disabled.

TMA_ISRC Timer A internal clock source select. This bit selects between the reference oscillator input (32.768 kHz).and the system clock input (4.194 MHz).

1 = 32.768 kHz internal clock selected.
0 = 4.194 MHz internal clock selected.

TMA_EDG Timer A external clock edge select. This bit selects the active edge of the external clock input, either rising or falling edge. Only relevant if TMA_EXT set.

1 = Falling edge selected.
0 = Rising edge selected

TMA_PS1:0 Timer A prescale select. These bits select the prescale value as follows:

00 = 1:1 prescale value
01 = 1:2 prescale value
10 = 1:4 prescale value
11 = 1:16 prescale value

8.6.8 TMRCTLB—Timer B Control Register (Address: 8063h)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	PWB1	PWB0	TMB_ON	TMB_EXT	TMB_ISRC	TMB_EDG	TMB_PS1	TMB_PS0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

PWB1:0 The two least most significant bits for Timer B pulse width control, TMRPWB.

TMB_ON Timer B On bit. This bit enables the Timer B.

1 = Timer B on.
0 = Timer B off.

TMB_EXT Timer B external clock select. This bit enables the clock input through port pin RA4.

1 = External clock input enabled.
0 = External clock input disabled.

TMB_ISRC Timer B internal clock source select. This bit selects between the reference oscillator input (32.768 kHz).and the system clock input (4.194 MHz).

1 = 32.768 kHz internal clock selected.
0 = 4.194 MHz internal clock selected.

TMB_EDG Timer B external clock edge select. This bit selects the active edge of the external clock input, either rising or falling edge. Only relevant if TMB_EXT set.

1 = Falling edge selected.
0 = Rising edge selected.

TMB_PS1:0 Timer B prescale select. These bits select the prescale value as follows:

00 = 1:1 prescale value
01 = 1:2 prescale value
10 = 1:4 prescale value
11 = 1:16 prescale value

8.6.9 TMRCTLC—Capture/Compare/PWM Control Register (Address: 8064h)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	PWA1	PWA0	MODE2	MODE1	MODE0	CAP_EDG	CAP_PS1	CAP_PS0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

PWA1:0 The two least most significant bits for Timer A pulse width control, TMRPWA.

MODE2:0 Capture/Compare/PWM mode select. These bits select the following modes:

000 = Normal timer mode, interrupt only on match
001 = Capture mode enabled
010 = enable Timer A PWM mode
011 = enable Timer A and Timer B PWM modes
100 = Compare mode enabled, interrupt and drive output high on match
101 = Compare mode enabled, interrupt and drive output low on match
110 = Reserved
111 = Reserved

CAP_EDG Capture prescaler edge select. This bit selects the active edge of the external event capture input on pin RA3, either rising or falling edge.

1 = External event capture is falling edge triggered.
0 = External event capture is rising edge triggered.

CAP_PS1:0 Capture prescaler select. These bits select the capture prescaler value as follows:

00 = 1:1 prescale value
01 = 1:2 prescale value
10 = 1:4 prescale value
11 = 1:16 prescale value

8.6.10 TMRPERA—Timer A Period Register (Address: 8065h)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	PERA7	PERA6	PERA5	PERA4	PERA3	PERA2	PERA1	PERA0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

PERA7:0 Timer A period register.

8.6.11 TMRPERB—Timer B Period Register (Address: 8066h)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	PERB7	PERB6	PERB5	PERB4	PERB3	PERB2	PERB1	PERB0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

PERB7:0 Timer B period register.

8.6.12 TMRPWA—Timer A Pulse Width Register (Address: 8067h)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	PWA9	PWA8	PWA7	PWA6	PWA5	PWA4	PWA3	PWA2
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

PWA9:2 Timer A pulse width register, MSBs.

8.6.13 TMRPWB—Timer B Pulse Width Register (Address: 8068h)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	PWB9	PWB8	PWB7	PWB6	PWB5	PWB4	PWB3	PWB2
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

PWB9:2 Timer B pulse width register, MSBs.

8.6.14 TMRPGMA—Timer A Program Register (Address: 8069h)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	PGMA7	PGMA6	PGMA5	PGMA4	PGMA3	PGMA2	PGMA1	PGMA0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

PGMA7:0 Timer A program register. Least significant byte if 16-bit mode is enabled

8.6.15 TMRPGMB—Timer B Program Register (Address: 806Ah)

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	PGMB7	PGMB6	PGMB5	PGMB4	PGMB3	PGMB2	PGMB1	PGMB0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

PGMB7:0 Timer B program register. Least significant byte if 16-bit mode is enabled

9 Capture Mode

To correctly operate in capture mode, Timers A and B must be configured for 16-bit mode (TM16=1) with one of the internal clock sources selected (TMA_EXT=0). Timer A control bits are used when TM16=1; Timer B control bits are ignored. During capture mode, TMRPWB:TMRPWA captures the 16-bit value of the TMRPGMB:TRMPGMA registers when an event occurs on pin RA2. RA2 is configured as an input by setting RAIEN2. If RA2 is configured as an output, a write to port A (RAOUT2=0) can force a capture event.

A 2-bit prescaler option is used to require multiple input edges (2, 4, or 16) before a capture event takes place, using control bits TMA_PS1:0. The capture event may be configured to use either rising or falling input edges, using the control bit TMA_EDG. Any LEVEL 0 or LEVEL 1 reset clears the prescaler counter. Changing the capture prescaler value may generate an interrupt. Since the prescaler counter is not automatically cleared when changing the prescaler value, the first capture may be from a nonunity prescaler setting. It is recommended that the capture mode be exited before changing the capture prescaler, to ensure the prescaler counter gets cleared.

When a capture event occurs, the Timer A interrupt request flag bit, TMAF(PFLAG<1>),gets set. This flag bit must be cleared in software. If another capture event occurs before capture mode TMRPWB:TMRPWA is read, the previously captured value is lost. Figure 9-1 shows a simplified block diagram of the capture mode operation.

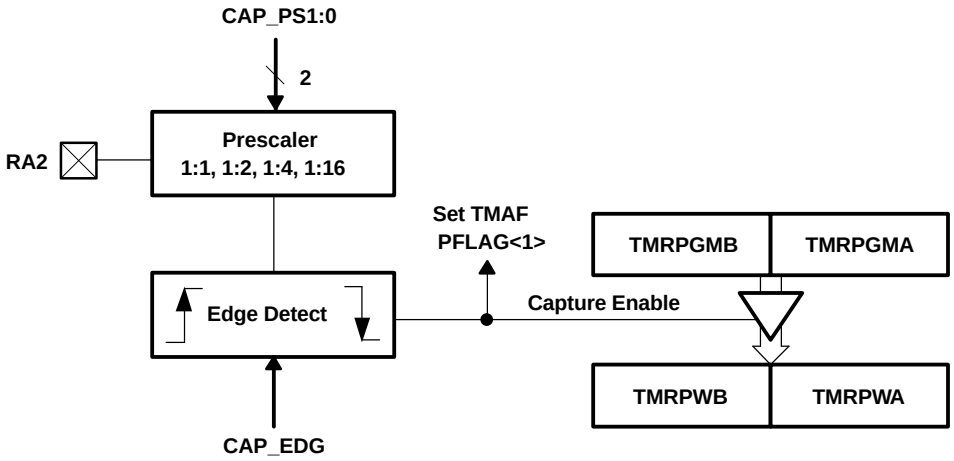


Figure 9-1. Capture Mode Block Diagram

10 Compare Mode

Compare mode is essentially the same as normal mode, but allows for external annunciation of comparison event via pin RC0. To correctly operate in Compare mode, Timers A and B must be configured for 16-bit mode (TM16=1). During compare mode, the register values in TMRPERB:TMRPERA are constantly compared against the 16-bit value in the TMRPGMB:TMRPGMA registers. When a match occurs, the interrupt flag bit, TMAF (PFLAG<1>), gets set. Additionally, the control bits MODE2:0 (TMRCTLC<5:3>) may be configured to perform the following functions when a match occurs:

- Drive RC0/PWM_A high, MODE2:0=100
- Drive RC0/PWM_A low, MODE2:0=101

If RC0/PWM_A is desired as a match output indicator, PWMA_EN (IOCTL<6>) must be set. RCPUP0 may be set to enable an internal pullup. Figure 10-1 shows a simplified block diagram of the compare mode operation.

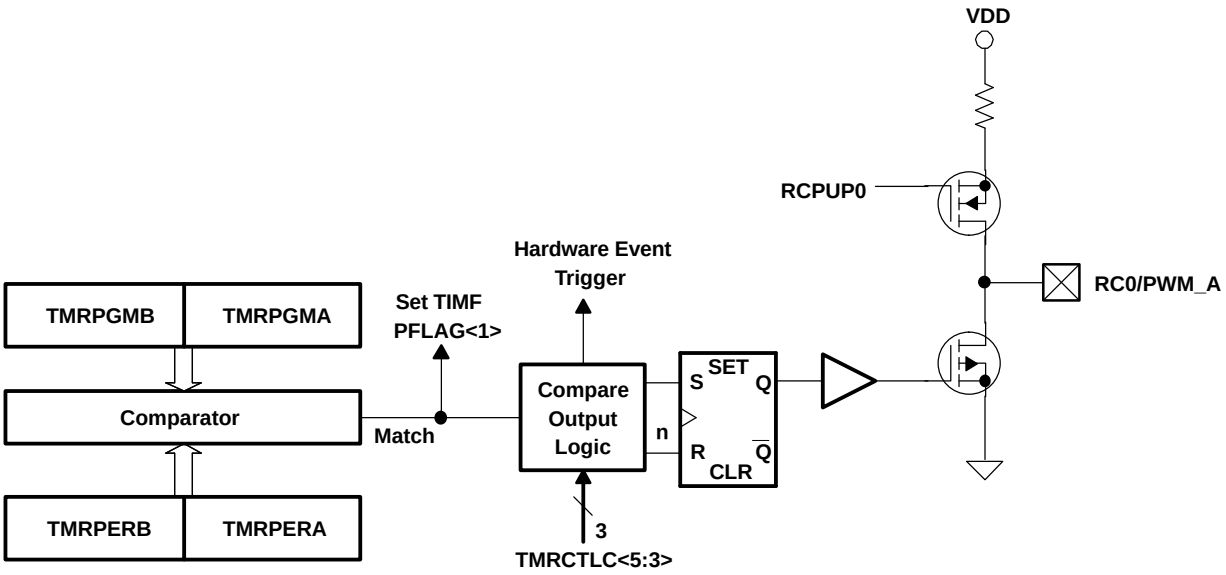


Figure 10-1. Compare Mode Block Diagram

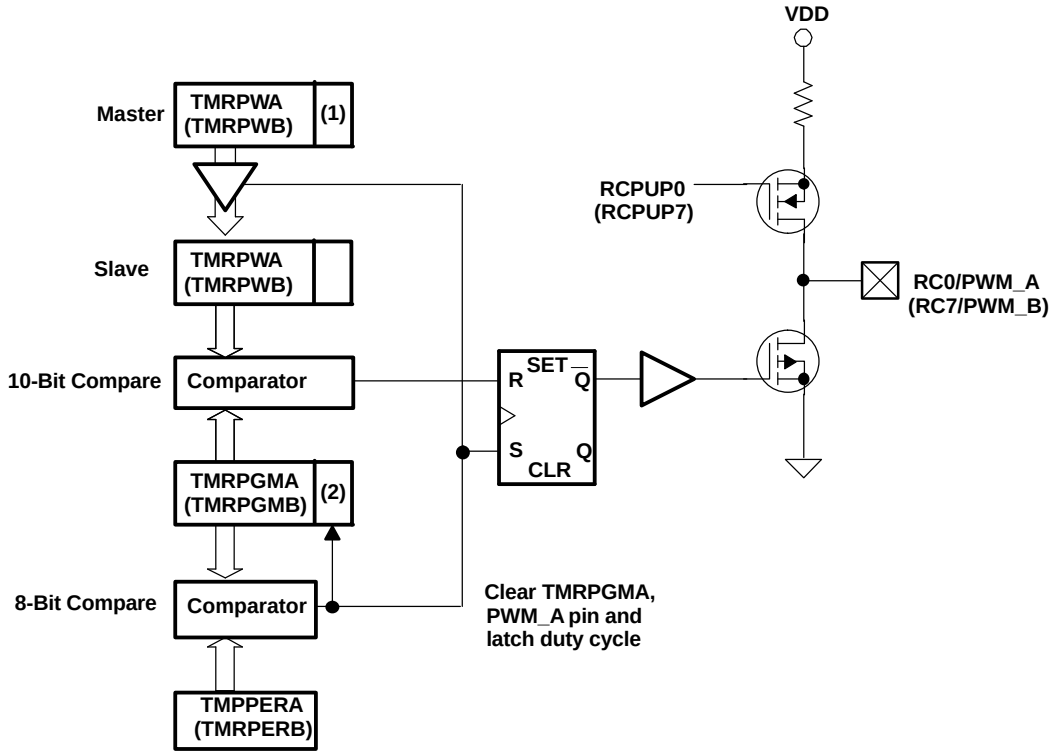
11 PWM Mode

Two pulse width modulation (PWM) modes are offered:

- Single PWM mode, with output forced on RC0/PWM_A (MODE2:0=010
- Dual PWM mode, with outputs forced on RC0/PWM_A and RC7/PWM_B (MODE2:0=011)

When used as PWM outputs, the internal pullups for RC0/PWM_A and RC7/PWM_B are enabled by setting RCPUP0 and RCPUP7 respectively. Writing to RCOUT0 and RCOUT7 bits must be avoided during PWM operation, to prevent corrupting the PWM output signal.

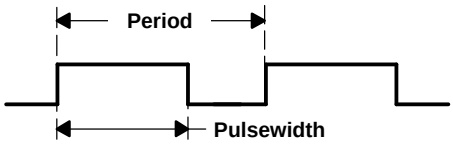
Figure 11-1 shows a simplified PWM block diagram for Timer A configured for PWM mode. Timer B PWM mode configuration is similar, with the substitute registers indicated in italics. PWM operation is described for the single PWM_A output (Timer A configuration) only, as Timer B behaves identically in PWM mode unless otherwise noted.



Notes: (1) PWA1:0 (or PWB1:0)
(2) TMRCTLA<1:0> (or TMRCTLB<1:0>

Figure 11-1. PWM Mode Block Diagram

Figure 11-2 illustrates a PWM output waveform. A write to the period register (TMRPERA or TMRPERB) and the prescaler control bits (TMRCTLA<1:0> or TMRCTLB<1:0>) sets the time base, $t_{(OSC)}$, for this waveform, and a write to the duty cycle registers (TMRPWA and PWA1:0 or TMRPWB and PWB1:0) defines the output high time.



PWM_A Pulsewidth = (TMRPWA:TMRCTLC<7:6>) x T_{OSC} x (Timer A Prescaler(1))
PWM_A Period = [(TMRPERA) x 4 x T_{OSC} x (Timer A Prescaler(1))

Note 1: Timer A prescaler value = 1, 2, 4, or 16 as indicated by TMA_PW1:0

Figure 11-2. PWM Output Waveform

The pulsewidth registers can be written at any time, but this 10-bit value is not used until after a match between the timer count register (TMRPGMA or TMRPGMB) and the respective period register (TMRPERA or TMRPERB) occurs, signifying the completion of a period. If the PWM pulsewidth value exceeds the PWM period, the PWM_A pin will never be forced low.

As an example, consider a desired PWM frequency of 24.90kHz to be generated using the 8.4MHz PLL as the Timer A input clock source (TMA_EXT=0, TMA_ISRC=0). The Timer A prescaler must be set to unity (TMA_PS1:0 = 00). The period register value is determined as follows:

PWM_A Period = [(TMRPERA +1) x 4 x t OSC x (prescaler (TMA_PS1:0)]

TMRPERA = [(1/24.9 kHz)/(4/4.194 MHz)] – 1

TMRPERA = 42 (or 2Ah)

The maximum resolution of the duty cycle that can be used is:

PWM Resolution = [log (4.194 MHz/24.90 kHz)/ log(2)] bits

PWM Resolution = 7.4 bits

Thus, slightly over 7 bits of pulse width resolution are available for a PWM frequency of 24.90 kHz, using the 4.194-MHz input clock. The valid duty cycle register values are: 0 ≤ [TMRPWA:TMRCTLC<7:6>] ≤ A8h. Any value greater then A8h results in a 100% duty cycle. To increase pulse width resolution, the PWM frequency must be decreased. Increasing PWM frequency results in a lower pulse width resolution. Table 11-1 lists several example PWM frequencies with associated pulse width resolution, and the required register set values.

Table 11-1. Example PWM Frequencies and Resolutions at 4.194 MHz (PLL Input Clock Source)

PWM Frequency	255.3 Hz	1.02 kHz	4.09 kHz	24.90 kHz	99.59 kHz	149.4 kHz
Timer Prescaler (1, 2, 4, 16)	16	4	1	1	1	1
TMRPERA Value	FFh	FFh	FFh	2Ah	Ah	0Dh
Maximum Resolution (bits)	10	10	10	7.4	5.4	4.8

12 I/O Pin Controller

The I/O controller manages the operation of the three general-purpose, 8-bit data ports on the bq80201A. These three ports, pins RA[7:0], RB[7:0] and RC[7:0] function independently as digital input pins, digital open-drain output pins, or both. In addition, the pins of the RC port can be selected as analog inputs to the analog-to-digital converter peripheral (ADC) and can be programmed to enable internal pullups to provide full push-pull digital output functionality.

Several of the RA and RB pins have predefined functionality providing communication interfaces for the two bq80201A serial communication peripherals, and providing external interrupt/event conditions to the onboard processor. The predefined functions can be disabled on the basis of the user program. The predefined pins are:

RA7 – SMBus data pin

RA6 – SMBus clock pin

RA5 – HDQ serial communication pin

RA1 – VOUT pin (voltage supply output)

RB1 – external event pin

RB0 – external interrupt pin

RC7 – Timer B PWM output pin

RC3 – Capture Timer input pin

RC0 – Timer A PWM output pin

NOTE

Attempting to use RA7, RA6 or RA5 as general-purpose I/O pins while the SMB or HDQ peripherals are enabled could produce undesired behavior. Therefore, the SMB or HDQ functionality is disabled via the IOCTL register before using these pins as general-purpose data pins. Likewise, the external interrupt/event conditions are disabled to prevent unintended interrupt/event conditions if RB1 or RB0 are to be used for general-purpose I/O.

Pin RA1 contains an internal pullup for use as an external power source controlled by the VOUT bit.

12.1 RA_OUT (address 8070h): RA Output Register

The RA output register controls the output state of the RA pins.

	RA_OUT REGISTER (ADDRESS 8070h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RAOUT7	RAOUT6	RAOUT5	RAOUT4	RAOUT3	RAOUT2	RAOUT1/VOUT	RAOUT0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

RAOUT7 (bit 7):

1 = Do not drive pin RA7 (open drain 3-state); required state for using SMBD

0 = Drive pin RA7 to a logic 0

RAOUT6 (bit 6):

1 = Do not drive pin RA6 (open drain 3-state); required state for using SMBC

0 = Drive pin RA6 to a logic 0

RAOUT5 (bit 5):

1 = Do not drive pin RA5 (open drain 3-state); required state for using HDQ

0 = Drive pin RA5 to a logic 0

RAOUT4 (bit 4):

1 = Do not drive pin RA4 (open drain 3-state)

0 = Drive pin RA4 to a logic 0

RAOUT3 (bit 3):

1 = Do not drive pin RA3 (open drain 3-state)

0 = Drive pin RA3 to a logic 0

RAOUT2 (bit 2):

1 = Do not drive pin RA2 (open drain 3-state)

0 = Drive pin RA2 to a logic 0

RAOUT1 (bit 1):

1 = Drive pin RA1/VOUT to a logic 1 if VOUTEN=1; otherwise, RA1 is open-drain 3-state

0 = Drive pin RA1/VOUT to a logic 0

RAOUT0 (bit 0):

1 = Do not drive pin RA0 (open drain 3-state)

0 = Drive pin RA0 to a logic 0

12.2 RB_OUT (address 8071h): RB Output Register

The RB output register controls the output state of the RB pins.

	RB_OUT REGISTER (ADDRESS 8071h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RBOUT7	RBOUT6	RBOUT5	RBOUT4	RBOUT3	RBOUT2	RBOUT1	RBOUT0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

RBOUT7 (bit 7):

1 = Do not drive pin RB7 (open drain 3-state)

0 = Drive pin RB7 to a logic 0

RBOUT6 (bit 6):

1 = Do not drive pin RB6 (open drain 3-state)

0 = Drive pin RB6 to a logic 0

RBOUT5 (bit 5):

1 = Do not drive pin RB5 (open drain 3-state)

0 = Drive pin RB5 to a logic 0

RBOUT4 (bit 4):

1 = Do not drive pin RB4 (open drain 3-state)

0 = Drive pin RB4 to a logic 0

RBOUT3 (bit 3):

1 = Do not drive pin RB3 (open drain 3-state)

0 = Drive pin RB3 to a logic 0

RBOUT2 (bit 2):

1 = Do not drive pin RB2 (open drain 3-state)

0 = Drive pin RB2 to a logic 0

RBOUT1 (bit 1):

1 = Drive pin RB1 (open drain 3-state) required state for using EV

0 = Drive pin RB1 to a logic 0

RBOUT0 (bit 0):

1 = Drive pin RB0 (open drain 3-state) required state for using INT

0 = Drive pin RB0 to a logic 0

12.3 RC_OUT (address 8072h): RC Output Register

This register controls the output state of the RC pins.

	RC_OUT REGISTER (ADDRESS 8072h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RCOUT7	RCOUT6	RCOUT5	RCOUT4	RCOUT3	RCOUT2	RCOUT1	RCOUT0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

RCOUT7 (bit 7):

1 = If RCPUP0=1, drive pin RC7 to a logic 1. If RCPUP0=0, do not drive pin RC7 (open drain 3-state)

0 = Drive pin RC7 to a logic 0

RCOUT6 (bit 6):

1 = If RCPUP0=1, drive pin RC6 to a logic 1. If RCPUP0=0, do not drive pin RC6 (open drain 3-state)

0 = Drive pin RC6 to a logic 0

RCOUT5 (bit 5):

1 = If RCPUP0=1, drive pin RC5 to a logic 1. If RCPUP0=0, do not drive pin RC5 (open drain 3-state)

0 = Drive pin RC5 to a logic 0

RCOUT4 (bit 4):

1 = If RCPUP0=1, drive pin RC4 to a logic 1. If RCPUP0=0, do not drive pin RC4 (open drain 3-state)

0 = Drive pin RC4 to a logic 0

RCOUT3 (bit 3):

1 = If RCPUP0=1, drive pin RC3 to a logic 1. If RCPUP0=0, do not drive pin RC3 (open drain 3-state)

0 = Drive pin RC3 to a logic 0

RCOUT2 (bit 2):

1 = If RCPUP0=1, drive pin RC2 to a logic 1. If RCPUP0=0, do not drive pin RC2 (open drain 3-state)

0 = Drive pin RC2 to a logic 0

RCOUT1 (bit 1):

1 = If RCPUP0=1, drive pin RC1 to a logic 1. If RCPUP0=0, do not drive pin RC1 (open drain 3-state)

0 = Drive pin RC1 to a logic 0

RCOUT0 (bit 0):

1 = If RCPUP0=1, drive pin RC0 to a logic 1 if RCPUP0=0, do not drive pin RC0 (open drain 3-state)

0 = Drive pin RC0 to a logic 0

12.4 RA_IN (address 8073h): RA Input Status Register

This register controls the output state of the RA pins.

	RA_IN REGISTER (ADDRESS 8073h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RAIN7	RAIN6	RAIN5	RAIN4	RAIN3	RAIN2	RAIN1	RAIN0
Access	Read	Read	Read	Read	Read	Read	Read	Read
Reset	0	0	0	0	0	0	0	0

RAIN7 (bit 7):

1 = Logic value driven on pin RA7 if RAIEN7=1

0 = Logic 0 value driven on pin RA7

RAIN6 (bit 6):

1 = Logic value driven on pin RA6 if RAIEN6=1

0 = Logic 0 value driven on pin RA6

RAIN5 (bit 5):

1 = Logic value driven on pin RA5 if RAIEN5=1

0 = Logic 0 value driven on pin RA5

RAIN4 (bit 4):

1 = Logic value driven on pin RA4 if RAIEN4=1

0 = Logic 0 value driven on pin RA4

RAIN3 (bit 3):

1 = Logic value driven on pin RA3 if RAIEN3=1

0 = Logic 0 value driven on pin RA3

RAIN2 (bit 2):

1 = Logic value driven on pin RA2 if RAIEN2=1

0 = Logic 0 value driven on pin RA2

RAIN1 (bit 1):

1 = Logic value driven on pin RA1 if RAIEN1=1

0 = Logic 0 value driven on pin RA1

RAIN0 (bit 0):

1 = Logic value driven on pin RA0 if RAIEN0=1

0 = Logic 0 value driven on pin RA0

12.5 RB_IN (address 8074h): RB Input Status Register

This register controls the output state of the RB pins.

	RB_IN REGISTER (ADDRESS 8074h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RBIN7	RBIN6	RBIN5	RBIN4	RBIN3	RBIN2	RBIN1	RBIN0
Access	Read	Read	Read	Read	Read	Read	Read	Read
Reset	0	0	0	0	0	0	0	0

RBIN7 (bit 7):

1 = Logic value driven on pin RB7 if RBIEN7=1

0 = Logic 0 value driven on pin RB7

RBIN6 (bit 6):

1 = Logic value driven on pin RB6 if RBIEN6=1

0 = Logic 0 value driven on pin RB6

RBIN5 (bit 5):

1 = Logic value driven on pin RB5 if RBIEN5=1

0 = Logic 0 value driven on pin RB5

RBIN4 (bit 4):

1 = Logic value driven on pin RB4 if RBIEN4=1

0 = Logic 0 value driven on pin RB4

RBIN3 (bit 3):

1 = Logic value driven on pin RB3 if RBIEN3=1

0 = Logic 0 value driven on pin RB3

RBIN2 (bit 2):

1 = Logic value driven on pin RB2 if RBIEN2=1

0 = Logic 0 value driven on pin RB2

RBIN1 (bit 1):

1 = Logic value driven on pin RB1 if RBIEN1=1

0 = Logic 0 value driven on pin RB1

RBIN0 (bit 0):

1 = Logic value driven on pin RB0 if RBIEN0=1

0 = Logic 0 value driven on pin RB0

12.6 RC_IN (address 8075h): RC Input Status Register

This register controls the output state of the RC pins.

	RC_IN REGISTER (ADDRESS 8075h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RCIN7	RCIN6	RCIN5	RCIN4	RCIN3	RCIN2	RCIN1	RCIN0
Access	Read	Read	Read	Read	Read	Read	Read	Read
Reset	0	0	0	0	0	0	0	0

RCIN7 (bit 7):

1 = Logic value driven on pin RC7 if RCIEN7=1

0 = Logic 0 value driven on pin RC7

RCIN6 (bit 6):

1 = Logic value driven on pin RC6 if RCIEN6=1

0 = Logic 0 value driven on pin RC6

RCIN5 (bit 5):

1 = Logic value driven on pin RC5 if RCIEN5=1

0 = Logic 0 value driven on pin RC5

RCIN4 (bit 4):

1 = Logic value driven on pin RC4 if RCIEN4=1

0 = Logic 0 value driven on pin RC4

RCIN3 (bit 3):

1 = Logic value driven on pin RC3 if RCIEN3=1

0 = Logic 0 value driven on pin RC3

RCIN2 (bit 2):

1 = Logic value driven on pin RC2 if RCIEN2=1

0 = Logic 0 value driven on pin RC2

RCIN1 (bit 1):

1 = Logic value driven on pin RC1 if RCIEN1=1

0 = Logic 0 value driven on pin RC1

RCIN0 (bit 0):

1 = Logic value driven on pin RC0 if RCIEN0=1

0 = Logic 0 value driven on pin RC0

12.7 RA_IEN (address 8076h): RA Input Enable Register

This register enables the RA register as an input.

	RA_IEN REGISTER (ADDRESS 8076h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RAIEN7	RAIEN6	RAIEN5	RAIEN4	RAIEN3	RAIEN2	RAIEN1	RAIEN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

RAIEN7 (bit 7):

1 = Enable reading of logic value on pin RA7 via RAIN7

0 = Disable reading of logic value and guard against floating input levels on pin RA7

RAIEN6 (bit 6):

1 = Enable reading of logic value on pin RA6 via RAIN6

0 = Disable reading of logic value and guard against floating input levels on pin RA6

RAIEN5 (bit 5):

1 = Enable reading of logic value on pin RA5 via RAIN5

0 = Disable reading of logic value and guard against floating input levels on pin RA5

RAIEN4 (bit 4):

1 = Enable reading of logic value on pin RA4 via RAIN4

0 = Disable reading of logic value and guard against floating input levels on pin RA4

RAIEN3 (bit 3):

1 = Enable reading of logic value on pin RA3 via RAIN3

0 = Disable reading of logic value and guard against floating input levels on pin RA3

RAIEN2 (bit 2):

1 = Enable reading of logic value on pin RA2 via RAIN2

0 = Disable reading of logic value and guard against floating input levels on pin RA2

RAIEN1 (bit 1):

1 = Enable reading of logic value on pin RA1 via RAIN1

0 = Disable reading of logic value and guard against floating input levels on pin RA1

RAIEN0 (bit 0):

1 = Enable reading of logic value on pin RA0 via RAIN0

0 = Disable reading of logic value and guard against floating input levels on pin RA0

12.8 RB_IEN (address 8077h): RB Input Enable Register

This register enables the RB pins as inputs.

	RB_IEN REGISTER (ADDRESS 8077h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RBIEN7	RBIEN6	RBIEN5	RBIEN4	RBIN3	RBIEN2	RBIEN1	RBIEN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

RBIEN7 (bit 7):

1 = Enable reading of logic value on pin RB7 via RBIN7 bit

0 = Disable reading of logic value and guard against floating input levels on pin RB7

RBIEN6 (bit 6):

1 = Enable reading of logic value on pin RB6 via RBIN6 bit

0 = Disable reading of logic value and guard against floating input levels on pin RB6

RBIEN5 (bit 5):

1 = Enable reading of logic value on pin RB5 via RBIN5 bit

0 = Disable reading of logic value and guard against floating input levels on pin RB5

RBIEN4 (bit 4):

1 = Enable reading of logic value on pin RB4 via RBIN4 bit

0 = Disable reading of logic value and guard against floating input levels on pin RB4

RBIEN3 (bit 3):

1 = Enable reading of logic value on pin RB3 via RBIN3 bit

0 = Disable reading of logic value and guard against floating input levels on pin RB3

RBIEN2 (bit 2):

1 = Enable reading of logic value on pin RB2 via RBIN2 bit

0 = Disable reading of logic value and guard against floating input levels on pin RB2

RBIEN1 (bit 1):

1 = Enable reading of logic value on pin RB1 via RBIN1 bit

0 = Disable reading of logic value and guard against floating input levels on pin RB1

RBIEN0 (bit 0):

1 = Enable reading of logic value on pin RB0 via RBIN0 bit

0 = Disable reading of logic value and guard against floating input levels on pin RB0

12.9 RC_IEN (address 8078h): RC Input Enable Register

This register enables the RB pins as inputs.

	RB_IEN REGISTER (ADDRESS 8077h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RCIEN7	RCIEN6	RCIEN5	RCIEN4	RCIEN3	RCIEN2	RCIEN1	RCIEN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

RCIEN7 (bit 7):

1 = Enable reading of logic value on pin RC7 via RCIN7 bit

0 = Disable reading of logic value and guard against floating input levels on pin RC7

RCIEN6 (bit 6):

1 = Enable reading of logic value on pin RC6 via RCIN6 bit

0 = Disable reading of logic value and guard against floating input levels on pin RC6

RCIEN5 (bit 5):

1 = Enable reading of logic value on pin RC5 via RCIN5 bit

0 = Disable reading of logic value and guard against floating input levels on pin RC5

RCIEN4 (bit 4):

1 = Enable reading of logic value on pin RC4 via RCIN4 bit

0 = Disable reading of logic value and guard against floating input levels on pin RC4

RCIEN3 (bit 3):

1 = Enable reading of logic value on pin RC3 via RCIN3 bit

0 = Disable reading of logic value and guard against floating input levels on pin RC3

RCIEN2 (bit 2):

1 = Enable reading of logic value on pin RC2 via RCIN2 bit

0 = Disable reading of logic value and guard against floating input levels on pin RC2

RCIEN1 (bit 1):

1 = Enable reading of logic value on pin RC1 via RCIN1 bit

0 = Disable reading of logic value and guard against floating input levels on pin RC1

RCIEN0 (bit 0):

1 = Enable reading of logic value on pin RC0 via RCIN0 bit

0 = Disable reading of logic value and guard against floating input levels on pin RC0

12.10 IOCTL (address 8079h): Input/Output Control Register

This register enables the predefined pin functions for RA1, RB0, RB1, RA3, RA4, RA5, RA6, and RA7, RB0, RB1, RC0, RC5 and RC7 pins.

	IOCTL REGISTER (ADDRESS 8079h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	32K_OUT	PWMAEN	PWMBEN	XEVEN	XINTEN	SMBEN	HDQEN	VOUTEN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

32K_OUT (bit 7): Enable 32.768kHz output

1 = Enable 32.7681-kHz clock on RC5

0 = Disable 32.7681-kHz output on RC5

NOTE

When 32K_OUT is enabled, RCOUT5 is set and cleared according to the state of the 32-kHz clock. RCOUT5 retains the last state of the 32-kHz clock output when 32K_OUT is disabled. Writing to RCOUT5 while 32K_OUT is enabled does not affect the 32-kHz clock output on the RC5 pin.

PWMAEN (bit 6): Enable Timer A functions on pin RC0 and RC3

1 = Enable Timer A functions on RC0 and RC3

0 = Enable Timer A functions on RC0 and RC3

PWMBEN (bit 5): Enable Timer B functions on pin RC7

1 = Enable Timer B functions on RC7

0 = Enable Timer B functions on RC7

XEVEN (bit 4): Enable external event pin

1 = Enable pin RB1 to function as CPU external event pin (RBIEN1 must also be set)

0 = Disable CPU external event functionality for pin RB1

XINTEN (bit 3): Enable external interrupt pin

1 = Enable pin RB0 to function as CPU external interrupt pin (RBIEN0 must also be set)

0 = Disable CPU external interrupt functionality for pin RB0

SMBEN (bit 2): Enable SMBus pins

1 = Enable pins RA7 and RA6 to function as SMB data and SMB clock (RAIEN7 and RAIEN6 must also be set)

0 = Disable SMBus functionality for pins RA7 and RA6

HDQEN (bit 1): Enable HDQ pin

1 = Enable pin RA5 to function as the HDQ communication pin (RAIEN5 must also be set)

0 = Disable HDQ functionality for pin RA5

VOUTEN (bit 0): Enable VOUT pin

1 = Enable pin RA1 to function as the VOUT power source pin

0 = Disable VOUT function for pin RA1

12.11 RC_PUP (address 807ch): RC Control Register

This register enables the internal pullups for the RC pins.

	RC_PUP REGISTER (ADDRESS 700ch807ch)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RCPUP7	RCPUP6	RCPUP5	RCPUP4	RCPUP3	RCPUP2	RCPUP1	RCPUP0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

RCPUP7 (bit 7):

1 = Enable internal pullup for pin RC7

0 = Disable internal pullup for pin RC7

RCPUP6 (bit 6):

1 = Enable internal pullup for pin RC6

0 = Disable internal pullup for pin RC6

RCPUP5 (bit 5):

1 = Enable internal pullup for pin RC5

0 = Disable internal pullup for pin RC5

RCPUP4 (bit 4):

1 = Enable internal pullup for pin RC4

0 = Disable internal pullup for pin RC4

RCPUP3 (bit 3):

1 = Enable internal pullup for pin RC3

0 = Disable internal pullup for pin RC3

RCPUP2 (bit 2):

1 = Enable internal pullup for pin RC2

0 = Disable internal pullup for pin RC2

RCPUP1 (bit 1):

1 = Enable internal pullup for pin RC1

0 = Disable internal pullup for pin RC1

RCPUP0 (bit 0):

1 = Enable internal pullup for pin RC0

0 = Disable internal pullup for pin RC0

13 Control Interrupts and Events

The bq80201A has three data registers (PFLAG, and PIE, and PCTL) for interrupt status and control. These are PFLAG and PIE. The internal CPU STAT register controls the servicing of interrupts.

13.1 PFLAG (address 8090h): Peripheral Flag Register

This register signals the status of the various interrupt flags.

	PFLAG REGISTER (ADDRESS 8090h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SMBF	HDQF	ADF	CCF	TIMF	WKF	TMAF	TMBF
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SMBF (bit 7): System management bus interrupt flag. This bit signals the SMBus circuit request for interrupt servicing. A controller interrupt to address vector (3h) is generated if SMBIE=GIE=1 when SMBF=1 (sets the CIN bit in the STAT register).

1 = SMBus circuit requests interrupt processing

0 = SMBus request did not occur

HDQF (bit 6): HDQ interrupt flag. This bit signals the HDQ communication circuit request for interrupt servicing. A controller interrupt to address vector (3h) is generated if HDQIE=GIE=1 when HDQF=1 (sets the CIN bit in the STAT register).

1 = HDQ circuit requests interrupt processing

0 = HDQ request did not occur

ADF (bit 5): ADC interrupt flag bit. This bit signals an ADC request for interrupt servicing at the end of a conversion. A controller interrupt to address vector (2h) is generated if DIE=PINE=GIE=1 when ADF=1 (sets the PIN bit in the STAT register).

1 = ADC circuit requests interrupt processing

0 = ADC request did not occur

CCF (bit 4): CC interrupt flag bit. This bit signals a coulomb counter request for interrupt servicing. A controller interrupt to address vector (2h) is generated if CCIE=PINE=GIE=1 when CCF=1 (sets the PIN bit in the STAT register).

1 = CC circuit requests interrupt processing

0 = CC request did not occur

TIMF (bit 3): Timer interrupt flag. This bit signals a timer request for interrupt servicing. A controller interrupt to address vector (2h) is generated if TIMIE=PINE=GIE=1 when TIMF=1 (sets the PIN bit in the STAT register).

1 = Timer circuit requests interrupt processing once every 7.8125ms (128 times per second)

0 = Timer request did not occur

WKF (bit 2): Wake Timer Flag bit. This bit enunciates that a wake timer out has occurred.

1 = Wake timer elapsed

0 = Wake timer elapse did not occur

TMAF (bit 1): Timer A Flag bit. This bit enunciates a Timer A request for interrupt servicing. A controller interrupt to address vector (2h) is generated if TMBIE=PIE=GIE=1 when TMAF=1 (sets PIN in STAT).

1 = Timer A circuit requests interrupt processing

0 = Timer A request did not occur

TMBF (bit 1): Timer B Flag bit. This bit enunciates a Timer B request for interrupt servicing. A controller interrupt to address vector (2h) is generated if TMBIE=PIE=GIE=1 when TMBF=1 (sets PIN in STAT).

1 = Timer B circuit requests interrupt processing

0 = Timer B request did not occur

13.2 PIE (address 8091h): Peripheral Interrupt Enable Register

This register enables the PIE interrupt from the various registers.

	PIE REGISTER (ADDRESS 8091h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SMBIE	HDQIE	ADIE	CCIE	TIMIE	WKEVE	TMAIE	TMBIE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SMBIE (bit 7): SMBus interrupt enable. This bit enables the SMBus interrupt flag to interrupt the controller. A controller interrupt to address vector (0003h) is generated if SMBF=GIE=1 when SMBIE=1 (sets the CIN bit in the STAT register).

1 = Enable SMBus circuit interrupt requests

0 = Disable SMBus circuit interrupt requests

HDQIE (bit 6): HDQ interrupt enable. This bit enables the HDQ communication flag to interrupt the controller. A controller interrupt to address vector (0003h) is generated if HDQF=GIE=1 when HDQIE=1 (sets the CIN bit in the STAT register).

1 = Enable HDQ circuit interrupt requests

0 = Disable HDQ circuit interrupt requests

ADIE (bit 5): ADC interrupt enable bit. This bit enables an ADC request for interrupt servicing at the end of a conversion. A controller interrupt to address vector (0002h) is generated if ADF=PINE=GIE=1 when ADIE=1 (sets the PIN bit in the STAT register).

1 = Enable ADC interrupt requests

0 = Disable ADC interrupt requests

CCIE (bit 4): CC interrupt enable bit. This bit enables a CC request for interrupt servicing. A controller interrupt to address vector (0002h) is generated if CCF=PINE=GIE=1 when CCIE=1 (sets the PIN bit in the STAT register).

1 = Enable CC interrupt requests

0 = Disable CC interrupt requests

TIMIE (bit 3): Timer interrupt enable. This bit enables a timer request for interrupt servicing. A controller interrupt to address vector (0002h) is generated if TIMF=PINE=GIE=1 when TIMIE=1 (sets the PIN bit in the STAT register).

1 = Enables timer interrupt requests

0 = Disables timer interrupt requests

WKEVE (bit 2): Wake timer event enable bit. This bit allows the wake timer event (not an interrupt) to restart the controller from the HALT.

1 = Enables a wake timer event to restart the controller from HALT

0 = Disables the wake timer event from restarting the controller from HALT

TMAIE (bit 1): Timer A interrupt enable bit. This bit enables a Timer A request for interrupt servicing. A controller interrupt to address vector (0002h) is generated if TMAF=PIE=GIE=1 when TMAIE=1 (sets PIN in STAT).

1 = Enables Timer A interrupt requests

0 = Disables Timer A interrupt requests

TMBIE (bit 0): Timer B interrupt enable bit. This bit enables a Timer B request for interrupt servicing. A controller interrupt to address vector (0002h) is generated if TMBF=PIE=GIE=1 when TMBIE=1 (sets PIN in STAT).

1 = Enables Timer B interrupt requests

0 = Disables Timer B interrupt requests

13.3 PCTL (address 8092h): Peripheral External Input Control Register

This register enables control of the polarity of external inputs for interrupts and events.

	PCTL REGISTER (ADDRESS 8092h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	—	XIN_EDG	XEV_EDG
Access	—	—	—	—	—	—	R/W	R/W
Reset	—	—	—	—	—	—	0	0

Reserved (bits 7:2): Do not use.

XIN_EDG (bit 1): External interrupt edge select bit. This bit selects the active edge, positive or negative,for the external interrupt input.

1 = The external interrupt is positive edge triggered.

0 = The external interrupt is negative edge triggered.

XEV_EDG (bit 0): External event edge select bit. This bit selects the active edge, positive or negative,for the external event input.

1 = The external event is positive edge triggered.

0 = The external event is negative edge triggered.

13.4 VTRIM (address 80a0h): Reference Voltage Trim Register

This register stores the trim voltage for the internal bq80201A reference. During a POR or MRST, the trim value for the internal 1.225-V reference is transferred from a reserved flash register to location 80a0h. This value is set to trim the internal voltage reference.

	VTRIM REGISTER (ADDRESS 80a0h)							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	VTRIM5	VTRIM4	VTRIM3	VTRIM2	VTRIM1	VTRIM0
Access	—	—	R/W	R/W	R/W	R/W	R/W	R/W
Reset	—	—	—	—	—	—	—	—

Reserved (bits 7:6): Do not use.

VTRIM5:0 (bits 5:0): Voltage trim values used to digitally adjust the 1.225-V reference. Each bit has a weight of approximately 1.4 mV.

14 Internal CPU Register Description

The bq80201A has 16 internal CPU registers. Refer to the *bq80xx Core Details Manual User's Guide* (TI literature number SLUU090) for a complete description. The status register is used in conjunction with several of the bq80201A peripherals and is included for ease of reference.

14.1 STAT (address eh): Internal CPU Status Register

This internal CPU register is used to enable interrupts and monitor their status.

	STAT REGISTER (Internal CPU Register: eh)							
	7 (MSB)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (LSB)**
Name	PINE	XINE	GIE	PIN	XIN	CIN	XEV	WEV
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	—	—	—0	—	—	—	—	—

PINE (bit 7): Peripheral interrupt enable bit. This bit enables a controller interrupt when PIN and GIE are asserted.

1 = PIN enabled to generate an interrupt if GIE=1

0 = PIN inhibited from generating an interrupt

XINE (bit 6): External interrupt enable bit. This bit enables a controller interrupt when XIN and GIE are asserted.

1 = XIN enabled to generate an interrupt if GIE=1

0 = XIN inhibited from generating an interrupt

GIE (bit 5): Global interrupt enable bit. This bit disables all interrupts when cleared. GIE is automatically cleared when an interrupt service routine is executed to prevent unwanted interrupt nesting.

1 = Allows PIN, XIN, and CIN interrupts to be processed by the controller

0 = Disables all interrupts

PIN (bit 4): Peripheral interrupt bit (lowest priority). This bit signals a peripheral circuit request for interrupt service.

1 = Peripheral circuit interrupt requested

0 = No peripheral interrupt service requested

XIN (bit 3): External interrupt bit (medium priority). This bit signals an external interrupt service request that was received via the INT (RB0) pin.

1 = External interrupt service requested

0 = No external interrupt service requested

CIN (bit 2): Communication interrupt bit (highest priority).This bit signals a communication circuit request for interrupt service.

1 = Communication circuit interrupt requested from the HDQ or SMBus

0 = No communication interrupt service requested

XEV (bit 1): External event bit. This bit signals that an external wake-timer event occurred via the EV (RB1) pin that can wake the controller from a HALT state.

1 = External event occurred

0 = External event has not occurred

WEV (bit 0): Wake event bit. This bit signals a wake timer event occurred that can wake the controller from a HALT state.

1 = Internal event occurred

0 = Internal wake timer event has not occurred

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